

Description

The 9ZXL15x0D/9ZXL19x0D/9ZXL1951D devices comprise a family of 2nd-generation enhanced performance buffers for PCIe and CPU applications. The family meets all published QPI/UPI, DB2000Q and PCIe Gen1–5 jitter specifications. Devices are either 15 or 19 outputs. The devices function as both fanout (FOB) and zero-delay (ZDB) buffers. All devices meet DB2000Q and DB1900Z jitter and skew requirements.

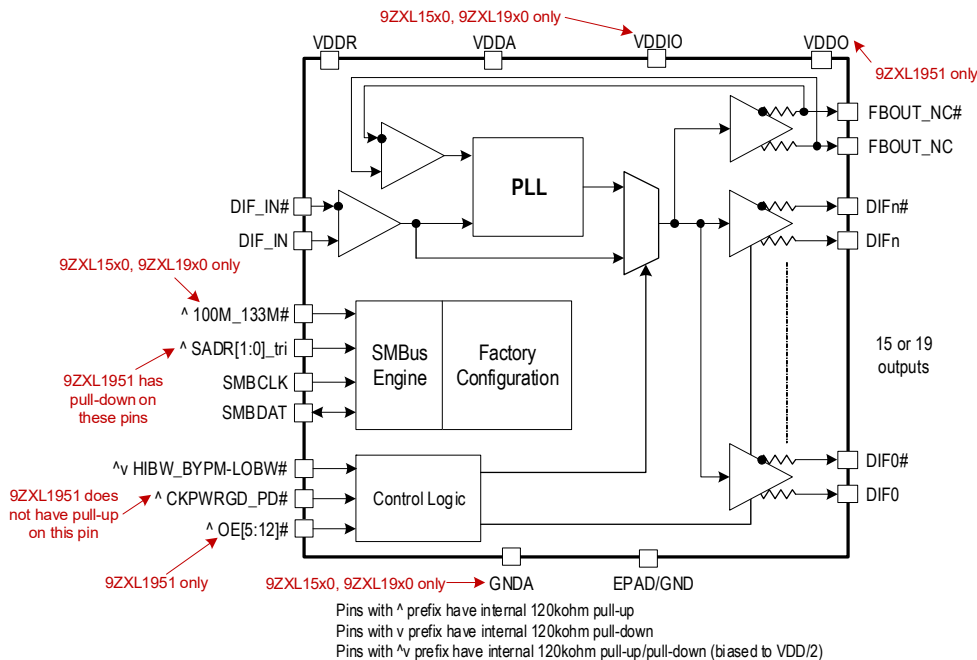
Key Specifications

- ZDB Mode phase jitter:
 - PCIe Gen5 CC < 22fs RMS (Low Bandwidth)
 - QPI/UPI 11.4GB/s < 120fs RMS (Low Bandwidth)
 - IF-UPI additive jitter < 130fs RMS (Low Bandwidth)
- Fanout Buffer Mode additive phase jitter:
 - PCIe Gen5 CC < 24fs RMS
 - DB2000Q additive jitter < 39fs RMS
 - QPI/UPI 11.4GB/s < 40fs RMS
 - IF-UPI additive jitter < 70fs RMS
- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: < 50ps

Outputs

- 15 or 19 Low-power HCSL (LP-HCSL) output pairs

Block Diagram



Features

- LP-HCSL outputs eliminate up to 4 resistors per output pair
- 9 selectable SMBus addresses
- Selectable PLL bandwidths minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of ZDB and FOB modes allow change without power cycle
- 8 OE# pins support PCIe CLKREQ# functionality (9ZXL1951)
- Spread spectrum compatible
- 100MHz and 133.33MHz ZDB mode (9ZXL15x0, 9ZXL19x0)
- 100MHz ZDB mode (9ZXL1951)
- 1–400MHz FOB mode (all devices)
- -40°C to +85°C operating temperature range
- Package information: see [Ordering Information](#) table

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- nVME Storage
- Networking
- Accelerators
- Industrial

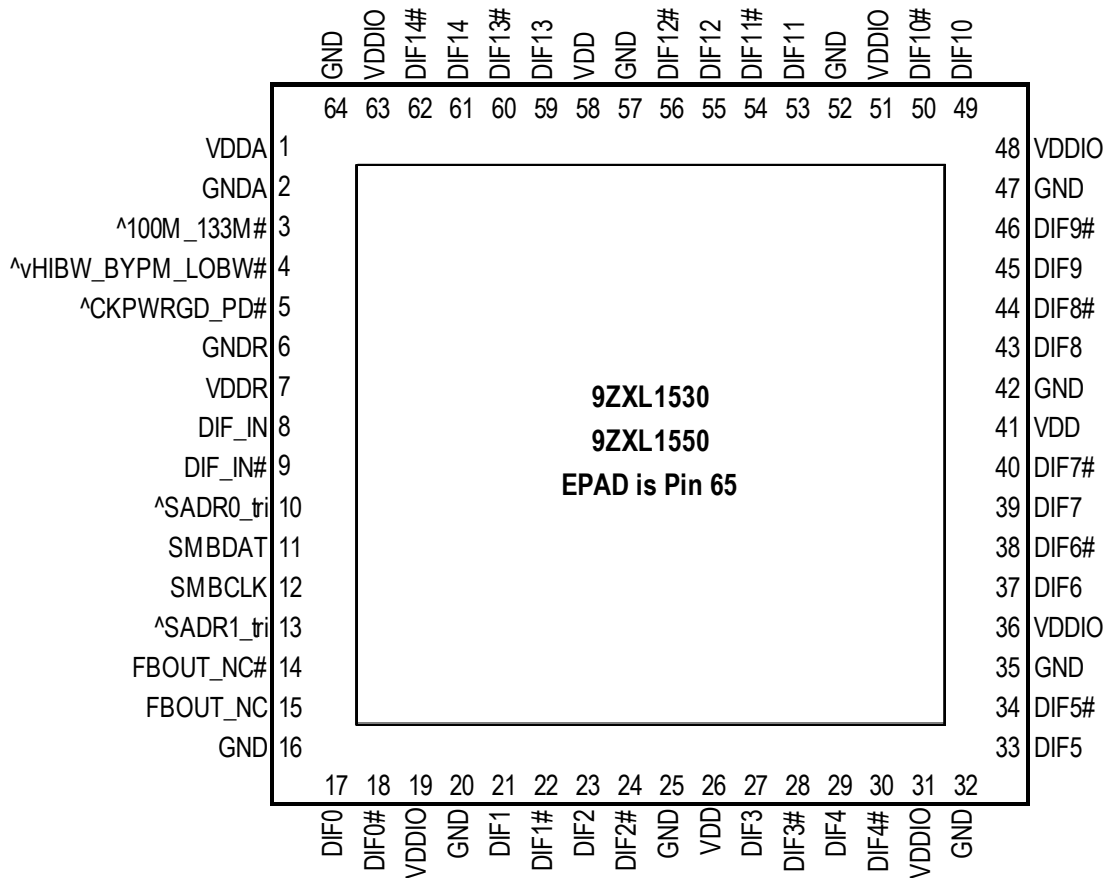
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Pin Assignments

9ZXL15x0D Pin Assignment

Figure 1. Pin Assignment for 9 × 9 mm 64-VFQFPN Package – Top View

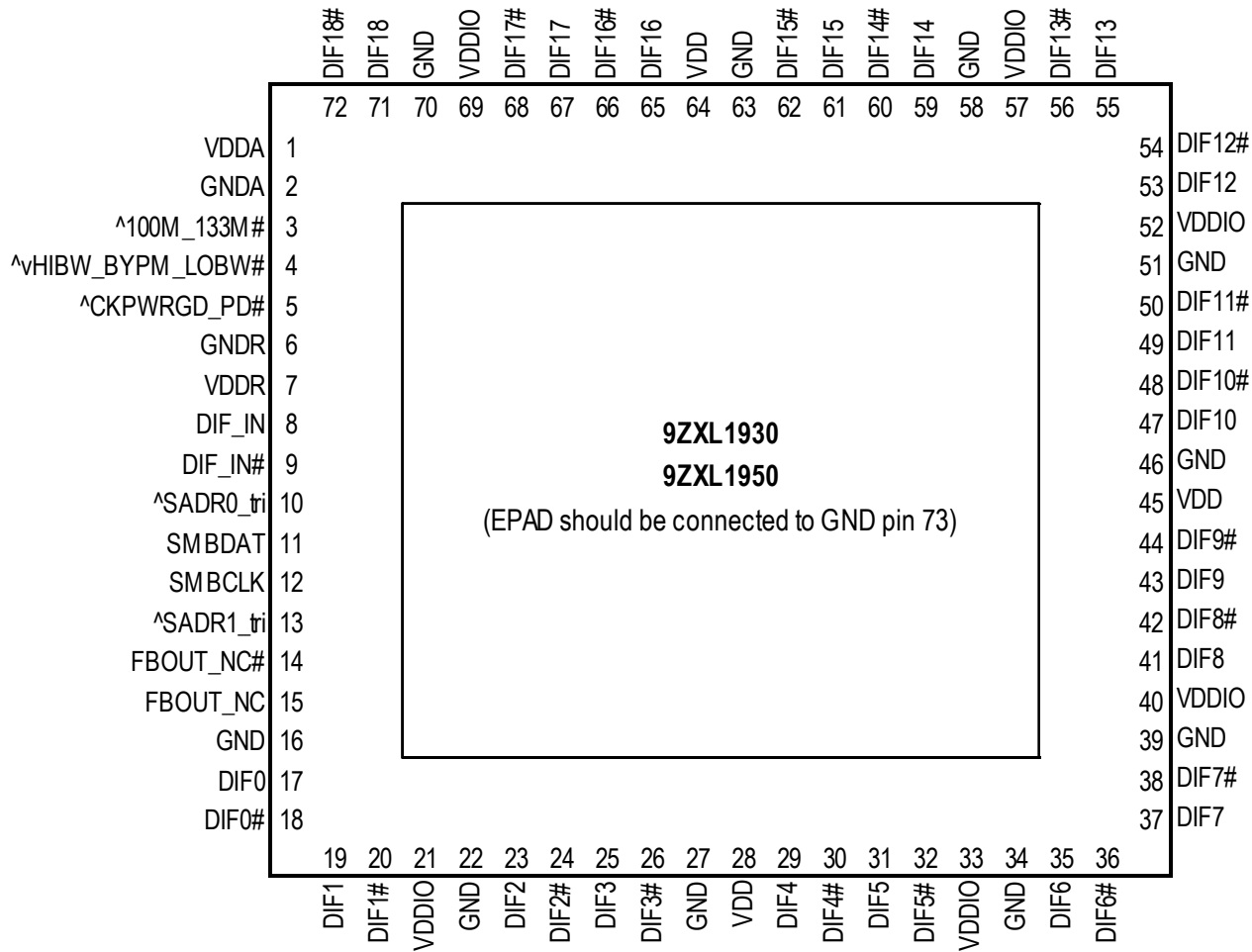


9 x 9 mm 64-VFQFPN

- Notes: Pins with ^ prefix have internal 120kohm pull-up
- Pins with v prefix have internal 120kohm pull-down
- Pins with ^v prefix have internal 120kohm pull-up/pull-down (biased to VDD/2)

9ZXL19x0D Pin Assignment

Figure 2. Pin Assignment for 10 × 10 mm 72-VFQFPN Package – Top View



10 x 10 mm 72-VFQFPN

- Notes: Pins with ^ prefix have internal 120kohm pull-up
- Pins with v prefix have internal 120kohm pull-down
- Pins with ^v prefix have internal 120kohm pull-up/pull-down (biased to VDD/2)

9ZXL1951D Pin Assignment

Figure 3. Pin Assignment for 6 × 6 mm 80-GQFN Package – Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---------|------------------------|--|--------|---------|-------|------------|-------------------|-----------------------------------|--------------------|--------------------|--------|---|
| A | DIF16# | DIF16 | DIF15# | DIF15 | DIF14# | DIF14 | NC | DIF13# | DIF13 | DIF12# | DIF12 | DIF11# | A |
| B | DIF17 | VDDO3.3 | NC | NC | VDDA3.3 | NC | vSADR0_tri | vSADR1_tri | [^] vHIBW_BYP M_LOBW# | [^] OE12# | VDDO3.3 | DIF11 | B |
| C | DIF17# | NC | <div style="border: 1px solid black; padding: 10px; text-align: center;"> <p>9ZXL1951D 6 x 6 x 0.5 mm 80-GQFN Package Top View EPAD is GND</p> </div> | | | | | | | | [^] OE11# | DIF10# | C |
| D | DIF18 | NC | | | | | | | | | NC | DIF10 | D |
| E | DIF18# | NC | | | | | | | | | [^] OE10# | NC | E |
| F | NC | FBOU _T _NC# | | | | | | | | | NC | DIF9# | F |
| G | DIF_IN | FBOU _T _NC | | | | | | | | | [^] OE9# | DIF9 | G |
| H | DIF_IN# | VDDR3.3 | | | | | | | | | CKPWRGD_ PD# | DIF8# | H |
| J | DIF0 | NC | | | | | | | | | [^] OE8# | DIF8 | J |
| K | DIF0# | NC | [^] OE7# | DIF7# | K | | | | | | | | |
| L | DIF1 | VDDO3.3 | NC | SMBDAT | SMBCLK | NC | NC | [^] OE5# | NC | [^] OE6# | VDDO3.3 | DIF7 | L |
| M | DIF1# | DIF2 | DIF2# | DIF3 | DIF3# | NC | DIF4 | DIF4# | DIF5 | DIF5# | DIF6 | DIF6# | M |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |

Pin Descriptions

Table 1. Pin Descriptions for 9ZXL15x0D/9ZXL19x0D

| Name | Type | Description | 9ZXL19x0 Pin No. | 9ZXL15x0 Pin No. |
|--------------------|------------|--|------------------|------------------|
| ^100M_133M# | Latched In | 3.3V Input to select operating frequency. This pin has an internal pull-up resistor. See Functionality at Power-Up (ZDB Mode) table for definition. | 3 | 3 |
| ^CKPWRGD_PD# | Input | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. | 5 | 5 |
| ^SADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-up resistor. See the SMBus Addressing table. | 10 | 10 |
| ^SADR1_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-up resistor. See the SMBus Addressing table. | 13 | 13 |
| ^vHIBW_BYPM_LO BW# | Latched In | Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull-up/pull down resistors. See PLL Operating Mode table for details. | 4 | 4 |
| DIF_IN | Input | HCSL true input. | 8 | 8 |
| DIF_IN# | Input | HCSL complementary input. | 9 | 9 |
| DIF0 | Output | Differential true clock output. | 17 | 17 |
| DIF0# | Output | Differential complementary clock output. | 18 | 18 |
| DIF1 | Output | Differential true clock output. | 19 | 21 |
| DIF1# | Output | Differential complementary clock output. | 20 | 22 |
| DIF10 | Output | Differential true clock output. | 47 | 49 |
| DIF10# | Output | Differential complementary clock output. | 48 | 50 |
| DIF11 | Output | Differential true clock output. | 49 | 53 |
| DIF11# | Output | Differential complementary clock output. | 50 | 54 |
| DIF12 | Output | Differential true clock output. | 53 | 55 |
| DIF12# | Output | Differential complementary clock output. | 54 | 56 |
| DIF13 | Output | Differential true clock output. | 55 | 59 |
| DIF13# | Output | Differential complementary clock output. | 56 | 60 |
| DIF14 | Output | Differential true clock output. | 59 | 61 |
| DIF14# | Output | Differential complementary clock output. | 60 | 62 |
| DIF15 | Output | Differential true clock output. | 61 | — |
| DIF15# | Output | Differential complementary clock output. | 62 | — |
| DIF16 | Output | Differential true clock output. | 65 | — |
| DIF16# | Output | Differential complementary clock output. | 66 | — |
| DIF17 | Output | Differential true clock output. | 67 | — |
| DIF17# | Output | Differential complementary clock output. | 68 | — |
| DIF18 | Output | Differential true clock output. | 71 | — |

Table 1. Pin Descriptions for 9ZXL15x0D/9ZXL19x0D (Cont.)

| Name | Type | Description | 9ZXL19x0 Pin No. | 9ZXL15x0 Pin No. |
|-----------|--------|---|-------------------------------|-------------------------------|
| DIF18# | Output | Differential complementary clock output. | 72 | — |
| DIF2 | Output | Differential true clock output. | 23 | 23 |
| DIF2# | Output | Differential complementary clock output. | 24 | 24 |
| DIF3 | Output | Differential true clock output. | 25 | 27 |
| DIF3# | Output | Differential complementary clock output. | 26 | 28 |
| DIF4 | Output | Differential true clock output. | 29 | 29 |
| DIF4# | Output | Differential complementary clock output. | 30 | 30 |
| DIF5 | Output | Differential true clock output. | 31 | 33 |
| DIF5# | Output | Differential complementary clock output. | 32 | 34 |
| DIF6 | Output | Differential true clock output. | 35 | 37 |
| DIF6# | Output | Differential complementary clock output. | 36 | 38 |
| DIF7 | Output | Differential true clock output. | 37 | 39 |
| DIF7# | Output | Differential complementary clock output. | 38 | 40 |
| DIF8 | Output | Differential true clock output. | 41 | 43 |
| DIF8# | Output | Differential complementary clock output. | 42 | 44 |
| DIF9 | Output | Differential true clock output. | 43 | 45 |
| DIF9# | Output | Differential complementary clock output. | 44 | 46 |
| epad | GND | Connect EPAD to ground. | 73 | 65 |
| FBOUT_NC | Output | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. | 15 | 15 |
| FBOUT_NC# | Output | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. | 14 | 14 |
| GND | GND | Ground pin. | 16,22,27,34,39,46,51,58,63,70 | 16,20,25,32,35,42,47,52,57,64 |
| GNDA | GND | Ground pin for the PLL core. | 2 | 2 |
| GNDR | GND | Analog ground pin for the differential input (receiver). | 6 | 6 |
| SMBCLK | Input | Clock pin of SMBUS circuitry. | 12 | 12 |
| SMBDAT | I/O | Data pin of SMBUS circuitry. | 11 | 11 |
| VDD | Power | Power supply, nominally 3.3V. | 28,45,64 | 26,41,58 |
| VDDA | Power | Power supply for PLL core. | 1 | 1 |
| VDDIO | Power | Power supply for differential outputs. | 21,33,40,52,57,69 | 19,31,26,48,51,63 |
| VDDR | Power | Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. | 7 | 7 |

Table 2. Pin Descriptions for 9ZXL1951D

| Name | Type | Description | Pin Number |
|-----------------------|---------------|--|------------|
| ^OE10# | Input | Active low input for enabling output 10. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | E11 |
| ^OE11# | Input | Active low input for enabling output 11. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | C11 |
| ^OE12# | Input | Active low input for enabling output 12. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | B10 |
| ^OE5# | Input | Active low input for enabling output 5. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | L8 |
| ^OE6# | Input | Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | L10 |
| ^OE7# | Input | Active low input for enabling output 7. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | K11 |
| ^OE8# | Input | Active low input for enabling output 8. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | J11 |
| ^OE9# | Input | Active low input for enabling output 9. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output. | G11 |
| ^vHIBW_BYPM_LO BW# | Latched In | Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass Mode) with internal pull-up/pull down resistors. See PLL Operating Mode table for details. | B9 |
| CKPWRGD_PD# | Input | 3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. | H11 |
| DIF_IN | Input | HCSL true input. | G1 |
| DIF_IN# | Input | HCSL complementary input. | H1 |
| DIF0 | Output | Differential true clock output. | J1 |
| DIF0# | Output | Differential complementary clock output. | K1 |
| DIF1 | Output | Differential true clock output. | L1 |
| DIF1# | Output | Differential complementary clock output. | M1 |
| DIF10 | Output | Differential true clock output. | D12 |
| DIF10# | Output | Differential complementary clock output. | C12 |
| DIF11 | Output | Differential true clock output. | B12 |
| DIF11# | Output | Differential complementary clock output. | A12 |
| DIF12 | Output | Differential true clock output. | A11 |
| DIF12# | Output | Differential complementary clock output. | A10 |
| DIF13 | Output | Differential true clock output. | A9 |
| DIF13# | Output | Differential complementary clock output. | A8 |
| DIF14 | Output | Differential true clock output. | A6 |
| DIF14# | Output | Differential complementary clock output. | A5 |
| DIF15 | Output | Differential true clock output. | A4 |

Table 2. Pin Descriptions for 9ZXL1951D (Cont.)

| Name | Type | Description | Pin Number |
|-----------|--------|---|------------|
| DIF15# | Output | Differential complementary clock output. | A3 |
| DIF16 | Output | Differential true clock output. | A2 |
| DIF16# | Output | Differential complementary clock output. | A1 |
| DIF17 | Output | Differential true clock output. | B1 |
| DIF17# | Output | Differential complementary clock output. | C1 |
| DIF18 | Output | Differential true clock output. | D1 |
| DIF18# | Output | Differential complementary clock output. | E1 |
| DIF2 | Output | Differential true clock output. | M2 |
| DIF2# | Output | Differential complementary clock output. | M3 |
| DIF3 | Output | Differential true clock output. | M4 |
| DIF3# | Output | Differential complementary clock output. | M5 |
| DIF4 | Output | Differential true clock output. | M7 |
| DIF4# | Output | Differential complementary clock output. | M8 |
| DIF5 | Output | Differential true clock output. | M9 |
| DIF5# | Output | Differential complementary clock output. | M10 |
| DIF6 | Output | Differential true clock output. | M11 |
| DIF6# | Output | Differential complementary clock output. | M12 |
| DIF7 | Output | Differential true clock output. | L12 |
| DIF7# | Output | Differential complementary clock output. | K12 |
| DIF8 | Output | Differential true clock output. | J12 |
| DIF8# | Output | Differential complementary clock output. | H12 |
| DIF9 | Output | Differential true clock output. | G12 |
| DIF9# | Output | Differential complementary clock output. | F12 |
| EPAD | GND | Connect epad to ground. | ZZ |
| FBOUT_NC | Output | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. | G2 |
| FBOUT_NC# | Output | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. | F2 |
| NC | — | No connection. | A7 |
| NC | — | No connection. | B3 |
| NC | — | No connection. | B4 |
| NC | — | No connection. | B6 |
| NC | — | No connection. | C2 |
| NC | — | No connection. | D2 |
| NC | — | No connection. | D11 |
| NC | — | No connection. | E2 |
| NC | — | No connection. | E12 |

Table 2. Pin Descriptions for 9ZXL1951D (Cont.)

| Name | Type | Description | Pin Number |
|------------|-------|--|------------|
| NC | — | No connection. | F1 |
| NC | — | No connection. | F11 |
| NC | — | No connection. | J2 |
| NC | — | No connection. | K2 |
| NC | — | No connection. | L3 |
| NC | — | No connection. | L6 |
| NC | — | No connection. | L7 |
| NC | — | No connection. | L9 |
| NC | — | No connection. | M6 |
| SMBCLK | Input | Clock pin of SMBUS circuitry. | L5 |
| SMBDAT | I/O | Data pin of SMBUS circuitry. | L4 |
| VDDA3.3 | Power | 3.3V power for the PLL core. | B5 |
| VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. | B2 |
| VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. | B11 |
| VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. | L2 |
| VDDO3.3 | Power | Power supply for outputs. Nominally 3.3V. | L11 |
| VDDR3.3 | Power | Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. | H2 |
| vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-down resistor. See the SMBus Addressing table. | B7 |
| vSADR1_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-down resistor. See the SMBus Addressing table. | B8 |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL15x0D/9ZXL19x0D/9ZXL1951D. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|--------------------|-----------------------------|-----------|---------|----------------|-------|-------|
| Supply Voltage | V_{DDx} | | | | 3.9 | V | 1,2 |
| Input Low Voltage | V_{IL} | | GND - 0.5 | | | V | 1 |
| Input High Voltage | V_{IH} | Except for SMBus interface. | | | $V_{DD} + 0.5$ | V | 1,3 |
| Input High Voltage, SMBus | $V_{IH\text{SMB}}$ | SMBus clock and data pins. | | | 3.9 | V | 1 |
| Storage Temperature | T_s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T_j | | | | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model. | 2500 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 3.9V.

Thermal Characteristics

Table 4. Thermal Characteristics

| Parameter | Symbol | Conditions | Package | Typical Values | Units | Notes |
|-----------------------------------|----------------|----------------------------------|---------|----------------|-------|-------|
| 9ZXL19x0 Thermal Resistance | θ_{JC} | Junction to case. | NLG72 | 19 | °C/W | 1 |
| | θ_{Jb} | Junction to base. | | 0.5 | °C/W | 1 |
| | θ_{JA0} | Junction to air, still air. | | 30 | °C/W | 1 |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 23 | °C/W | 1 |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 20 | °C/W | 1 |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 19 | °C/W | 1 |
| 9ZXL15x0 Thermal Resistance | θ_{JC} | Junction to case. | NLG64 | 14 | °C/W | 1 |
| | θ_{Jb} | Junction to base. | | 1 | °C/W | 1 |
| | θ_{JA0} | Junction to air, still air. | | 28 | °C/W | 1 |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 21 | °C/W | 1 |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 19 | °C/W | 1 |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 18 | °C/W | 1 |

Table 4. Thermal Characteristics (Cont.)

| Parameter | Symbol | Conditions | Package | Typical Values | Units | Notes |
|-----------------------------------|----------------|----------------------------------|---------|----------------|-------|-------|
| 9ZXL1951 Thermal Resistance | θ_{JC} | Junction to case. | NHG80 | 44 | °C/W | 1 |
| | θ_{Jb} | Junction to base. | | 2 | °C/W | 1 |
| | θ_{JA0} | Junction to air, still air. | | 33 | °C/W | 1 |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 29 | °C/W | 1 |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 28 | °C/W | 1 |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 27 | °C/W | 1 |

¹ EPAD soldered to board.

Electrical Characteristics

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

Table 5. SMBus Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|--------------|---|---------|---------|-------------|-------|-------|
| SMBus Input Low Voltage | V_{ILSMB} | | | | 0.8 | V | |
| SMBus Input High Voltage | V_{IHSMB} | | 2.1 | | V_{DDSMB} | V | |
| SMBus Output Low Voltage | V_{OLSMB} | At I_{PULLUP} . | | | 0.4 | V | |
| SMBus Sink Current | I_{PULLUP} | At V_{OL} . | 4 | | | mA | |
| Nominal Bus Voltage | V_{DDSMB} | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | t_{RSMB} | (Max $V_{IL} - 0.15V$) to (Min $V_{IH} + 0.15V$). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t_{FSMB} | (Min $V_{IH} + 0.15V$) to (Max $V_{IL} - 0.15V$). | | | 300 | ns | 1 |
| SMBus Operating Frequency | f_{SMBMAX} | SMBus operating frequency. | | | 400 | kHz | 5 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ The differential input clock must be running for the SMBus to be active.

Table 6. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------------------|-------------|---|---------|---------|---------|-------|-------|
| Input Crossover Voltage – DIF_IN | V_{CROSS} | Crossover voltage. | 150 | | 900 | mV | 1 |
| Input Swing – DIF_IN | V_{SWING} | Differential value. | 300 | | | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}$, $V_{IN} = GND$. | -5 | | 5 | μA | |
| Input Duty Cycle | d_{tin} | Measurement from differential waveform. | 45 | | 55 | % | 1 |
| Input Jitter – Cycle to Cycle | J_{DIFIn} | Differential measurement. | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through ±75mV window centered around differential zero.

Table 7. Input/Supply/Common Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------------------|-----------------|---|-----------|------------|----------------|--------|-------|
| Supply Voltage | V_{DDx} | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | |
| Output Supply Voltage | V_{DDIO} | Supply voltage for DIF outputs, if present. | 0.95 | 1.05 | 3.465 | V | 5 |
| Ambient Operating Temperature | T_{AMB} | Industrial range (T_{IND}). | -40 | 25 | 85 | °C | |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus, tri-level inputs. | 2 | | $V_{DD} + 0.3$ | V | |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus, tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input High Voltage | V_{IH} | Tri-level inputs. | 2.2 | | $V_{DD} + 0.3$ | V | |
| Input Mid Voltage | V_{IM} | Tri-level inputs. | 1.2 | $V_{DD}/2$ | 1.8 | V | |
| Input Low Voltage | V_{IL} | Tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = \text{GND}$, $V_{IN} = V_{DD}$. | -5 | | 5 | μA | |
| | I_{INP} | Single-ended inputs. $V_{IN} = 0 \text{ V}$; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors. | -50 | | 50 | μA | |
| Input Frequency | F_{ibyp} | $V_{DD} = 3.3 \text{ V}$, Bypass Mode. | 1 | | 400 | MHz | |
| | F_{ipll} | $V_{DD} = 3.3 \text{ V}$, 100MHz PLL Mode. | 98.5 | 100.00 | 102.5 | MHz | |
| | F_{ipll} | $V_{DD} = 3.3 \text{ V}$, 133.33MHz PLL Mode. | 132 | 133.33 | 135 | MHz | 6 |
| ppm Error Contribution | ppm | ppm error contributed to input clock. | 0 | | | ppm | |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| | C_{OUT} | Output pin capacitance. | | | 6 | pF | 1 |
| Clk Stabilization | T_{STAB} | From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock. | | 1 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable frequency for PCIe applications (Triangular modulation). | 30 | | 33 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion. DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# deassertion. | | | 300 | μs | 1,3 |
| Tfall | t_F | Fall time of control inputs. | | | 5 | ns | 2 |
| Trise | t_R | Rise time of control inputs. | | | 5 | ns | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ Not present on 9ZXL1951D.

⁶ 9ZXL15x0 and 9ZXL19x0 only.

Table 8. Current Consumption – 9ZXL1951D

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|------------------|---|---------|---------|---------|-------|-------|
| Operating Supply Current | $I_{DDVDDA/R}$ | PLL Mode, all outputs 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 45 | 55 | mA | 1 |
| | I_{DDVDD} | All outputs 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 171 | 200 | mA | |
| Power Down Current | $I_{DDVDDPD}$ | All differential pairs low-low. | | 1 | 2 | mA | |
| | $I_{DDVDDA/RPD}$ | All differential pairs low-low. | | 4 | 6 | mA | |

¹ In Bypass Mode (PLL of) $I_{DDVDDA/R}$ is 12mA.

Table 9. Current Consumption – 9ZXL19x0D

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|-------------|--|---------|---------|---------|-------|-------|
| Operating Supply Current | I_{DDA+R} | $V_{DDA} + V_{DDR}$ pins, all outputs at 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 54 | 65 | mA | 1 |
| | I_{DDO} | V_{DDIO} pins, all outputs at 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 136 | 169 | mA | |
| | I_{DDx} | All other V_{DD} pins, all outputs at 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 28 | 38 | mA | |
| Power Down Current | I_{DDA+R} | $V_{DDA} + V_{DDR}$ pins, all outputs Low/Low. | | 4 | 5 | mA | |
| | I_{DDO} | V_{DDIO} pins, all outputs Low/Low. | | 0.04 | 0.1 | mA | |
| | I_{DDx} | All other V_{DD} pins, all outputs Low/Low. | | 0.4 | 1 | mA | |

¹ In Bypass Mode (PLL of) $I_{DDVDDA/R}$ is 12mA.

Table 10. Current Consumption – 9ZXL15x0D

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|-------------|--|---------|---------|---------|-------|-------|
| Operating Supply Current | I_{DDA+R} | $V_{DDA} + V_{DDR}$ pins, all outputs at 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 54 | 65 | mA | 1 |
| | I_{DDO} | V_{DDIO} pins, all outputs at 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 77 | 92 | mA | |
| | I_{DDx} | All other V_{DD} pins, all outputs at 100MHz, $C_L = 2\text{pF}$; $Z_o = 85\Omega$. | | 27 | 34 | mA | |
| Power Down Current | I_{DDA+R} | $V_{DDA} + V_{DDR}$ pins, all outputs Low/Low. | | 4 | 5 | mA | |
| | I_{DDO} | V_{DDIO} pins, all outputs Low/Low. | | 0.04 | 0.1 | mA | |
| | I_{DDx} | All other V_{DD} pins, all outputs Low/Low. | | 0.46 | 0.6 | mA | |

¹ In Bypass Mode (PLL of) $I_{DDVDDA/R}$ is 12mA.

Table 11. Skew and Differential Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------|----------------------------------|---|---------|---------|---------|----------|-----------|
| CLK_IN, DIF[x:0] | t _{SPO_PLL} | Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage. | -100 | -21.3 | 100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t _{PD_BYP} | Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage. | 2.2 | 2.7 | 3.5 | ns | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t _{DSPO_PLL} | Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature. | -50 | 0 | 50 | ps | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t _{DSPO_BYP} | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature. T _{AMB} = -0°C to +70°C. | -250 | | 250 | ps | 1,2,3,5,7 |
| | | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T _{AMB} = -40°C to +85°C. | -350 | | 350 | ps | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t _{DTE} | Random differential tracking error between two 9ZX devices in High BW Mode. | | 3 | 5 | ps (RMS) | 1,2,3,5,7 |
| CLK_IN, DIF[x:0] | t _{DSSTE} | Random differential spread spectrum tracking error between two 9ZX devices in High BW Mode. | | 23 | 50 | ps | 1,2,3,5,7 |
| DIF[x:0] | t _{SKREW_ALL} | Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz. | | | 50 | ps | 1,2,3,7 |
| PLL Jitter Peaking | j _{peak-hibw} | LOBW#_BYPASS_HIBW = 1. | 0 | 1.3 | 2.5 | dB | 6,7 |
| PLL Jitter Peaking | j _{peak-lobw} | LOBW#_BYPASS_HIBW = 0. | 0 | 1.3 | 2 | dB | 6,7 |
| PLL Bandwidth | p _{llHIBW} | LOBW#_BYPASS_HIBW = 1. | 2 | 2.6 | 4 | MHz | 7,8 |
| PLL Bandwidth | p _{llLOBW} | LOBW#_BYPASS_HIBW = 0. | 0.7 | 1.0 | 1.4 | MHz | 7,8 |
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode. | 45 | 50.3 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially, Bypass Mode at 100MHz. | -1 | 0 | 1 | % | 1,9 |
| Jitter, Cycle to Cycle | t _{j_{cyc-cyc}} | PLL Mode. | | 14 | 50 | ps | 1,10 |
| | | Additive jitter in Bypass Mode. | | 0.1 | 5 | ps | 1,10 |

¹ Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

³ All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

⁴ This parameter is deterministic for a given device.

⁵ Measured with scope averaging on to find mean value.

⁶ “t” is the period of the input clock.

⁶ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

⁷ Guaranteed by design and characterization, not 100% tested in production.

⁸ Measured at 3db down or half power point.

⁹ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

¹⁰ Measured from differential waveform.

Table 12. LP-HCSL Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limit | Units | Notes |
|------------------------|------------------------|--|---------|---------|---------|---------------------|-------|-------|
| Slew Rate | dV/dt | Scope averaging on. | 2 | 2.6 | 4 | 1–4 | V/ns | 1,2,3 |
| Slew Rate Matching | ΔdV/dt | Single-ended measurement. | | 7.1 | 20 | 20 | % | 1,4,7 |
| Maximum Voltage | V _{max} | Measurement on single-ended signal using absolute value (scope averaging off). | 700 | 778 | 900 | 660–1150 | mV | 7,8 |
| Minimum Voltage | V _{min} | | -125 | -21 | 50 | -300–150 | | 7,8 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off. | 250 | 389 | 550 | 250–550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ-V _{cross} | Scope averaging off. | | 24 | 75 | 140 | mV | 1,6,7 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ-V_{cross} to be smaller than V_{cross} absolute.

⁷ At default SMBus settings.

⁸ Includes previously separate values of +300mV overshoot and -300mV of undershoot.

Table 13. PCIe Phase Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limits | Units | Notes |
|---|-----------------------------|-------------------------------|---------|---------|---------|----------|----------|---------|
| PCIe Phase Jitter, Low Bandwidth ZDB Mode (Common Clocked Architecture) | t _{jphPCIeG1-CC} | PCIe Gen 1 (2.5 GT/s) | | 2.6 | 6.8 | 86 | ps (p-p) | 1,2 |
| | t _{jphPCIeG2-CC} | PCIe Gen 2 Hi Band (5.0 GT/s) | | 0.09 | 0.16 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen 2 Lo Band (5.0 GT/s) | | 0.08 | 0.12 | 3.1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG3-CC} | PCIe Gen 3 (8.0 GT/s) | | 0.05 | 0.07 | 1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG4-CC} | PCIe Gen 4 (16.0 GT/s) | | 0.05 | 0.07 | 0.5 | ps (RMS) | 1,2,3,4 |
| t _{jphPCIeG5-CC} | PCIe Gen 5 (32.0 GT/s) | | 0.018 | 0.022 | 0.15 | ps (RMS) | 1,2,3,5 | |
| PCIe Phase Jitter, Low Bandwidth ZDB Mode (SRIS Architecture) | t _{jphPCIeG1-SRIS} | PCIe Gen 1 (2.5 GT/s) | | 8.71 | 8.73 | N/A | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen 2 (5.0 GT/s) | | 0.81 | 0.83 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen 3 (8.0 GT/s) | | 0.329 | 0.335 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen 4 (16.0 GT/s) | | 0.222 | 0.235 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG5-SRIS} | PCIe Gen 5 (32.0 GT/s) | | 0.084 | 0.091 | | ps (RMS) | 1,2,6 |

Table 13. PCIe Phase Jitter Parameters (Cont.)

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limits | Units | Notes |
|--|-----------------------------|-------------------------------|---------|---------|---------|----------|----------|---------|
| PCIe Phase Jitter, High Bandwidth ZDB Mode (Common Clocked Architecture) | t _{jphPCIeG1-CC} | PCIe Gen 1 (2.5 GT/s) | | 5.4 | 6.9 | 86 | ps (p-p) | 1,2 |
| | t _{jphPCIeG2-CC} | PCIe Gen 2 Hi Band (5.0 GT/s) | | 0.19 | 0.25 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen 2 Lo Band (5.0 GT/s) | | 0.09 | 0.13 | 3.1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG3-CC} | PCIe Gen 3 (8.0 GT/s) | | 0.10 | 0.13 | 1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG4-CC} | PCIe Gen 4 (16.0 GT/s) | | 0.10 | 0.13 | 0.5 | ps (RMS) | 1,2,3,4 |
| t _{jphPCIeG5-CC} | PCIe Gen 5 (32.0 GT/s) | | 0.032 | 0.042 | 0.15 | ps (RMS) | 1,2,3,5 | |
| PCIe Phase Jitter, High Bandwidth ZDB Mode (SRIS Architecture) | t _{jphPCIeG1-SRIS} | PCIe Gen 1 (2.5 GT/s) | | 8.61 | 8.63 | N/A | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen 2 (5.0 GT/s) | | 0.88 | 0.96 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen 3 (8.0 GT/s) | | 0.354 | 0.375 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen 4 (16.0 GT/s) | | 0.271 | 0.305 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG5-SRIS} | PCIe Gen 5 (32.0 GT/s) | | 0.097 | 0.109 | | ps (RMS) | 1,2,6 |

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

³ SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

⁴ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁵ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁶ The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A “rule-of-thumb” SRIS limit would be either $0.5\text{ps RMS}/\sqrt{2} = 0.35\text{ps RMS}$ if the clock chip is far from the clock input, or $0.7\text{ps RMS}/\sqrt{2} = 0.5\text{ps RMS}$ if the clock chip is near the clock input.

Table 14. Additive PCIe Phase Jitter for Fanout Buffer Mode

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limits | Units | Notes |
|---|-----------------------------|-------------------------------|---------|---------|---------|----------|----------|---------|
| Additive PCIe Phase Jitter, Fanout Buffer Mode ⁷ (Common Clocked Architecture) | t _{jphPCIeG1-CC} | PCIe Gen 1 (2.5 GT/s) | | 1.3 | 1.9 | 86 | ps (p-p) | 1,2 |
| | t _{jphPCIeG2-CC} | PCIe Gen 2 Hi Band (5.0 GT/s) | | 0.089 | 0.126 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen 2 Lo Band (5.0 GT/s) | | 0.023 | 0.034 | 3.1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG3-CC} | PCIe Gen 3 (8.0 GT/s) | | 0.044 | 0.062 | 1 | ps (RMS) | 1,2 |
| | t _{jphPCIeG4-CC} | PCIe Gen 4 (16.0 GT/s) | | 0.044 | 0.062 | 0.5 | ps (RMS) | 1,2,3,4 |
| t _{jphPCIeG5-CC} | PCIe Gen 5 (32.0 GT/s) | | 0.017 | 0.024 | 0.15 | ps (RMS) | 1,2,3,5 | |
| Additive PCIe Phase Jitter, Fanout Buffer Mode ⁷ (SRIS Architecture) | t _{jphPCIeG1-SRIS} | PCIe Gen 1 (2.5 GT/s) | | 0.127 | 0.181 | N/A | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen 2 (5.0 GT/s) | | 0.112 | 0.159 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen 3 (8.0 GT/s) | | 0.029 | 0.042 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen 4 (16.0 GT/s) | | 0.031 | 0.043 | | ps (RMS) | 1,2,6 |
| | t _{jphPCIeG5-SRIS} | PCIe Gen 5 (32.0 GT/s) | | 0.027 | 0.038 | | ps (RMS) | 1,2,6 |

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

³ SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

⁴ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁵ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

⁶ The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A “rule-of-thumb” SRIS limit would be either $0.5\text{ps RMS}/\sqrt{2} = 0.35\text{ps RMS}$ if the clock chip is far from the clock input, or $0.7\text{ps RMS}/\sqrt{2} = 0.5\text{ps RMS}$ if the clock chip is near the clock input.

⁷ Additive jitter for RMS values is calculated by solving for “b” where $b = \sqrt{c^2 - a^2}$ and “a” is rms input jitter and “c” is rms output jitter.

Table 15. Filtered Phase Jitter Parameters – QPI/UPI, IF-UPI and DB2000Q

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------------------|-------------------------|--|---------|---------|---------|----------------------|----------|-------|
| Phase Jitter, ZDB Mode | t _{jphQPI_UPI} | QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.16 | 0.37 | 0.5 | ps (RMS) | 1,2 |
| | | QPI and UPI (100MHz, 8.0Gb/s, 12UI) | | 0.10 | 0.15 | 0.3 | ps (RMS) | 1,2 |
| | | QPI and UPI (100MHz, ≤11.4Gb/s, 12UI) | | 0.08 | 0.12 | 0.2 | ps (RMS) | 1,2 |
| Additive Phase Jitter, Fanout Mode | t _{jphQPI_UPI} | QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.03 | 0.05 | N/A | ps (RMS) | 1,2,3 |
| | | QPI and UPI (100MHz, 8.0Gb/s, 12UI) | | 0.03 | 0.05 | | ps (RMS) | 1,2,3 |
| | | QPI and UPI (100MHz, ≤11.4Gb/s, 12UI) | | 0.02 | 0.04 | | ps (RMS) | 1,2,3 |
| | t _{jphIF-UPI} | IF-UPI, Lo-BW ZDB Mode | | 0.10 | 0.13 | 1 | ps (RMS) | 1,4,5 |
| | | IF-UPI, Hi-BW ZDB Mode | | 0.17 | 0.20 | 1 | ps (RMS) | 1,4,5 |
| | | IF-UPI, Fanout Mode | | 0.06 | 0.07 | 1 | ps (RMS) | 1,4 |
| | t _{jphDB2000Q} | DB2000Q, Fanout Mode | | 28 | 39 | 80 | fs (RMS) | 1,4,5 |

¹ Applies to all differential outputs, guaranteed by design and characterization. See [Test Loads](#) for measurement setup details.

² Calculated from Intel-supplied clock jitter tool.

³ For RMS values, additive jitter is calculated by solving for “b” where $b = \sqrt{c^2 - a^2}$, “a” is rms input jitter and “c” is rms total jitter.

⁴ Calculated from phase noise analyzer with Intel-specified brick-wall filter applied. This is an additive jitter specification regardless of buffer operating mode.

⁵ The IF-UPI specification is an additive specification, regardless of the buffer operating mode. The enhanced 9ZXL devices meet this specification in all operating modes.

Table 16. Phase Jitter Parameters – 12kHz to 20MHz

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|---|----------------------------|-------------------------------------|---------|---------|---------|----------------------|----------|-------|
| 12kHz–20MHz Additive Phase Jitter, Fanout Buffer Mode | t _{jph12k-20MFOB} | Fanout Buffer Mode, SSC OFF, 100MHz | | 98 | 125 | N/A | fs (RMS) | 1,2,3 |

¹ Applies to all differential outputs, guaranteed by design and characterization. See [Test Loads](#) for measurement setup details.

² 12kHz to 20MHz brick wall filter.

³ For RMS values, additive jitter is calculated by solving for “b” where $b = \sqrt{c^2 - a^2}$, “a” is rms input jitter and “c” is rms total jitter.

Power Management

Table 17. Power Management

| CKPWRGD_PD# | DIF_IN | SMBus EN bit | OE[5:12]# Pin (9ZXL1951D only) | DIF[x] | PLL State (in ZDB Mode) |
|-------------|---------|--------------|-----------------------------------|---------|----------------------------|
| 0 | X | X | X | Low/Low | Off |
| 1 | Running | 0 | 0 | Low/Low | On |
| | | 0 | 1 | Low/Low | On |
| | | 1 | 0 | Running | On |
| | | 1 | 1 | Low/Low | On |

Table 18. Functionality at Power-Up (ZDB Mode)

| 100M_133M# | DIF_IN (MHz) | DIF[x] |
|------------|--------------|--------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

Note: 9ZXL1951D is 100MHz only.

Table 19. PLL Operating Mode

| HIBW_BYPM_LOBW# | Mode | PLL |
|-----------------|-----------|---------|
| Low | ZDB Lo BW | Running |
| Mid | Bypass | Off |
| High | ZDB Hi BW | Running |

Note: See SMBus Byte 0, bits 7 and 6 for additional information.

Test Loads

Figure 4. Test Load for AC/DC Measurements

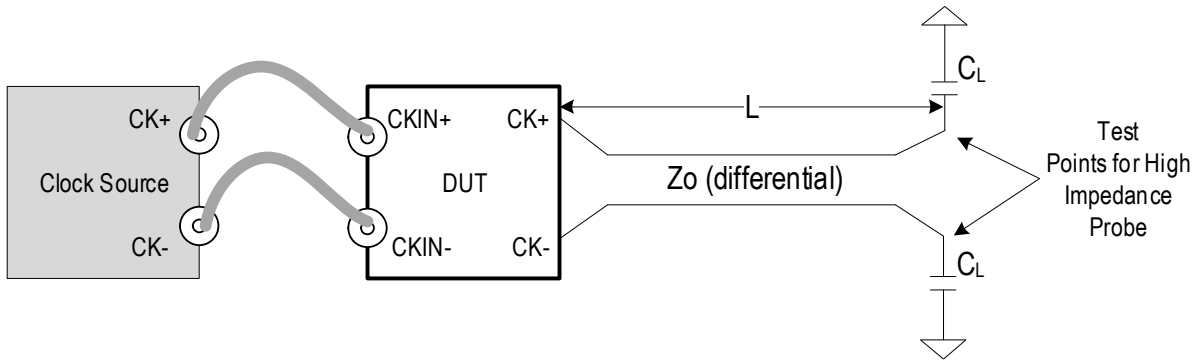


Table 20. Parameters for AC/DC Measurements

| Clock Source | Device Under Test (DUT) | Rs (Ω) | Differential Zo (Ω) | L (cm) | CL (pF) | Parameters Measured |
|--------------|-------------------------|-----------------|------------------------------|--------|---------|---------------------|
| SMA100B | 9ZXLxx3x | 27 External | 85 | 25.4 | 2 | AC/DC parameters |
| SMA100B | 9ZXLxx5x | Internal | 85 | 25.4 | 2 | |

Figure 5. Test Load for Phase Jitter Measurements using Phase Noise Analyzer

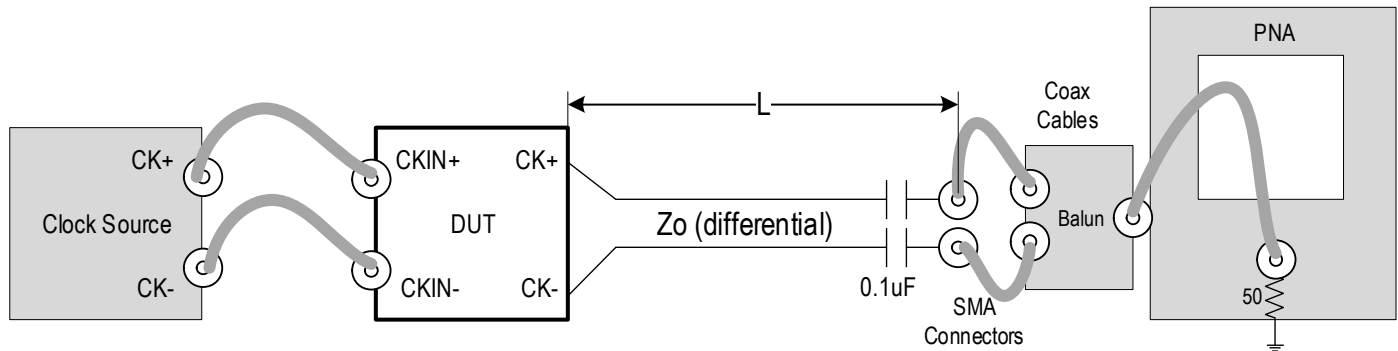


Table 21. Parameters for Phase Jitter Measurements using Phase Noise Analyzer

| Clock Source | Device Under Test (DUT) | Rs (Ω) | Differential Zo (Ω) | L (cm) | CL (pF) | Notes | Parameters Measured |
|--------------|-------------------------|-----------------|------------------------------|--------|---------|-------------|-----------------------|
| SMA100B | 9ZXLxx3x | 27 External | 85 | 25.4 | N/A | Fanout Mode | PCIe, IF-UPI, DB2000Q |
| 9FGV1006 | 9ZXLxx3x | 27 External | 85 | 25.4 | | ZDB Mode | |
| SMA100B | 9ZXLxx5x | Internal | 85 | 25.4 | | Fanout Mode | |
| 9FGV1006 | 9ZXLxx5x | Internal | 85 | 25.4 | | ZDB Mode | |

Figure 6. Test Load for Phase Jitter Measurements using Oscilloscope

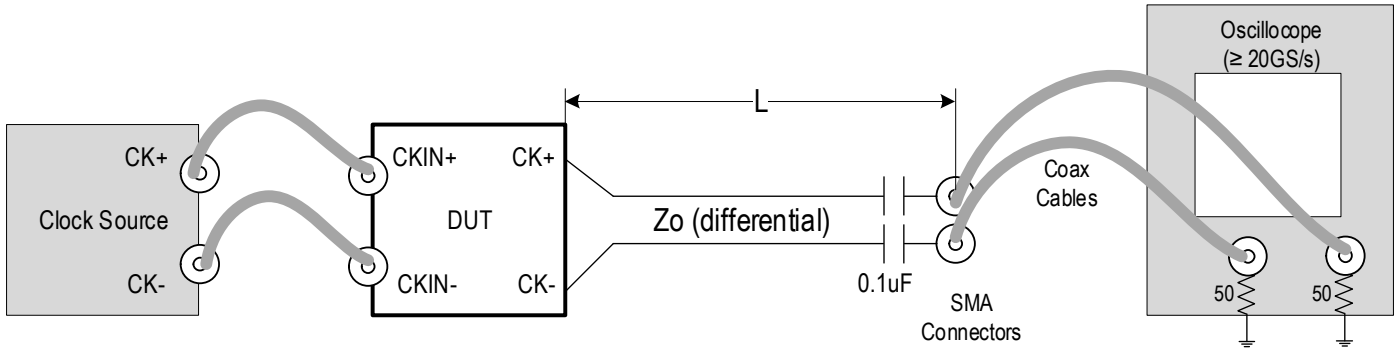


Table 22. Parameters for Phase Jitter Measurements using Oscilloscope

| Clock Source | Device Under Test (DUT) | R_s (Ω) | Differential Z_o (Ω) | L (cm) | C_L (pF) | Notes | Parameters Measured |
|--------------|-------------------------|--------------------|---------------------------------|--------|------------|-------------|---------------------|
| SMA100B | 9ZXLxx3x | 27 External | 85 | 25.4 | N/A | Fanout Mode | QPI/UPI |
| 9FGV1006 | 9ZXLxx3x | 27 External | 85 | 25.4 | | ZDB Mode | |
| SMA100B | 9ZXLxx5x | Internal | 85 | 25.4 | | Fanout Mode | |
| 9FGV1006 | 9ZXLxx5x | Internal | 85 | 25.4 | | ZDB Mode | |

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending **Byte N–Byte N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|--------------------------|
| Controller (Host) | | Renesas (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | |
| | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends **Byte N+X-1**
- Renesas clock sends **Byte 0–Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|--------------|--------------------------|
| Controller (Host) | | Renesas (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| ACK | | |
| ACK | | Beginning Byte N |
| O | | O |
| O | | O |
| O | | O |
| | | Byte N + X - 1 |
| N | Not | |
| P | stoP bit | |

Table 23. SMBus Addressing

| SADR[1:0]_tri | SMBus Address (Read/Write bit = 0) |
|---------------|------------------------------------|
| 00 | D8 |
| 0M | DA |
| 01 | DE |
| M0 | C2 |
| MM | C4 |
| M1 | C6 |
| 10 | CA |
| 1M | CC |
| 11 | CE |

Table 24. Byte 0: PLL Mode, Frequency Select and Output Enable Register 0

| Byte 0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------|-------------------------------|-------------------------------|------------------------------|------------------------------|------------------------------|----------|----------|---------------------------|
| Control Function | PLL Operating Mode Readback 1 | PLL Operating Mode Readback 0 | Output Enable | | | Reserved | Reserved | Frequency Select Readback |
| Type | R | R | RW | RW | RW | | | R |
| 0 | 00 = Low BW ZDB Mode | 01 = Bypass (Fanout Buffer) | Output is Disabled (Low/Low) | Output is Disabled (Low/Low) | Output is Disabled (Low/Low) | | | 133MHz |
| 1 | 10 = Reserved | 11 = High BW ZDB Mode | Output is Enabled | Output is Enabled | Output is Enabled | 100MHz | | |
| 9ZXL19x0 Name | PLL_Mode[1] | PLL_Mode[0] | DIF18_En | DIF17_En | DIF16_En | Reserved | Reserved | 100M_133M# |
| 9ZXL19x0 Default | Latch | Latch | 1 | 1 | 1 | 0 | 0 | Latch |
| 9ZXL15x0 Name | PLL_Mode[1] | PLL_Mode[0] | Reserved | DIF14_En | DIF13_En | Reserved | Reserved | 100M_133M# |
| 9ZXL15x0 Default | Latch | Latch | 0 | 1 | 1 | 0 | 0 | Latch |
| 9ZXL1951 Name | PLL_Mode[1] | PLL_Mode[0] | DIF18_En | DIF17_En | DIF16_En | Reserved | Reserved | Reserved |
| 9ZXL1951 Default | Latch | Latch | 1 | 1 | 1 | 0 | 0 | 0 |

Table 25. Byte 1: Output Control Register 1

| Byte 1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|---|----------|---------|---------|---------|---------|---------|----------|
| Control Function | Output Enable | | | | | | | |
| Type | RW | | | | | | | |
| 0 | Disabled (Low/Low) | | | | | | | |
| 1 | Output Enabled or Output controlled by OE# pin (DIF[5:12] on 9ZXL1951 only) | | | | | | | |
| 9ZXL19x0 Name | DIF7_en | DIF6_en | DIF5_en | DIF4_en | DIF3_en | DIF2_en | DIF1_en | DIF0_en |
| 9ZXL19x0 Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9ZXL15x0 Name | DIF5_En | Reserved | DIF4_En | DIF3_En | DIF2_En | DIF1_En | DIF0_En | Reserved |
| 9ZXL15x0 Default | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 9ZXL1951 Name | DIF7_En | DIF6_En | DIF5_En | DIF4_En | DIF3_En | DIF2_En | DIF1_En | DIF0_En |
| 9ZXL1951 Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Table 26. Byte 2: Output Control Register 2

| Byte 2 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|---|----------|----------|----------|----------|----------|---------|----------|
| Control Function | Output_enable | | | | | | | |
| Type | RW | | | | | | | |
| 0 | Low/Low | | | | | | | |
| 1 | Output Enabled or Output controlled by OE# pin (DIF[5:12] on 9ZXL1951 only) | | | | | | | |
| 9ZXL19x0 Name | DIF15_En | DIF14_En | DIF13_En | DIF12_En | DIF11_En | DIF10_En | DIF9_En | DIF8_En |
| 9ZXL19x0 Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9ZXL15x0 Name | DIF5_En | Reserved | DIF4_En | DIF3_En | DIF2_En | DIF1_En | DIF0_En | Reserved |
| 9ZXL15x0 Default | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 9ZXL1951 Name | DIF12_En | DIF11_En | DIF10_En | Reserved | DIF9_En | DIF8_En | DIF7_En | DIF6_En |
| 9ZXL1951 Default | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

Table 27. Byte 3: Output Amplitude and PLL Software Control Register

| Byte 3 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|---|--------|--------|----------|------------------------------|-------------------------------------|----------------------|----------|
| Control Function | Global Differential Amplitude Control | | | Reserved | Enable S/W control of PLL BW | PLL Operating Mode 1 | PLL Operating Mode 0 | Reserved |
| Type | RW | RW | RW | | RW | RW | RW | |
| 0 | 0.3V–1V 100mV/step Default = 0.8V (101) | | | | Hardware Latch | See definition of Byte 0, bits[7:6] | | |
| 1 | | | | | SMBus Control | | | |
| 9ZXL19x0 Name | amp[2] | amp[1] | amp[0] | Reserved | PLL_SW_EN | PLL_Mode[1] | PLL_Mode[0] | Reserved |
| 9ZXL19x0 Default | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 9ZXL15x0 Name | amp[2] | amp[1] | amp[0] | Reserved | PLL_SW_EN | PLL_Mode[1] | PLL_Mode[0] | Reserved |
| 9ZXL15x0 Default | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 9ZXL1951 Name | Reserved | | | Reserved | PLL_SW_EN | PLL_Mode[1] | PLL_Mode[0] | Reserved |
| 9ZXL1951 Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Note: Setting bit 3 to '1' allows the user to override the Latch value from pin 4 via use of bits 2 and 1. Use the values from the PLL Operating Mode Table. Note that Byte 0, Bits 7:6 will keep the value originally latched. A warm reset of the system will have to be accomplished if the user changes these bits.

Table 28. Byte 4: OE Pin Configuration Register A

| Byte 4 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|-------------------------------------|----------------------|----------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Control Function | OE12# Controls DIF12 | OE11# Controls DIF11 | OE10# Controls DIF10 | OE9# Controls DIF9 | OE8# Controls DIF8 | OE7# Controls DIF7 | OE6# Controls DIF6 | OE5# Controls DIF5 |
| Type | RW | RW | RW | RW | RW | RW | RW | RW |
| 0 | OE# pin does not control the output | | | | | | | |
| 1 | OE# pin controls the output | | | | | | | |
| 9ZXL19x0 Name | Reserved | | | | | | | |
| 9ZXL19x0 Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9ZXL15x0 Name | Reserved | | | | | | | |
| 9ZXL15x0 Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9ZXL1951 Name | OE12#_CFG | OE11#_CFG | OE10#_CFG | OE9#_CFG | OE8#_CFG | OE7#_CFG | OE6#_CFG | OE5#_CFG |
| 9ZXL1951 Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 29. Byte 5: Revision and Vendor ID Register

| Byte 5 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|-------------|-------|-------|-------|--------------------|-------|-------|-------|
| Control Function | Revision ID | | | | Vendor ID | | | |
| Type | R | R | R | R | R | R | R | R |
| 0 | Revision ID | | | | IDT/Renesas = 0001 | | | |
| 1 | | | | | | | | |
| Name | RID 3 | RID 2 | RID 1 | RID 0 | VID 3 | VID 2 | VID 1 | VID 0 |
| 9ZXL19x0 Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 9ZXL15x0 Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 9ZXL1951 Default | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

Table 30. Byte 6: Device ID Register

| Byte 6 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|---------------|---------|---------|---------|---------|---------|---------|---------|
| Control Function | N/A | | | | | | | |
| Type | R | R | R | R | R | R | R | R |
| 0 | Device ID | | | | | | | |
| 1 | | | | | | | | |
| Name | DevID 7 (MSB) | DevID 6 | DevID 5 | DevID 4 | DevID 3 | DevID 2 | DevID 1 | DevID 0 |
| 9ZXL19x0 | 0hC3 | | | | | | | |
| 9ZXL15x0 | 0h9B | | | | | | | |
| 9ZXL1951 | 0hC4 | | | | | | | |

Table 31. Byte 7: Byte Count Register

| Byte 7 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------------------|----------|----------|----------|---|------|------|------|------|
| Control Function | Reserved | Reserved | Reserved | Writing to this register configures how many bytes will be read back on a block read. | | | | |
| Type | | | | RW | RW | RW | RW | RW |
| 0 | | | | Default value is 8. | | | | |
| 1 | | | | | | | | |
| Name | | | | BC4 | BC3 | BC2 | BC1 | BC0 |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Table 32. Byte 8: OE Pin Configuration Register B (9ZXL1951 only)

| Byte 8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------|-------------------------------------|-------------------------|-------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| Control Function | OE12# Controls DIF13 | OE11# Controls DIF14 | OE10# Controls DIF15 | OE9# Controls DIF0 | OE8# Controls DIF1 | OE7# Controls DIF2 | OE6# Controls DIF3 | OE5# Controls DIF4 |
| Type | RW | RW | RW | RW | RW | RW | RW | RW |
| 0 | OE# pin does not control the output | | | | | | | |
| 1 | OE# pin controls the output | | | | | | | |
| 9ZXL1951 Name | OE12#_CFGB | OE11#_CFGB | OE10#_CFGB | OE09#_CFGB | OE08#_CFGB | OE07#_CFGB | OE06#_CFGB | OE05#_CFGB |
| 9ZXL1951 Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

9ZXL15x0D:

www.idt.com/document/psc/64-vfqfpn-package-outline-drawing-90-x-90-x-09-mm-body-05mm-pitch-epad-615-x-615-mm-nlg64p2

9ZXL19x0D:

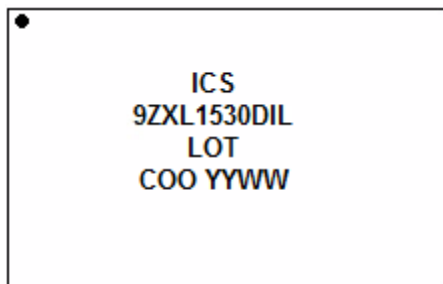
www.idt.com/document/psc/72-vfqfpn-package-outline-drawing-100-x-100-x-090-mm-body-epad-595-x-595-mm-050mm-pitch-nlg72p1

9ZXL1951D:

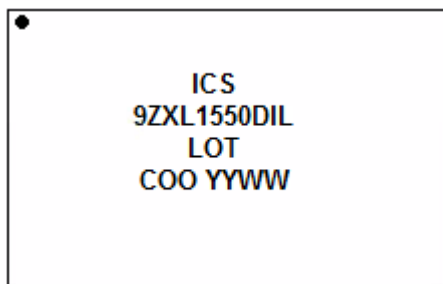
www.idt.com/document/psc/nhg80-package-outline-600x600mm-body-050mm050mm-pitch-gqfn

Marking Diagrams

9ZXL15x0D



- Lines 1 and 2: truncated part number.
- Line 3: "LOT" denotes the lot number.
- Line 4: "COO" denotes country of origin; "YYWW" is the last two digits of the year and the work week the part was assembled.



9ZXL19x0D

●

ICS
9ZXL1930DKIL
LOT
COO YYWW

- Lines 1 and 2: truncated part number.
- Line 3: "LOT" denotes the lot number.
- Line 4: "COO" denotes country of origin; "YYWW" is the last two digits of the year and the work week the part was assembled.

●

ICS
9ZXL1950DKIL
LOT
COO YYWW

9ZXL1951D

IDT9ZXL1
951DNHGI
YYWW\$

● LOT

- Lines 1 and 2: part number.
- Line 3:
 - "YYWW" is the last two digits of the year and the work week the part was assembled.
 - "\$" denotes the mark code.
- "LOT" denotes the lot number.

Ordering Information

Table 33. Ordering Information

| Number of Clock Outputs | Output Impedance | Orderable Part Number | Package | Temperature | Part Number Suffix and Shipping Method |
|-------------------------|------------------|-----------------------|-------------------------------|-------------------|---|
| 15 | 33 | 9ZXL1530DKILF | 9 × 9 × 0.5 mm 64-VFQFPN | -40°C to +85°C | None = Trays "T" or "8" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 34 for more details) |
| | | 9ZXL1530DKILFT | | | |
| | 85 | 9ZXL1550DKILF | | | |
| | | 9ZXL1550DKILFT | | | |
| 19 | 33 | 9ZXL1930DKILF | 10 × 10 × 0.5 mm 72-VFQFPN | -40°C to +85°C | |
| | | 9ZXL1930DKILFT | | | |
| | 85 | 9ZXL1950DKILF | | | |
| | | 9ZXL1950DKILFT | | | |
| 19 | 85 | 9ZXL1951DNHGI | 6 × 6 × 0.5 mm 80-GQFN | -40°C to +85°C | |
| | | 9ZXL1951DNHGI8 | | | |

"D" is the device revision designator (will not correlate with the datasheet revision).

"LF" or "G" denotes Pb-free configuration, RoHS compliant.

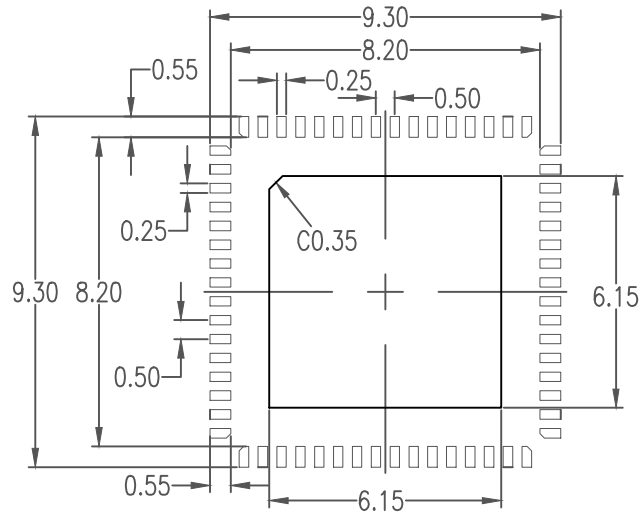
"T" or "8" is the orderable suffix for Tape and Reel packaging.

Table 34. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|---|
| T or 8 | Quadrant 1 (EIA-481-C) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |

Revision History

| Revision Date | Description of Change |
|-------------------|---|
| August 25, 2020 | Updated PCIe Gen5 CC, DB2000Q, and QPI/UPI specifications in <i>Key Specifications</i> section on front page. |
| October 30, 2019 | Updated default values of Byte 3, bits 1 and 2. |
| October 22, 2019 | Combined 9ZXL1530D_1550D, 9ZXL1930D_1950D, and 9ZXL1951D datasheets into one single document. |
| February 14, 2019 | Last revision date of the 9ZXL1530D_1550D datasheet. |
| April 24, 2019 | Last revision date of the 9ZXL1930D_1950D datasheet. |
| February 26, 2019 | Last revision date of the 9ZXL1951D datasheet. |

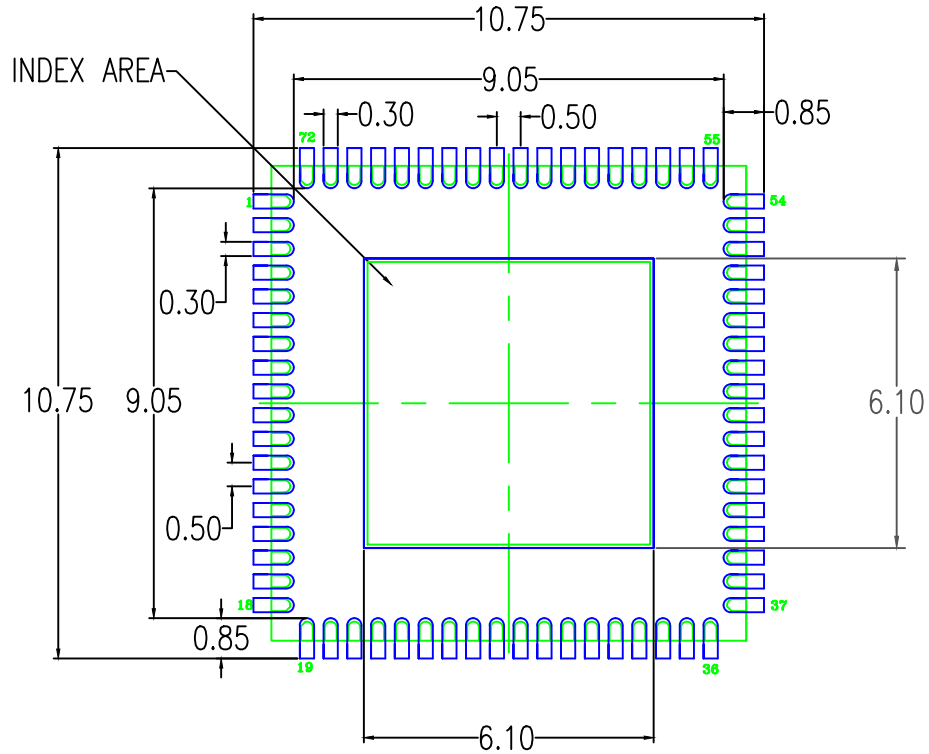


RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

| Package Revision History | | |
|--------------------------|---------|--|
| Date Created | Rev No. | Description |
| Feb 21, 2018 | Rev 01 | New Format, Change QFN to VFQFPN, Added P2 |
| Nov 3, 2015 | Rev 00 | Initial Release |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|--------------------------|---------|--|
| Date Created | Rev No. | Description |
| Sept 3, 2019 | Rev 03 | Update P1 Dimension from 5.8 to 5.95 mm SQ |
| May 8, 2017 | Rev 02 | Change Package Code QFN to VFQFPN |