A1 Flash Memory Controller

hyperstone®


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A1

Flash Memory Controller

The Hyperstone A1 family of Flash Memory Controllers together with provided application and flash specific firmware offers an easy-to-use turnkey platform for high endurance flash disks of various form factors and interface standards.

- Patented superior read and write wear leveling together with up to 24-Bit ECC ensuring highest reliability and endurance
- Exceptional power fail robustness
- Optimized 32-Bit RISC core, instruction set and firmware for flash handling
- Dual channel controller provides optimal performance
- Most power efficient design together with power saving features
- S.M.A.R.T. features supported
- ASSP with minimal external active components
- Turnkey solution including firmware, manufacturing kit, test and development hardware, and reference schematics for CF card or 2.5" solid state disk
- Custom features can be implemented with simple firmware upgrades

Targeted Applications

- High reliability & industrial Compact Flash™ Cards (CFC)
- Solid State Disks (SSD)
- IDE Disk-on-Modules (DoM)
- Embedded Flash
- Multi-Chip-Modules (MCM)
- Multi-Chip-Package (MCP)
- PCMCIA or ATA PC cards
- Disk-on-Board

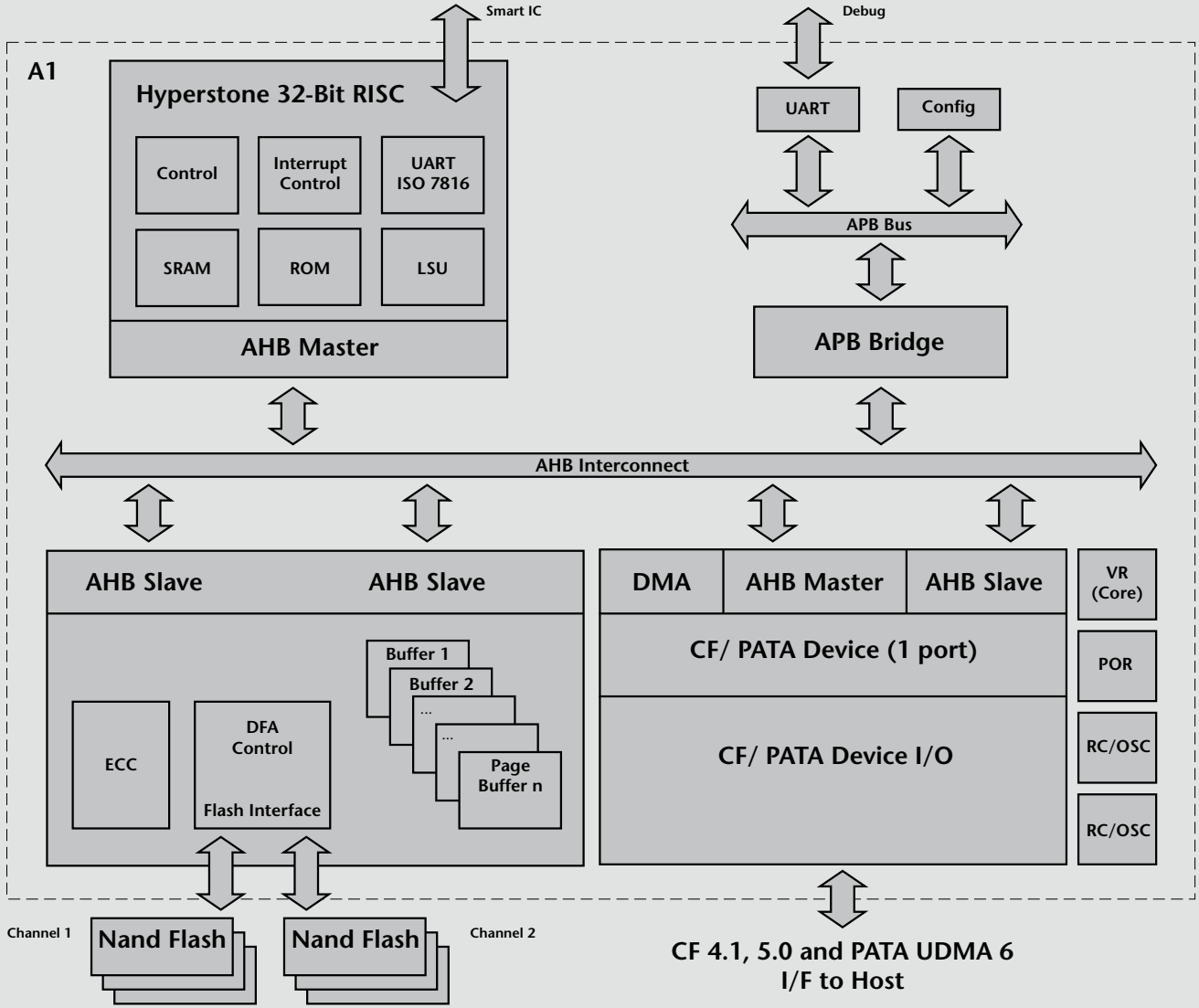
Order Information

- A1-LBT06 --- TQFP 128, 16 CEs, RoHS, 0 to +70 °C
- A1-ILBT06 --- TQFP 128, 16 CEs, RoHS, -40 to +85 °C
- A1-LBT06U --- TQFP 128, 8 CEs, ISO7816, UART, RoHS, 0 to +70 °C
- A1-ILBT06U --- TQFP 128, 8 CEs, ISO7816, UART, RoHS, -40 to +85 °C
- A1-LBL07 --- LQFP 144, 16 CEs, RoHS, 0 to +70°C
- A1-ILBL07 --- LQFP 144, 16 CEs, RoHS, -40 to +85°C
- A1-0BBD0 --- KGD / Wafer, 16 CEs, ISO7816, UART

Compliance & Performance

- Fully compliant to CompactFlash™ 4.1 and compatible to 5.0 specifications
- Fast ATA supporting PIO mode 6, MDMA mode 4, UDMA mode 6 in True-IDE mode
- PCMCIA specification version 2.1
- Configurable as removable, hot swappable, and fixed drive
- Sustained read up to 60 MB/s
- Sustained write up to 60 MB/s
- 4K random write IOPS: up to 300
- Host data transfer rate in PIO mode 6 or MDMA mode 4 up to 25 MB/s
- Host data transfer rate in UDMA mode 6 up to 133 MB/s
- CF current consumption < 100mA

A1 Block Diagram



Controller & CPU

- High performance 32-Bit Hyperstone RISC microprocessor
- 20 to 80 MHz clock frequency using adjustable internal oscillator
- Large internal RAM provides firmware flexibility
- Supply voltage 3.3V ± 10%
- 5V tolerant host side I/O
- On-chip switching voltage regulator for 1.5V core power supply
- Internal voltage detector

Host Interface & Compliance

- Fully compliant to CompactFlash™ 4.1 and compatible to CF 5.0 specifications
- Fast ATA supporting PIO mode 6, MDMA mode 4, UDMA mode 6 in True-IDE mode
- PCMCIA specification version 2.1
- Configurable as removable, hot swappable, and fixed drive
- Memory mapped or I/O operation
- Automatic sensing of PCMCIA or True-IDE mode
- PCMCIA attribute memory
- PCMCIA configuration option register, card configuration and status register and pin replacement register support

Flash Memory Interface & Handling

- Dual channel with two direct flash memory access (DFA) units including sector buffers and interleaving capability
- Supporting all control signals for NAND type flash memory connection
- Asynchronous SDR interface, ONFI 1.0 compliant and compatible with ONFI 2.x.
- Supporting direct connection of up to 16 flash memory chip enables (CE) - eight per channel
- Flash memory power down logic and flash memory write protect control
- BCH Error Correcting Code (ECC) capable of correcting 6 or 8 Bit in a 512 bytes sector and 24 Bit in a 1024 bytes double-sector with additional CRC
- Supporting all flash technologies MLC and SLC
- LBA 48 Support to design drives larger than 128 GB
- Power down detection for increased power cycling robustness
- Capacitor buffered power down and write recovery possible
- Automatic power-down during wait periods, power saving including automatic wake-up and sleep mode with Icc < 1 mA
- CF current consumption < 100 mA
- Flash management including mapping of logical block addresses (LBA) to corresponding physical block addresses (PBA)
- Bad Block Management
- Minimal Write Amplification
- Static and Global Wear Leveling to maximize write endurance
- Read Wear leveling to maximize data retention and refresh data subject to read disturbance
- Sudden power-fail management
- Interleaving, cache, and multi-plane programming
- Firmware is stored in NAND Flash and loaded into internal memory by the boot ROM
- Firmware can be stored redundantly for recovery and for periodic refresh
- Future Flashes can be supported by simple firmware upgrades
- Customized firmware, optimizations and feature implementations possible upon request