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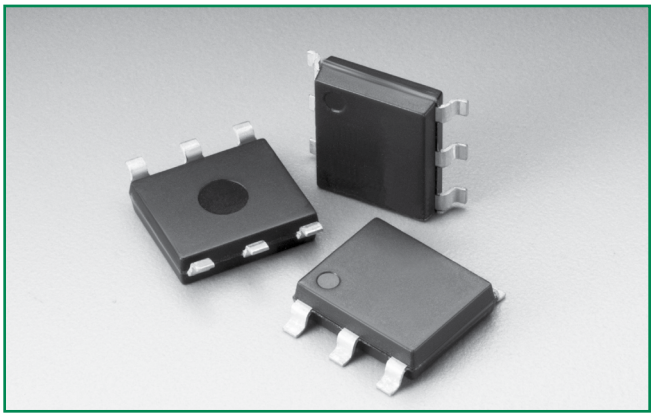
SIDACtor® Protection Thyristors
LCAS Protection

Asymmetrical Multiport Series - MS-013



Description

Asymmetrical Multiport Series are SIDACtor® components designed to protect LCAS (Line Circuit Access Switch) devices from damaging overvoltage transients.
The series provides a specialized asymmetrical dual port overvoltage protection solution that enables equipment to comply with various global requlatory standards.

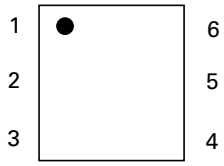
Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Replaces four discrete components
- Two-port protection
- RoHS Compliant, Lead-Free and Halogen Free
- LCAS specific tip and ring thresholds
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin (Sn) (IPC/JEDEC J-STD-609A.01)

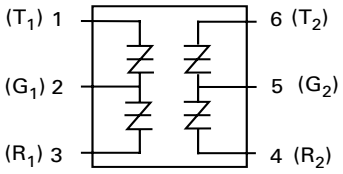
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Part Marking	V_{DRM} @I_{DRM} = 5µA	V_S @100V/µs	V_{DRM} @I_{DRM} = 5µA	V_S @100V/µs	V_T@I_T = 2.2 Amps	I_S mA	I_T A	I_H mA
		V	V	V	V	V			
		Pins 2-3, 5-6		Pins 1-2, 4-5		Pins 1-2, 2-3, 4-5, 5-6			
A1220UA4Lxx	A1220UA4	100	130	180	220	4	800	2.2	120
A1225UA4Lxx	A1250UA4	100	130	230	290	4	800	2.2	120
A1220UC4Lxx	A1220UC4	100	130	180	220	4	800	2.2	120
A1225UC4Lxx	A1250UC4	100	130	230	290	4	800	2.2	120

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- All electrical characteristics shown are defined from Tip to Ground (pin 1 to pin 2 and pin 6 to pin 5) and Ring to Ground (pin 3 to pin 2 and pin 4 to pin 5).
- XX = Part Number Suffix: 'TP' (Tube Pack) or 'RP' (Reel Pack).

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Capacitance Values

Part Number	pF Pin 1-2 / 4-5 Ring-Ground		pF Pin 3-2 / 6-5 Tip-Ground		pF Pin 1-3 (4-6) Tip-Ring	
	MIN	MAX	MIN	MAX	MIN	MAX
A1220UA4Lxx	15	25	30	50	5	20
A1225UA4Lxx	15	25	30	50	5	20
A1220UC4Lxx	35	50	60	90	20	35
A1225UC4Lxx	35	50	60	90	20	35

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Surge Ratings

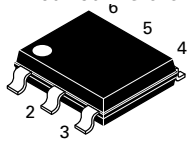
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

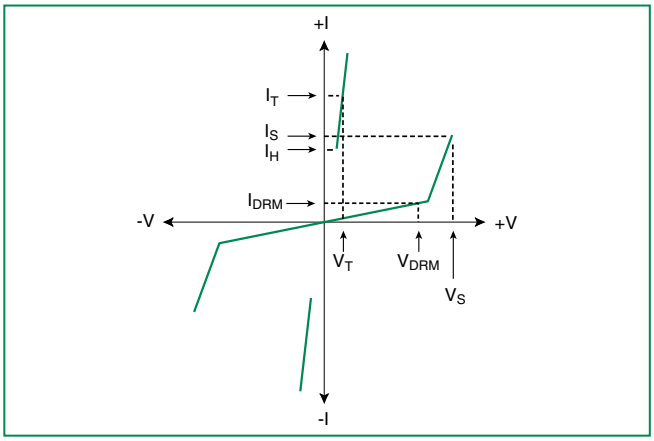
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

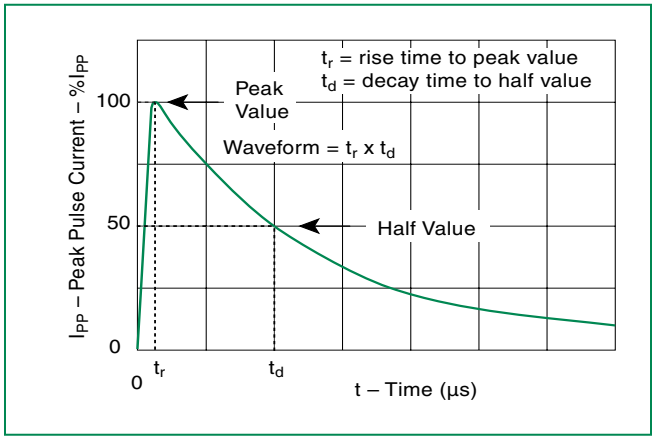
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

V-I Characteristics



t_r x t_d Pulse Waveform



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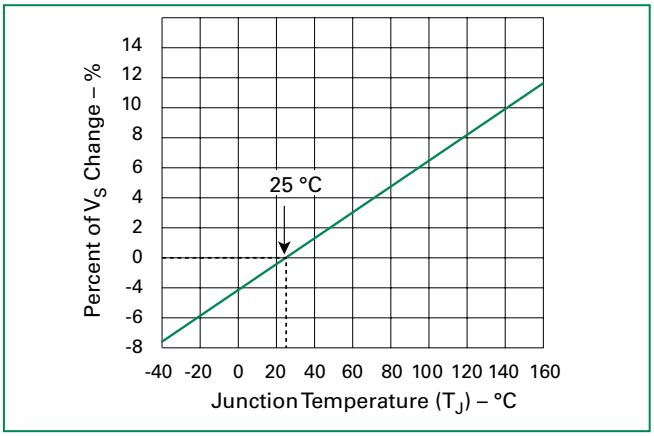
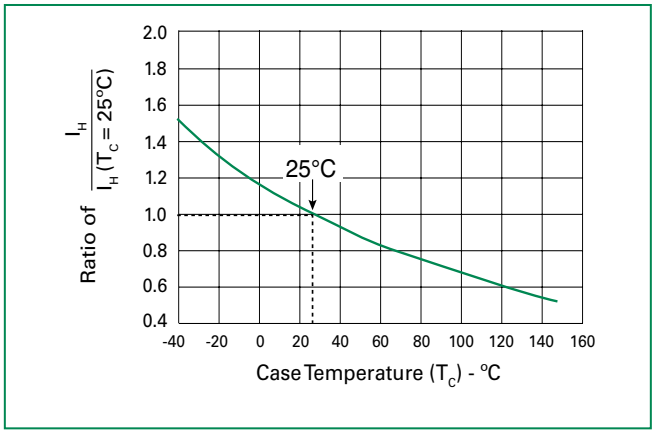
Normalized V_S Change vs. Junction Temperature



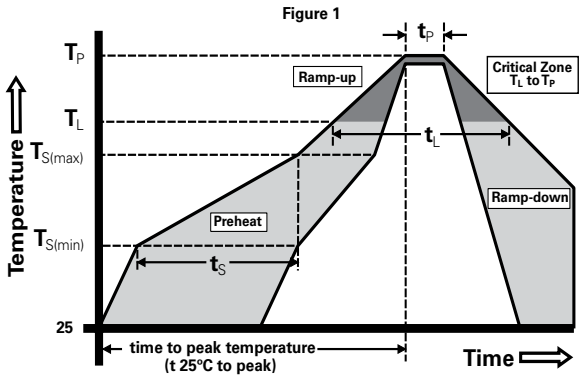
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

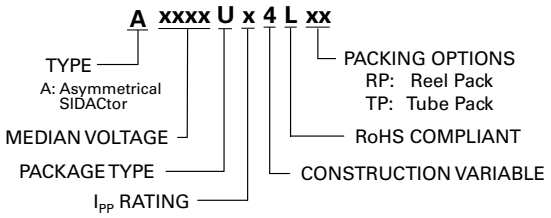
Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

Part Numbering



Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

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