

ProASIC3E Flash Family FPGAs with Optional Soft ARM Support

DS0098

Features and Benefits

High Capacity

- 600 k to 3 Million System Gates
- 108 to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

On-Chip User Nonvolatile Memory

- 1 kbit of FlashROM with Synchronous Interfacing

High Performance

- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI

In-System Programming (ISP) and Security

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532-compliant)
- FlashLock[®] Designed to Secure FPGA Contents

Low Power

- Core Voltage for Low Power
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- Ultra-Fast Local and Long-Line Network
- Enhanced High-Speed, Very-Long-Line Network
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Pro (Professional) I/O

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay
- Schmitt Trigger Option on Single-Ended Inputs
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC[®]3E Family

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, Each with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback
- Wide Input Frequency Range (1.5 MHz to 350 MHz)

SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation up to 350 MHz

ARM[®] Processor Support in ProASIC3E FPGAs

- M1 ProASIC3E Devices—Cortex-M1 Soft Processor Available with or without Debug

Table 1-1 • ProASIC3E Product Family

| ProASIC3E Devices | A3PE600 | A3PE1500 | A3PE3000 |
|--|--------------|-----------------------|------------------------------|
| Cortex-M1 Devices ¹ | | M1A3PE1500 | M1A3PE3000 |
| System Gates | 600,000 | 1,500,000 | 3,000,000 |
| VersaTiles (D-flip-flops) | 13,824 | 38,400 | 75,264 |
| RAM Kbits (1,024 bits) | 108 | 270 | 504 |
| 4,608-Bit Blocks | 24 | 60 | 112 |
| FlashROM Kbits | 1 | 1 | 1 |
| Secure (AES) ISP | Yes | Yes | Yes |
| CCCs with Integrated PLLs ² | 6 | 6 | 6 |
| VersaNet Globals ³ | 18 | 18 | 18 |
| I/O Banks | 8 | 8 | 8 |
| Maximum User I/Os | 270 | 444 | 620 |
| Package Pins PQFP FBGA | FG256, FG484 | PQ208 FG484, FG676 | PQ208 FG324, FG484, FG896 |

Notes:

1. Refer to the [Cortex-M1 product brief](#) for more information.
2. The PQ208 package supports six CCCs and two PLLs.
3. Six chip (main) and three quadrant global networks are available.
4. For devices supporting lower densities, refer to the [ProASIC3 Flash Family FPGAs datasheet](#).

I/Os Per Package¹

| ProASIC3E Devices | A3PE600 | | A3PE1500 ³ | | A3PE3000 ³ | |
|--------------------------------|-------------------------------|------------------------|-------------------------------|------------------------|-------------------------------|------------------------|
| Cortex-M1 Devices ² | | | M1A3PE1500 | | M1A3PE3000 | |
| Package | I/O Types | | | | | |
| | Single-Ended I/O ¹ | Differential I/O Pairs | Single-Ended I/O ¹ | Differential I/O Pairs | Single-Ended I/O ¹ | Differential I/O Pairs |
| PQ208 | – | – | 147 | 65 | 147 | 65 |
| FG256 | 165 | 79 | – | – | – | – |
| FG324 | – | – | – | – | 221 | 110 |
| FG484 | 270 | 135 | 280 | 139 | 341 | 168 |
| FG676 | – | – | 444 | 222 | – | – |
| FG896 | – | – | – | – | 620 | 310 |

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3E FPGA Fabric User's Guide](#) to ensure compliance with design and board migration requirements.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:
 - SSTL3(I) and (II): up to 40 I/Os per north or south bank
 - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
 - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
- FG256 and FG484 are footprint-compatible packages.
- When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).
- "G" indicates RoHS-compliant packages. Refer to the ["ProASIC3E Ordering Information"](#) on page III for the location of the "G" in the part number.

Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions

| Package | PQ208 | FG256 | FG324 | FG484 | FG676 | FG896 |
|---------------------------------|---------|---------|---------|---------|---------|---------|
| Length × Width (mm\mm) | 28 × 28 | 17 × 17 | 19 × 19 | 23 × 23 | 27 × 27 | 31 × 31 |
| Nominal Area (mm ²) | 784 | 289 | 361 | 529 | 729 | 961 |
| Pitch (mm) | 0.5 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| Height (mm) | 3.40 | 1.60 | 1.63 | 2.23 | 2.23 | 2.23 |

ProASIC3E Device Status

| ProASIC3E Devices | Status | M1 ProASIC3E Devices | Status |
|-------------------|------------|----------------------|------------|
| A3PE600 | Production | | |
| A3PE1500 | Production | M1A3PE1500 | Production |
| A3PE3000 | Production | M1A3PE3000 | Production |

ProASIC3E Ordering Information



ProASIC3E Devices

- A3PE600 = 600,000 System Gates
- A3PE1500 = 1,500,000 System Gates
- A3PE3000 = 3,000,000 System Gates

ProASIC3E Devices with Cortex-M1

- M1A3PE1500 = 1,500,000 System Gates
- M1A3PE3000 = 3,000,000 System Gates

Temperature Grade Offerings

| Package | A3PE600 | A3PE1500 | A3PE3000 |
|--------------------------|---------|-------------------|-------------------|
| Cortex-M1 Devices | | M1A3PE1500 | M1A3PE3000 |
| PQ208 | – | C, I | C, I |
| FG256 | C, I | – | – |
| FG324 | – | – | C, I |
| FG484 | C, I | C, I | C, I |
| FG676 | – | C, I | – |
| FG896 | – | – | C, I |

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature
 I = Industrial temperature range: –40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

| Temperature Grade | Std. | –1 | –2 |
|-------------------|------|----|----|
| C ¹ | ✓ | ✓ | ✓ |
| I ² | ✓ | ✓ | ✓ |

Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature
2. I = Industrial temperature range: –40°C to 85°C ambient temperature

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability:
www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article.

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1 – ProASIC3E Device Family Overview

General Description

ProASIC3E, the third-generation family of Microsemi flash FPGAs, offers performance, density, and features beyond those of the ProASIC^{PLUS}® family. Nonvolatile flash technology gives ProASIC3E devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to three million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

Several ProASIC3E devices support the Cortex-M1 soft IP cores, and the ARM-Enabled devices have Microsemi ordering numbers that begin with M1A3PE.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3E devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3E devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3E devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3E devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3E family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3E device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to

be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3E FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based ProASIC3E devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC3E devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3E device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3E devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3E flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3E FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3E devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3E devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3E devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The ProASIC3E family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

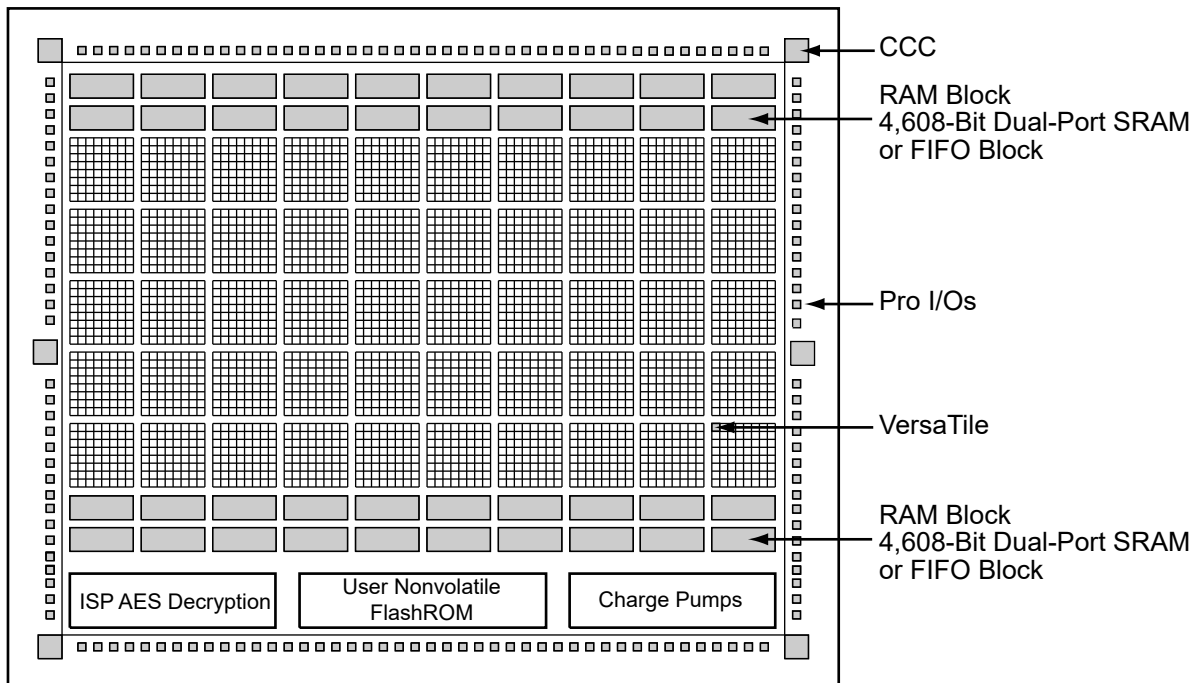


Figure 1-1 • ProASIC3E Device Architecture Overview

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-2](#) for VersaTile configurations.

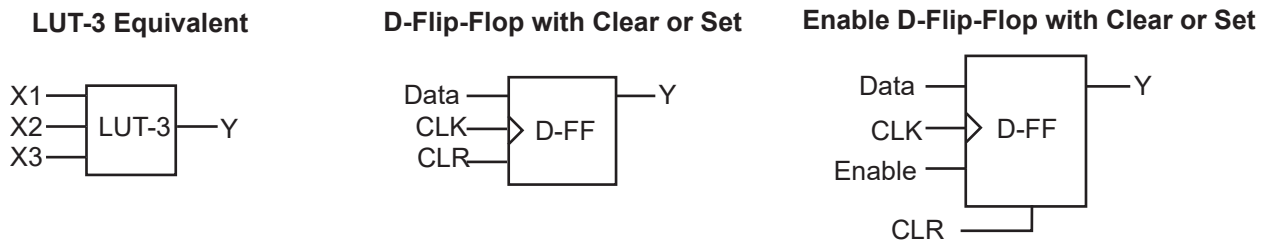


Figure 1-2 • VersaTile Configurations

User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero[®] System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port.

For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from -7.56 ns to $+11.12$ ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0° , 90° , 180° , and 270° . Output phase shift depends on the output divider configuration.
- Output duty cycle = $50\% \pm 1.5\%$ or better
- Low output jitter: worst case $< 2.5\% \times$ clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = $300 \mu\text{s}$
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of $40 \text{ ps} \times (350 \text{ MHz} / f_{OUT_CCC})$

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the [FlashPro User's Guide](#) for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-3 on page 1-7](#)).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High
 - 0 – I/O is set to drive out logic Low
 - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
 - Z -Tri-State: I/O is tristated

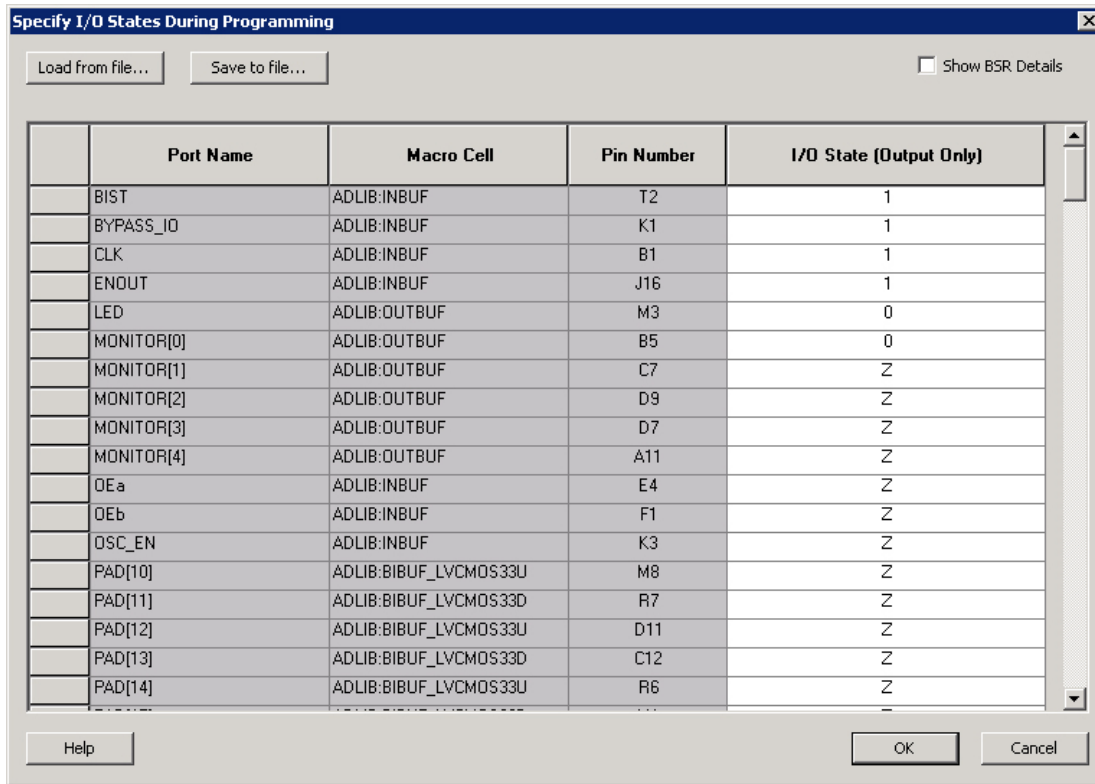


Figure 1-3 • I/O States During Programming Window

6. Click OK to return to the FlashPoint – Programming File Generator window.
I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – ProASIC3E DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

| Symbol | Parameter | Limits | Units |
|-------------------------------|-------------------------------------|---|-------|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI ² | DC I/O output buffer supply voltage | –0.3 to 3.75 | V |
| VMV ² | DC I/O input buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| T _{STG} ³ | Storage temperature | –65 to +150 | °C |
| T _J ³ | Junction temperature | +125 | °C |

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-3 on page 2-2](#).
2. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on [page 3-1](#) for further information.
3. For flash programming and retention maximum limits, refer to [Table 2-3 on page 2-2](#), and for recommended operating limits, refer to [Table 2-2 on page 2-2](#).

Table 2-2 • Recommended Operating Conditions¹

| Symbol | Parameter | Commercial | Industrial | Units | |
|---------------------------|--------------------------------------|-------------------------------|----------------|--------------|---|
| T _A | Ambient temperature | 0 to +70 | –40 to +85 | °C | |
| T _J | Junction temperature | 0 to +85 | –40 to +100 | °C | |
| VCC | 1.5 V DC core supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| VJTAG | JTAG DC voltage | 1.4 to 3.6 | 1.4 to 3.6 | V | |
| VPUMP | Programming voltage | Programming Mode ² | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation ³ | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| VCCI and VMV ⁴ | 1.5 V DC supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| | 1.8 V DC supply voltage | 1.7 to 1.9 | 1.7 to 1.9 | V | |
| | 2.5 V DC supply voltage | 2.3 to 2.7 | 2.3 to 2.7 | V | |
| | 3.3 V DC supply voltage | 3.0 to 3.6 | 3.0 to 3.6 | V | |
| | 3.0 V DC supply voltage ⁵ | 2.7 to 3.6 | 2.7 to 3.6 | V | |
| | LVDS/B-LVDS/M-LVDS differential I/O | 2.375 to 2.625 | 2.375 to 2.625 | V | |
| | LVPECL differential I/O | 3.0 to 3.6 | 3.0 to 3.6 | V | |

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. The programming temperature range supported is $T_{ambient} = 0^{\circ}\text{C}$ to 85°C .
3. VPUMP can be left floating during normal operation (not programming mode).
4. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-13 on page 2-17](#). VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "[VMVx I/O Supply Voltage \(quiet\)](#)" section on [page 3-1](#) for further information.
5. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.
6. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature¹

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature T _{STG} (°C) ² | Maximum Operating Junction Temperature T _J (°C) ² |
|---------------|--------------------|-------------------------------------|--|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits¹

| VCCI and VMV | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ² | Maximum Overshoot/Undershoot ² |
|---------------|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC[®]3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#).

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1 on page 2-4](#)).
2. $VCCI > VCC - 0.75\text{ V}$ (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$
 Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$

VCC Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$
 Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLXL exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-4 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3E FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

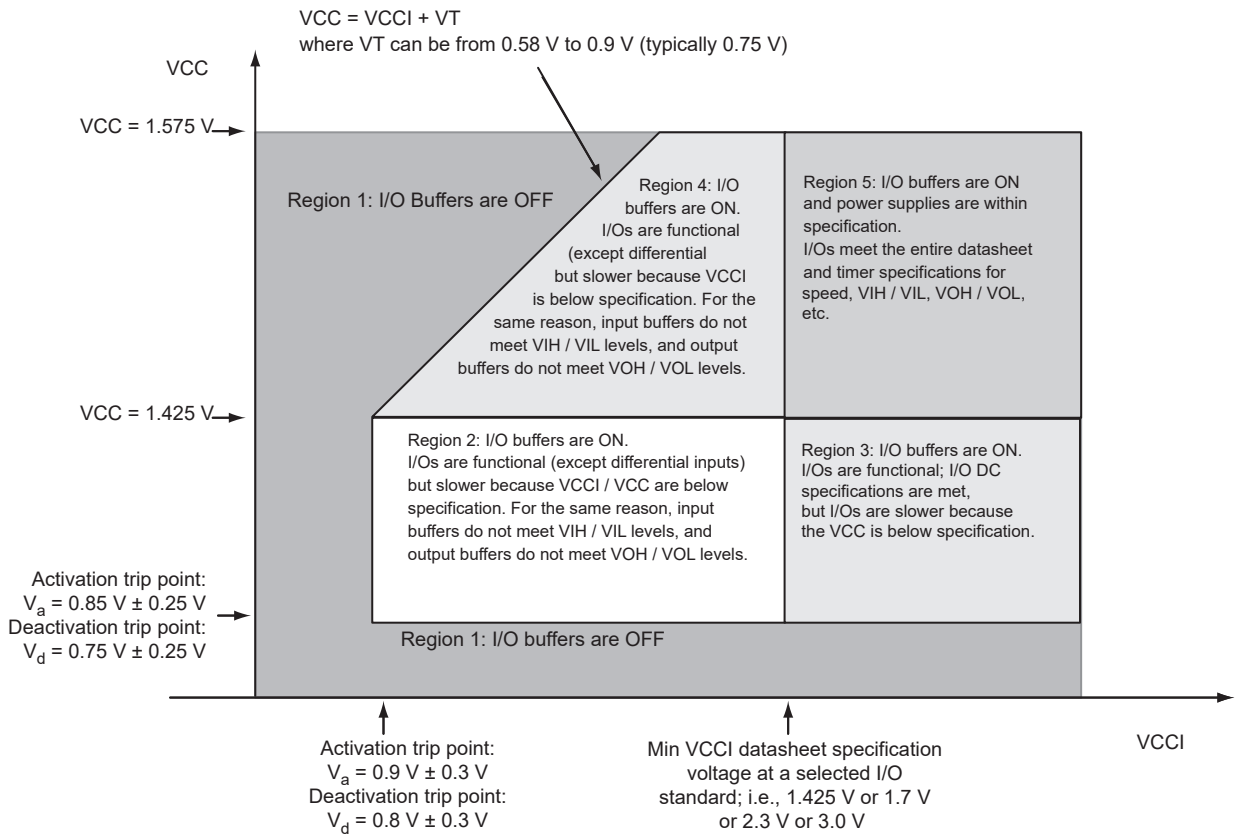


Figure 2-1 • I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in [Table 2-5](#).

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (\text{}^\circ\text{C/W)}} = \frac{110^\circ\text{C} - 70^\circ\text{C}}{13.6^\circ\text{C/W}} = 5.88 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

| Package Type | Pin Count | θ_{jc} | θ_{ja} | | | Units |
|--|-----------|---------------|---------------|--------------|--------------|-------|
| | | | Still Air | 200 ft./min. | 500 ft./min. | |
| Plastic Quad Flat Package (PQFP) | 208 | 8.0 | 26.1 | 22.5 | 20.8 | C/W |
| Plastic Quad Flat Package (PQFP) with embedded heat spreader in A3PE3000 | 208 | 3.8 | 16.2 | 13.3 | 11.9 | C/W |
| Fine Pitch Ball Grid Array (FBGA) | 256 | 3.8 | 26.9 | 22.8 | 21.5 | C/W |
| | 484 | 3.2 | 20.5 | 17.0 | 15.9 | C/W |
| | 676 | 3.2 | 16.4 | 13.0 | 12.0 | C/W |
| | 896 | 2.4 | 13.6 | 10.4 | 9.4 | C/W |

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$)

| Array Voltage VCC (V) | Junction Temperature ($^\circ\text{C}$) | | | | | |
|--------------------------|---|-------------------|--------------------|--------------------|--------------------|---------------------|
| | -40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.425 | 0.87 | 0.92 | 0.95 | 1.00 | 1.02 | 1.04 |
| 1.500 | 0.83 | 0.88 | 0.90 | 0.95 | 0.97 | 0.98 |
| 1.575 | 0.80 | 0.85 | 0.87 | 0.92 | 0.93 | 0.95 |

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

| | A3PE600 | A3PE1500 | A3PE3000 |
|--------------------------------|---------|----------|----------|
| Typical (25°C) | 5 mA | 12 mA | 25 mA |
| Maximum (Commercial) | 30 mA | 70 mA | 150 mA |
| Maximum (Industrial) | 45 mA | 105 mA | 225 mA |

Notes:

1. I_{DD} Includes V_{CC} , V_{PUMP} , V_{CCI} , and V_{MV} currents. Values do not include I/O static contribution, which is shown in Table 2-8 and Table 2-9 on page 2-7.
2. $-F$ speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.

Power per I/O Pin

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

| | VMV (V) | Static Power PDC2 (mW) ¹ | Dynamic Power PAC9 ($\mu\text{W}/\text{MHz}$) ² |
|---|------------|--|---|
| Single-Ended | | | |
| 3.3 V LVTTTL/LVCMOS | 3.3 | – | 17.39 |
| 3.3 V LVTTTL/LVCMOS – Schmitt trigger | 3.3 | – | 25.51 |
| 3.3 V LVTTTL/LVCMOS Wide Range ³ | 3.3 | – | 16.34 |
| 3.3 V LVTTTL/LVCMOS Wide Range – Schmitt trigger ³ | 3.3 | – | 24.49 |
| 2.5 V LVCMOS | 2.5 | – | 5.76 |
| 2.5 V LVCMOS – Schmitt trigger | 2.5 | – | 7.16 |
| 1.8 V LVCMOS | 1.8 | – | 2.72 |
| 1.8 V LVCMOS – Schmitt trigger | 1.8 | – | 2.80 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 2.08 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt trigger | 1.5 | – | 2.00 |
| 3.3 V PCI | 3.3 | – | 18.82 |

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VCC and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings (continued)

| | VMV (V) | Static Power PDC2 (mW) ¹ | Dynamic Power PAC9 (μW/MHz) ² |
|-------------------------------|---------|-------------------------------------|--|
| 3.3 V PCI – Schmitt trigger | 3.3 | – | 20.12 |
| 3.3 V PCI-X | 3.3 | – | 18.82 |
| 3.3 V PCI-X – Schmitt trigger | 3.3 | – | 20.12 |
| Voltage-Referenced | | | |
| 3.3 V GTL | 3.3 | 2.90 | 8.23 |
| 2.5 V GTL | 2.5 | 2.13 | 4.78 |
| 3.3 V GTL+ | 3.3 | 2.81 | 4.14 |
| 2.5 V GTL+ | 2.5 | 2.57 | 3.71 |
| HSTL (I) | 1.5 | 0.17 | 2.03 |
| HSTL (II) | 1.5 | 0.17 | 2.03 |
| SSTL2 (I) | 2.5 | 1.38 | 4.48 |
| SSTL2 (II) | 2.5 | 1.38 | 4.48 |
| SSTL3 (I) | 3.3 | 3.21 | 9.26 |
| SSTL3 (II) | 3.3 | 3.21 | 9.26 |
| Differential | | | |
| LVDS/B-LVDS/M-LVDS | 2.5 | 2.26 | 1.50 |
| LVPECL | 3.3 | 5.71 | 2.17 |

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VCC and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹

| | C _{LOAD} (pF) | VCCI (V) | Static Power PDC3 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|---|------------------------|----------|-------------------------------------|---|
| Single-Ended | | | | |
| 3.3 V LVTTTL/LVCMOS | 35 | 3.3 | – | 474.70 |
| 3.3 V LVTTTL/LVCMOS Wide Range ⁴ | 35 | 3.3 | – | 474.70 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 270.73 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 151.78 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 104.55 |
| 3.3 V PCI | 10 | 3.3 | – | 204.61 |
| 3.3 V PCI-X | 10 | 3.3 | – | 204.61 |
| Voltage-Referenced | | | | |
| 3.3 V GTL | 10 | 3.3 | – | 24.08 |
| 2.5 V GTL | 10 | 2.5 | – | 13.52 |
| 3.3 V GTL+ | 10 | 3.3 | – | 24.10 |
| 2.5 V GTL+ | 10 | 2.5 | – | 13.54 |

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings (continued) (continued)¹

| | C_{LOAD} (pF) | VCCI (V) | Static Power PDC3 (mW)² | Dynamic Power PAC10 (μW/MHz)³ |
|--|---------------------------------|--------------------|---|---|
| HSTL (I) | 20 | 1.5 | 7.08 | 26.22 |
| HSTL (II) | 20 | 1.5 | 13.88 | 27.22 |
| SSTL2 (I) | 30 | 2.5 | 16.69 | 105.56 |
| SSTL2 (II) | 30 | 2.5 | 25.91 | 116.60 |
| Notes: | | | | |
| 1. Dynamic power consumption is given for standard load and software default drive strength and output slew. | | | | |
| 2. PDC3 is the static power (where applicable) measured on VCCI. | | | | |
| 3. PAC10 is the total dynamic power measured on VCC and VCCI. | | | | |
| 4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification. | | | | |
| SSTL3 (I) | 30 | 3.3 | 26.02 | 114.87 |
| SSTL3 (II) | 30 | 3.3 | 42.21 | 131.76 |
| Differential | | | | |
| LVDS/B-LVDS/M-LVDS | – | 2.5 | 7.70 | 89.62 |
| LVPECL | – | 3.3 | 19.42 | 168.02 |
| Notes: | | | | |
| 1. Dynamic power consumption is given for standard load and software default drive strength and output slew. | | | | |
| 2. PDC3 is the static power (where applicable) measured on VCCI. | | | | |
| 3. PAC10 is the total dynamic power measured on VCC and VCCI. | | | | |
| 4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification. | | | | |

Power Consumption of Various Internal Resources

Table 2-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices

| Parameter | Definition | Device-Specific Dynamic Contributions (μW/MHz) | | |
|------------------|--|---|-----------------|-----------------|
| | | A3PE600 | A3PE1500 | A3PE3000 |
| PAC1 | Clock contribution of a Global Rib | 12.77 | 16.21 | 19.7 |
| PAC2 | Clock contribution of a Global Spine | 1.85 | 3.06 | 4.16 |
| PAC3 | Clock contribution of a VersaTile row | 0.88 | | |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.12 | | |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.07 | | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.29 | | |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.29 | | |
| PAC8 | Average contribution of a routing net | 0.70 | | |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-8 on page 2-6. | | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-9 on page 2-7 | | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | | |

Table 2-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices

| Parameter | Definition | Device-Specific Dynamic Contributions (μW/MHz) | | |
|-----------|--|--|----------|----------|
| | | A3PE600 | A3PE1500 | A3PE3000 |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | | |
| PAC13 | Static PLL contribution | 2.55 mW | | |
| PAC14 | Dynamic contribution for PLL | 2.60 | | |

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-11 on page 2-12](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-12 on page 2-12](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-12 on page 2-12](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [ProASIC3E FPGA Fabric User's Guide](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [ProASIC3E FPGA Fabric User's Guide](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-12](#).

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-12](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-12](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-11 on page 2-12](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-11 on page 2-12](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-12 on page 2-12](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 2-12 on page 2-12](#).

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-12 on page 2-12](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC14 * F_{CLKOUT}$ product) to the total PLL contribution.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-11 • Toggle Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|------------|----------------------------------|-----------|
| α_1 | Toggle rate of VersaTile outputs | 10% |
| α_2 | I/O buffer toggle rate | 10% |

Table 2-12 • Enable Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|-----------|--------------------------------------|-----------|
| β_1 | I/O output buffer enable rate | 100% |
| β_2 | RAM enable rate for read operations | 12.5% |
| β_3 | RAM enable rate for write operations | 12.5% |

User I/O Characteristics

Timing Model

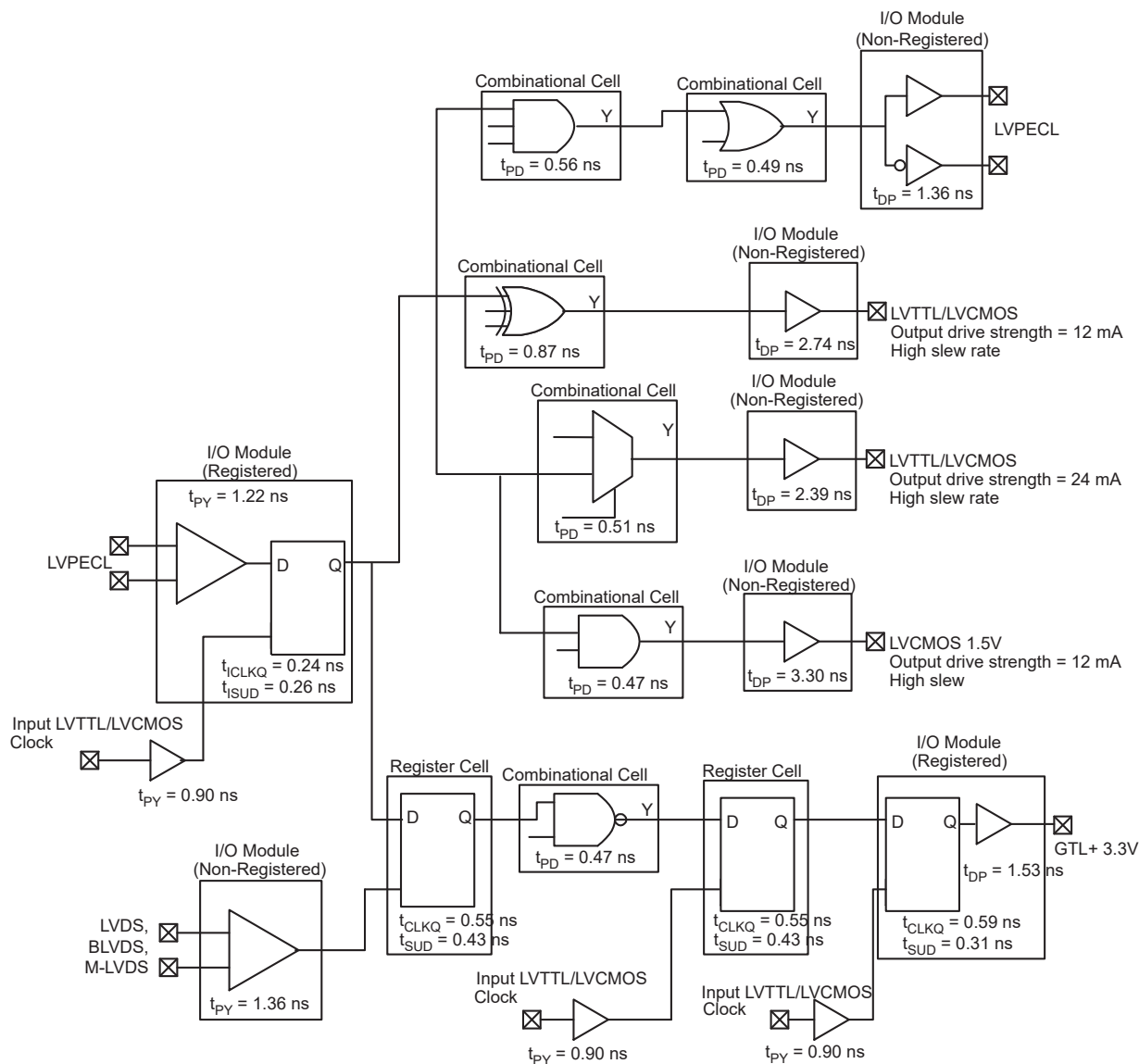
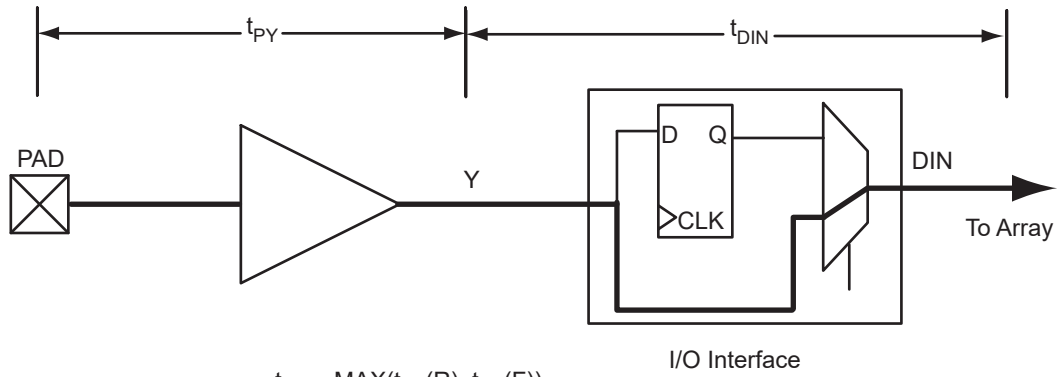


Figure 2-2 • Timing Model
 Operating Conditions: -2 Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst-Case
 $V_{CC} = 1.425\text{ V}$



$$t_{PY} = \text{MAX}(t_{PY}(R), t_{PY}(F))$$

$$t_{DIN} = \text{MAX}(t_{DIN}(R), t_{DIN}(F))$$

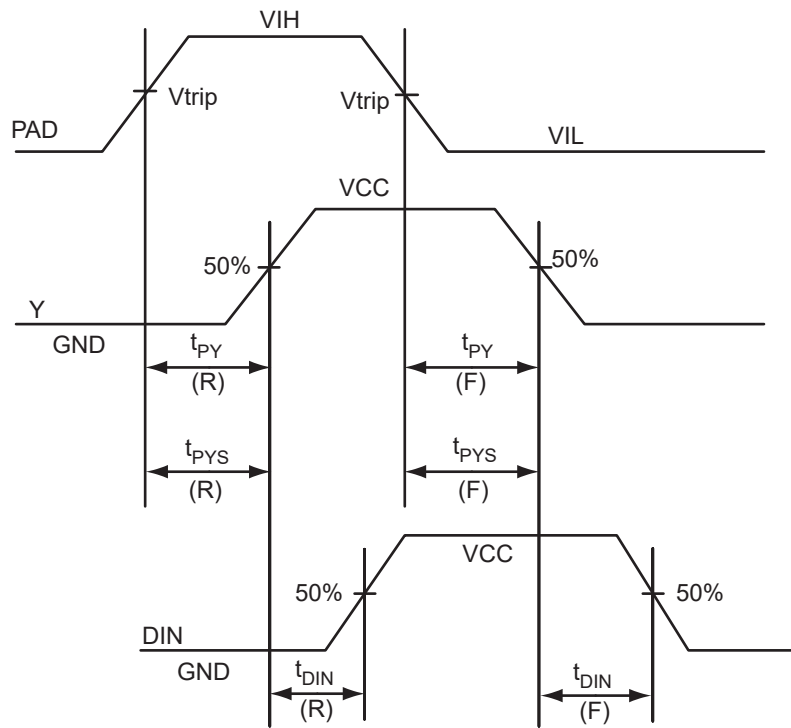


Figure 2-3 • Input Buffer Timing Model and Delays (example)

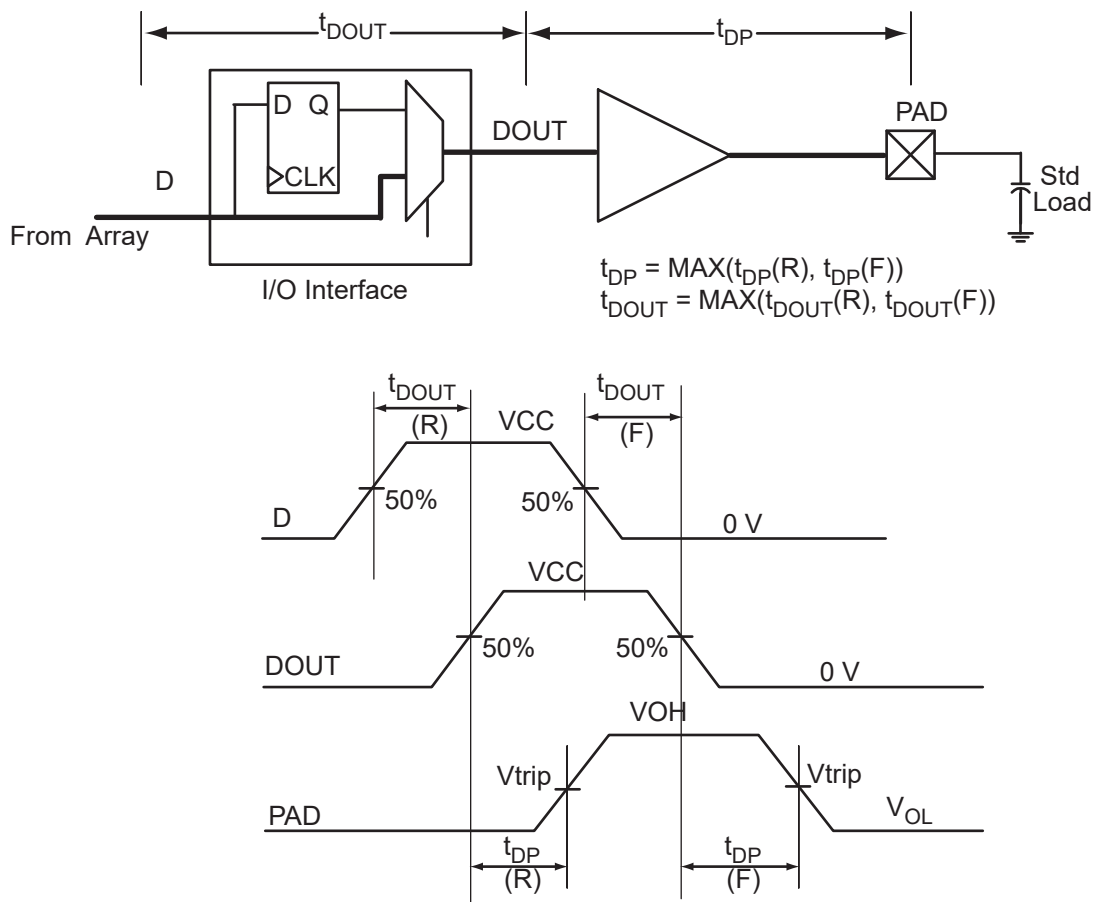


Figure 2-4 • Output Buffer Model and Delays (example)

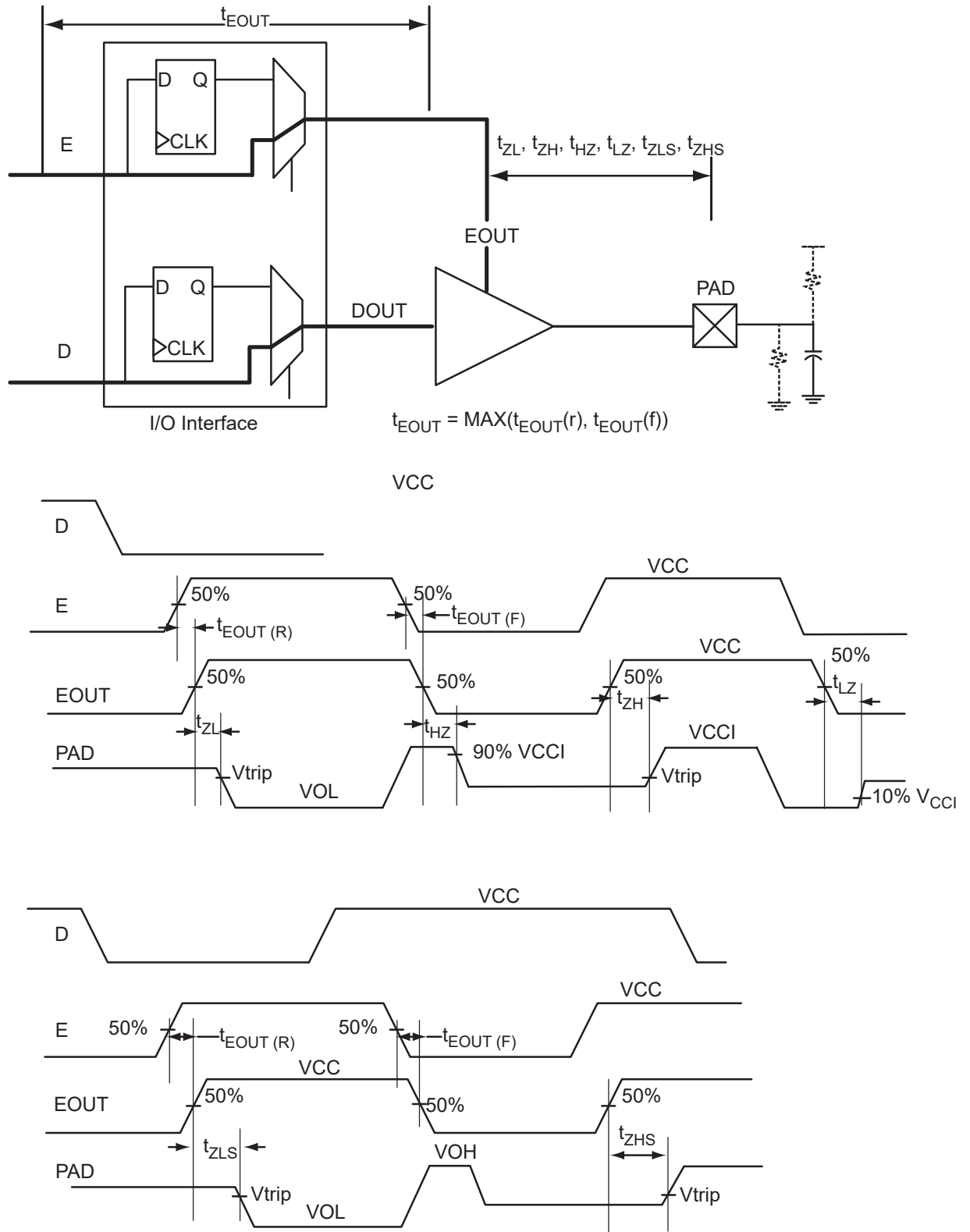


Figure 2-5 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-13 • Summary of Maximum and Minimum DC Input and Output Levels
Applicable to Commercial and Industrial Conditions**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Slew Rate | VIL | | VIH | | VOL | VOH | IOL ³ | IOH ³ |
|------------------------------|-------------------------|--|-----------|--------|-------------|-------------|--------|-------------|-------------|------------------|------------------|
| | | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVC MOS | 12 mA | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3 V LVC MOS Wide Range | 100 μ A | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI - 0.2 | 0.1 | 0.1 |
| 2.5 V LVC MOS | 12 mA | 12 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVC MOS | 12 mA | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 12 | 12 |
| 1.5 V LVC MOS | 12 mA | 12 mA | High | -0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI Specification | | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X Specification | | | | | | | | | | |
| 3.3 V GTL | 20 mA ² | 20 mA ² | High | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 |
| 2.5 V GTL | 20 mA ² | 20 mA ² | High | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 |
| 3.3 V GTL+ | 35 mA | 35 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 35 | 35 |
| 2.5 V GTL+ | 33 mA | 33 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 33 | 33 |
| HSTL (I) | 8 mA | 8 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 8 | 8 |
| HSTL (II) | 15 mA ² | 15 mA ² | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 15 | 15 |
| SSTL2 (I) | 15 mA | 15 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI - 0.62 | 15 | 15 |
| SSTL2 (II) | 18 mA | 18 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI - 0.43 | 18 | 18 |
| SSTL3 (I) | 14 mA | 14 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI - 1.1 | 14 | 14 |
| SSTL3 (II) | 21 mA | 21 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI - 0.9 | 21 | 21 |

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Output drive strength is below JEDEC specification.
3. Currents are measured at 85°C junction temperature.
4. Output Slew Rates can be extracted from IBIS Models, located at http://www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.

**Table 2-14 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions**

| DC I/O Standards | Commercial ¹ | | Industrial ² | |
|-----------------------------|-------------------------|------------------|-------------------------|------------------|
| | IIL ³ | IIH ⁴ | IIL ³ | IIH ⁴ |
| | μA | μA | μA | μA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V LVCMOS Wide Range | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V PCI | 10 | 10 | 15 | 15 |
| 3.3 V PCI-X | 10 | 10 | 15 | 15 |
| 3.3 V GTL | 10 | 10 | 15 | 15 |
| 2.5 V GTL | 10 | 10 | 15 | 15 |
| 3.3 V GTL+ | 10 | 10 | 15 | 15 |
| 2.5 V GTL+ | 10 | 10 | 15 | 15 |
| HSTL (I) | 10 | 10 | 15 | 15 |
| HSTL (II) | 10 | 10 | 15 | 15 |
| SSTL2 (I) | 10 | 10 | 15 | 15 |
| SSTL2 (II) | 10 | 10 | 15 | 15 |
| SSTL3 (I) | 10 | 10 | 15 | 15 |
| SSTL3 (II) | 10 | 10 | 15 | 15 |

Notes:

1. Commercial range ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
3. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
4. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-15 • Summary of AC Measuring Points

| Standard | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_REF) | Measuring Trip Point (Vtrip) |
|-----------------------------|------------------------------------|-------------------------------------|---|
| 3.3 V LVTTTL / 3.3 V LVCMOS | – | – | 1.4 V |
| 3.3 V LVCMOS Wide Range | – | – | 1.4 V |
| 2.5 V LVCMOS | – | – | 1.2 V |
| 1.8 V LVCMOS | – | – | 0.90 V |
| 1.5 V LVCMOS | – | – | 0.75 V |
| 3.3 V PCI | – | – | 0.285 * VCCI (RR) 0.615 * VCCI (FF)) |
| 3.3 V PCI-X | – | – | 0.285 * VCCI (RR) 0.615 * VCCI (FF) |
| 3.3 V GTL | 0.8 V | 1.2 V | VREF |
| 2.5 V GTL | 0.8 V | 1.2 V | VREF |
| 3.3 V GTL+ | 1.0 V | 1.5 V | VREF |
| 2.5 V GTL+ | 1.0 V | 1.5 V | VREF |
| HSTL (I) | 0.75 V | 0.75 V | VREF |
| HSTL (II) | 0.75 V | 0.75 V | VREF |
| SSTL2 (I) | 1.25 V | 1.25 V | VREF |
| SSTL2 (II) | 1.25 V | 1.25 V | VREF |
| SSTL3 (I) | 1.5 V | 1.485 V | VREF |
| SSTL3 (II) | 1.5 V | 1.485 V | VREF |
| LVDS | – | – | Cross point |
| LVPECL | – | – | Cross point |

Table 2-16 • I/O AC Parameter Definitions

| Parameter | Definition |
|------------|---|
| t_{DP} | Data to Pad delay through the Output Buffer |
| t_{PY} | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| t_{DOUT} | Data to Output Buffer delay through the I/O interface |
| t_{EOUT} | Enable to Output Buffer Tristate Control delay through the I/O interface |
| t_{DIN} | Input Buffer to Data delay through the I/O interface |
| t_{PYS} | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| t_{HZ} | Enable to Pad delay through the Output Buffer—High to Z |
| t_{ZH} | Enable to Pad delay through the Output Buffer—Z to High |
| t_{LZ} | Enable to Pad delay through the Output Buffer—Low to Z |
| t_{ZL} | Enable to Pad delay through the Output Buffer—Z to Low |
| t_{ZHS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| t_{ZLS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

Table 2-17 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option) ¹ | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | t_{DOUT} (ns) | t_{DP} (ns) | t_{DIN} (ns) | t_{PY} (ns) | t_{PYS} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | t_{ZLS} (ns) | t_{ZHS} (ns) |
|--------------------------------------|---------------------|---|-----------|----------------------|--------------------------------|-----------------|---------------|----------------|---------------|----------------|-----------------|---------------|---------------|---------------|---------------|----------------|----------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 2.74 | 0.03 | 0.90 | 1.17 | 0.32 | 2.79 | 2.14 | 2.45 | 2.70 | 4.46 | 3.81 |
| 3.3 V LVCMOS Wide Range ² | 100 μA | 12 | High | 35 | – | 0.49 | 4.24 | 0.03 | 1.36 | 1.78 | 0.32 | 4.24 | 3.25 | 3.78 | 4.17 | 6.77 | 5.79 |
| 2.5 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 |
| 1.8 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 |
| 1.5 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 ³ | 0.49 | 2.09 | 0.03 | 0.78 | 1.17 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 ³ | 0.49 | 2.09 | 0.03 | 0.78 | 1.17 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 |
| 3.3 V GTL | 20 ⁴ | – | High | 10 | 25 | 0.45 | 1.55 | 0.03 | 2.19 | – | 0.32 | 1.52 | 1.55 | – | – | 3.19 | 3.22 |
| 2.5 V GTL | 20 ⁴ | – | High | 10 | 25 | 0.45 | 1.59 | 0.03 | 1.83 | – | 0.32 | 1.61 | 1.59 | – | – | 3.28 | 3.26 |
| 3.3 V GTL+ | 35 | – | High | 10 | 25 | 0.45 | 1.53 | 0.03 | 1.19 | – | 0.32 | 1.56 | 1.53 | – | – | 3.23 | 3.20 |
| 2.5 V GTL+ | 33 | – | High | 10 | 25 | 0.45 | 1.65 | 0.03 | 1.13 | – | 0.32 | 1.68 | 1.57 | – | – | 3.35 | 3.24 |
| HSTL (I) | 8 | – | High | 20 | 50 | 0.49 | 2.37 | 0.03 | 1.59 | – | 0.32 | 2.42 | 2.35 | – | – | 4.09 | 4.02 |
| HSTL (II) | 15 ⁴ | – | High | 20 | 25 | 0.49 | 2.26 | 0.03 | 1.59 | – | 0.32 | 2.30 | 2.03 | – | – | 3.97 | 3.70 |
| SSTL2 (I) | 15 | – | High | 30 | 50 | 0.49 | 1.59 | 0.03 | 1.00 | – | 0.32 | 1.62 | 1.38 | – | – | 3.29 | 3.05 |
| SSTL2 (II) | 18 | – | High | 30 | 25 | 0.49 | 1.62 | 0.03 | 1.00 | – | 0.32 | 1.65 | 1.32 | – | – | 3.32 | 2.99 |
| SSTL3 (I) | 14 | – | High | 30 | 50 | 0.49 | 1.72 | 0.03 | 0.93 | – | 0.32 | 1.75 | 1.37 | – | – | 3.42 | 3.04 |
| SSTL3 (II) | 21 | – | High | 30 | 25 | 0.49 | 1.54 | 0.03 | 0.93 | – | 0.32 | 1.57 | 1.25 | – | – | 3.24 | 2.92 |
| LVDS/B-LVDS/M-LVDS | 24 | – | High | – | – | 0.49 | 1.40 | 0.03 | 1.36 | – | – | – | – | – | – | – | – |
| LVPECL | 24 | – | High | – | – | 0.49 | 1.36 | 0.03 | 1.22 | – | – | – | – | – | – | – | – |

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-39](#) for connectivity. This resistor is not required during normal operation.
4. Output drive strength is below JEDEC specification.
5. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#).

Detailed I/O DC Characteristics

Table 2-18 • Input Capacitance

| Symbol | Definition | Conditions | Min. | Max. | Units |
|--------------------|------------------------------------|----------------------------------|------|------|-------|
| C _{IN} | Input capacitance | V _{IN} = 0, f = 1.0 MHz | | 8 | pF |
| C _{INCLK} | Input capacitance on the clock pin | V _{IN} = 0, f = 1.0 MHz | | 8 | pF |

Table 2-19 • I/O Output Buffer Maximum Resistances¹

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-----------------------------|-----------------------------|---|---------------------------------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 3.3 V LVCMOS Wide Range | 100 μA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |
| 3.3 V GTL | 20 mA ⁴ | 11 | – |
| 2.5 V GTL | 20 mA ⁴ | 14 | – |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Output drive strength is below JEDEC specification.

Table 2-19 • I/O Output Buffer Maximum Resistances¹ (continued)

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|------------|--------------------|---|---------------------------------------|
| 3.3 V GTL+ | 35 mA | 12 | – |
| 2.5 V GTL+ | 33 mA | 15 | – |
| HSTL (I) | 8 mA | 50 | 50 |
| HSTL (II) | 15 mA ⁴ | 25 | 25 |
| SSTL2 (I) | 15 mA | 27 | 31 |
| SSTL2 (II) | 18 mA | 13 | 15 |
| SSTL3 (I) | 14 mA | 44 | 69 |
| SSTL3 (II) | 21 mA | 18 | 32 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Output drive strength is below JEDEC specification.

**Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | R _(WEAK PULL-UP) ¹ (Ω) | | R _(WEAK PULL-DOWN) ² (Ω) | |
|-------------------------|---|------|---|-------|
| | Min. | Max. | Min. | Max. |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 3.3 V (Wide Range I/Os) | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

Table 2-21 • I/O Short Currents IOSH/IOSL

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|-----------------------------|----------------|------------------------------|------------------------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS Wide Range | 100 μ A | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |

Notes:

1. $T_J = 100^\circ\text{C}$
2. *Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-22 • Duration of Short Circuit Event Before Failure

| Temperature | Time before Failure |
|-------------|---------------------|
| -40°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |

Table 2-22 • Duration of Short Circuit Event Before Failure (continued)

| Temperature | Time before Failure |
|-------------|---------------------|
| 85°C | 2 years |
| 100°C | 6 months |

Table 2-23 • Schmitt Trigger Input Hysteresis Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

| Input Buffer Configuration | Hysteresis Value (typ.) |
|--|-------------------------|
| 3.3 V LVTTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode) | 240 mV |
| 2.5 V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8 V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5 V LVCMOS (Schmitt trigger mode) | 60 mV |

Table 2-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|--|-----------------------------|---|------------------|
| LVTTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns * | 20 years (110°C) |
| LVTTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis. | 20 years (110°C) |
| HSTL/SSTL/GTL | No requirement | 10 ns * | 10 years (100°C) |
| LVDS/B-LVDS/M-LVDS/LVPECL | No requirement | 10 ns * | 10 years (100°C) |

Note: *For clock signals and similar edge-generating signals, refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the *ProASIC3E FPGA Fabric User's Guide*. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-25 • Minimum and Maximum DC Input and Output Levels

| 3.3 V LVTTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------------------|-----------|-----------|------------|-----------|-----------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min., V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 10 | 10 |
| 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

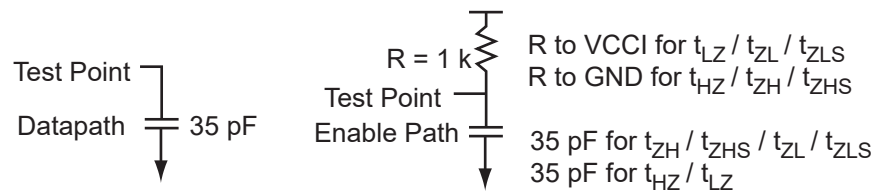


Figure 2-6 • AC Loading

Table 2-26 • 3.3 V LVTTTL / 3.3 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 3.3 | 1.4 | – | 35 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-27 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 7.88 | 0.04 | 1.20 | 1.57 | 0.43 | 8.03 | 6.70 | 2.69 | 2.59 | 10.26 | 8.94 | ns |
| | -1 | 0.56 | 6.71 | 0.04 | 1.02 | 1.33 | 0.36 | 6.83 | 5.70 | 2.29 | 2.20 | 8.73 | 7.60 | ns |
| | -2 | 0.49 | 5.89 | 0.03 | 0.90 | 1.17 | 0.32 | 6.00 | 5.01 | 2.01 | 1.93 | 7.67 | 6.67 | ns |
| 4 mA | Std. | 0.66 | 7.88 | 0.04 | 1.20 | 1.57 | 0.43 | 8.03 | 6.70 | 2.69 | 2.59 | 10.26 | 8.94 | ns |
| | -1 | 0.56 | 6.71 | 0.04 | 1.02 | 1.33 | 0.36 | 6.83 | 5.70 | 2.29 | 2.20 | 8.73 | 7.60 | ns |
| | -2 | 0.49 | 5.89 | 0.03 | 0.90 | 1.17 | 0.32 | 6.00 | 5.01 | 2.01 | 1.93 | 7.67 | 6.67 | ns |
| 6 mA | Std. | 0.66 | 5.08 | 0.04 | 1.20 | 1.57 | 0.43 | 5.17 | 4.14 | 3.05 | 3.21 | 7.41 | 6.38 | ns |
| | -1 | 0.56 | 4.32 | 0.04 | 1.02 | 1.33 | 0.36 | 4.40 | 3.52 | 2.59 | 2.73 | 6.30 | 5.43 | ns |
| | -2 | 0.49 | 3.79 | 0.03 | 0.90 | 1.17 | 0.32 | 3.86 | 3.09 | 2.28 | 2.40 | 5.53 | 4.76 | ns |
| 8 mA | Std. | 0.66 | 5.08 | 0.04 | 1.20 | 1.57 | 0.43 | 5.17 | 4.14 | 3.05 | 3.21 | 7.41 | 6.38 | ns |
| | -1 | 0.56 | 4.32 | 0.04 | 1.02 | 1.33 | 0.36 | 4.40 | 3.52 | 2.59 | 2.73 | 6.30 | 5.43 | ns |
| | -2 | 0.49 | 3.79 | 0.03 | 0.90 | 1.17 | 0.32 | 3.86 | 3.09 | 2.28 | 2.40 | 5.53 | 4.76 | ns |
| 12 mA | Std. | 0.66 | 3.67 | 0.04 | 1.20 | 1.57 | 0.43 | 3.74 | 2.87 | 3.28 | 3.61 | 5.97 | 5.11 | ns |
| | -1 | 0.56 | 3.12 | 0.04 | 1.02 | 1.33 | 0.36 | 3.18 | 2.44 | 2.79 | 3.07 | 5.08 | 4.34 | ns |
| | -2 | 0.49 | 2.74 | 0.03 | 0.90 | 1.17 | 0.32 | 2.79 | 2.14 | 2.45 | 2.70 | 4.46 | 3.81 | ns |
| 16 mA | Std. | 0.66 | 3.46 | 0.04 | 1.20 | 1.57 | 0.43 | 3.53 | 2.61 | 3.33 | 3.72 | 5.76 | 4.84 | ns |
| | -1 | 0.56 | 2.95 | 0.04 | 1.02 | 1.33 | 0.36 | 3.00 | 2.22 | 2.83 | 3.17 | 4.90 | 4.12 | ns |
| | -2 | 0.49 | 2.59 | 0.03 | 0.90 | 1.17 | 0.32 | 2.63 | 1.95 | 2.49 | 2.78 | 4.30 | 3.62 | ns |
| 24 mA | Std. | 0.66 | 3.21 | 0.04 | 1.20 | 1.57 | 0.43 | 3.27 | 2.16 | 3.39 | 4.13 | 5.50 | 4.39 | ns |
| | -1 | 0.56 | 2.73 | 0.04 | 1.02 | 1.33 | 0.36 | 2.78 | 1.83 | 2.88 | 3.51 | 4.68 | 3.74 | ns |
| | -2 | 0.49 | 2.39 | 0.03 | 0.90 | 1.17 | 0.32 | 2.44 | 1.61 | 2.53 | 3.08 | 4.11 | 3.28 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-28 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 11.01 | 0.04 | 1.20 | 1.57 | 0.43 | 11.21 | 9.05 | 2.69 | 2.44 | 13.45 | 11.29 | ns |
| | -1 | 0.56 | 9.36 | 0.04 | 1.02 | 1.33 | 0.36 | 9.54 | 7.70 | 2.29 | 2.08 | 11.44 | 9.60 | ns |
| | -2 | 0.49 | 8.22 | 0.03 | 0.90 | 1.17 | 0.32 | 8.37 | 6.76 | 2.01 | 1.82 | 10.04 | 8.43 | ns |
| 4 mA | Std. | 0.66 | 11.01 | 0.04 | 1.20 | 1.57 | 0.43 | 11.21 | 9.05 | 2.69 | 2.44 | 13.45 | 11.29 | ns |
| | -1 | 0.56 | 9.36 | 0.04 | 1.02 | 1.33 | 0.36 | 9.54 | 7.70 | 2.29 | 2.08 | 11.44 | 9.60 | ns |
| | -2 | 0.49 | 8.22 | 0.03 | 0.90 | 1.17 | 0.32 | 8.37 | 6.76 | 2.01 | 1.82 | 10.04 | 8.43 | ns |
| 6 mA | Std. | 0.66 | 7.86 | 0.04 | 1.20 | 1.57 | 0.43 | 8.01 | 6.44 | 3.04 | 3.06 | 10.24 | 8.68 | ns |
| | -1 | 0.56 | 6.69 | 0.04 | 1.02 | 1.33 | 0.36 | 6.81 | 5.48 | 2.58 | 2.61 | 8.71 | 7.38 | ns |
| | -2 | 0.49 | 5.87 | 0.03 | 0.90 | 1.17 | 0.32 | 5.98 | 4.81 | 2.27 | 2.29 | 7.65 | 6.48 | ns |
| 8 mA | Std. | 0.66 | 7.86 | 0.04 | 1.20 | 1.57 | 0.43 | 8.01 | 6.44 | 3.04 | 3.06 | 10.24 | 8.68 | ns |
| | -1 | 0.56 | 6.69 | 0.04 | 1.02 | 1.33 | 0.36 | 6.81 | 5.48 | 2.58 | 2.61 | 8.71 | 7.38 | ns |

Table 2-28 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| | -2 | 0.49 | 5.87 | 0.03 | 0.90 | 1.17 | 0.32 | 5.98 | 4.81 | 2.27 | 2.29 | 7.65 | 6.48 | ns |
| 12 mA | Std. | 0.66 | 6.03 | 0.04 | 1.20 | 1.57 | 0.43 | 6.14 | 5.02 | 3.28 | 3.47 | 8.37 | 7.26 | ns |
| | -1 | 0.56 | 5.13 | 0.04 | 1.02 | 1.33 | 0.36 | 5.22 | 4.27 | 2.79 | 2.95 | 7.12 | 6.17 | ns |
| | -2 | 0.49 | 4.50 | 0.03 | 0.90 | 1.17 | 0.32 | 4.58 | 3.75 | 2.45 | 2.59 | 6.25 | 5.42 | ns |
| 16 mA | Std. | 0.66 | 5.62 | 0.04 | 1.20 | 1.57 | 0.43 | 5.72 | 4.72 | 3.32 | 3.58 | 7.96 | 6.96 | ns |
| | -1 | 0.56 | 4.78 | 0.04 | 1.02 | 1.33 | 0.36 | 4.87 | 4.02 | 2.83 | 3.04 | 6.77 | 5.92 | ns |
| | -2 | 0.49 | 4.20 | 0.03 | 0.90 | 1.17 | 0.32 | 4.27 | 3.53 | 2.48 | 2.67 | 5.94 | 5.20 | ns |
| 24 mA | Std. | 0.66 | 5.24 | 0.04 | 1.20 | 1.57 | 0.43 | 5.34 | 4.69 | 3.39 | 3.96 | 7.58 | 6.93 | ns |
| | -1 | 0.56 | 4.46 | 0.04 | 1.02 | 1.33 | 0.36 | 4.54 | 3.99 | 2.88 | 3.37 | 6.44 | 5.89 | ns |
| | -2 | 0.49 | 3.92 | 0.03 | 0.90 | 1.17 | 0.32 | 3.99 | 3.50 | 2.53 | 2.96 | 5.66 | 5.17 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

3.3 V LVCMOS Wide Range

Table 2-29 • Minimum and Maximum DC Input and Output Levels

| 3.3 V LVCMOS Wide Range | Equivalent Software Default Drive | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ² | IIH ³ |
|-------------------------|-----------------------------------|--------|--------|--------|--------|--------|-----------|-----|-----|----------------------|----------------------|------------------|------------------|
| | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | μA | μA | Max. mA ⁴ | Max. mA ⁴ | μA ⁵ | μA ⁵ |
| 100 μA | 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 27 | 25 | 10 | 10 |
| 100 μA | 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 27 | 25 | 10 | 10 |
| 100 μA | 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 54 | 51 | 10 | 10 |
| 100 μA | 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 54 | 51 | 10 | 10 |
| 100 μA | 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 109 | 103 | 10 | 10 |
| 100 μA | 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 127 | 132 | 10 | 10 |
| 100 μA | 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 181 | 268 | 10 | 10 |

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

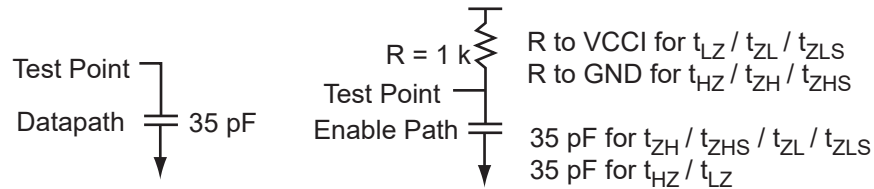


Figure 2-7 • AC Loading

Table 2-30 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 3.3 | 1.4 | - | 35 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-31 • 3.3 V LVC MOS Wide Range High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

| Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 100 μA | 4 mA | Std. | 0.66 | 12.19 | 0.04 | 1.83 | 2.38 | 0.43 | 12.19 | 10.17 | 4.16 | 4.00 | 15.58 | 13.57 | ns |
| | | -1 | 0.56 | 10.37 | 0.04 | 1.55 | 2.02 | 0.36 | 10.37 | 8.66 | 3.54 | 3.41 | 13.26 | 11.54 | ns |
| | | -2 | 0.49 | 9.10 | 0.03 | 1.36 | 1.78 | 0.32 | 9.10 | 7.60 | 3.11 | 2.99 | 11.64 | 10.13 | ns |
| 100 μA | 8 mA | Std. | 0.66 | 7.85 | 0.04 | 1.83 | 2.38 | 0.43 | 7.85 | 6.29 | 4.71 | 4.97 | 11.24 | 9.68 | ns |
| | | -1 | 0.56 | 6.68 | 0.04 | 1.55 | 2.02 | 0.36 | 6.68 | 5.35 | 4.01 | 4.22 | 9.57 | 8.24 | ns |
| | | -2 | 0.49 | 5.86 | 0.03 | 1.36 | 1.78 | 0.32 | 5.86 | 4.70 | 3.52 | 3.71 | 8.40 | 7.23 | ns |
| 100 μA | 12 mA | Std. | 0.66 | 5.67 | 0.04 | 1.83 | 2.38 | 0.43 | 5.67 | 4.36 | 5.06 | 5.59 | 9.07 | 7.75 | ns |
| | | -1 | 0.56 | 4.82 | 0.04 | 1.55 | 2.02 | 0.36 | 4.82 | 3.71 | 4.31 | 4.75 | 7.71 | 6.59 | ns |
| | | -2 | 0.49 | 4.24 | 0.03 | 1.36 | 1.78 | 0.32 | 4.24 | 3.25 | 3.78 | 4.17 | 6.77 | 5.79 | ns |
| 100 μA | 16 mA | Std. | 0.66 | 5.35 | 0.04 | 1.83 | 2.38 | 0.43 | 5.35 | 3.96 | 5.15 | 5.76 | 8.75 | 7.35 | ns |
| | | -1 | 0.56 | 4.55 | 0.04 | 1.55 | 2.02 | 0.36 | 4.55 | 3.36 | 4.38 | 4.90 | 7.44 | 6.25 | ns |
| | | -2 | 0.49 | 4.00 | 0.03 | 1.36 | 1.78 | 0.32 | 4.00 | 2.95 | 3.85 | 4.30 | 6.53 | 5.49 | ns |
| 100 μA | 24 mA | Std. | 0.66 | 4.96 | 0.04 | 1.83 | 2.38 | 0.43 | 4.96 | 3.27 | 5.23 | 6.38 | 8.35 | 6.67 | ns |
| | | -1 | 0.56 | 4.22 | 0.04 | 1.55 | 2.02 | 0.36 | 4.22 | 2.78 | 4.45 | 5.43 | 7.11 | 5.67 | ns |
| | | -2 | 0.49 | 3.70 | 0.03 | 1.36 | 1.78 | 0.32 | 3.70 | 2.44 | 3.91 | 4.76 | 6.24 | 4.98 | ns |

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

| Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| | | | Std. | -1 | -2 | Std. | -1 | -2 | Std. | -1 | -2 | Std. | -1 | -2 | |
| 100 μA | 4 mA | Std. | 0.66 | 17.02 | 0.04 | 1.83 | 2.38 | 0.43 | 17.02 | 13.74 | 4.16 | 3.78 | 20.42 | 17.14 | ns |
| | | -1 | 0.56 | 14.48 | 0.04 | 1.55 | 2.02 | 0.36 | 14.48 | 11.69 | 3.54 | 3.21 | 17.37 | 14.58 | ns |
| | | -2 | 0.49 | 12.71 | 0.03 | 1.36 | 1.78 | 0.32 | 12.71 | 10.26 | 3.11 | 2.82 | 15.25 | 12.80 | ns |
| 100 μA | 8 mA | Std. | 0.66 | 12.16 | 0.04 | 1.83 | 2.38 | 0.43 | 12.16 | 9.78 | 4.70 | 4.74 | 15.55 | 13.17 | ns |
| | | -1 | 0.56 | 10.34 | 0.04 | 1.55 | 2.02 | 0.36 | 10.34 | 8.32 | 4.00 | 4.03 | 13.23 | 11.20 | ns |
| | | -2 | 0.49 | 9.08 | 0.03 | 1.36 | 1.78 | 0.32 | 9.08 | 7.30 | 3.51 | 3.54 | 11.61 | 9.84 | ns |
| 100 μA | 12 mA | Std. | 0.66 | 9.32 | 0.04 | 1.83 | 2.38 | 0.43 | 9.32 | 7.62 | 5.06 | 5.36 | 12.71 | 11.02 | ns |
| | | -1 | 0.56 | 7.93 | 0.04 | 1.55 | 2.02 | 0.36 | 7.93 | 6.48 | 4.31 | 4.56 | 10.81 | 9.37 | ns |
| | | -2 | 0.49 | 6.96 | 0.03 | 1.36 | 1.78 | 0.32 | 6.96 | 5.69 | 3.78 | 4.00 | 9.49 | 8.23 | ns |
| 100 μA | 16 mA | Std. | 0.66 | 8.69 | 0.04 | 1.83 | 2.38 | 0.43 | 8.69 | 7.17 | 5.14 | 5.53 | 12.08 | 10.57 | ns |
| | | -1 | 0.56 | 7.39 | 0.04 | 1.55 | 2.02 | 0.36 | 7.39 | 6.10 | 4.37 | 4.71 | 10.28 | 8.99 | ns |
| | | -2 | 0.49 | 6.49 | 0.03 | 1.36 | 1.78 | 0.32 | 6.49 | 5.36 | 3.83 | 4.13 | 9.02 | 7.89 | ns |
| 100 μA | 24 mA | Std. | 0.66 | 8.11 | 0.04 | 1.83 | 2.38 | 0.43 | 8.11 | 7.13 | 5.23 | 6.13 | 11.50 | 10.52 | ns |
| | | -1 | 0.56 | 6.90 | 0.04 | 1.55 | 2.02 | 0.36 | 6.90 | 6.06 | 4.45 | 5.21 | 9.78 | 8.95 | ns |
| | | -2 | 0.49 | 6.05 | 0.03 | 1.36 | 1.78 | 0.32 | 6.05 | 5.32 | 3.91 | 4.57 | 8.59 | 7.86 | ns |

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JEDEC8-5) used for general-purpose 2.5 V applications.

Table 2-33 • Minimum and Maximum DC Input and Output Levels

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------|-----------|-----------|-----------|-----------|------------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max., V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

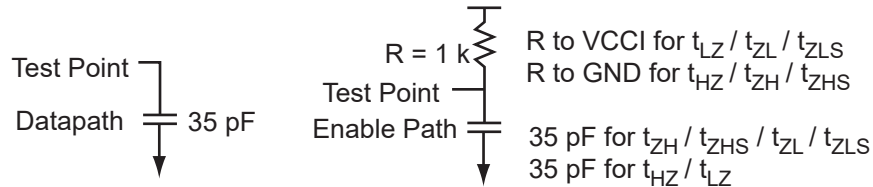


Figure 2-8 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 2.5 | 1.2 | – | 35 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-35 • 2.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 8.82 | 0.04 | 1.51 | 1.66 | 0.43 | 8.13 | 8.82 | 2.72 | 2.29 | 10.37 | 11.05 | ns |
| | -1 | 0.56 | 7.50 | 0.04 | 1.29 | 1.41 | 0.36 | 6.92 | 7.50 | 2.31 | 1.95 | 8.82 | 9.40 | ns |
| | -2 | 0.49 | 6.58 | 0.03 | 1.13 | 1.24 | 0.32 | 6.07 | 6.58 | 2.03 | 1.71 | 7.74 | 8.25 | ns |
| 8 mA | Std. | 0.66 | 5.27 | 0.04 | 1.51 | 1.66 | 0.43 | 5.27 | 5.27 | 3.10 | 3.03 | 7.50 | 7.51 | ns |
| | -1 | 0.56 | 4.48 | 0.04 | 1.29 | 1.41 | 0.36 | 4.48 | 4.48 | 2.64 | 2.58 | 6.38 | 6.38 | ns |
| | -2 | 0.49 | 3.94 | 0.03 | 1.13 | 1.24 | 0.32 | 3.93 | 3.94 | 2.32 | 2.26 | 5.60 | 5.61 | ns |
| 12 mA | Std. | 0.66 | 3.74 | 0.04 | 1.51 | 1.66 | 0.43 | 3.81 | 3.49 | 3.37 | 3.49 | 6.05 | 5.73 | ns |
| | -1 | 0.56 | 3.18 | 0.04 | 1.29 | 1.41 | 0.36 | 3.24 | 2.97 | 2.86 | 2.97 | 5.15 | 4.87 | ns |
| | -2 | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 | ns |
| 16 mA | Std. | 0.66 | 3.53 | 0.04 | 1.51 | 1.66 | 0.43 | 3.59 | 3.12 | 3.42 | 3.62 | 5.83 | 5.35 | ns |
| | -1 | 0.56 | 3.00 | 0.04 | 1.29 | 1.41 | 0.36 | 3.06 | 2.65 | 2.91 | 3.08 | 4.96 | 4.55 | ns |
| | -2 | 0.49 | 2.63 | 0.03 | 1.13 | 1.24 | 0.32 | 2.68 | 2.33 | 2.56 | 2.71 | 4.35 | 4.00 | ns |
| 24 mA | Std. | 0.66 | 3.26 | 0.04 | 1.51 | 1.66 | 0.43 | 3.32 | 2.48 | 3.49 | 4.11 | 5.56 | 4.72 | ns |
| | -1 | 0.56 | 2.77 | 0.04 | 1.29 | 1.41 | 0.36 | 2.83 | 2.11 | 2.97 | 3.49 | 4.73 | 4.01 | ns |
| | -2 | 0.49 | 2.44 | 0.03 | 1.13 | 1.24 | 0.32 | 2.48 | 1.85 | 2.61 | 3.07 | 4.15 | 3.52 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-36 • 2.5 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.66 | 12.00 | 0.04 | 1.51 | 1.66 | 0.43 | 12.23 | 11.61 | 2.72 | 2.20 | 14.46 | 13.85 | ns |
| | -1 | 0.56 | 10.21 | 0.04 | 1.29 | 1.41 | 0.36 | 10.40 | 9.88 | 2.31 | 1.87 | 12.30 | 11.78 | ns |
| | -2 | 0.49 | 8.96 | 0.03 | 1.13 | 1.24 | 0.32 | 9.13 | 8.67 | 2.03 | 1.64 | 10.80 | 10.34 | ns |
| 8 mA | Std. | 0.66 | 8.73 | 0.04 | 1.51 | 1.66 | 0.43 | 8.89 | 8.01 | 3.10 | 2.93 | 11.13 | 10.25 | ns |
| | -1 | 0.56 | 7.43 | 0.04 | 1.29 | 1.41 | 0.36 | 7.57 | 6.82 | 2.64 | 2.49 | 9.47 | 8.72 | ns |
| | -2 | 0.49 | 6.52 | 0.03 | 1.13 | 1.24 | 0.32 | 6.64 | 5.98 | 2.32 | 2.19 | 8.31 | 7.65 | ns |
| 12 mA | Std. | 0.66 | 6.77 | 0.04 | 1.51 | 1.66 | 0.43 | 6.90 | 6.11 | 3.37 | 3.39 | 9.14 | 8.34 | ns |
| | -1 | 0.56 | 5.76 | 0.04 | 1.29 | 1.41 | 0.36 | 5.87 | 5.20 | 2.86 | 2.89 | 7.77 | 7.10 | ns |
| | -2 | 0.49 | 5.06 | 0.03 | 1.13 | 1.24 | 0.32 | 5.15 | 4.56 | 2.51 | 2.53 | 6.82 | 6.23 | ns |
| 16 mA | Std. | 0.66 | 6.31 | 0.04 | 1.51 | 1.66 | 0.43 | 6.42 | 5.73 | 3.42 | 3.52 | 8.66 | 7.96 | ns |
| | -1 | 0.56 | 5.37 | 0.04 | 1.29 | 1.41 | 0.36 | 5.46 | 4.87 | 2.91 | 3.00 | 7.37 | 6.77 | ns |
| | -2 | 0.49 | 4.71 | 0.03 | 1.13 | 1.24 | 0.32 | 4.80 | 4.28 | 2.56 | 2.63 | 6.47 | 5.95 | ns |
| 24 mA | Std. | 0.66 | 5.93 | 0.04 | 1.51 | 1.66 | 0.43 | 6.04 | 5.70 | 3.49 | 4.00 | 8.28 | 7.94 | ns |
| | -1 | 0.56 | 5.05 | 0.04 | 1.29 | 1.41 | 0.36 | 5.14 | 4.85 | 2.97 | 3.40 | 7.04 | 6.75 | ns |
| | -2 | 0.49 | 4.43 | 0.03 | 1.13 | 1.24 | 0.32 | 4.51 | 4.26 | 2.61 | 2.99 | 6.18 | 5.93 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-37 • Minimum and Maximum DC Input and Output Levels

| 1.8 V LVCMOS Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------------------|--------|-------------|-------------|--------|--------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



Figure 2-9 • AC Loading

Table 2-38 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 1.8 | 0.9 | - | 35 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-39 • 1.8 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 12.10 | 0.04 | 1.45 | 1.91 | 0.43 | 9.59 | 12.10 | 2.78 | 1.64 | 11.83 | 14.34 | ns |
| | -1 | 0.56 | 10.30 | 0.04 | 1.23 | 1.62 | 0.36 | 8.16 | 10.30 | 2.37 | 1.39 | 10.06 | 12.20 | ns |
| | -2 | 0.49 | 9.04 | 0.03 | 1.08 | 1.42 | 0.32 | 7.16 | 9.04 | 2.08 | 1.22 | 8.83 | 10.71 | ns |
| 4 mA | Std. | 0.66 | 7.05 | 0.04 | 1.45 | 1.91 | 0.43 | 6.20 | 7.05 | 3.25 | 2.86 | 8.44 | 9.29 | ns |
| | -1 | 0.56 | 6.00 | 0.04 | 1.23 | 1.62 | 0.36 | 5.28 | 6.00 | 2.76 | 2.44 | 7.18 | 7.90 | ns |
| | -2 | 0.49 | 5.27 | 0.03 | 1.08 | 1.42 | 0.32 | 4.63 | 5.27 | 2.43 | 2.14 | 6.30 | 6.94 | ns |
| 6 mA | Std. | 0.66 | 4.52 | 0.04 | 1.45 | 1.91 | 0.43 | 4.47 | 4.52 | 3.57 | 3.47 | 6.70 | 6.76 | ns |
| | -1 | 0.56 | 3.85 | 0.04 | 1.23 | 1.62 | 0.36 | 3.80 | 3.85 | 3.04 | 2.95 | 5.70 | 5.75 | ns |
| | -2 | 0.49 | 3.38 | 0.03 | 1.08 | 1.42 | 0.32 | 3.33 | 3.38 | 2.66 | 2.59 | 5.00 | 5.05 | ns |
| 8 mA | Std. | 0.66 | 4.12 | 0.04 | 1.45 | 1.91 | 0.43 | 4.20 | 3.99 | 3.63 | 3.62 | 6.43 | 6.23 | ns |
| | -1 | 0.56 | 3.51 | 0.04 | 1.23 | 1.62 | 0.36 | 3.57 | 3.40 | 3.09 | 3.08 | 5.47 | 5.30 | ns |
| | -2 | 0.49 | 3.08 | 0.03 | 1.08 | 1.42 | 0.32 | 3.14 | 2.98 | 2.71 | 2.71 | 4.81 | 4.65 | ns |
| 12 mA | Std. | 0.66 | 3.80 | 0.04 | 1.45 | 1.91 | 0.43 | 3.87 | 3.09 | 3.73 | 4.24 | 6.10 | 5.32 | ns |
| | -1 | 0.56 | 3.23 | 0.04 | 1.23 | 1.62 | 0.36 | 3.29 | 2.63 | 3.18 | 3.60 | 5.19 | 4.53 | ns |
| | -2 | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |
| 16 mA | Std. | 0.66 | 3.80 | 0.04 | 1.45 | 1.91 | 0.43 | 3.87 | 3.09 | 3.73 | 4.24 | 6.10 | 5.32 | ns |
| | -1 | 0.56 | 3.23 | 0.04 | 1.23 | 1.62 | 0.36 | 3.29 | 2.63 | 3.18 | 3.60 | 5.19 | 4.53 | ns |
| | -2 | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-40 • 1.8 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 15.84 | 0.04 | 1.45 | 1.91 | 0.43 | 15.65 | 15.84 | 2.78 | 1.58 | 17.89 | 18.07 | ns |
| | -1 | 0.56 | 13.47 | 0.04 | 1.23 | 1.62 | 0.36 | 13.31 | 13.47 | 2.37 | 1.35 | 15.22 | 15.37 | ns |
| | -2 | 0.49 | 11.83 | 0.03 | 1.08 | 1.42 | 0.32 | 11.69 | 11.83 | 2.08 | 1.18 | 13.36 | 13.50 | ns |
| 4 mA | Std. | 0.66 | 11.39 | 0.04 | 1.45 | 1.91 | 0.43 | 11.60 | 10.76 | 3.26 | 2.77 | 13.84 | 12.99 | ns |
| | -1 | 0.56 | 9.69 | 0.04 | 1.23 | 1.62 | 0.36 | 9.87 | 9.15 | 2.77 | 2.36 | 11.77 | 11.05 | ns |
| | -2 | 0.49 | 8.51 | 0.03 | 1.08 | 1.42 | 0.32 | 8.66 | 8.03 | 2.43 | 2.07 | 10.33 | 9.70 | ns |
| 6 mA | Std. | 0.66 | 8.97 | 0.04 | 1.45 | 1.91 | 0.43 | 9.14 | 8.10 | 3.57 | 3.36 | 11.37 | 10.33 | ns |
| | -1 | 0.56 | 7.63 | 0.04 | 1.23 | 1.62 | 0.36 | 7.77 | 6.89 | 3.04 | 2.86 | 9.67 | 8.79 | ns |
| | -2 | 0.49 | 6.70 | 0.03 | 1.08 | 1.42 | 0.32 | 6.82 | 6.05 | 2.66 | 2.51 | 8.49 | 7.72 | ns |
| 8 mA | Std. | 0.66 | 8.35 | 0.04 | 1.45 | 1.91 | 0.43 | 8.50 | 7.59 | 3.64 | 3.52 | 10.74 | 9.82 | ns |
| | -1 | 0.56 | 7.10 | 0.04 | 1.23 | 1.62 | 0.36 | 7.23 | 6.45 | 3.10 | 3.00 | 9.14 | 8.35 | ns |
| | -2 | 0.49 | 6.24 | 0.03 | 1.08 | 1.42 | 0.32 | 6.35 | 5.66 | 2.72 | 2.63 | 8.02 | 7.33 | ns |
| 12 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | -1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | -2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |
| 16 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | -1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | -2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-41 • Minimum and Maximum DC Input and Output Levels

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------|--------|-------------|------------|--------|-------------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | -0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | -0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | -0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | -0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 55 | 66 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

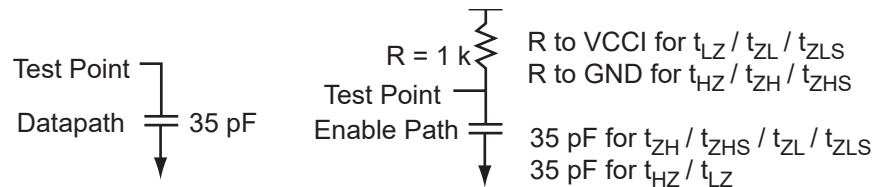


Figure 2-10 • AC Loading

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 1.5 | 0.75 | – | 35 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-43 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 8.53 | 0.04 | 1.70 | 2.14 | 0.43 | 7.26 | 8.53 | 3.39 | 2.79 | 9.50 | 10.77 | ns |
| | -1 | 0.56 | 7.26 | 0.04 | 1.44 | 1.82 | 0.36 | 6.18 | 7.26 | 2.89 | 2.37 | 8.08 | 9.16 | ns |
| | -2 | 0.49 | 6.37 | 0.03 | 1.27 | 1.60 | 0.32 | 5.42 | 6.37 | 2.53 | 2.08 | 7.09 | 8.04 | ns |
| 4 mA | Std. | 0.66 | 5.41 | 0.04 | 1.70 | 2.14 | 0.43 | 5.22 | 5.41 | 3.75 | 3.48 | 7.45 | 7.65 | ns |
| | -1 | 0.56 | 4.60 | 0.04 | 1.44 | 1.82 | 0.36 | 4.44 | 4.60 | 3.19 | 2.96 | 6.34 | 6.50 | ns |
| | -2 | 0.49 | 4.04 | 0.03 | 1.27 | 1.60 | 0.32 | 3.89 | 4.04 | 2.80 | 2.60 | 5.56 | 5.71 | ns |
| 6 mA | Std. | 0.66 | 4.80 | 0.04 | 1.70 | 2.14 | 0.43 | 4.89 | 4.75 | 3.83 | 3.67 | 7.13 | 6.98 | ns |
| | -1 | 0.56 | 4.09 | 0.04 | 1.44 | 1.82 | 0.36 | 4.16 | 4.04 | 3.26 | 3.12 | 6.06 | 5.94 | ns |
| | -2 | 0.49 | 3.59 | 0.03 | 1.27 | 1.60 | 0.32 | 3.65 | 3.54 | 2.86 | 2.74 | 5.32 | 5.21 | ns |
| 8 mA | Std. | 0.66 | 4.42 | 0.04 | 1.70 | 2.14 | 0.43 | 4.50 | 3.62 | 3.96 | 4.37 | 6.74 | 5.86 | ns |
| | -1 | 0.56 | 3.76 | 0.04 | 1.44 | 1.82 | 0.36 | 3.83 | 3.08 | 3.37 | 3.72 | 5.73 | 4.98 | ns |
| | -2 | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |
| 12 mA | Std. | 0.66 | 4.42 | 0.04 | 1.70 | 2.14 | 0.43 | 4.50 | 3.62 | 3.96 | 4.37 | 6.74 | 5.86 | ns |
| | -1 | 0.56 | 3.76 | 0.04 | 1.44 | 1.82 | 0.36 | 3.83 | 3.08 | 3.37 | 3.72 | 5.73 | 4.98 | ns |
| | -2 | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-44 • 1.5 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 0.66 | 14.11 | 0.04 | 1.70 | 2.14 | 0.43 | 14.37 | 13.14 | 3.40 | 2.68 | 16.61 | 15.37 | ns |
| | -1 | 0.56 | 12.00 | 0.04 | 1.44 | 1.82 | 0.36 | 12.22 | 11.17 | 2.90 | 2.28 | 14.13 | 13.08 | ns |
| | -2 | 0.49 | 10.54 | 0.03 | 1.27 | 1.60 | 0.32 | 10.73 | 9.81 | 2.54 | 2.00 | 12.40 | 11.48 | ns |
| 4 mA | Std. | 0.66 | 11.23 | 0.04 | 1.70 | 2.14 | 0.43 | 11.44 | 9.87 | 3.77 | 3.36 | 13.68 | 12.10 | ns |
| | -1 | 0.56 | 9.55 | 0.04 | 1.44 | 1.82 | 0.36 | 9.73 | 8.39 | 3.21 | 2.86 | 11.63 | 10.29 | ns |
| | -2 | 0.49 | 8.39 | 0.03 | 1.27 | 1.60 | 0.32 | 8.54 | 7.37 | 2.81 | 2.51 | 10.21 | 9.04 | ns |
| 6 mA | Std. | 0.66 | 10.45 | 0.04 | 1.70 | 2.14 | 0.43 | 10.65 | 9.24 | 3.84 | 3.55 | 12.88 | 11.48 | ns |
| | -1 | 0.56 | 8.89 | 0.04 | 1.44 | 1.82 | 0.36 | 9.06 | 7.86 | 3.27 | 3.02 | 10.96 | 9.76 | ns |
| | -2 | 0.49 | 7.81 | 0.03 | 1.27 | 1.60 | 0.32 | 7.95 | 6.90 | 2.87 | 2.65 | 9.62 | 8.57 | ns |
| 8 mA | Std. | 0.66 | 10.02 | 0.04 | 1.70 | 2.14 | 0.43 | 10.20 | 9.23 | 3.97 | 4.22 | 12.44 | 11.47 | ns |
| | -1 | 0.56 | 8.52 | 0.04 | 1.44 | 1.82 | 0.36 | 8.68 | 7.85 | 3.38 | 3.59 | 10.58 | 9.75 | ns |
| | -2 | 0.49 | 7.48 | 0.03 | 1.27 | 1.60 | 0.32 | 7.62 | 6.89 | 2.97 | 3.15 | 9.29 | 8.56 | ns |
| 12 mA | Std. | 0.66 | 10.02 | 0.04 | 1.70 | 2.14 | 0.43 | 10.20 | 9.23 | 3.97 | 4.22 | 12.44 | 11.47 | ns |
| | -1 | 0.56 | 8.52 | 0.04 | 1.44 | 1.82 | 0.36 | 8.68 | 7.85 | 3.38 | 3.59 | 10.58 | 9.75 | ns |
| | -2 | 0.49 | 7.48 | 0.03 | 1.27 | 1.60 | 0.32 | 7.62 | 6.89 | 2.97 | 3.15 | 9.29 | 8.56 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-45 • Minimum and Maximum DC Input and Output Levels

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|-----------------------|----------------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.



Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-46.

Table 2-46 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|--|-----------------|------------------------|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$ | – | 10 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-47 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.66 | 2.81 | 0.04 | 1.05 | 1.67 | 0.43 | 2.86 | 2.00 | 3.28 | 3.61 | 5.09 | 4.23 | ns |
| -1 | 0.56 | 2.39 | 0.04 | 0.89 | 1.42 | 0.36 | 2.43 | 1.70 | 2.79 | 3.07 | 4.33 | 3.60 | ns |
| -2 | 0.49 | 2.09 | 0.03 | 0.78 | 1.25 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-48 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} | I_{OSL} | I_{OSH} | I_{IL} | I_{IH} |
|--------------------|----------|------------------|------------------|--------|----------|----------|----------|----------|----------------------|----------------------|-----------------|-----------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA^2 | μA^2 |
| 20 mA ³ | -0.3 | $V_{REF} - 0.05$ | $V_{REF} + 0.05$ | 3.6 | 0.4 | - | 20 | 20 | 181 | 268 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.



Figure 2-12 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | V_{REF} (typ.) (V) | V_{TT} (typ.) (V) | C_{LOAD} (pF) |
|------------------|------------------|----------------------|----------------------|---------------------|-----------------|
| $V_{REF} - 0.05$ | $V_{REF} + 0.05$ | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = V_{trip} . See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-50 • 3.3 V GTL

**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$**

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.60 | 2.08 | 0.04 | 2.93 | 0.43 | 2.04 | 2.08 | | | 4.27 | 4.31 | ns |
| -1 | 0.51 | 1.77 | 0.04 | 2.50 | 0.36 | 1.73 | 1.77 | | | 3.63 | 3.67 | ns |
| -2 | 0.45 | 1.55 | 0.03 | 2.19 | 0.32 | 1.52 | 1.55 | | | 3.19 | 3.22 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

| 2.5 GTL Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|---------------------------|---------|-------------|-------------|--------|--------|--------|-----|-----|-----------------|-----------------|-----------------|-----------------|
| | Min., V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | mA ¹ | mA ¹ | μA ² | μA ² |
| 20 mA ³ | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 | 124 | 169 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

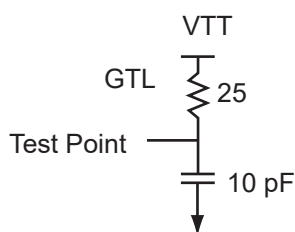


Figure 2-13 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-53 • 2.5 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.60 | 2.13 | 0.04 | 2.46 | 0.43 | 2.16 | 2.13 | | | 4.40 | 4.36 | ns |
| -1 | 0.51 | 1.81 | 0.04 | 2.09 | 0.36 | 1.84 | 1.81 | | | 3.74 | 3.71 | ns |
| -2 | 0.45 | 1.59 | 0.03 | 1.83 | 0.32 | 1.61 | 1.59 | | | 3.28 | 3.26 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-54 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|------------|--------|------------|------------|--------|--------|--------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 35 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 35 | 35 | 181 | 268 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

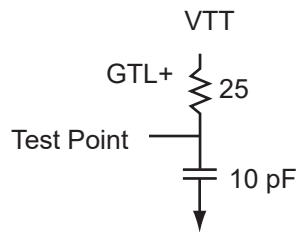


Figure 2-14 • AC Loading

Table 2-55 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-56 • 3.3 V GTL+

**Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V**

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.60 | 2.06 | 0.04 | 1.59 | 0.43 | 2.09 | 2.06 | | | 4.33 | 4.29 | ns |
| -1 | 0.51 | 1.75 | 0.04 | 1.35 | 0.36 | 1.78 | 1.75 | | | 3.68 | 3.65 | ns |
| -2 | 0.45 | 1.53 | 0.03 | 1.19 | 0.32 | 1.56 | 1.53 | | | 3.23 | 3.20 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-57 • Minimum and Maximum DC Input and Output Levels

| 2.5 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|------------|--------|------------|------------|--------|--------|--------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 33 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 33 | 33 | 124 | 169 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

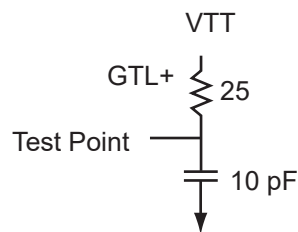


Figure 2-15 • AC Loading

Table 2-58 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-59 • 2.5 V GTL+

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.60 | 2.21 | 0.04 | 1.51 | 0.43 | 2.25 | 2.10 | | | 4.48 | 4.34 | ns |
| -1 | 0.51 | 1.88 | 0.04 | 1.29 | 0.36 | 1.91 | 1.79 | | | 3.81 | 3.69 | ns |
| -2 | 0.45 | 1.65 | 0.03 | 1.13 | 0.32 | 1.68 | 1.57 | | | 3.35 | 3.24 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-60 • Minimum and Maximum DC Input and Output Levels

| HSTL Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|--------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 8 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 8 | 8 | 39 | 32 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.



Figure 2-16 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-62 • HSTL Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = .4 V, VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 3.18 | 0.04 | 2.12 | 0.43 | 3.24 | 3.14 | | | 5.47 | 5.38 | ns |
| -1 | 0.56 | 2.70 | 0.04 | 1.81 | 0.36 | 2.75 | 2.67 | | | 4.66 | 4.58 | ns |
| -2 | 0.49 | 2.37 | 0.03 | 1.59 | 0.32 | 2.42 | 2.35 | | | 4.09 | 4.02 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-63 • Minimum and Maximum DC Input and Output Levels

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|--------------------|--------|------------|------------|--------|---------|------------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max., V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 15 mA ³ | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 15 | 15 | 55 | 66 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

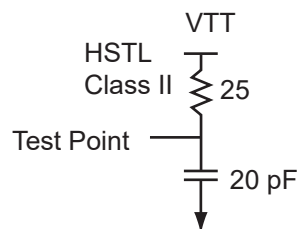


Figure 2-17 • AC Loading

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-65 • HSTL Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{py} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 3.02 | 0.04 | 2.12 | 0.43 | 3.08 | 2.71 | | | 5.32 | 4.95 | ns |
| -1 | 0.56 | 2.57 | 0.04 | 1.81 | 0.36 | 2.62 | 2.31 | | | 4.52 | 4.21 | ns |
| -2 | 0.49 | 2.26 | 0.03 | 1.59 | 0.32 | 2.30 | 2.03 | | | 3.97 | 3.70 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-66 • Minimum and Maximum DC Input and Output Levels

| SSTL2 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|---------------|--------|------------|------------|--------|--------|-------------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 15 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI - 0.62 | 15 | 15 | 87 | 83 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.



Figure 2-18 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-68 • SSTL 2 Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.13 | 0.04 | 1.33 | 0.43 | 2.17 | 1.85 | | | 4.40 | 4.08 | ns |
| -1 | 0.56 | 1.81 | 0.04 | 1.14 | 0.36 | 1.84 | 1.57 | | | 3.74 | 3.47 | ns |
| -2 | 0.49 | 1.59 | 0.03 | 1.00 | 0.32 | 1.62 | 1.38 | | | 3.29 | 3.05 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-69 • Minimum and Maximum DC Input and Output Levels

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|----------------|--------|------------|------------|--------|--------|-------------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 18 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI - 0.43 | 18 | 18 | 124 | 169 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.



Figure 2-19 • AC Loading

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-71 • SSTL 2 Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 0.66 | 2.17 | 0.04 | 1.33 | 0.43 | 2.21 | 1.77 | | | 4.44 | ns |
| -1 | 0.56 | 0.56 | 1.84 | 0.04 | 1.14 | 0.36 | 1.88 | 1.51 | | | 3.78 | ns |
| -2 | 0.49 | 0.49 | 1.62 | 0.03 | 1.00 | 0.32 | 1.65 | 1.32 | | | 3.32 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-72 • Minimum and Maximum DC Input and Output Levels

| SSTL3 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|---------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 14 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI - 1.1 | 14 | 14 | 54 | 51 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

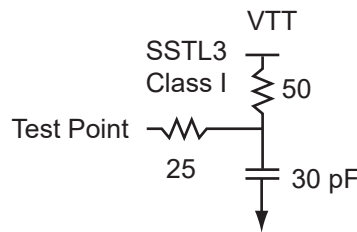


Figure 2-20 • AC Loading

Table 2-73 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-74 • SSTL3 Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.31 | 0.04 | 1.25 | 0.43 | 2.35 | 1.84 | | | 4.59 | 4.07 | ns |
| -1 | 0.56 | 1.96 | 0.04 | 1.06 | 0.36 | 2.00 | 1.56 | | | 3.90 | 3.46 | ns |
| -2 | 0.49 | 1.72 | 0.03 | 0.93 | 0.32 | 1.75 | 1.37 | | | 3.42 | 3.04 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-75 • Minimum and Maximum DC Input and Output Levels

| SSTL3 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|----------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|-----------------|-----------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ¹ | Max. mA ¹ | μA ² | μA ² |
| 21 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI - 0.9 | 21 | 21 | 109 | 103 | 10 | 10 |

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.



Figure 2-21 • AC Loading

Table 2-76 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-77 • SSTL3 Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.66 | 2.07 | 0.04 | 1.25 | 0.43 | 2.10 | 1.67 | | | 4.34 | 3.91 | ns |
| -1 | 0.56 | 1.76 | 0.04 | 1.06 | 0.36 | 1.79 | 1.42 | | | 3.69 | 3.32 | ns |
| -2 | 0.49 | 1.54 | 0.03 | 0.93 | 0.32 | 1.57 | 1.25 | | | 3.24 | 2.92 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-22](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

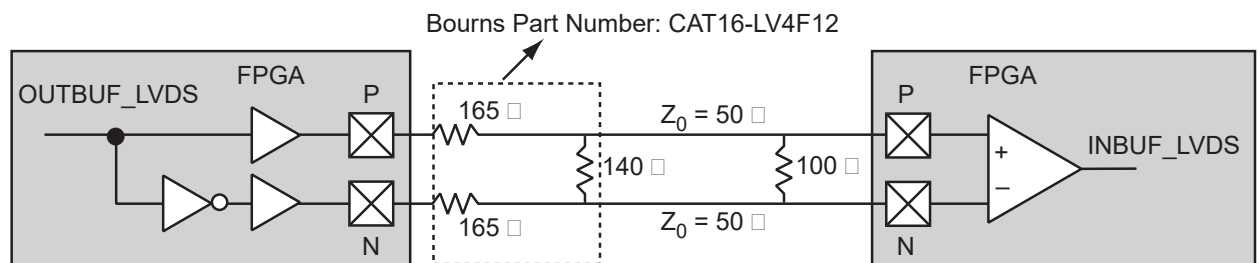


Figure 2-22 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|------------------|---|-------|-------|-------|-------|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL ¹ | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH ¹ | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIH ² | Input High Leakage Current | | | 10 | μA |
| IIL ² | Input Low Leakage Current | | | 10 | μA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage ² | 100 | 350 | | mV |

Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network).
2. Currents are measured at 85°C junction temperature.

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---------------|----------------|----------------------|-----------------|
| 1.075 | 1.325 | Cross point | – |

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-80 • LVDS

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{pY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.66 | 1.87 | 0.04 | 1.82 | ns |
| -1 | 0.56 | 1.59 | 0.04 | 1.55 | ns |
| -2 | 0.49 | 1.40 | 0.03 | 1.36 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) on [page 2-6](#) for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-23](#). The input and output buffer delays are available in the LVDS section in [Table 2-80](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

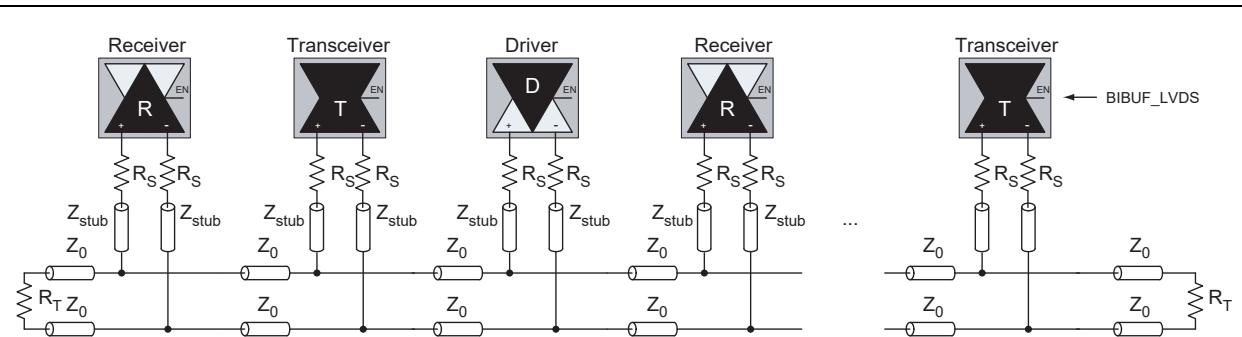


Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-24. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

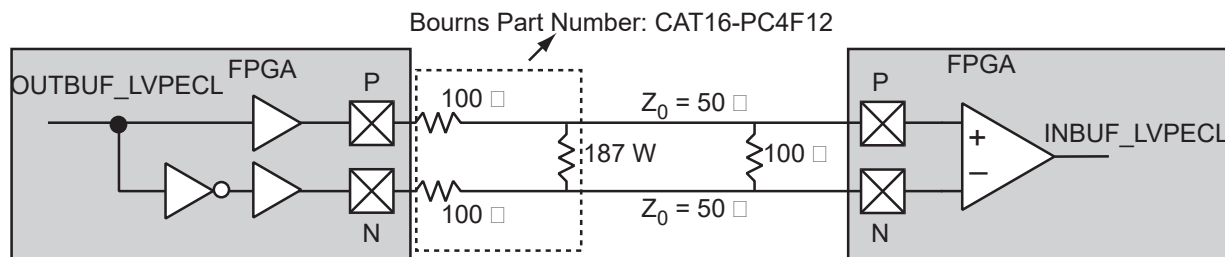


Figure 2-24 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-81 • Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|--------------|--------------------------------|-------|------|-------|------|-------|------|-------|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---------------|----------------|----------------------|-----------------|
| 1.64 | 1.94 | Cross point | – |

Note: *Measuring point = V_{trip} . See Table 2-15 on page 2-19 for a complete table of trip points.

Timing Characteristics

Table 2-83 • LVPECL

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{pY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.66 | 1.83 | 0.04 | 1.63 | ns |
| -1 | 0.56 | 1.55 | 0.04 | 1.39 | ns |
| -2 | 0.49 | 1.36 | 0.03 | 1.22 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

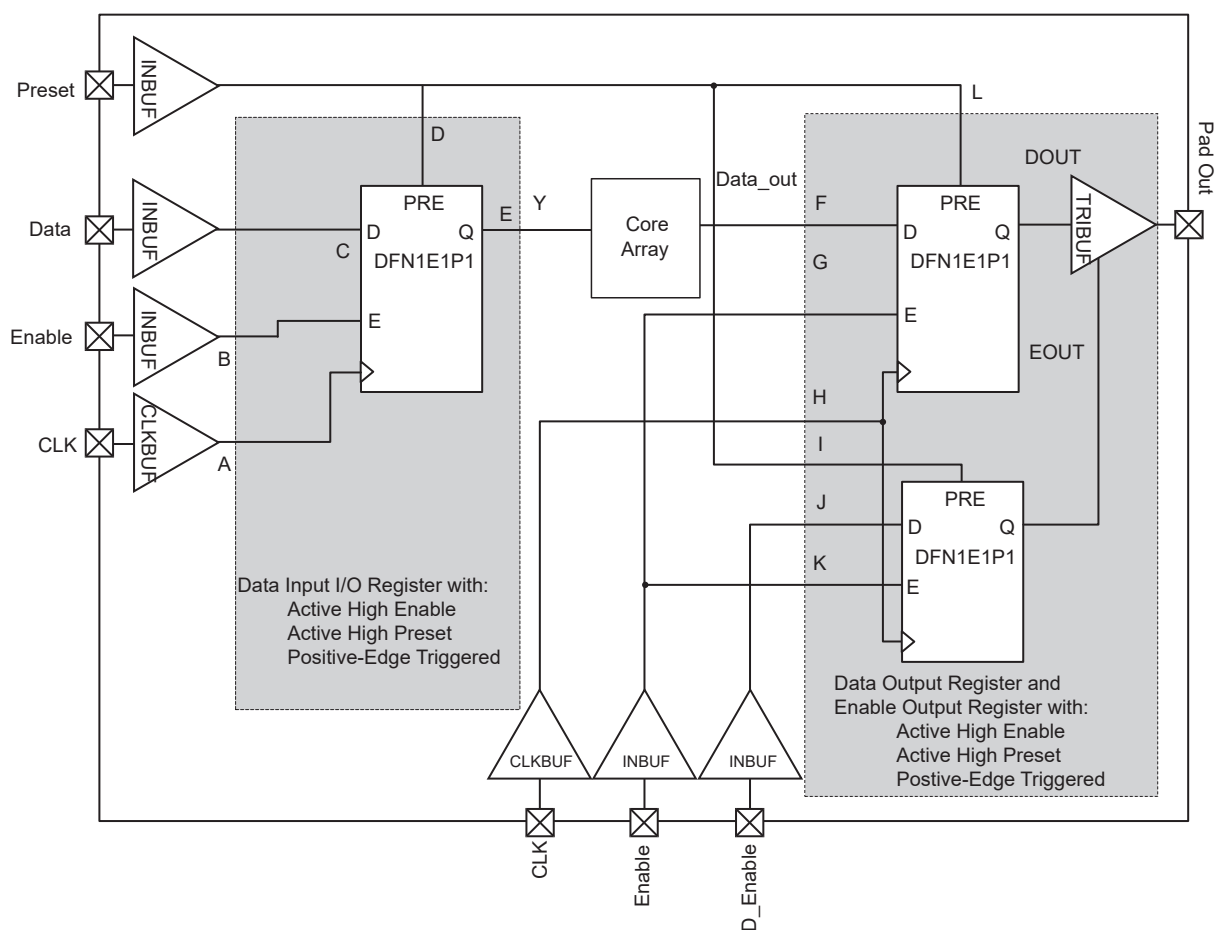


Figure 2-25 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-84 • Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------|--|-----------------------------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | H, DOUT |
| t_{OSUD} | Data Setup Time for the Output Data Register | F, H |
| t_{OHD} | Data Hold Time for the Output Data Register | F, H |
| t_{OSUE} | Enable Setup Time for the Output Data Register | G, H |
| t_{OHE} | Enable Hold Time for the Output Data Register | G, H |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | H, EOUT |
| t_{OESUD} | Data Setup Time for the Output Enable Register | J, H |
| t_{OEHD} | Data Hold Time for the Output Enable Register | J, H |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | K, H |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | K, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| t_{ICLKQ} | Clock-to-Q of the Input Data Register | A, E |
| t_{ISUD} | Data Setup Time for the Input Data Register | C, A |
| t_{IHD} | Data Hold Time for the Input Data Register | C, A |
| t_{ISUE} | Enable Setup Time for the Input Data Register | B, A |
| t_{IHE} | Enable Hold Time for the Input Data Register | B, A |
| t_{IPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

Note: *See Figure 2-25 on page 2-55 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear



Figure 2-26 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-85 • Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------|---|-----------------------------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | HH, DOUT |
| t_{OSUD} | Data Setup Time for the Output Data Register | FF, HH |
| t_{OHD} | Data Hold Time for the Output Data Register | FF, HH |
| t_{OSUE} | Enable Setup Time for the Output Data Register | GG, HH |
| t_{OHE} | Enable Hold Time for the Output Data Register | GG, HH |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OERMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | HH, EOUT |
| t_{OESUD} | Data Setup Time for the Output Enable Register | JJ, HH |
| t_{OEHD} | Data Hold Time for the Output Enable Register | JJ, HH |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | KK, HH |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OERMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERCCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| t_{iCLKQ} | Clock-to-Q of the Input Data Register | AA, EE |
| t_{iSUD} | Data Setup Time for the Input Data Register | CC, AA |
| t_{iHD} | Data Hold Time for the Input Data Register | CC, AA |
| t_{iSUE} | Enable Setup Time for the Input Data Register | BB, AA |
| t_{iHE} | Enable Hold Time for the Input Data Register | BB, AA |
| t_{iCLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{iREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{iRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See Figure 2-26 on page 2-57 for more information.

Input Register



Figure 2-27 • Input Register Timing Diagram

Timing Characteristics

Table 2-86 • Input Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------------|---|------|------|------|-------|
| t_{ICLKQ} | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | ns |
| t_{ISUD} | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | ns |
| t_{IHD} | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{ISUE} | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | ns |
| t_{IHE} | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{ICLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| t_{IPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| t_{IEMCLR} | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{IRECCLR} | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{IEMPRE} | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{IRECPRE} | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{IWCLR} | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{IWPRE} | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{ICKMPWH} | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.41 | 0.48 | ns |
| t_{ICKMPWL} | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.37 | 0.43 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Register



Figure 2-28 • Output Register Timing Diagram

Timing Characteristics

Table 2-87 • Output Data Register Propagation Delays

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|--|------|------|------|-------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | 0.59 | 0.67 | 0.79 | ns |
| t_{OSUD} | Data Setup Time for the Output Data Register | 0.31 | 0.36 | 0.42 | ns |
| t_{OHD} | Data Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OSUE} | Enable Setup Time for the Output Data Register | 0.44 | 0.50 | 0.59 | ns |
| t_{OHE} | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.32 | 0.37 | 0.43 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Enable Register



Figure 2-29 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-88 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | 0.59 | 0.67 | 0.79 | ns |
| t_{OESUD} | Data Setup Time for the Output Enable Register | 0.31 | 0.36 | 0.42 | ns |
| t_{OEHD} | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | 0.44 | 0.50 | 0.58 | ns |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OEWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| t_{OEWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.32 | 0.37 | 0.43 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

DDR Module Specifications

Input DDR Module

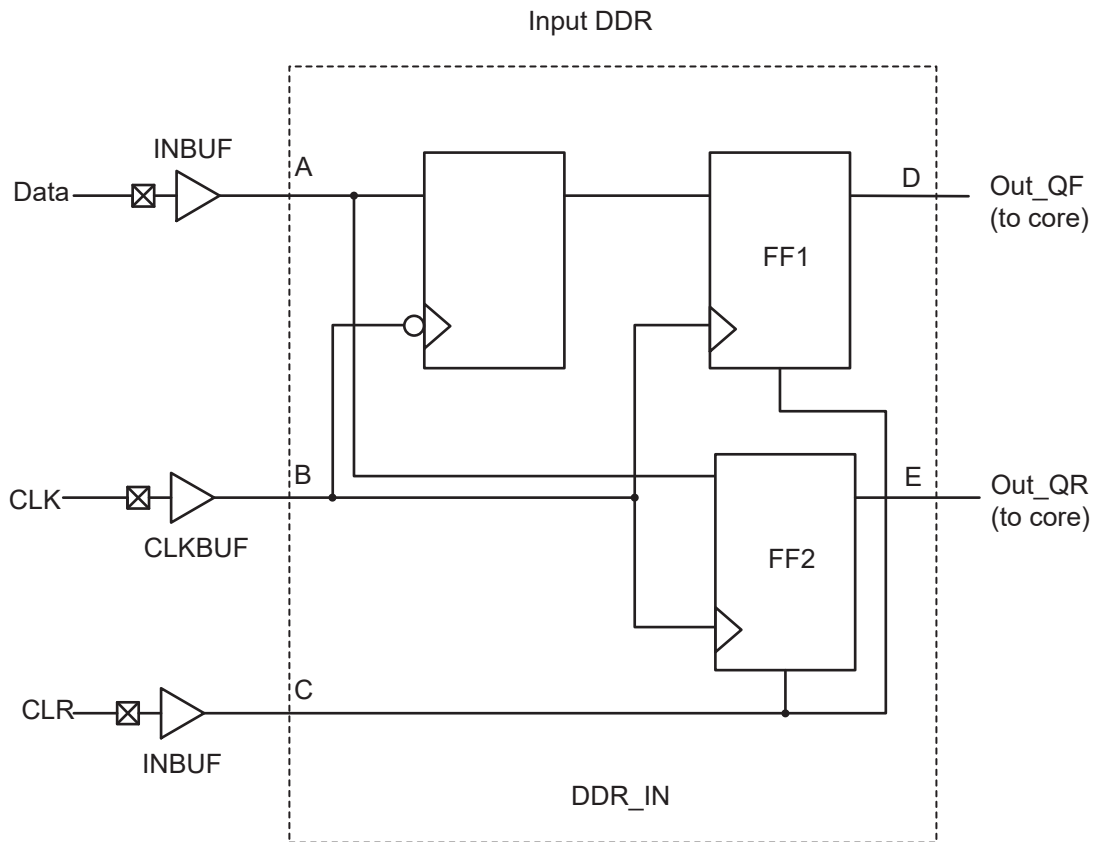


Figure 2-30 • Input DDR Timing Model

Table 2-89 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|------------------------------|----------------------------|
| $t_{DDRICKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| t_{DDRIHD} | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |



Figure 2-31 • Input DDR Timing Diagram

Timing Characteristics

Table 2-90 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|-------------------------|--|------|------|------|-------|
| t_{DDRICKQ1} | Clock-to-Out Out_QR for Input DDR | 0.39 | 0.44 | 0.52 | ns |
| t_{DDRICKQ2} | Clock-to-Out Out_QF for Input DDR | 0.27 | 0.31 | 0.37 | ns |
| t_{DDRISUD} | Data Setup for Input DDR | 0.28 | 0.32 | 0.38 | ns |
| t_{DDRIHD} | Data Hold for Input DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRICLR2Q1}}$ | Asynchronous Clear to Out Out_QR for Input DDR | 0.57 | 0.65 | 0.76 | ns |
| $t_{\text{DDRICLR2Q2}}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.46 | 0.53 | 0.62 | ns |
| $t_{\text{DDRIREMCLR}}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{\text{DDRIRECCLR}}$ | Asynchronous Clear Recovery Time for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDR IWCLR}}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{\text{DDRICKMPWH}}$ | Clock Minimum Pulse Width High for Input DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{\text{DDRICKMPWL}}$ | Clock Minimum Pulse Width Low for Input DDR | 0.32 | 0.37 | 0.43 | ns |
| F_{DDRIMAX} | Maximum Frequency for Input DDR | 1404 | 1232 | 1048 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output DDR Module



Figure 2-32 • Output DDR Timing Model

Table 2-91 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|---------------------------|----------------------------|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |



Figure 2-33 • Output DDR Timing Diagram

Timing Characteristics

Table 2-92 • Output DDR Propagation Delays

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|------------------|---|------|------|------|-------|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 0.70 | 0.80 | 0.94 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 0.80 | 0.91 | 1.07 | ns |
| $t_{DDROEMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.32 | 0.37 | 0.43 | ns |
| F_{DDOMAX} | Maximum Frequency for the Output DDR | 1404 | 1232 | 1048 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.



Figure 2-34 • Sample of Combinatorial Cells

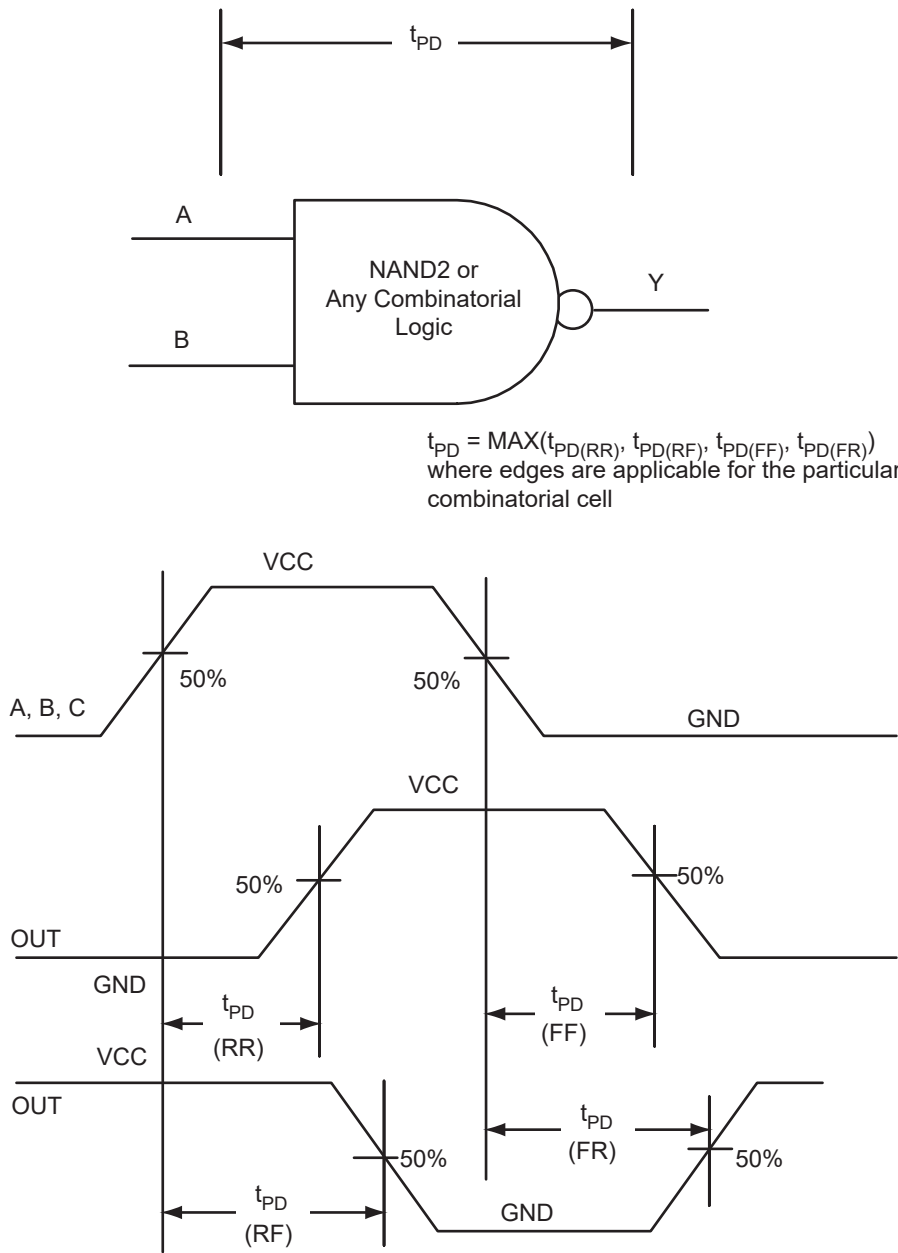


Figure 2-35 • Timing Model and Waveforms

Timing Characteristics

Table 2-93 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Combinatorial Cell | Equation | Parameter | -2 | -1 | Std. | Units |
|--------------------|---------------------------|-----------|------|------|------|-------|
| INV | $Y = !A$ | t_{PD} | 0.40 | 0.46 | 0.54 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 0.47 | 0.54 | 0.63 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | $Y = \text{MAJ}(A, B, C)$ | t_{PD} | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | $Y = A !S + B S$ | t_{PD} | 0.51 | 0.58 | 0.68 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 0.56 | 0.64 | 0.75 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.



Figure 2-36 • Sample of Sequential Cells



Figure 2-37 • Timing Model and Waveforms

Timing Characteristics

Table 2-94 • Register Delays

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------------|---|------|------|------|-------|
| t_{CLKQ} | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| t_{SUD} | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| t_{HD} | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| t_{HE} | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{RECCLR} | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. [Figure 2-38](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-38](#) is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-

flip-flops in the device.



Figure 2-38 • Example of Global Tree Use in an A3PE600 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits" section on page 2-73](#). [Table 2-95 on page 2-72](#), [Table 2-96 on page 2-72](#), and [Table 2-97 on page 2-72](#) present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-95 • A3PE600 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t _{RCKL} | Input Low Delay for Global Clock | 0.83 | 1.04 | 0.94 | 1.18 | 1.11 | 1.39 | ns |
| t _{RCKH} | Input High Delay for Global Clock | 0.81 | 1.06 | 0.93 | 1.21 | 1.09 | 1.42 | ns |
| t _{RCKMPWH} | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| t _{RCKMPWL} | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| t _{RCKSW} | Maximum Skew for Global Clock | | 0.25 | | 0.28 | | 0.33 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-96 • A3PE1500 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t _{RCKL} | Input Low Delay for Global Clock | 1.07 | 1.29 | 1.22 | 1.47 | 1.43 | 1.72 | ns |
| t _{RCKH} | Input High Delay for Global Clock | 1.06 | 1.32 | 1.21 | 1.50 | 1.42 | 1.76 | ns |
| t _{RCKMPWH} | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| t _{RCKMPWL} | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| t _{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-97 • A3PE3000 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | | -1 | | Std. | | Units |
|----------------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | Min. ¹ | Max. ² | Min. ¹ | Max. ² | |
| t _{RCKL} | Input Low Delay for Global Clock | 1.41 | 1.62 | 1.60 | 1.85 | 1.88 | 2.17 | ns |
| t _{RCKH} | Input High Delay for Global Clock | 1.40 | 1.66 | 1.59 | 1.89 | 1.87 | 2.22 | ns |
| t _{RCKMPWH} | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| t _{RCKMPWL} | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| t _{RCKSW} | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.35 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-98 • ProASIC3E CCC/PLL Specification

| Parameter | Minimum | Typical | Maximum | Units |
|--|--------------------------------|------------------|------------------------|---------|
| Clock Conditioning Circuitry Input Frequency f_{IN_CCC} | 1.5 | | 350 | MHz |
| Clock Conditioning Circuitry Output Frequency f_{OUT_CCC} | 0.75 | | 350 | MHz |
| Delay Increments in Programmable Delay Blocks ^{1, 2} | | 160 ³ | | ps |
| Serial Clock (SCLK) for Dynamic PLL ⁴ | | | 125 | MHz |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Input Period Jitter | | | 1.5 | ns |
| CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | | 0.70% | |
| 24 MHz to 100 MHz | 1.00% | | 1.20% | |
| 100 MHz to 250 MHz | 1.75% | | 2.00% | |
| 250 MHz to 350 MHz | 2.50% | | 5.60% | |
| Acquisition Time | LockControl = 0 | | 300 | μ s |
| | LockControl = 1 | | 6.0 | ms |
| Tracking Jitter ⁵ | LockControl = 0 | | 1.6 | ns |
| | LockControl = 1 | | 0.8 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 ^{1, 2} | 0.6 | | 5.56 | ns |
| Delay Range in Block: Programmable Delay 2 ^{1, 2} | 0.025 | | 5.56 | ns |
| Delay Range in Block: Fixed Delay ^{1, 4} | | 2.2 | | ns |

Notes:

1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) for deratings
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$.
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.
4. Maximum value obtained for a -2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-39 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

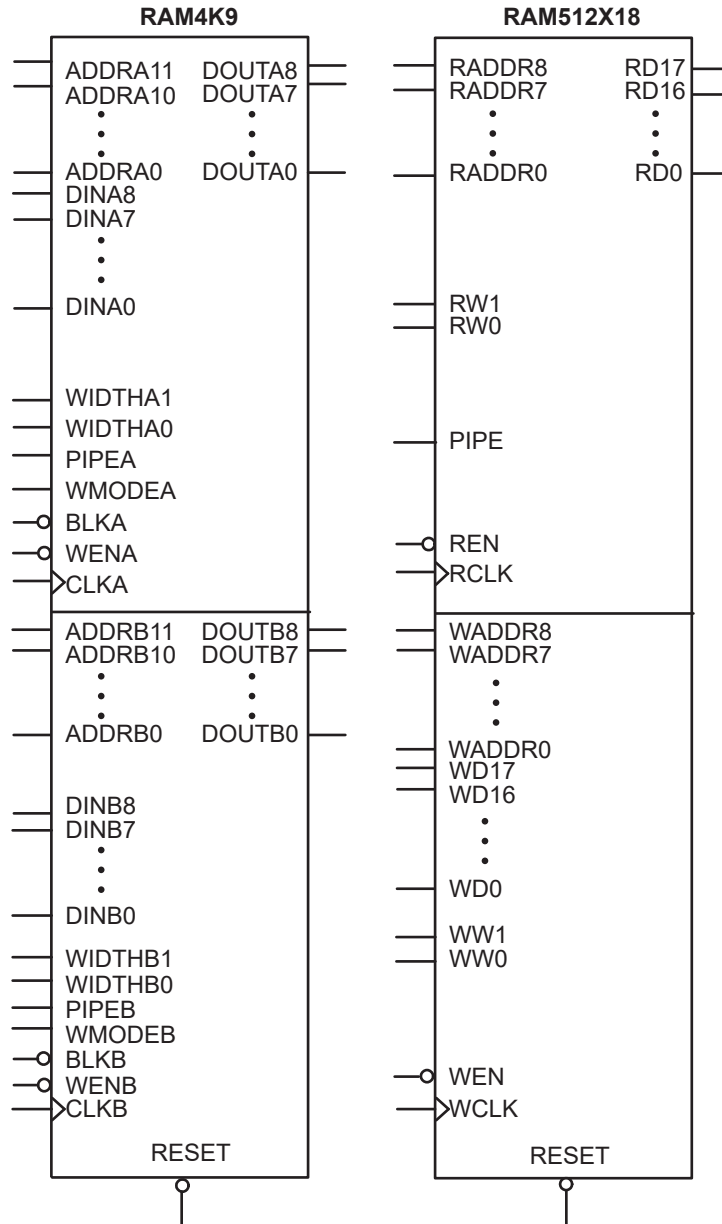


Figure 2-40 • RAM Models

Timing Waveforms

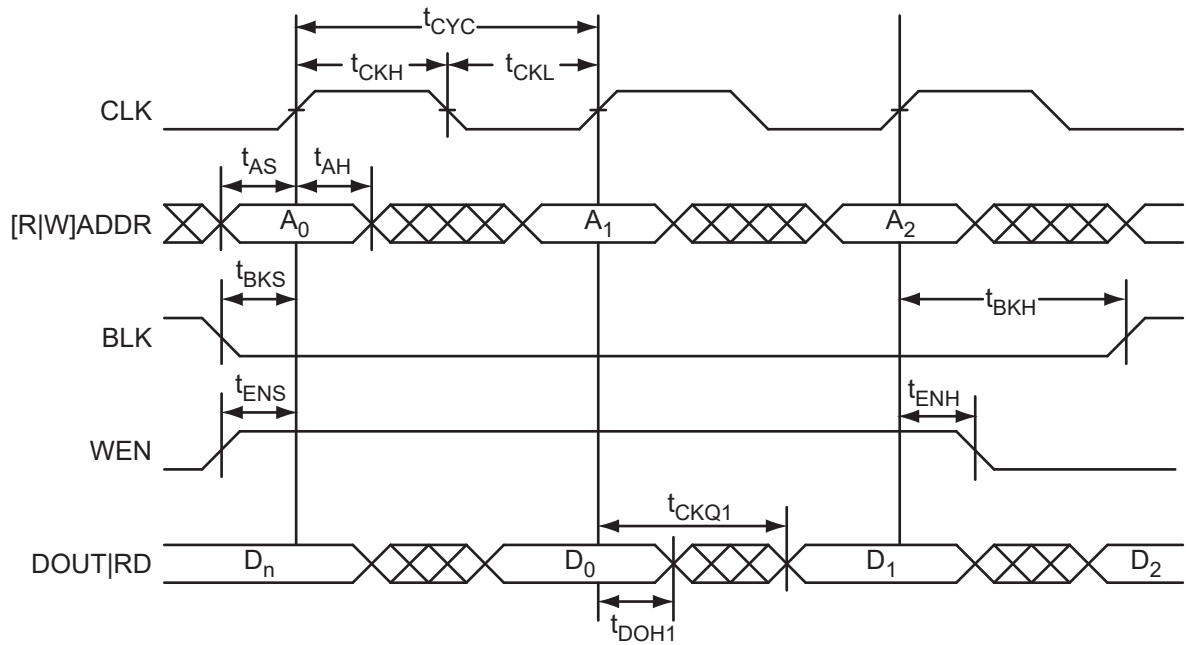


Figure 2-41 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.

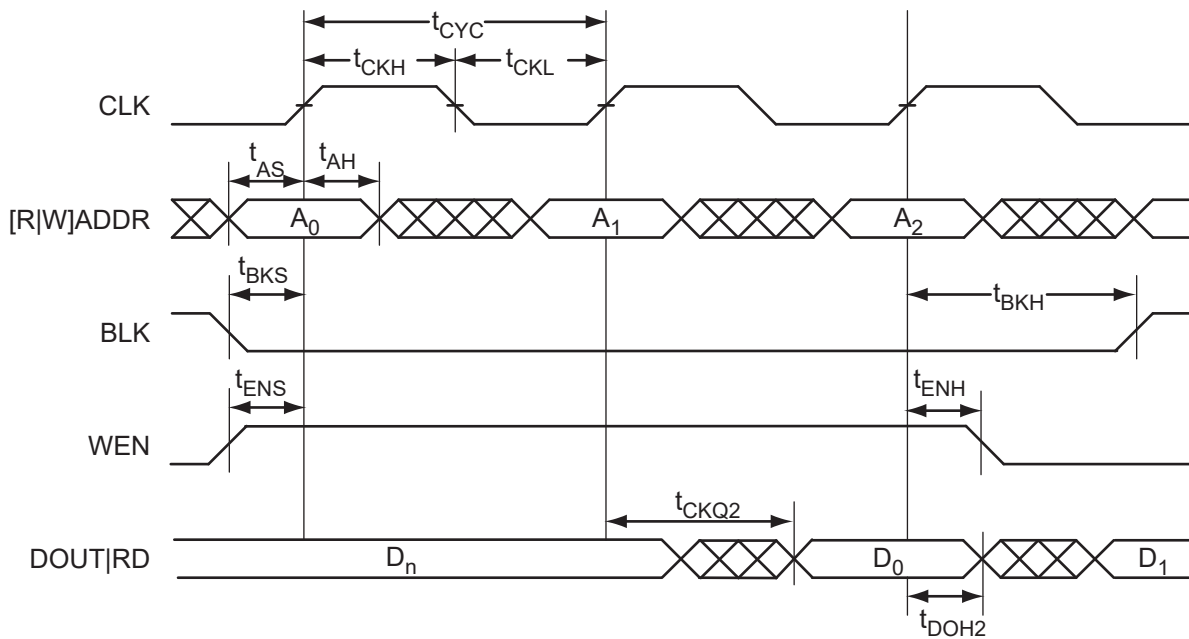


Figure 2-42 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.

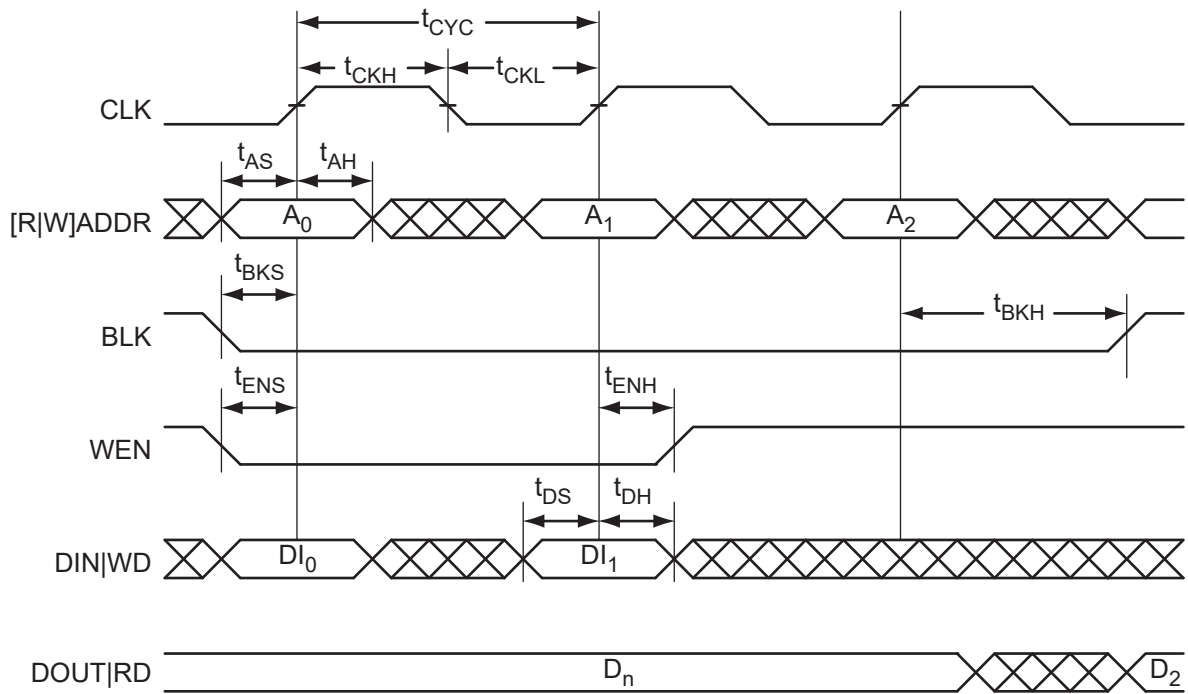


Figure 2-43 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

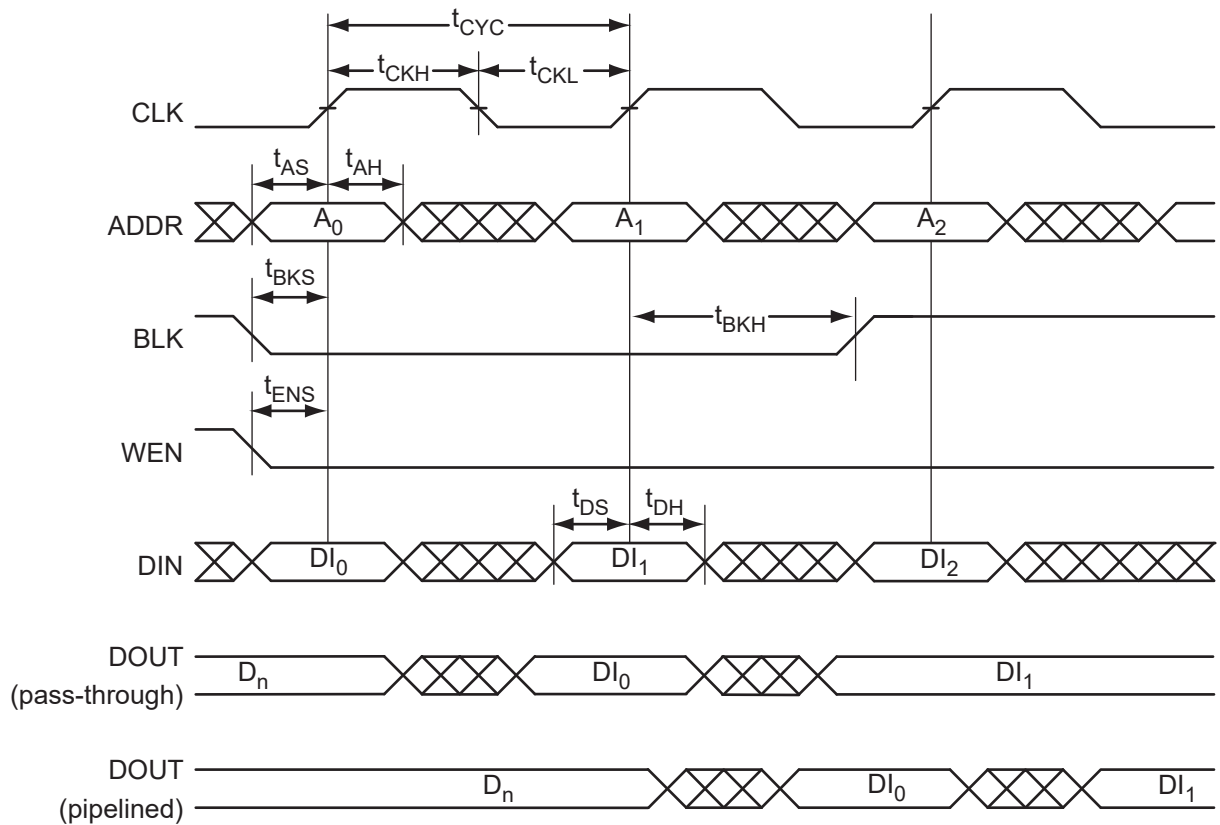


Figure 2-44 • RAM Write, Output as Write Data. Applicable to RAM4K9 Only.



Figure 2-45 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.

Timing Characteristics

Table 2-99 • RAM4K9

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|---|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| t_{ENH} | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| t_{BKS} | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| t_{BKH} | BLK hold time | 0.02 | 0.02 | 0.02 | ns |
| t_{DS} | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 1.79 | 2.03 | 2.39 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.36 | 2.68 | 3.15 | ns |
| t_{CKQ2} | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t_{C2CWWL}^1 | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge | 0.33 | 0.28 | 0.25 | ns |
| t_{C2CWWH}^1 | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| t_{RSTBQ} | RESET Low to data out Low on DO (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DO (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-100 • RAM512X18
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|----------------|--|------|------|------|-------|
| t_{AS} | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| t_{AH} | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{ENS} | REN, WEN setup time | 0.18 | 0.20 | 0.24 | ns |
| t_{ENH} | REN, WEN hold time | 0.06 | 0.07 | 0.08 | ns |
| t_{DS} | Input data (WD) setup time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input data (WD) hold time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to new data valid on RD (output retained) | 2.16 | 2.46 | 2.89 | ns |
| t_{CKQ2} | Clock High to new data valid on RD (pipelined) | 0.90 | 1.02 | 1.20 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.50 | 0.43 | 0.38 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.59 | 0.50 | 0.44 | ns |
| t_{RSTBQ} | RESET Low to data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum frequency | 310 | 272 | 231 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) on page 2-6 for derating values.

FIFO

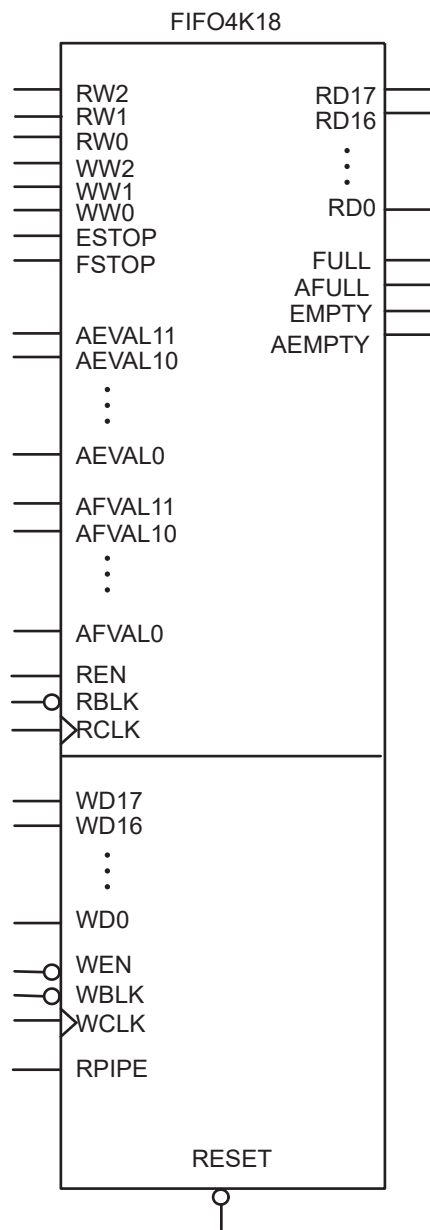


Figure 2-46 • FIFO Model

Timing Waveforms



Figure 2-47 • FIFO Read



Figure 2-48 • FIFO Write

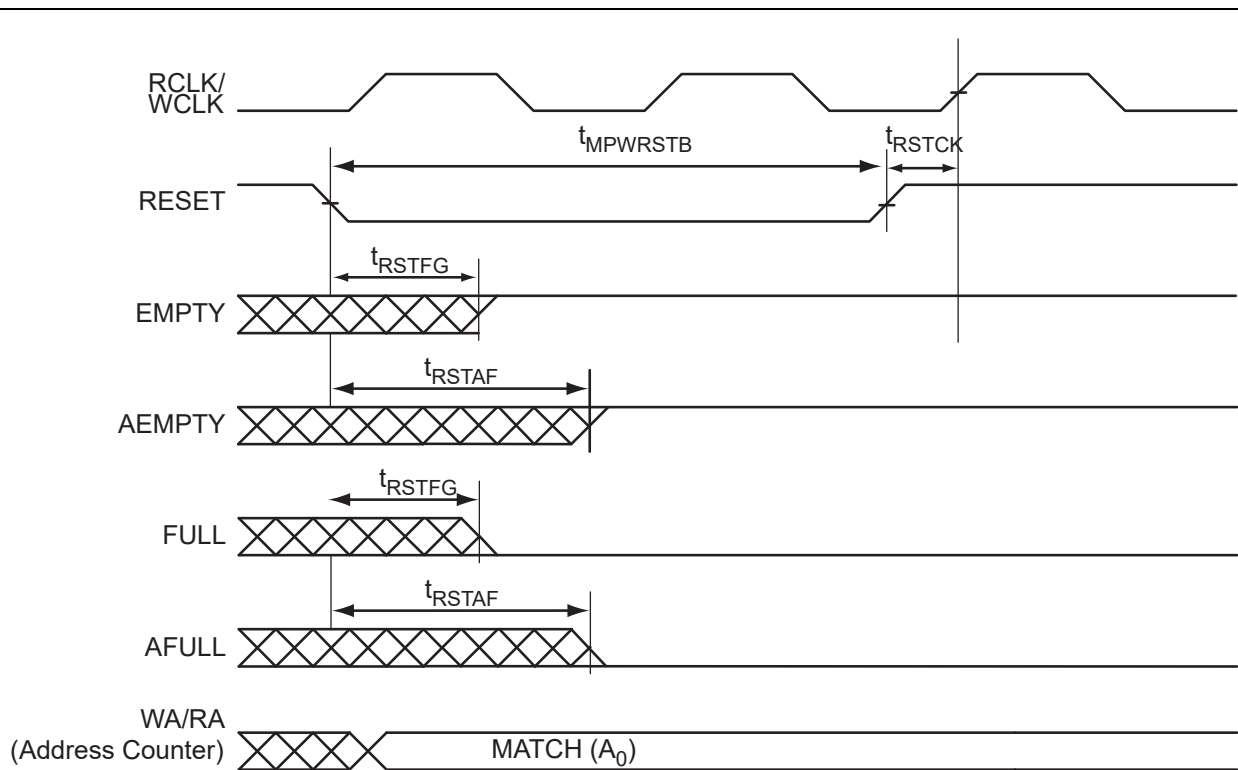


Figure 2-49 • FIFO Reset

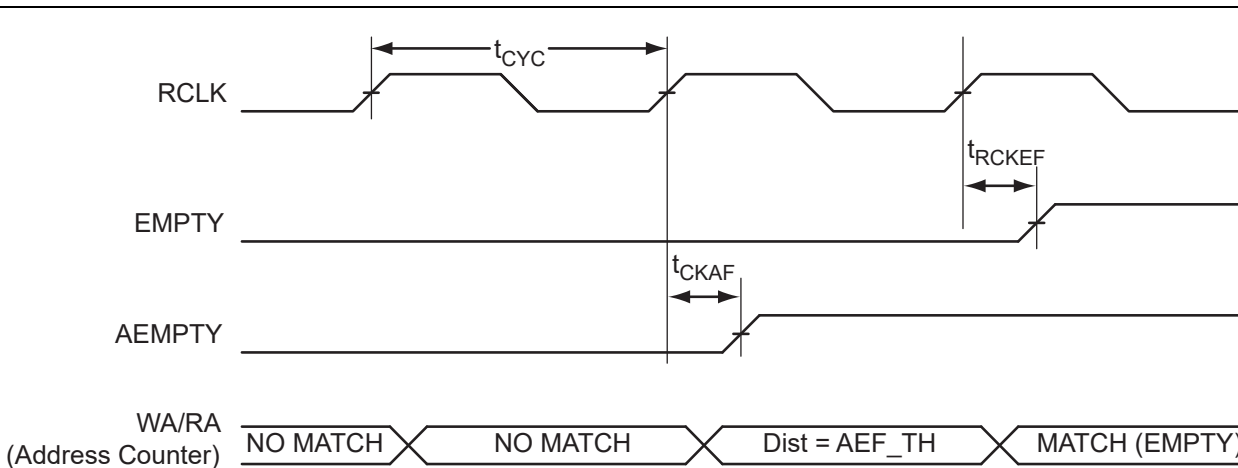


Figure 2-50 • FIFO EMPTY Flag and AEMPTY Flag Assertion



Figure 2-51 • FIFO FULL Flag and AFULL Flag Assertion



Figure 2-52 • FIFO EMPTY Flag and AEMPTY Flag Deassertion



Figure 2-53 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 2-101 • FIFO

 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | -2 | -1 | Std. | Units |
|---------------|---|------|------|------|-------|
| t_{ENS} | REN, WEN Setup Time | 1.38 | 1.57 | 1.84 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.02 | 0.02 | 0.02 | ns |
| t_{BKS} | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| t_{BKH} | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{DS} | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| t_{DH} | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| t_{CKQ1} | Clock High to New Data Valid on RD (pass-through) | 2.36 | 2.68 | 3.15 | ns |
| t_{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| t_{RCKEF} | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| t_{WCKFF} | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| t_{CKAF} | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| t_{RSTFG} | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| t_{RSTAF} | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| t_{RSTBQ} | RESET Low to Data Out Low on RD (pass-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| t_{CYC} | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| F_{MAX} | Maximum Frequency | 310 | 272 | 231 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

3 – Pin Descriptions and Packaging

Supply Pins

GND**Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ**Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC**Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx**I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

VMVx**I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F**PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the [ProASIC3E FPGA Fabric User's Guide](#) for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

VCOMPLA/B/C/D/E/F**PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

VJTAG**JTAG Supply Voltage**

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG

interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to [Table 3-1](#) for more information.

Table 3-1 • Recommended Tie-Off Values for the TCK and TRST Pins

| VJTAG | Tie-Off Resistance |
|----------------|------------------------------|
| VJTAG at 3.3 V | 200 Ω to 1 k Ω |
| VJTAG at 2.5 V | 200 Ω to 1 k Ω |
| VJTAG at 1.8 V | 500 Ω to 1 k Ω |
| VJTAG at 1.5 V | 500 Ω to 1 k Ω |

Notes:

1. Equivalent parallel resistance if more than one device is on the JTAG chain
2. The TCK pin can be pulled up/down.
3. The TRST pin is pulled down.

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from [Table 3-1](#) and must satisfy the parallel resistance value requirement. The values in [Table 3-1](#) correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC

No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC

Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

ProASIC3E FPGA Fabric User's Guide

http://www.microsemi.com/document-portal/doc_download/130883-proasic3e-fpga-fabric-user-s-guide

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/document-portal/doc_download/131095-package-mechanical-drawings

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: <http://www.microsemi.com/products/fpga-soc/solutions>.

4 – Package Pin Assignments

PQ208



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

Package Pin Assignments

| PQ208 | | PQ208 | | PQ208 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| 1 | GND | 37 | IO184PDB6V2 | 73 | IO145NDB5V1 |
| 2 | GNDQ | 38 | IO184NDB6V2 | 74 | IO145PDB5V1 |
| 3 | VMV7 | 39 | IO180PSB6V1 | 75 | IO143NDB5V1 |
| 4 | GAB2/IO220PSB7V3 | 40 | VCCIB6 | 76 | IO143PDB5V1 |
| 5 | GAA2/IO221PDB7V3 | 41 | GND | 77 | IO137NDB5V0 |
| 6 | IO221NDB7V3 | 42 | IO176PDB6V1 | 78 | IO137PDB5V0 |
| 7 | GAC2/IO219PDB7V3 | 43 | IO176NDB6V1 | 79 | IO135NDB5V0 |
| 8 | IO219NDB7V3 | 44 | GEC1/IO169PDB6V0 | 80 | IO135PDB5V0 |
| 9 | IO215PDB7V3 | 45 | GEC0/IO169NDB6V0 | 81 | GND |
| 10 | IO215NDB7V3 | 46 | GEB1/IO168PPB6V0 | 82 | IO131NDB4V2 |
| 11 | IO212PDB7V2 | 47 | GEA1/IO167PPB6V0 | 83 | IO131PDB4V2 |
| 12 | IO212NDB7V2 | 48 | GEB0/IO168NPB6V0 | 84 | IO129NDB4V2 |
| 13 | IO208PDB7V2 | 49 | GEA0/IO167NPB6V0 | 85 | IO129PDB4V2 |
| 14 | IO208NDB7V2 | 50 | VMV6 | 86 | IO127NDB4V2 |
| 15 | IO204PSB7V1 | 51 | GNDQ | 87 | IO127PDB4V2 |
| 16 | VCC | 52 | GND | 88 | VCC |
| 17 | GND | 53 | VMV5 | 89 | VCCIB4 |
| 18 | VCCIB7 | 54 | GNDQ | 90 | IO121NDB4V1 |
| 19 | IO200PDB7V1 | 55 | IO166NDB5V3 | 91 | IO121PDB4V1 |
| 20 | IO200NDB7V1 | 56 | GEA2/IO166PDB5V3 | 92 | IO119NDB4V1 |
| 21 | IO196PSB7V0 | 57 | IO165NDB5V3 | 93 | IO119PDB4V1 |
| 22 | GFC1/IO192PSB7V0 | 58 | GEB2/IO165PDB5V3 | 94 | IO113NDB4V0 |
| 23 | GFB1/IO191PDB7V0 | 59 | IO164NDB5V3 | 95 | GDC2/IO113PDB4V0 |
| 24 | GFB0/IO191NDB7V0 | 60 | GEC2/IO164PDB5V3 | 96 | IO112NDB4V0 |
| 25 | VCOMPLF | 61 | IO163PSB5V3 | 97 | GND |
| 26 | GFA0/IO190NPB6V2 | 62 | VCCIB5 | 98 | GDB2/IO112PDB4V0 |
| 27 | VCCPLF | 63 | IO161PSB5V3 | 99 | GDA2/IO111PSB4V0 |
| 28 | GFA1/IO190PPB6V2 | 64 | IO157NDB5V2 | 100 | GNDQ |
| 29 | GND | 65 | GND | 101 | TCK |
| 30 | GFA2/IO189PDB6V2 | 66 | IO157PDB5V2 | 102 | TDI |
| 31 | IO189NDB6V2 | 67 | IO153NDB5V2 | 103 | TMS |
| 32 | GFB2/IO188PPB6V2 | 68 | IO153PDB5V2 | 104 | VMV4 |
| 33 | GFC2/IO187PPB6V2 | 69 | IO149NDB5V1 | 105 | GND |
| 34 | IO188NPB6V2 | 70 | IO149PDB5V1 | 106 | VPUMP |
| 35 | IO187NPB6V2 | 71 | VCC | 107 | GNDQ |
| 36 | VCC | 72 | VCCIB5 | 108 | TDO |

| PQ208 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | VMV3 |
| 112 | GDA0/IO110NPB3V2 |
| 113 | GDB0/IO109NPB3V2 |
| 114 | GDA1/IO110PPB3V2 |
| 115 | GDB1/IO109PPB3V2 |
| 116 | GDC0/IO108NDB3V2 |
| 117 | GDC1/IO108PDB3V2 |
| 118 | IO105NDB3V2 |
| 119 | IO105PDB3V2 |
| 120 | IO101NDB3V1 |
| 121 | IO101PDB3V1 |
| 122 | GND |
| 123 | VCCIB3 |
| 124 | GCC2/IO90PSB3V0 |
| 125 | GCB2/IO89PSB3V0 |
| 126 | NC |
| 127 | IO88NDB3V0 |
| 128 | GCA2/IO88PDB3V0 |
| 129 | GCA1/IO87PPB3V0 |
| 130 | GND |
| 131 | VCCPLC |
| 132 | GCA0/IO87NPB3V0 |
| 133 | VCOMPLC |
| 134 | GCB0/IO86NDB2V3 |
| 135 | GCB1/IO86PDB2V3 |
| 136 | GCC1/IO85PSB2V3 |
| 137 | IO83NDB2V3 |
| 138 | IO83PDB2V3 |
| 139 | IO81PSB2V3 |
| 140 | VCCIB2 |
| 141 | GND |
| 142 | VCC |
| 143 | IO73NDB2V2 |
| 144 | IO73PDB2V2 |

| PQ208 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| 145 | IO71NDB2V2 |
| 146 | IO71PDB2V2 |
| 147 | IO67NDB2V1 |
| 148 | IO67PDB2V1 |
| 149 | IO65NDB2V1 |
| 150 | IO65PDB2V1 |
| 151 | GBC2/IO60PSB2V0 |
| 152 | GBA2/IO58PSB2V0 |
| 153 | GBB2/IO59PSB2V0 |
| 154 | VMV2 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV1 |
| 158 | GNDQ |
| 159 | GBA1/IO57PDB1V3 |
| 160 | GBA0/IO57NDB1V3 |
| 161 | GBB1/IO56PDB1V3 |
| 162 | GND |
| 163 | GBB0/IO56NDB1V3 |
| 164 | GBC1/IO55PDB1V3 |
| 165 | GBC0/IO55NDB1V3 |
| 166 | IO51PDB1V2 |
| 167 | IO51NDB1V2 |
| 168 | IO47PDB1V1 |
| 169 | IO47NDB1V1 |
| 170 | VCCIB1 |
| 171 | VCC |
| 172 | IO43PSB1V1 |
| 173 | IO41PDB1V1 |
| 174 | IO41NDB1V1 |
| 175 | IO35PDB1V0 |
| 176 | IO35NDB1V0 |
| 177 | IO31PDB0V3 |
| 178 | GND |
| 179 | IO31NDB0V3 |
| 180 | IO29PDB0V3 |

| PQ208 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| 181 | IO29NDB0V3 |
| 182 | IO27PDB0V3 |
| 183 | IO27NDB0V3 |
| 184 | IO23PDB0V2 |
| 185 | IO23NDB0V2 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO18PDB0V2 |
| 189 | IO18NDB0V2 |
| 190 | IO15PDB0V1 |
| 191 | IO15NDB0V1 |
| 192 | IO12PSB0V1 |
| 193 | IO11PDB0V1 |
| 194 | IO11NDB0V1 |
| 195 | GND |
| 196 | IO08PDB0V1 |
| 197 | IO08NDB0V1 |
| 198 | IO05PDB0V0 |
| 199 | IO05NDB0V0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO02PDB0V0 |
| 202 | GAC0/IO02NDB0V0 |
| 203 | GAB1/IO01PDB0V0 |
| 204 | GAB0/IO01NDB0V0 |
| 205 | GAA1/IO00PDB0V0 |
| 206 | GAA0/IO00NDB0V0 |
| 207 | GNDQ |
| 208 | VMV0 |

Package Pin Assignments

| PQ208 | | PQ208 | | PQ208 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| 1 | GND | 40 | VCCIB6 | 79 | IO194NDB5V0 |
| 2 | GNDQ | 41 | GND | 80 | IO194PDB5V0 |
| 3 | VMV7 | 42 | IO244PDB6V1 | 81 | GND |
| 4 | GAB2/IO308PSB7V4 | 43 | IO244NDB6V1 | 82 | IO184NDB4V3 |
| 5 | GAA2/IO309PDB7V4 | 44 | GEC1/IO236PDB6V0 | 83 | IO184PDB4V3 |
| 6 | IO309NDB7V4 | 45 | GEC0/IO236NDB6V0 | 84 | IO180NDB4V3 |
| 7 | GAC2/IO307PDB7V4 | 46 | GEB1/IO235PPB6V0 | 85 | IO180PDB4V3 |
| 8 | IO307NDB7V4 | 47 | GEA1/IO234PPB6V0 | 86 | IO176NDB4V2 |
| 9 | IO303PDB7V3 | 48 | GEB0/IO235NPB6V0 | 87 | IO176PDB4V2 |
| 10 | IO303NDB7V3 | 49 | GEA0/IO234NPB6V0 | 88 | VCC |
| 11 | IO299PDB7V3 | 50 | VMV6 | 89 | VCCIB4 |
| 12 | IO299NDB7V3 | 51 | GNDQ | 90 | IO170NDB4V2 |
| 13 | IO295PDB7V2 | 52 | GND | 91 | IO170PDB4V2 |
| 14 | IO295NDB7V2 | 53 | VMV5 | 92 | IO166NDB4V1 |
| 15 | IO291PSB7V2 | 54 | GNDQ | 93 | IO166PDB4V1 |
| 16 | VCC | 55 | IO233NDB5V4 | 94 | IO156NDB4V0 |
| 17 | GND | 56 | GEA2/IO233PDB5V4 | 95 | GDC2/IO156PDB4V0 |
| 18 | VCCIB7 | 57 | IO232NDB5V4 | 96 | IO154NPB4V0 |
| 19 | IO285PDB7V1 | 58 | GEB2/IO232PDB5V4 | 97 | GND |
| 20 | IO285NDB7V1 | 59 | IO231NDB5V4 | 98 | GDB2/IO155PSB4V0 |
| 21 | IO279PSB7V0 | 60 | GEC2/IO231PDB5V4 | 99 | GDA2/IO154PPB4V0 |
| 22 | GFC1/IO275PSB7V0 | 61 | IO230PSB5V4 | 100 | GNDQ |
| 23 | GFB1/IO274PDB7V0 | 62 | VCCIB5 | 101 | TCK |
| 24 | GFB0/IO274NDB7V0 | 63 | IO218NDB5V3 | 102 | TDI |
| 25 | VCOMPLF | 64 | IO218PDB5V3 | 103 | TMS |
| 26 | GFA0/IO273NPB6V4 | 65 | GND | 104 | VMV4 |
| 27 | VCCPLF | 66 | IO214PSB5V2 | 105 | GND |
| 28 | GFA1/IO273PPB6V4 | 67 | IO212NDB5V2 | 106 | VPUMP |
| 29 | GND | 68 | IO212PDB5V2 | 107 | GNDQ |
| 30 | GFA2/IO272PDB6V4 | 69 | IO208NDB5V1 | 108 | TDO |
| 31 | IO272NDB6V4 | 70 | IO208PDB5V1 | 109 | TRST |
| 32 | GFB2/IO271PPB6V4 | 71 | VCC | 110 | VJTAG |
| 33 | GFC2/IO270PPB6V4 | 72 | VCCIB5 | 111 | VMV3 |
| 34 | IO271NPB6V4 | 73 | IO202NDB5V1 | 112 | GDA0/IO153NPB3V4 |
| 35 | IO270NPB6V4 | 74 | IO202PDB5V1 | 113 | GDB0/IO152NPB3V4 |
| 36 | VCC | 75 | IO198NDB5V0 | 114 | GDA1/IO153PPB3V4 |
| 37 | IO252PDB6V2 | 76 | IO198PDB5V0 | 115 | GDB1/IO152PPB3V4 |
| 38 | IO252NDB6V2 | 77 | IO197NDB5V0 | 116 | GDC0/IO151NDB3V4 |
| 39 | IO248PSB6V1 | 78 | IO197PDB5V0 | 117 | GDC1/IO151PDB3V4 |

| PQ208 | | PQ208 | | PQ208 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| 118 | IO134NDB3V2 | 157 | VMV1 | 196 | IO11PDB0V1 |
| 119 | IO134PDB3V2 | 158 | GNDQ | 197 | IO11NDB0V1 |
| 120 | IO132NDB3V2 | 159 | GBA1/IO81PDB1V4 | 198 | IO08PDB0V0 |
| 121 | IO132PDB3V2 | 160 | GBA0/IO81NDB1V4 | 199 | IO08NDB0V0 |
| 122 | GND | 161 | GBB1/IO80PDB1V4 | 200 | VCCIB0 |
| 123 | VCCIB3 | 162 | GND | 201 | GAC1/IO02PDB0V0 |
| 124 | GCC2/IO117PSB3V0 | 163 | GBB0/IO80NDB1V4 | 202 | GAC0/IO02NDB0V0 |
| 125 | GCB2/IO116PSB3V0 | 164 | GBC1/IO79PDB1V4 | 203 | GAB1/IO01PDB0V0 |
| 126 | NC | 165 | GBC0/IO79NDB1V4 | 204 | GAB0/IO01NDB0V0 |
| 127 | IO115NDB3V0 | 166 | IO74PDB1V4 | 205 | GAA1/IO00PDB0V0 |
| 128 | GCA2/IO115PDB3V0 | 167 | IO74NDB1V4 | 206 | GAA0/IO00NDB0V0 |
| 129 | GCA1/IO114PPB3V0 | 168 | IO70PDB1V3 | 207 | GNDQ |
| 130 | GND | 169 | IO70NDB1V3 | 208 | VMV0 |
| 131 | VCCPLC | 170 | VCCIB1 | | |
| 132 | GCA0/IO114NPB3V0 | 171 | VCC | | |
| 133 | VCOMPLC | 172 | IO56PSB1V1 | | |
| 134 | GCB0/IO113NDB2V3 | 173 | IO55PDB1V1 | | |
| 135 | GCB1/IO113PDB2V3 | 174 | IO55NDB1V1 | | |
| 136 | GCC1/IO112PSB2V3 | 175 | IO54PDB1V1 | | |
| 137 | IO110NDB2V3 | 176 | IO54NDB1V1 | | |
| 138 | IO110PDB2V3 | 177 | IO40PDB0V4 | | |
| 139 | IO106PSB2V3 | 178 | GND | | |
| 140 | VCCIB2 | 179 | IO40NDB0V4 | | |
| 141 | GND | 180 | IO37PDB0V4 | | |
| 142 | VCC | 181 | IO37NDB0V4 | | |
| 143 | IO99NDB2V2 | 182 | IO35PDB0V4 | | |
| 144 | IO99PDB2V2 | 183 | IO35NDB0V4 | | |
| 145 | IO96NDB2V1 | 184 | IO32PDB0V3 | | |
| 146 | IO96PDB2V1 | 185 | IO32NDB0V3 | | |
| 147 | IO91NDB2V1 | 186 | VCCIB0 | | |
| 148 | IO91PDB2V1 | 187 | VCC | | |
| 149 | IO88NDB2V0 | 188 | IO28PDB0V3 | | |
| 150 | IO88PDB2V0 | 189 | IO28NDB0V3 | | |
| 151 | GBC2/IO84PSB2V0 | 190 | IO24PDB0V2 | | |
| 152 | GBA2/IO82PSB2V0 | 191 | IO24NDB0V2 | | |
| 153 | GBB2/IO83PSB2V0 | 192 | IO21PSB0V2 | | |
| 154 | VMV2 | 193 | IO16PDB0V1 | | |
| 155 | GNDQ | 194 | IO16NDB0V1 | | |
| 156 | GND | 195 | GND | | |

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

| FG256 | |
|------------|------------------|
| Pin Number | A3PE600 Function |
| A1 | GND |
| A2 | GAA0/IO00NDB0V0 |
| A3 | GAA1/IO00PDB0V0 |
| A4 | GAB0/IO01NDB0V0 |
| A5 | IO05PDB0V0 |
| A6 | IO10PDB0V1 |
| A7 | IO12PDB0V2 |
| A8 | IO16NDB0V2 |
| A9 | IO23NDB1V0 |
| A10 | IO23PDB1V0 |
| A11 | IO28NDB1V1 |
| A12 | IO28PDB1V1 |
| A13 | GBB1/IO34PDB1V1 |
| A14 | GBA0/IO35NDB1V1 |
| A15 | GBA1/IO35PDB1V1 |
| A16 | GND |
| B1 | GAB2/IO133PDB7V1 |
| B2 | GAA2/IO134PDB7V1 |
| B3 | GNDQ |
| B4 | GAB1/IO01PDB0V0 |
| B5 | IO05NDB0V0 |
| B6 | IO10NDB0V1 |
| B7 | IO12NDB0V2 |
| B8 | IO16PDB0V2 |
| B9 | IO20NDB1V0 |
| B10 | IO24NDB1V0 |
| B11 | IO24PDB1V0 |
| B12 | GBC1/IO33PDB1V1 |
| B13 | GBB0/IO34NDB1V1 |
| B14 | GNDQ |
| B15 | GBA2/IO36PDB2V0 |
| B16 | IO42NDB2V0 |
| C1 | IO133NDB7V1 |
| C2 | IO134NDB7V1 |
| C3 | VMV7 |
| C4 | VCCPLA |

| FG256 | |
|------------|------------------|
| Pin Number | A3PE600 Function |
| C5 | GAC0/IO02NDB0V0 |
| C6 | GAC1/IO02PDB0V0 |
| C7 | IO15NDB0V2 |
| C8 | IO15PDB0V2 |
| C9 | IO20PDB1V0 |
| C10 | IO25NDB1V0 |
| C11 | IO27PDB1V0 |
| C12 | GBC0/IO33NDB1V1 |
| C13 | VCCPLB |
| C14 | VMV2 |
| C15 | IO36NDB2V0 |
| C16 | IO42PDB2V0 |
| D1 | IO128PDB7V1 |
| D2 | IO129PDB7V1 |
| D3 | GAC2/IO132PDB7V1 |
| D4 | VCOMPLA |
| D5 | GNDQ |
| D6 | IO09NDB0V1 |
| D7 | IO09PDB0V1 |
| D8 | IO13PDB0V2 |
| D9 | IO21PDB1V0 |
| D10 | IO25PDB1V0 |
| D11 | IO27NDB1V0 |
| D12 | GNDQ |
| D13 | VCOMPLB |
| D14 | GBB2/IO37PDB2V0 |
| D15 | IO39PDB2V0 |
| D16 | IO39NDB2V0 |
| E1 | IO128NDB7V1 |
| E2 | IO129NDB7V1 |
| E3 | IO132NDB7V1 |
| E4 | IO130PDB7V1 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO13NDB0V2 |

| FG256 | |
|------------|------------------|
| Pin Number | A3PE600 Function |
| E9 | IO21NDB1V0 |
| E10 | VCCIB1 |
| E11 | VCCIB1 |
| E12 | VMV1 |
| E13 | GBC2/IO38PDB2V0 |
| E14 | IO37NDB2V0 |
| E15 | IO41NDB2V0 |
| E16 | IO41PDB2V0 |
| F1 | IO124PDB7V0 |
| F2 | IO125PDB7V0 |
| F3 | IO126PDB7V0 |
| F4 | IO130NDB7V1 |
| F5 | VCCIB7 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB2 |
| F13 | IO38NDB2V0 |
| F14 | IO40NDB2V0 |
| F15 | IO40PDB2V0 |
| F16 | IO45PSB2V1 |
| G1 | IO124NDB7V0 |
| G2 | IO125NDB7V0 |
| G3 | IO126NDB7V0 |
| G4 | GFC1/IO120PPB7V0 |
| G5 | VCCIB7 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB2 |

Package Pin Assignments

| FG256 | | FG256 | | FG256 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | A3PE600 Function | Pin Number | A3PE600 Function | Pin Number | A3PE600 Function |
| G13 | GCC1/IO50PPB2V1 | K1 | GFC2/IO115PSB6V1 | M5 | VMV5 |
| G14 | IO44NDB2V1 | K2 | IO113PPB6V1 | M6 | VCCIB5 |
| G15 | IO44PDB2V1 | K3 | IO112PDB6V1 | M7 | VCCIB5 |
| G16 | IO49NSB2V1 | K4 | IO112NDB6V1 | M8 | IO84NDB5V0 |
| H1 | GFB0/IO119NPB7V0 | K5 | VCCIB6 | M9 | IO84PDB5V0 |
| H2 | GFA0/IO118NDB6V1 | K6 | VCC | M10 | VCCIB4 |
| H3 | GFB1/IO119PPB7V0 | K7 | GND | M11 | VCCIB4 |
| H4 | VCOMPLF | K8 | GND | M12 | VMV3 |
| H5 | GFC0/IO120NPB7V0 | K9 | GND | M13 | VCCPLD |
| H6 | VCC | K10 | GND | M14 | GDB1/IO66PPB3V1 |
| H7 | GND | K11 | VCC | M15 | GDC1/IO65PDB3V1 |
| H8 | GND | K12 | VCCIB3 | M16 | IO61NDB3V1 |
| H9 | GND | K13 | IO54NPB3V0 | N1 | IO105PDB6V0 |
| H10 | GND | K14 | IO57NPB3V0 | N2 | IO105NDB6V0 |
| H11 | VCC | K15 | IO55NPB3V0 | N3 | GEC1/IO104PPB6V0 |
| H12 | GCC0/IO50NPB2V1 | K16 | IO57PPB3V0 | N4 | VCOMPLE |
| H13 | GCB1/IO51PPB2V1 | L1 | IO113NPB6V1 | N5 | GNDQ |
| H14 | GCA0/IO52NPB3V0 | L2 | IO109PPB6V0 | N6 | GEA2/IO101PPB5V2 |
| H15 | VCOMPLC | L3 | IO108PDB6V0 | N7 | IO92NDB5V1 |
| H16 | GCB0/IO51NPB2V1 | L4 | IO108NDB6V0 | N8 | IO90NDB5V1 |
| J1 | GFA2/IO117PSB6V1 | L5 | VCCIB6 | N9 | IO82NDB5V0 |
| J2 | GFA1/IO118PDB6V1 | L6 | GND | N10 | IO74NDB4V1 |
| J3 | VCCPLF | L7 | VCC | N11 | IO74PDB4V1 |
| J4 | IO116NDB6V1 | L8 | VCC | N12 | GNDQ |
| J5 | GFB2/IO116PDB6V1 | L9 | VCC | N13 | VCOMPLD |
| J6 | VCC | L10 | VCC | N14 | VJTAG |
| J7 | GND | L11 | GND | N15 | GDC0/IO65NDB3V1 |
| J8 | GND | L12 | VCCIB3 | N16 | GDA1/IO67PDB3V1 |
| J9 | GND | L13 | GDB0/IO66NPB3V1 | P1 | GEB1/IO103PDB6V0 |
| J10 | GND | L14 | IO60NDB3V1 | P2 | GEB0/IO103NDB6V0 |
| J11 | VCC | L15 | IO60PDB3V1 | P3 | VMV6 |
| J12 | GCB2/IO54PPB3V0 | L16 | IO61PDB3V1 | P4 | VCCPLE |
| J13 | GCA1/IO52PPB3V0 | M1 | IO109NPB6V0 | P5 | IO101NPB5V2 |
| J14 | GCC2/IO55PPB3V0 | M2 | IO106NDB6V0 | P6 | IO95PPB5V1 |
| J15 | VCCPLC | M3 | IO106PDB6V0 | P7 | IO92PDB5V1 |
| J16 | GCA2/IO53PSB3V0 | M4 | GEC0/IO104NPB6V0 | P8 | IO90PDB5V1 |

| FG256 | |
|------------|------------------|
| Pin Number | A3PE600 Function |
| P9 | IO82PDB5V0 |
| P10 | IO76NDB4V1 |
| P11 | IO76PDB4V1 |
| P12 | VMV4 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO67NDB3V1 |
| R1 | GEA1/IO102PDB6V0 |
| R2 | GEA0/IO102NDB6V0 |
| R3 | GNDQ |
| R4 | GEC2/IO99PDB5V2 |
| R5 | IO95NPB5V1 |
| R6 | IO91NDB5V1 |
| R7 | IO91PDB5V1 |
| R8 | IO83NDB5V0 |
| R9 | IO83PDB5V0 |
| R10 | IO77NDB4V1 |
| R11 | IO77PDB4V1 |
| R12 | IO69NDB4V0 |
| R13 | GDB2/IO69PDB4V0 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO100NDB5V2 |
| T3 | GEB2/IO100PDB5V2 |
| T4 | IO99NDB5V2 |
| T5 | IO88NDB5V0 |
| T6 | IO88PDB5V0 |
| T7 | IO89NSB5V0 |
| T8 | IO80NSB4V1 |
| T9 | IO81NDB4V1 |
| T10 | IO81PDB4V1 |
| T11 | IO70NDB4V0 |
| T12 | GDC2/IO70PDB4V0 |

| FG256 | |
|------------|------------------|
| Pin Number | A3PE600 Function |
| T13 | IO68NDB4V0 |
| T14 | GDA2/IO68PDB4V0 |
| T15 | TMS |
| T16 | GND |

FG324



Note: This is the bottom view of the package.

Note

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| FG324 | |
|------------|------------------|
| Pin Number | A3PE3000 FBGA |
| A1 | GND |
| A2 | IO08NDB0V0 |
| A3 | IO08PDB0V0 |
| A4 | IO10NDB0V1 |
| A5 | IO10PDB0V1 |
| A6 | IO12PDB0V1 |
| A7 | GND |
| A8 | IO32NDB0V3 |
| A9 | IO32PDB0V3 |
| A10 | IO42PPB1V0 |
| A11 | IO52NPB1V1 |
| A12 | GND |
| A13 | IO66NDB1V3 |
| A14 | IO72NDB1V3 |
| A15 | IO72PDB1V3 |
| A16 | IO74NDB1V4 |
| A17 | IO74PDB1V4 |
| A18 | GND |
| B1 | IO305PDB7V3 |
| B2 | GAB2/IO308PDB7V4 |
| B3 | GAA0/IO00NPB0V0 |
| B4 | VCCIB0 |
| B5 | GNDQ |
| B6 | IO12NDB0V1 |
| B7 | IO18NDB0V2 |
| B8 | VCCIB0 |
| B9 | IO42NPB1V0 |
| B10 | IO44NDB1V0 |
| B11 | VCCIB1 |
| B12 | IO52PPB1V1 |
| B13 | IO66PDB1V3 |
| B14 | GNDQ |
| B15 | VCCIB1 |
| B16 | GBA0/IO81NDB1V4 |
| B17 | GBA1/IO81PDB1V4 |
| B18 | IO88PDB2V0 |

| FG324 | |
|------------|------------------|
| Pin Number | A3PE3000 FBGA |
| C1 | IO305NDB7V3 |
| C2 | IO308NDB7V4 |
| C3 | GAA2/IO309PPB7V4 |
| C4 | GAA1/IO00PPB0V0 |
| C5 | VMV0 |
| C6 | IO14NDB0V1 |
| C7 | IO18PDB0V2 |
| C8 | IO40NDB0V4 |
| C9 | IO40PDB0V4 |
| C10 | IO44PDB1V0 |
| C11 | IO56NDB1V1 |
| C12 | IO64NDB1V2 |
| C13 | IO64PDB1V2 |
| C14 | VMV1 |
| C15 | GBC0/IO79NDB1V4 |
| C16 | GBC1/IO79PDB1V4 |
| C17 | GBB2/IO83PPB2V0 |
| C18 | IO88NDB2V0 |
| D1 | IO303PDB7V3 |
| D2 | VCCIB7 |
| D3 | GAC2/IO307PPB7V4 |
| D4 | IO309NPB7V4 |
| D5 | GAB1/IO01PPB0V0 |
| D6 | IO14PDB0V1 |
| D7 | IO24NDB0V2 |
| D8 | IO24PDB0V2 |
| D9 | IO28PDB0V3 |
| D10 | IO48NDB1V0 |
| D11 | IO56PDB1V1 |
| D12 | IO60PPB1V2 |
| D13 | GBB0/IO80NDB1V4 |
| D14 | GBB1/IO80PDB1V4 |
| D15 | GBA2/IO82PDB2V0 |
| D16 | IO83NPB2V0 |
| D17 | VCCIB2 |
| D18 | IO90PDB2V1 |

| FG324 | |
|------------|-----------------|
| Pin Number | A3PE3000 FBGA |
| E1 | IO303NDB7V3 |
| E2 | GNDQ |
| E3 | VMV7 |
| E4 | IO307NPB7V4 |
| E5 | VCCPLA |
| E6 | GAB0/IO01NPB0V0 |
| E7 | VCCIB0 |
| E8 | GND |
| E9 | IO28NDB0V3 |
| E10 | IO48PDB1V0 |
| E11 | GND |
| E12 | VCCIB1 |
| E13 | IO60NPB1V2 |
| E14 | VCCPLB |
| E15 | IO82NDB2V0 |
| E16 | VMV2 |
| E17 | GNDQ |
| E18 | IO90NDB2V1 |
| F1 | IO299NDB7V3 |
| F2 | IO299PDB7V3 |
| F3 | IO295PDB7V2 |
| F4 | IO295NDB7V2 |
| F5 | VCOMPLA |
| F6 | IO291PPB7V2 |
| F7 | GAC0/IO02NDB0V0 |
| F8 | GAC1/IO02PDB0V0 |
| F9 | IO26PDB0V3 |
| F10 | IO34PDB0V4 |
| F11 | IO58NDB1V2 |
| F12 | IO58PDB1V2 |
| F13 | IO94PPB2V1 |
| F14 | VCOMPLB |
| F15 | GBC2/IO84PDB2V0 |
| F16 | IO84NDB2V0 |
| F17 | IO92NDB2V1 |
| F18 | IO92PDB2V1 |

Package Pin Assignments

| FG324 | | FG324 | | FG324 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | A3PE3000 FBGA | Pin Number | A3PE3000 FBGA | Pin Number | A3PE3000 FBGA |
| G1 | GND | J1 | IO267NDB6V4 | L1 | IO263NDB6V3 |
| G2 | IO287PDB7V1 | J2 | GFA0/IO273NDB6V4 | L2 | VCCIB6 |
| G3 | IO287NDB7V1 | J3 | VCOMPLF | L3 | IO259PDB6V3 |
| G4 | IO283PPB7V1 | J4 | GFA2/IO272PDB6V4 | L4 | IO259NDB6V3 |
| G5 | VCCIB7 | J5 | GFB0/IO274NPB7V0 | L5 | GND |
| G6 | IO279PDB7V0 | J6 | GFC0/IO275NDB7V0 | L6 | IO270NPB6V4 |
| G7 | IO291NPB7V2 | J7 | GFC1/IO275PDB7V0 | L7 | VCC |
| G8 | VCC | J8 | GND | L8 | VCC |
| G9 | IO26NDB0V3 | J9 | GND | L9 | GND |
| G10 | IO34NDB0V4 | J10 | GND | L10 | GND |
| G11 | VCC | J11 | GND | L11 | VCC |
| G12 | IO94NPB2V1 | J12 | GCA2/IO115PDB3V0 | L12 | VCC |
| G13 | IO98PDB2V2 | J13 | GCA1/IO114PDB3V0 | L13 | IO132PDB3V2 |
| G14 | VCCIB2 | J14 | GCA0/IO114NDB3V0 | L14 | GND |
| G15 | GCC0/IO112NPB2V3 | J15 | GCB0/IO113NDB2V3 | L15 | IO117NDB3V0 |
| G16 | IO104PDB2V2 | J16 | VCOMPLC | L16 | IO128NPB3V1 |
| G17 | IO104NDB2V2 | J17 | IO120NPB3V0 | L17 | VCCIB3 |
| G18 | GND | J18 | IO108NDB2V3 | L18 | IO124PPB3V1 |
| H1 | IO267PDB6V4 | K1 | IO263PDB6V3 | M1 | GND |
| H2 | VCCIB7 | K2 | GFA1/IO273PDB6V4 | M2 | IO255PDB6V2 |
| H3 | IO283NPB7V1 | K3 | VCCPLF | M3 | IO255NDB6V2 |
| H4 | GFB1/IO274PPB7V0 | K4 | IO272NDB6V4 | M4 | IO251PPB6V2 |
| H5 | GND | K5 | GFC2/IO270PPB6V4 | M5 | VCCIB6 |
| H6 | IO279NDB7V0 | K6 | GFB2/IO271PDB6V4 | M6 | GEB0/IO235NDB6V0 |
| H7 | VCC | K7 | IO271NDB6V4 | M7 | GEB1/IO235PDB6V0 |
| H8 | VCC | K8 | GND | M8 | VCC |
| H9 | GND | K9 | GND | M9 | IO192PPB4V4 |
| H10 | GND | K10 | GND | M10 | IO154NPB4V0 |
| H11 | VCC | K11 | GND | M11 | VCC |
| H12 | VCC | K12 | IO115NDB3V0 | M12 | GDA0/IO153NPB3V4 |
| H13 | IO98NDB2V2 | K13 | GCB2/IO116PDB3V0 | M13 | IO132NDB3V2 |
| H14 | GND | K14 | IO116NDB3V0 | M14 | VCCIB3 |
| H15 | GCB1/IO113PDB2V3 | K15 | GCC2/IO117PDB3V0 | M15 | IO134NDB3V2 |
| H16 | GCC1/IO112PPB2V3 | K16 | VCCPLC | M16 | IO134PDB3V2 |
| H17 | VCCIB2 | K17 | IO124NPB3V1 | M17 | IO128PPB3V1 |
| H18 | IO108PDB2V3 | K18 | IO120PPB3V0 | M18 | GND |

| FG324 | | FG324 | | FG324 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | A3PE3000 FBGA | Pin Number | A3PE3000 FBGA | Pin Number | A3PE3000 FBGA |
| N1 | IO247NDB6V1 | R1 | IO245NDB6V1 | U1 | IO241NDB6V0 |
| N2 | IO247PDB6V1 | R2 | VCCIB6 | U2 | GEA2/IO233PPB5V4 |
| N3 | IO251NPB6V2 | R3 | GEA1/IO234PPB6V0 | U3 | GEC2/IO231PPB5V4 |
| N4 | GEC0/IO236NDB6V0 | R4 | IO232NDB5V4 | U4 | VCCIB5 |
| N5 | VCOMPLE | R5 | GEB2/IO232PDB5V4 | U5 | GNDQ |
| N6 | IO212NDB5V2 | R6 | IO214NDB5V2 | U6 | IO208PDB5V1 |
| N7 | IO212PDB5V2 | R7 | IO202PDB5V1 | U7 | IO198PPB5V0 |
| N8 | IO192NPB4V4 | R8 | IO194PDB5V0 | U8 | VCCIB5 |
| N9 | IO174PDB4V2 | R9 | IO186PDB4V4 | U9 | IO182NPB4V3 |
| N10 | IO170PDB4V2 | R10 | IO178PDB4V3 | U10 | IO180NPB4V3 |
| N11 | GDA2/IO154PPB4V0 | R11 | IO168NSB4V1 | U11 | VCCIB4 |
| N12 | GDB2/IO155PPB4V0 | R12 | IO164PDB4V1 | U12 | IO166PPB4V1 |
| N13 | GDA1/IO153PPB3V4 | R13 | GDC2/IO156PDB4V0 | U13 | IO162PDB4V1 |
| N14 | VCOMPLD | R14 | TCK | U14 | GNDQ |
| N15 | GDB0/IO152NDB3V4 | R15 | VPUMP | U15 | VCCIB4 |
| N16 | GDB1/IO152PDB3V4 | R16 | TRST | U16 | TMS |
| N17 | IO138NDB3V3 | R17 | VCCIB3 | U17 | VMV3 |
| N18 | IO138PDB3V3 | R18 | IO142NDB3V3 | U18 | IO146NDB3V4 |
| P1 | IO245PDB6V1 | T1 | IO241PDB6V0 | V1 | GND |
| P2 | GNDQ | T2 | GEA0/IO234NPB6V0 | V2 | IO218NDB5V3 |
| P3 | VMV6 | T3 | IO233NPB5V4 | V3 | IO218PDB5V3 |
| P4 | GEC1/IO236PDB6V0 | T4 | IO231NPB5V4 | V4 | IO206NDB5V1 |
| P5 | VCCPLE | T5 | VMV5 | V5 | IO206PDB5V1 |
| P6 | IO214PDB5V2 | T6 | IO208NDB5V1 | V6 | IO198NPB5V0 |
| P7 | VCCIB5 | T7 | IO202NDB5V1 | V7 | GND |
| P8 | GND | T8 | IO194NDB5V0 | V8 | IO190NDB4V4 |
| P9 | IO174NDB4V2 | T9 | IO186NDB4V4 | V9 | IO190PDB4V4 |
| P10 | IO170NDB4V2 | T10 | IO178NDB4V3 | V10 | IO182PPB4V3 |
| P11 | GND | T11 | IO166NPB4V1 | V11 | IO180PPB4V3 |
| P12 | VCCIB4 | T12 | IO164NDB4V1 | V12 | GND |
| P13 | IO155NPB4V0 | T13 | IO156NDB4V0 | V13 | IO162NDB4V1 |
| P14 | VCCPLD | T14 | VMV4 | V14 | IO160NDB4V0 |
| P15 | VJTAG | T15 | TDI | V15 | IO160PDB4V0 |
| P16 | GDC0/IO151NDB3V4 | T16 | GNDQ | V16 | IO158NDB4V0 |
| P17 | GDC1/IO151PDB3V4 | T17 | TDO | V17 | IO158PDB4V0 |
| P18 | IO142PDB3V3 | T18 | IO146PDB3V4 | V18 | GND |

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

| FG484 | |
|------------|------------------|
| Pin Number | A3PE600 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO06NDB0V1 |
| A5 | IO06PDB0V1 |
| A6 | IO08NDB0V1 |
| A7 | IO08PDB0V1 |
| A8 | IO11PDB0V1 |
| A9 | IO17PDB0V2 |
| A10 | IO18NDB0V2 |
| A11 | IO18PDB0V2 |
| A12 | IO22PDB1V0 |
| A13 | IO26PDB1V0 |
| A14 | IO29NDB1V1 |
| A15 | IO29PDB1V1 |
| A16 | IO31NDB1V1 |
| A17 | IO31PDB1V1 |
| A18 | IO32NDB1V1 |
| A19 | NC |
| A20 | VCCIB1 |
| A21 | GND |
| A22 | GND |
| AA1 | GND |
| AA2 | VCCIB6 |
| AA3 | NC |
| AA4 | IO98PDB5V2 |
| AA5 | IO96NDB5V2 |
| AA6 | IO96PDB5V2 |
| AA7 | IO86NDB5V0 |
| AA8 | IO86PDB5V0 |
| AA9 | IO85PDB5V0 |
| AA10 | IO85NDB5V0 |
| AA11 | IO78PPB4V1 |
| AA12 | IO79NDB4V1 |
| AA13 | IO79PDB4V1 |
| AA14 | NC |

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| Pin Number | A3PE600 Function |
| AA15 | NC |
| AA16 | IO71NDB4V0 |
| AA17 | IO71PDB4V0 |
| AA18 | NC |
| AA19 | NC |
| AA20 | NC |
| AA21 | VCCIB3 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB5 |
| AB4 | IO97NDB5V2 |
| AB5 | IO97PDB5V2 |
| AB6 | IO93NDB5V1 |
| AB7 | IO93PDB5V1 |
| AB8 | IO87NDB5V0 |
| AB9 | IO87PDB5V0 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO75NDB4V1 |
| AB13 | IO75PDB4V1 |
| AB14 | IO72NDB4V0 |
| AB15 | IO72PDB4V0 |
| AB16 | IO73NDB4V0 |
| AB17 | IO73PDB4V0 |
| AB18 | NC |
| AB19 | NC |
| AB20 | VCCIB4 |
| AB21 | GND |
| AB22 | GND |
| B1 | GND |
| B2 | VCCIB7 |
| B3 | NC |
| B4 | IO03NDB0V0 |
| B5 | IO03PDB0V0 |
| B6 | IO07NDB0V1 |

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| Pin Number | A3PE600 Function |
| B7 | IO07PDB0V1 |
| B8 | IO11NDB0V1 |
| B9 | IO17NDB0V2 |
| B10 | IO14PDB0V2 |
| B11 | IO19PDB0V2 |
| B12 | IO22NDB1V0 |
| B13 | IO26NDB1V0 |
| B14 | NC |
| B15 | NC |
| B16 | IO30NDB1V1 |
| B17 | IO30PDB1V1 |
| B18 | IO32PDB1V1 |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB2 |
| B22 | GND |
| C1 | VCCIB7 |
| C2 | NC |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | IO04NDB0V0 |
| C7 | IO04PDB0V0 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO14NDB0V2 |
| C11 | IO19NDB0V2 |
| C12 | NC |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |

Package Pin Assignments

| FG484 | | FG484 | | FG484 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | A3PE600 Function | Pin Number | A3PE600 Function | Pin Number | A3PE600 Function |
| C21 | NC | E13 | IO24NDB1V0 | G5 | IO129PDB7V1 |
| C22 | VCCIB2 | E14 | IO24PDB1V0 | G6 | GAC2/IO132PDB7V1 |
| D1 | NC | E15 | GBC1/IO33PDB1V1 | G7 | VCOMPLA |
| D2 | NC | E16 | GBB0/IO34NDB1V1 | G8 | GNDQ |
| D3 | NC | E17 | GNDQ | G9 | IO09NDB0V1 |
| D4 | GND | E18 | GBA2/IO36PDB2V0 | G10 | IO09PDB0V1 |
| D5 | GAA0/IO00NDB0V0 | E19 | IO42NDB2V0 | G11 | IO13PDB0V2 |
| D6 | GAA1/IO00PDB0V0 | E20 | GND | G12 | IO21PDB1V0 |
| D7 | GAB0/IO01NDB0V0 | E21 | NC | G13 | IO25PDB1V0 |
| D8 | IO05PDB0V0 | E22 | NC | G14 | IO27NDB1V0 |
| D9 | IO10PDB0V1 | F1 | NC | G15 | GNDQ |
| D10 | IO12PDB0V2 | F2 | IO131NDB7V1 | G16 | VCOMPLB |
| D11 | IO16NDB0V2 | F3 | IO131PDB7V1 | G17 | GBB2/IO37PDB2V0 |
| D12 | IO23NDB1V0 | F4 | IO133NDB7V1 | G18 | IO39PDB2V0 |
| D13 | IO23PDB1V0 | F5 | IO134NDB7V1 | G19 | IO39NDB2V0 |
| D14 | IO28NDB1V1 | F6 | VMV7 | G20 | IO43PDB2V0 |
| D15 | IO28PDB1V1 | F7 | VCCPLA | G21 | IO43NDB2V0 |
| D16 | GBB1/IO34PDB1V1 | F8 | GAC0/IO02NDB0V0 | G22 | NC |
| D17 | GBA0/IO35NDB1V1 | F9 | GAC1/IO02PDB0V0 | H1 | NC |
| D18 | GBA1/IO35PDB1V1 | F10 | IO15NDB0V2 | H2 | NC |
| D19 | GND | F11 | IO15PDB0V2 | H3 | VCC |
| D20 | NC | F12 | IO20PDB1V0 | H4 | IO128NDB7V1 |
| D21 | NC | F13 | IO25NDB1V0 | H5 | IO129NDB7V1 |
| D22 | NC | F14 | IO27PDB1V0 | H6 | IO132NDB7V1 |
| E1 | NC | F15 | GBC0/IO33NDB1V1 | H7 | IO130PDB7V1 |
| E2 | NC | F16 | VCCPLB | H8 | VMV0 |
| E3 | GND | F17 | VMV2 | H9 | VCCIB0 |
| E4 | GAB2/IO133PDB7V1 | F18 | IO36NDB2V0 | H10 | VCCIB0 |
| E5 | GAA2/IO134PDB7V1 | F19 | IO42PDB2V0 | H11 | IO13NDB0V2 |
| E6 | GNDQ | F20 | NC | H12 | IO21NDB1V0 |
| E7 | GAB1/IO01PDB0V0 | F21 | NC | H13 | VCCIB1 |
| E8 | IO05NDB0V0 | F22 | NC | H14 | VCCIB1 |
| E9 | IO10NDB0V1 | G1 | IO127NDB7V1 | H15 | VMV1 |
| E10 | IO12NDB0V2 | G2 | IO127PDB7V1 | H16 | GBC2/IO38PDB2V0 |
| E11 | IO16PDB0V2 | G3 | NC | H17 | IO37NDB2V0 |
| E12 | IO20NDB1V0 | G4 | IO128PDB7V1 | H18 | IO41NDB2V0 |

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|------------|------------------|
| Pin Number | A3PE600 Function |
| H19 | IO41PDB2V0 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | IO123NDB7V0 |
| J2 | IO123PDB7V0 |
| J3 | NC |
| J4 | IO124PDB7V0 |
| J5 | IO125PDB7V0 |
| J6 | IO126PDB7V0 |
| J7 | IO130NDB7V1 |
| J8 | VCCIB7 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB2 |
| J16 | IO38NDB2V0 |
| J17 | IO40NDB2V0 |
| J18 | IO40PDB2V0 |
| J19 | IO45PPB2V1 |
| J20 | NC |
| J21 | IO48PDB2V1 |
| J22 | IO46PDB2V1 |
| K1 | IO121NDB7V0 |
| K2 | IO121PDB7V0 |
| K3 | NC |
| K4 | IO124NDB7V0 |
| K5 | IO125NDB7V0 |
| K6 | IO126NDB7V0 |
| K7 | GFC1/IO120PPB7V0 |
| K8 | VCCIB7 |
| K9 | VCC |
| K10 | GND |

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| Pin Number | A3PE600 Function |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB2 |
| K16 | GCC1/IO50PPB2V1 |
| K17 | IO44NDB2V1 |
| K18 | IO44PDB2V1 |
| K19 | IO49NPB2V1 |
| K20 | IO45NPB2V1 |
| K21 | IO48NDB2V1 |
| K22 | IO46NDB2V1 |
| L1 | NC |
| L2 | IO122PDB7V0 |
| L3 | IO122NDB7V0 |
| L4 | GFB0/IO119NPB7V0 |
| L5 | GFA0/IO118NDB6V1 |
| L6 | GFB1/IO119PPB7V0 |
| L7 | VCOMPLF |
| L8 | GFC0/IO120NPB7V0 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO50NPB2V1 |
| L16 | GCB1/IO51PPB2V1 |
| L17 | GCA0/IO52NPB3V0 |
| L18 | VCOMPLC |
| L19 | GCB0/IO51NPB2V1 |
| L20 | IO49PPB2V1 |
| L21 | IO47NDB2V1 |
| L22 | IO47PDB2V1 |
| M1 | NC |
| M2 | IO114NPB6V1 |

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| Pin Number | A3PE600 Function |
| M3 | IO117NDB6V1 |
| M4 | GFA2/IO117PDB6V1 |
| M5 | GFA1/IO118PDB6V1 |
| M6 | VCCPLF |
| M7 | IO116NDB6V1 |
| M8 | GFB2/IO116PDB6V1 |
| M9 | VCC |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO54PPB3V0 |
| M16 | GCA1/IO52PPB3V0 |
| M17 | GCC2/IO55PPB3V0 |
| M18 | VCCPLC |
| M19 | GCA2/IO53PDB3V0 |
| M20 | IO53NDB3V0 |
| M21 | IO56PDB3V0 |
| M22 | NC |
| N1 | IO114PPB6V1 |
| N2 | IO111NDB6V1 |
| N3 | NC |
| N4 | GFC2/IO115PPB6V1 |
| N5 | IO113PPB6V1 |
| N6 | IO112PDB6V1 |
| N7 | IO112NDB6V1 |
| N8 | VCCIB6 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB3 |
| N16 | IO54NPB3V0 |

Package Pin Assignments

| FG484 | | FG484 | | FG484 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | A3PE600 Function | Pin Number | A3PE600 Function | Pin Number | A3PE600 Function |
| N17 | IO57NPB3V0 | R9 | VCCIB5 | U1 | NC |
| N18 | IO55NPB3V0 | R10 | VCCIB5 | U2 | IO107PDB6V0 |
| N19 | IO57PPB3V0 | R11 | IO84NDB5V0 | U3 | IO107NDB6V0 |
| N20 | NC | R12 | IO84PDB5V0 | U4 | GEB1/IO103PDB6V0 |
| N21 | IO56NDB3V0 | R13 | VCCIB4 | U5 | GEB0/IO103NDB6V0 |
| N22 | IO58PDB3V0 | R14 | VCCIB4 | U6 | VMV6 |
| P1 | NC | R15 | VMV3 | U7 | VCCPLE |
| P2 | IO111PDB6V1 | R16 | VCCPLD | U8 | IO101NPB5V2 |
| P3 | IO115NPB6V1 | R17 | GDB1/IO66PPB3V1 | U9 | IO95PPB5V1 |
| P4 | IO113NPB6V1 | R18 | GDC1/IO65PDB3V1 | U10 | IO92PDB5V1 |
| P5 | IO109PPB6V0 | R19 | IO61NDB3V1 | U11 | IO90PDB5V1 |
| P6 | IO108PDB6V0 | R20 | VCC | U12 | IO82PDB5V0 |
| P7 | IO108NDB6V0 | R21 | IO59NDB3V0 | U13 | IO76NDB4V1 |
| P8 | VCCIB6 | R22 | IO62PDB3V1 | U14 | IO76PDB4V1 |
| P9 | GND | T1 | NC | U15 | VMV4 |
| P10 | VCC | T2 | IO110NDB6V0 | U16 | TCK |
| P11 | VCC | T3 | NC | U17 | VPUMP |
| P12 | VCC | T4 | IO105PDB6V0 | U18 | TRST |
| P13 | VCC | T5 | IO105NDB6V0 | U19 | GDA0/IO67NDB3V1 |
| P14 | GND | T6 | GEC1/IO104PPB6V0 | U20 | NC |
| P15 | VCCIB3 | T7 | VCOMPLE | U21 | IO64NDB3V1 |
| P16 | GDB0/IO66NPB3V1 | T8 | GNDQ | U22 | IO63PDB3V1 |
| P17 | IO60NDB3V1 | T9 | GEA2/IO101PPB5V2 | V1 | NC |
| P18 | IO60PDB3V1 | T10 | IO92NDB5V1 | V2 | NC |
| P19 | IO61PDB3V1 | T11 | IO90NDB5V1 | V3 | GND |
| P20 | NC | T12 | IO82NDB5V0 | V4 | GEA1/IO102PDB6V0 |
| P21 | IO59PDB3V0 | T13 | IO74NDB4V1 | V5 | GEA0/IO102NDB6V0 |
| P22 | IO58NDB3V0 | T14 | IO74PDB4V1 | V6 | GNDQ |
| R1 | NC | T15 | GNDQ | V7 | GEC2/IO99PDB5V2 |
| R2 | IO110PDB6V0 | T16 | VCOMPLD | V8 | IO95NPB5V1 |
| R3 | VCC | T17 | VJTAG | V9 | IO91NDB5V1 |
| R4 | IO109NPB6V0 | T18 | GDC0/IO65NDB3V1 | V10 | IO91PDB5V1 |
| R5 | IO106NDB6V0 | T19 | GDA1/IO67PDB3V1 | V11 | IO83NDB5V0 |
| R6 | IO106PDB6V0 | T20 | NC | V12 | IO83PDB5V0 |
| R7 | GEC0/IO104NPB6V0 | T21 | IO64PDB3V1 | V13 | IO77NDB4V1 |
| R8 | VMV5 | T22 | IO62NDB3V1 | V14 | IO77PDB4V1 |

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| Pin Number | A3PE600 Function |
| V15 | IO69NDB4V0 |
| V16 | GDB2/IO69PDB4V0 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | IO63NDB3V1 |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO100NDB5V2 |
| W6 | GEB2/IO100PDB5V2 |
| W7 | IO99NDB5V2 |
| W8 | IO88NDB5V0 |
| W9 | IO88PDB5V0 |
| W10 | IO89NDB5V0 |
| W11 | IO80NDB4V1 |
| W12 | IO81NDB4V1 |
| W13 | IO81PDB4V1 |
| W14 | IO70NDB4V0 |
| W15 | GDC2/IO70PDB4V0 |
| W16 | IO68NDB4V0 |
| W17 | GDA2/IO68PDB4V0 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB6 |
| Y2 | NC |
| Y3 | NC |
| Y4 | IO98NDB5V2 |
| Y5 | GND |
| Y6 | IO94NDB5V1 |

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| Pin Number | A3PE600 Function |
| Y7 | IO94PDB5V1 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO89PDB5V0 |
| Y11 | IO80PDB4V1 |
| Y12 | IO78NPB4V1 |
| Y13 | NC |
| Y14 | VCC |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB3 |

Package Pin Assignments

| FG484 | | FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| A1 | GND | AA15 | NC | B7 | IO10PDB0V1 |
| A2 | GND | AA16 | IO117NDB4V0 | B8 | IO15NDB0V1 |
| A3 | VCCIB0 | AA17 | IO117PDB4V0 | B9 | IO17NDB0V2 |
| A4 | IO05NDB0V0 | AA18 | IO115NDB4V0 | B10 | IO20PDB0V2 |
| A5 | IO05PDB0V0 | AA19 | IO115PDB4V0 | B11 | IO29PDB0V3 |
| A6 | IO11NDB0V1 | AA20 | NC | B12 | IO32NDB1V0 |
| A7 | IO11PDB0V1 | AA21 | VCCIB3 | B13 | IO43NDB1V1 |
| A8 | IO15PDB0V1 | AA22 | GND | B14 | NC |
| A9 | IO17PDB0V2 | AB1 | GND | B15 | NC |
| A10 | IO27NDB0V3 | AB2 | GND | B16 | IO53NDB1V2 |
| A11 | IO27PDB0V3 | AB3 | VCCIB5 | B17 | IO53PDB1V2 |
| A12 | IO32PDB1V0 | AB4 | IO159NDB5V3 | B18 | IO54PDB1V3 |
| A13 | IO43PDB1V1 | AB5 | IO159PDB5V3 | B19 | NC |
| A14 | IO47NDB1V1 | AB6 | IO149NDB5V1 | B20 | NC |
| A15 | IO47PDB1V1 | AB7 | IO149PDB5V1 | B21 | VCCIB2 |
| A16 | IO51NDB1V2 | AB8 | IO138NDB5V0 | B22 | GND |
| A17 | IO51PDB1V2 | AB9 | IO138PDB5V0 | C1 | VCCIB7 |
| A18 | IO54NDB1V3 | AB10 | NC | C2 | NC |
| A19 | NC | AB11 | NC | C3 | NC |
| A20 | VCCIB1 | AB12 | IO127NDB4V2 | C4 | NC |
| A21 | GND | AB13 | IO127PDB4V2 | C5 | GND |
| A22 | GND | AB14 | IO125NDB4V1 | C6 | IO07NDB0V0 |
| AA1 | GND | AB15 | IO125PDB4V1 | C7 | IO07PDB0V0 |
| AA2 | VCCIB6 | AB16 | IO122NDB4V1 | C8 | VCC |
| AA3 | NC | AB17 | IO122PDB4V1 | C9 | VCC |
| AA4 | IO161PDB5V3 | AB18 | NC | C10 | IO20NDB0V2 |
| AA5 | IO155NDB5V2 | AB19 | NC | C11 | IO29NDB0V3 |
| AA6 | IO155PDB5V2 | AB20 | VCCIB4 | C12 | NC |
| AA7 | IO154NDB5V2 | AB21 | GND | C13 | NC |
| AA8 | IO154PDB5V2 | AB22 | GND | C14 | VCC |
| AA9 | IO143PDB5V1 | B1 | GND | C15 | VCC |
| AA10 | IO143NDB5V1 | B2 | VCCIB7 | C16 | NC |
| AA11 | IO131PPB4V2 | B3 | NC | C17 | NC |
| AA12 | IO129NDB4V2 | B4 | IO03NDB0V0 | C18 | GND |
| AA13 | IO129PDB4V2 | B5 | IO03PDB0V0 | C19 | NC |
| AA14 | NC | B6 | IO10NDB0V1 | C20 | NC |

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| Pin Number | A3PE1500 Function |
| C21 | NC |
| C22 | VCCIB2 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00NDB0V0 |
| D6 | GAA1/IO00PDB0V0 |
| D7 | GAB0/IO01NDB0V0 |
| D8 | IO09PDB0V1 |
| D9 | IO13PDB0V1 |
| D10 | IO21PDB0V2 |
| D11 | IO31NDB0V3 |
| D12 | IO37NDB1V0 |
| D13 | IO37PDB1V0 |
| D14 | IO49NDB1V2 |
| D15 | IO49PDB1V2 |
| D16 | GBB1/IO56PDB1V3 |
| D17 | GBA0/IO57NDB1V3 |
| D18 | GBA1/IO57PDB1V3 |
| D19 | GND |
| D20 | NC |
| D21 | IO69PDB2V1 |
| D22 | NC |
| E1 | NC |
| E2 | IO218PPB7V3 |
| E3 | GND |
| E4 | GAB2/IO220PDB7V3 |
| E5 | GAA2/IO221PDB7V3 |
| E6 | GNDQ |
| E7 | GAB1/IO01PDB0V0 |
| E8 | IO09NDB0V1 |
| E9 | IO13NDB0V1 |
| E10 | IO21NDB0V2 |
| E11 | IO31PDB0V3 |
| E12 | IO35NDB1V0 |

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| Pin Number | A3PE1500 Function |
| E13 | IO41NDB1V1 |
| E14 | IO41PDB1V1 |
| E15 | GBC1/IO55PDB1V3 |
| E16 | GBB0/IO56NDB1V3 |
| E17 | GNDQ |
| E18 | GBA2/IO58PDB2V0 |
| E19 | IO63NDB2V0 |
| E20 | GND |
| E21 | IO69NDB2V1 |
| E22 | NC |
| F1 | IO218NPB7V3 |
| F2 | IO216NDB7V3 |
| F3 | IO216PDB7V3 |
| F4 | IO220NDB7V3 |
| F5 | IO221NDB7V3 |
| F6 | VMV7 |
| F7 | VCCPLA |
| F8 | GAC0/IO02NDB0V0 |
| F9 | GAC1/IO02PDB0V0 |
| F10 | IO23NDB0V2 |
| F11 | IO23PDB0V2 |
| F12 | IO35PDB1V0 |
| F13 | IO39NDB1V0 |
| F14 | IO45PDB1V1 |
| F15 | GBC0/IO55NDB1V3 |
| F16 | VCCPLB |
| F17 | VMV2 |
| F18 | IO58NDB2V0 |
| F19 | IO63PDB2V0 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | IO211NDB7V2 |
| G2 | IO211PDB7V2 |
| G3 | NC |
| G4 | IO214PDB7V3 |

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| Pin Number | A3PE1500 Function |
| G5 | IO217PDB7V3 |
| G6 | GAC2/IO219PDB7V3 |
| G7 | VCOMPLA |
| G8 | GNDQ |
| G9 | IO19NDB0V2 |
| G10 | IO19PDB0V2 |
| G11 | IO25PDB0V3 |
| G12 | IO33PDB1V0 |
| G13 | IO39PDB1V0 |
| G14 | IO45NDB1V1 |
| G15 | GNDQ |
| G16 | VCOMPLB |
| G17 | GBB2/IO59PDB2V0 |
| G18 | IO62PDB2V0 |
| G19 | IO62NDB2V0 |
| G20 | IO71PDB2V2 |
| G21 | IO71NDB2V2 |
| G22 | NC |
| H1 | IO209PSB7V2 |
| H2 | NC |
| H3 | VCC |
| H4 | IO214NDB7V3 |
| H5 | IO217NDB7V3 |
| H6 | IO219NDB7V3 |
| H7 | IO215PDB7V3 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO25NDB0V3 |
| H12 | IO33NDB1V0 |
| H13 | VCCIB1 |
| H14 | VCCIB1 |
| H15 | VMV1 |
| H16 | GBC2/IO60PDB2V0 |
| H17 | IO59NDB2V0 |
| H18 | IO67NDB2V1 |

Package Pin Assignments

| FG484 | | FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| H19 | IO67PDB2V1 | K11 | GND | M3 | IO189NDB6V2 |
| H20 | VCC | K12 | GND | M4 | GFA2/IO189PDB6V2 |
| H21 | VMV2 | K13 | GND | M5 | GFA1/IO190PDB6V2 |
| H22 | IO74PSB2V2 | K14 | VCC | M6 | VCCPLF |
| J1 | IO212NDB7V2 | K15 | VCCIB2 | M7 | IO188NDB6V2 |
| J2 | IO212PDB7V2 | K16 | GCC1/IO85PPB2V3 | M8 | GFB2/IO188PDB6V2 |
| J3 | VMV7 | K17 | IO73NDB2V2 | M9 | VCC |
| J4 | IO206PDB7V1 | K18 | IO73PDB2V2 | M10 | GND |
| J5 | IO204PDB7V1 | K19 | IO81NPB2V3 | M11 | GND |
| J6 | IO210PDB7V2 | K20 | IO75NPB2V2 | M12 | GND |
| J7 | IO215NDB7V3 | K21 | IO77NDB2V2 | M13 | GND |
| J8 | VCCIB7 | K22 | IO79NDB2V3 | M14 | VCC |
| J9 | GND | L1 | NC | M15 | GCB2/IO89PPB3V0 |
| J10 | VCC | L2 | IO196PDB7V0 | M16 | GCA1/IO87PPB3V0 |
| J11 | VCC | L3 | IO196NDB7V0 | M17 | GCC2/IO90PPB3V0 |
| J12 | VCC | L4 | GFB0/IO191NPB7V0 | M18 | VCCPLC |
| J13 | VCC | L5 | GFA0/IO190NDB6V2 | M19 | GCA2/IO88PDB3V0 |
| J14 | GND | L6 | GFB1/IO191PPB7V0 | M20 | IO88NDB3V0 |
| J15 | VCCIB2 | L7 | VCOMPLF | M21 | IO93PDB3V0 |
| J16 | IO60NDB2V0 | L8 | GFC0/IO192NPB7V0 | M22 | NC |
| J17 | IO65NDB2V1 | L9 | VCC | N1 | IO185PPB6V2 |
| J18 | IO65PDB2V1 | L10 | GND | N2 | IO183NDB6V2 |
| J19 | IO75PPB2V2 | L11 | GND | N3 | VMV6 |
| J20 | GNDQ | L12 | GND | N4 | GFC2/IO187PPB6V2 |
| J21 | IO77PDB2V2 | L13 | GND | N5 | IO184PPB6V2 |
| J22 | IO79PDB2V3 | L14 | VCC | N6 | IO186PDB6V2 |
| K1 | IO200NDB7V1 | L15 | GCC0/IO85NPB2V3 | N7 | IO186NDB6V2 |
| K2 | IO200PDB7V1 | L16 | GCB1/IO86PPB2V3 | N8 | VCCIB6 |
| K3 | GNDQ | L17 | GCA0/IO87NPB3V0 | N9 | VCC |
| K4 | IO206NDB7V1 | L18 | VCOMPLC | N10 | GND |
| K5 | IO204NDB7V1 | L19 | GCB0/IO86NPB2V3 | N11 | GND |
| K6 | IO210NDB7V2 | L20 | IO81PPB2V3 | N12 | GND |
| K7 | GFC1/IO192PPB7V0 | L21 | IO83NDB2V3 | N13 | GND |
| K8 | VCCIB7 | L22 | IO83PDB2V3 | N14 | VCC |
| K9 | VCC | M1 | GNDQ | N15 | VCCIB3 |
| K10 | GND | M2 | IO185NPB6V2 | N16 | IO89NPB3V0 |

| FG484 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| N17 | IO91NPB3V0 |
| N18 | IO90NPB3V0 |
| N19 | IO91PPB3V0 |
| N20 | GNDQ |
| N21 | IO93NDB3V0 |
| N22 | IO95PDB3V1 |
| P1 | NC |
| P2 | IO183PDB6V2 |
| P3 | IO187NPB6V2 |
| P4 | IO184NPB6V2 |
| P5 | IO176PPB6V1 |
| P6 | IO182PDB6V1 |
| P7 | IO182NDB6V1 |
| P8 | VCCIB6 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB3 |
| P16 | GDB0/IO109NPB3V2 |
| P17 | IO97NDB3V1 |
| P18 | IO97PDB3V1 |
| P19 | IO99PDB3V1 |
| P20 | VMV3 |
| P21 | IO98PDB3V1 |
| P22 | IO95NDB3V1 |
| R1 | NC |
| R2 | IO177PDB6V1 |
| R3 | VCC |
| R4 | IO176NPB6V1 |
| R5 | IO174NDB6V0 |
| R6 | IO174PDB6V0 |
| R7 | GEC0/IO169NPB6V0 |
| R8 | VMV5 |

| FG484 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| R9 | VCCIB5 |
| R10 | VCCIB5 |
| R11 | IO135NDB5V0 |
| R12 | IO135PDB5V0 |
| R13 | VCCIB4 |
| R14 | VCCIB4 |
| R15 | VMV3 |
| R16 | VCCPLD |
| R17 | GDB1/IO109PPB3V2 |
| R18 | GDC1/IO108PDB3V2 |
| R19 | IO99NDB3V1 |
| R20 | VCC |
| R21 | IO98NDB3V1 |
| R22 | IO101PDB3V1 |
| T1 | NC |
| T2 | IO177NDB6V1 |
| T3 | NC |
| T4 | IO171PDB6V0 |
| T5 | IO171NDB6V0 |
| T6 | GEC1/IO169PPB6V0 |
| T7 | VCOMPLE |
| T8 | GNDQ |
| T9 | GEA2/IO166PPB5V3 |
| T10 | IO145NDB5V1 |
| T11 | IO141NDB5V0 |
| T12 | IO139NDB5V0 |
| T13 | IO119NDB4V1 |
| T14 | IO119PDB4V1 |
| T15 | GNDQ |
| T16 | VCOMPLD |
| T17 | VJTAG |
| T18 | GDC0/IO108NDB3V2 |
| T19 | GDA1/IO110PDB3V2 |
| T20 | NC |
| T21 | IO103PDB3V2 |
| T22 | IO101NDB3V1 |

| FG484 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| U1 | IO175PPB6V1 |
| U2 | IO173PDB6V0 |
| U3 | IO173NDB6V0 |
| U4 | GEB1/IO168PDB6V0 |
| U5 | GEB0/IO168NDB6V0 |
| U6 | VMV6 |
| U7 | VCCPLE |
| U8 | IO166NPB5V3 |
| U9 | IO157PPB5V2 |
| U10 | IO145PDB5V1 |
| U11 | IO141PDB5V0 |
| U12 | IO139PDB5V0 |
| U13 | IO121NDB4V1 |
| U14 | IO121PDB4V1 |
| U15 | VMV4 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO110NDB3V2 |
| U20 | NC |
| U21 | IO103NDB3V2 |
| U22 | IO105PDB3V2 |
| V1 | NC |
| V2 | IO175NPB6V1 |
| V3 | GND |
| V4 | GEA1/IO167PDB6V0 |
| V5 | GEA0/IO167NDB6V0 |
| V6 | GNDQ |
| V7 | GEC2/IO164PDB5V3 |
| V8 | IO157NPB5V2 |
| V9 | IO151NDB5V2 |
| V10 | IO151PDB5V2 |
| V11 | IO137NDB5V0 |
| V12 | IO137PDB5V0 |
| V13 | IO123NDB4V1 |
| V14 | IO123PDB4V1 |

Package Pin Assignments

| FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| V15 | IO112NDB4V0 | Y7 | IO163PDB5V3 |
| V16 | GDB2/IO112PDB4V0 | Y8 | VCC |
| V17 | TDI | Y9 | VCC |
| V18 | GNDQ | Y10 | IO147PDB5V1 |
| V19 | TDO | Y11 | IO133PDB4V2 |
| V20 | GND | Y12 | IO131NPB4V2 |
| V21 | NC | Y13 | NC |
| V22 | IO105NDB3V2 | Y14 | VCC |
| W1 | NC | Y15 | VCC |
| W2 | NC | Y16 | NC |
| W3 | NC | Y17 | NC |
| W4 | GND | Y18 | GND |
| W5 | IO165NDB5V3 | Y19 | NC |
| W6 | GEB2/IO165PDB5V3 | Y20 | NC |
| W7 | IO164NDB5V3 | Y21 | NC |
| W8 | IO153NDB5V2 | Y22 | VCCIB3 |
| W9 | IO153PDB5V2 | | |
| W10 | IO147NDB5V1 | | |
| W11 | IO133NDB4V2 | | |
| W12 | IO130NDB4V2 | | |
| W13 | IO130PDB4V2 | | |
| W14 | IO113NDB4V0 | | |
| W15 | GDC2/IO113PDB4V0 | | |
| W16 | IO111NDB4V0 | | |
| W17 | GDA2/IO111PDB4V0 | | |
| W18 | TMS | | |
| W19 | GND | | |
| W20 | NC | | |
| W21 | NC | | |
| W22 | NC | | |
| Y1 | VCCIB6 | | |
| Y2 | NC | | |
| Y3 | NC | | |
| Y4 | IO161NDB5V3 | | |
| Y5 | GND | | |
| Y6 | IO163NDB5V3 | | |

| FG484 | | FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| A1 | GND | AA15 | IO170PDB4V2 | B7 | IO14PDB0V1 |
| A2 | GND | AA16 | IO166NDB4V1 | B8 | IO18NDB0V2 |
| A3 | VCCIB0 | AA17 | IO166PDB4V1 | B9 | IO24NDB0V2 |
| A4 | IO10NDB0V1 | AA18 | IO160NDB4V0 | B10 | IO34PDB0V4 |
| A5 | IO10PDB0V1 | AA19 | IO160PDB4V0 | B11 | IO40PDB0V4 |
| A6 | IO16NDB0V1 | AA20 | IO158NPB4V0 | B12 | IO46NDB1V0 |
| A7 | IO16PDB0V1 | AA21 | VCCIB3 | B13 | IO54NDB1V1 |
| A8 | IO18PDB0V2 | AA22 | GND | B14 | IO62NDB1V2 |
| A9 | IO24PDB0V2 | AB1 | GND | B15 | IO62PDB1V2 |
| A10 | IO28NDB0V3 | AB2 | GND | B16 | IO68NDB1V3 |
| A11 | IO28PDB0V3 | AB3 | VCCIB5 | B17 | IO68PDB1V3 |
| A12 | IO46PDB1V0 | AB4 | IO216NDB5V2 | B18 | IO72PDB1V3 |
| A13 | IO54PDB1V1 | AB5 | IO216PDB5V2 | B19 | IO74PDB1V4 |
| A14 | IO56NDB1V1 | AB6 | IO210NDB5V2 | B20 | IO76NPB1V4 |
| A15 | IO56PDB1V1 | AB7 | IO210PDB5V2 | B21 | VCCIB2 |
| A16 | IO64NDB1V2 | AB8 | IO208NDB5V1 | B22 | GND |
| A17 | IO64PDB1V2 | AB9 | IO208PDB5V1 | C1 | VCCIB7 |
| A18 | IO72NDB1V3 | AB10 | IO197NDB5V0 | C2 | IO303PDB7V3 |
| A19 | IO74NDB1V4 | AB11 | IO197PDB5V0 | C3 | IO305PDB7V3 |
| A20 | VCCIB1 | AB12 | IO174NDB4V2 | C4 | IO06NPB0V0 |
| A21 | GND | AB13 | IO174PDB4V2 | C5 | GND |
| A22 | GND | AB14 | IO172NDB4V2 | C6 | IO12NDB0V1 |
| AA1 | GND | AB15 | IO172PDB4V2 | C7 | IO12PDB0V1 |
| AA2 | VCCIB6 | AB16 | IO168NDB4V1 | C8 | VCC |
| AA3 | IO228PDB5V4 | AB17 | IO168PDB4V1 | C9 | VCC |
| AA4 | IO224PDB5V3 | AB18 | IO162NDB4V1 | C10 | IO34NDB0V4 |
| AA5 | IO218NDB5V3 | AB19 | IO162PDB4V1 | C11 | IO40NDB0V4 |
| AA6 | IO218PDB5V3 | AB20 | VCCIB4 | C12 | IO48NDB1V0 |
| AA7 | IO212NDB5V2 | AB21 | GND | C13 | IO48PDB1V0 |
| AA8 | IO212PDB5V2 | AB22 | GND | C14 | VCC |
| AA9 | IO198PDB5V0 | B1 | GND | C15 | VCC |
| AA10 | IO198NDB5V0 | B2 | VCCIB7 | C16 | IO70NDB1V3 |
| AA11 | IO188PPB4V4 | B3 | IO06PPB0V0 | C17 | IO70PDB1V3 |
| AA12 | IO180NDB4V3 | B4 | IO08NDB0V0 | C18 | GND |
| AA13 | IO180PDB4V3 | B5 | IO08PDB0V0 | C19 | IO76PPB1V4 |
| AA14 | IO170NDB4V2 | B6 | IO14NDB0V1 | C20 | IO88NDB2V0 |

Package Pin Assignments

| FG484 | | FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| C21 | IO94PPB2V1 | E13 | IO58NDB1V2 | G5 | IO297PDB7V2 |
| C22 | VCCIB2 | E14 | IO58PDB1V2 | G6 | GAC2/IO307PDB7V4 |
| D1 | IO293PDB7V2 | E15 | GBC1/IO79PDB1V4 | G7 | VCOMPLA |
| D2 | IO303NDB7V3 | E16 | GBB0/IO80NDB1V4 | G8 | GNDQ |
| D3 | IO305NDB7V3 | E17 | GNDQ | G9 | IO26NDB0V3 |
| D4 | GND | E18 | GBA2/IO82PDB2V0 | G10 | IO26PDB0V3 |
| D5 | GAA0/IO00NDB0V0 | E19 | IO86NDB2V0 | G11 | IO36PDB0V4 |
| D6 | GAA1/IO00PDB0V0 | E20 | GND | G12 | IO42PDB1V0 |
| D7 | GAB0/IO01NDB0V0 | E21 | IO90NDB2V1 | G13 | IO50PDB1V1 |
| D8 | IO20PDB0V2 | E22 | IO98PDB2V2 | G14 | IO60NDB1V2 |
| D9 | IO22PDB0V2 | F1 | IO299NPB7V3 | G15 | GNDQ |
| D10 | IO30PDB0V3 | F2 | IO301NDB7V3 | G16 | VCOMPLB |
| D11 | IO38NDB0V4 | F3 | IO301PDB7V3 | G17 | GBB2/IO83PDB2V0 |
| D12 | IO52NDB1V1 | F4 | IO308NDB7V4 | G18 | IO92PDB2V1 |
| D13 | IO52PDB1V1 | F5 | IO309NDB7V4 | G19 | IO92NDB2V1 |
| D14 | IO66NDB1V3 | F6 | VMV7 | G20 | IO102PDB2V2 |
| D15 | IO66PDB1V3 | F7 | VCCPLA | G21 | IO102NDB2V2 |
| D16 | GBB1/IO80PDB1V4 | F8 | GAC0/IO02NDB0V0 | G22 | IO105NDB2V2 |
| D17 | GBA0/IO81NDB1V4 | F9 | GAC1/IO02PDB0V0 | H1 | IO286PSB7V1 |
| D18 | GBA1/IO81PDB1V4 | F10 | IO32NDB0V3 | H2 | IO291NPB7V2 |
| D19 | GND | F11 | IO32PDB0V3 | H3 | VCC |
| D20 | IO88PDB2V0 | F12 | IO44PDB1V0 | H4 | IO295NDB7V2 |
| D21 | IO90PDB2V1 | F13 | IO50NDB1V1 | H5 | IO297NDB7V2 |
| D22 | IO94NPB2V1 | F14 | IO60PDB1V2 | H6 | IO307NDB7V4 |
| E1 | IO293NDB7V2 | F15 | GBC0/IO79NDB1V4 | H7 | IO287PDB7V1 |
| E2 | IO299PPB7V3 | F16 | VCCPLB | H8 | VMV0 |
| E3 | GND | F17 | VMV2 | H9 | VCCIB0 |
| E4 | GAB2/IO308PDB7V4 | F18 | IO82NDB2V0 | H10 | VCCIB0 |
| E5 | GAA2/IO309PDB7V4 | F19 | IO86PDB2V0 | H11 | IO36NDB0V4 |
| E6 | GNDQ | F20 | IO96PDB2V1 | H12 | IO42NDB1V0 |
| E7 | GAB1/IO01PDB0V0 | F21 | IO96NDB2V1 | H13 | VCCIB1 |
| E8 | IO20NDB0V2 | F22 | IO98NDB2V2 | H14 | VCCIB1 |
| E9 | IO22NDB0V2 | G1 | IO289NDB7V1 | H15 | VMV1 |
| E10 | IO30NDB0V3 | G2 | IO289PDB7V1 | H16 | GBC2/IO84PDB2V0 |
| E11 | IO38PDB0V4 | G3 | IO291PPB7V2 | H17 | IO83NDB2V0 |
| E12 | IO44NDB1V0 | G4 | IO295PDB7V2 | H18 | IO100NDB2V2 |

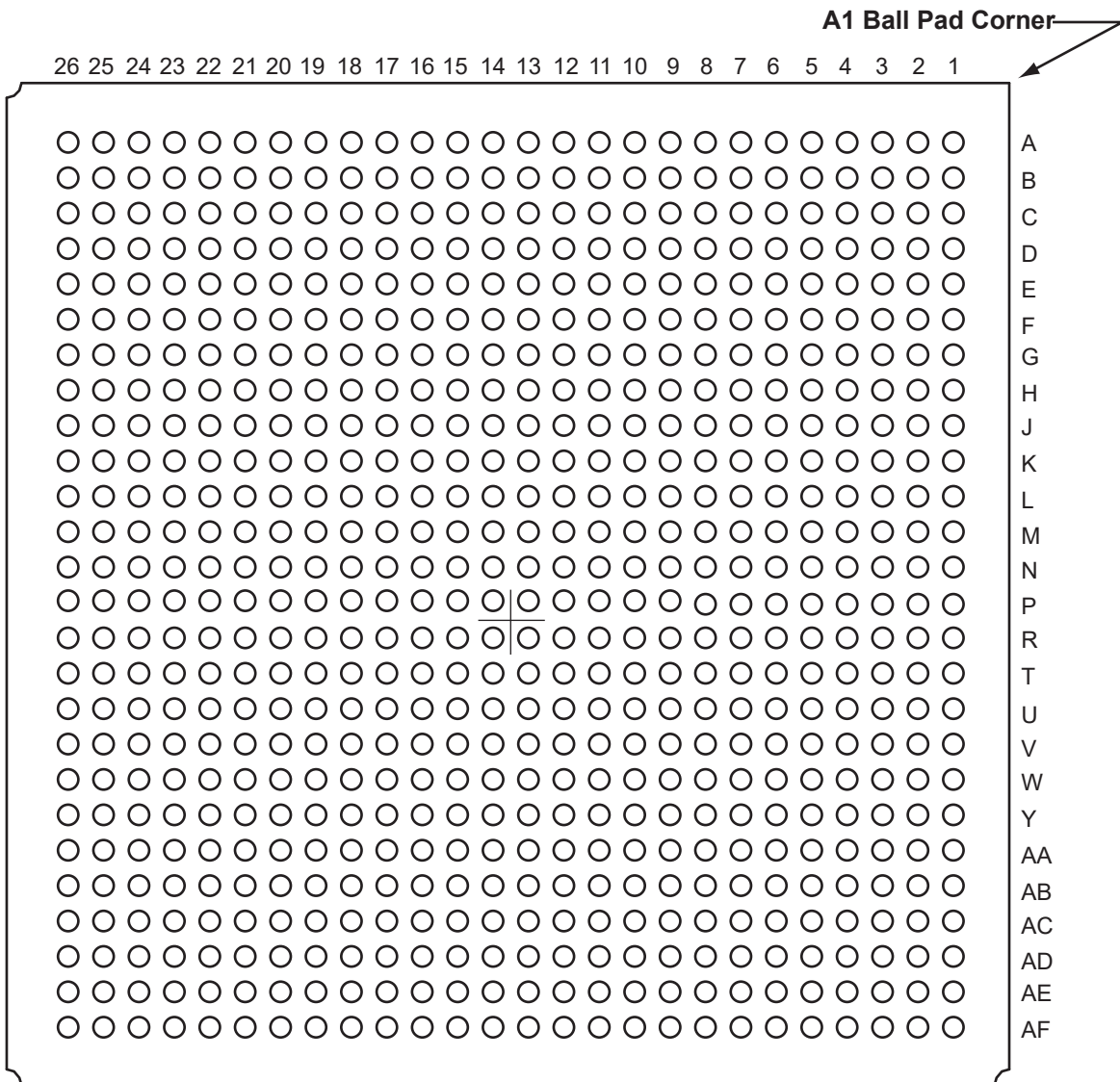
| FG484 | | FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| H19 | IO100PDB2V2 | K11 | GND | M3 | IO272NDB6V4 |
| H20 | VCC | K12 | GND | M4 | GFA2/IO272PDB6V4 |
| H21 | VMV2 | K13 | GND | M5 | GFA1/IO273PDB6V4 |
| H22 | IO105PDB2V2 | K14 | VCC | M6 | VCCPLF |
| J1 | IO285NDB7V1 | K15 | VCCIB2 | M7 | IO271NDB6V4 |
| J2 | IO285PDB7V1 | K16 | GCC1/IO112PPB2V3 | M8 | GFB2/IO271PDB6V4 |
| J3 | VMV7 | K17 | IO108NDB2V3 | M9 | VCC |
| J4 | IO279PDB7V0 | K18 | IO108PDB2V3 | M10 | GND |
| J5 | IO283PDB7V1 | K19 | IO110NPB2V3 | M11 | GND |
| J6 | IO281PDB7V0 | K20 | IO106NPB2V3 | M12 | GND |
| J7 | IO287NDB7V1 | K21 | IO109NDB2V3 | M13 | GND |
| J8 | VCCIB7 | K22 | IO107NDB2V3 | M14 | VCC |
| J9 | GND | L1 | IO257PSB6V2 | M15 | GCB2/IO116PPB3V0 |
| J10 | VCC | L2 | IO276PDB7V0 | M16 | GCA1/IO114PPB3V0 |
| J11 | VCC | L3 | IO276NDB7V0 | M17 | GCC2/IO117PPB3V0 |
| J12 | VCC | L4 | GFB0/IO274NPB7V0 | M18 | VCCPLC |
| J13 | VCC | L5 | GFA0/IO273NDB6V4 | M19 | GCA2/IO115PDB3V0 |
| J14 | GND | L6 | GFB1/IO274PPB7V0 | M20 | IO115NDB3V0 |
| J15 | VCCIB2 | L7 | VCOMPLF | M21 | IO126PDB3V1 |
| J16 | IO84NDB2V0 | L8 | GFC0/IO275NPB7V0 | M22 | IO124PSB3V1 |
| J17 | IO104NDB2V2 | L9 | VCC | N1 | IO255PPB6V2 |
| J18 | IO104PDB2V2 | L10 | GND | N2 | IO253NDB6V2 |
| J19 | IO106PPB2V3 | L11 | GND | N3 | VMV6 |
| J20 | GNDQ | L12 | GND | N4 | GFC2/IO270PPB6V4 |
| J21 | IO109PDB2V3 | L13 | GND | N5 | IO261PPB6V3 |
| J22 | IO107PDB2V3 | L14 | VCC | N6 | IO263PDB6V3 |
| K1 | IO277NDB7V0 | L15 | GCC0/IO112NPB2V3 | N7 | IO263NDB6V3 |
| K2 | IO277PDB7V0 | L16 | GCB1/IO113PPB2V3 | N8 | VCCIB6 |
| K3 | GNDQ | L17 | GCA0/IO114NPB3V0 | N9 | VCC |
| K4 | IO279NDB7V0 | L18 | VCOMPLC | N10 | GND |
| K5 | IO283NDB7V1 | L19 | GCB0/IO113NPB2V3 | N11 | GND |
| K6 | IO281NDB7V0 | L20 | IO110PPB2V3 | N12 | GND |
| K7 | GFC1/IO275PPB7V0 | L21 | IO111NDB2V3 | N13 | GND |
| K8 | VCCIB7 | L22 | IO111PDB2V3 | N14 | VCC |
| K9 | VCC | M1 | GNDQ | N15 | VCCIB3 |
| K10 | GND | M2 | IO255NPB6V2 | N16 | IO116NPB3V0 |

Package Pin Assignments

| FG484 | | FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| N17 | IO132NPB3V2 | R9 | VCCIB5 | U1 | IO240PPB6V0 |
| N18 | IO117NPB3V0 | R10 | VCCIB5 | U2 | IO238PDB6V0 |
| N19 | IO132PPB3V2 | R11 | IO196NDB5V0 | U3 | IO238NDB6V0 |
| N20 | GNDQ | R12 | IO196PDB5V0 | U4 | GEB1/IO235PDB6V0 |
| N21 | IO126NDB3V1 | R13 | VCCIB4 | U5 | GEB0/IO235NDB6V0 |
| N22 | IO128PDB3V1 | R14 | VCCIB4 | U6 | VMV6 |
| P1 | IO247PDB6V1 | R15 | VMV3 | U7 | VCCPLE |
| P2 | IO253PDB6V2 | R16 | VCCPLD | U8 | IO233NPB5V4 |
| P3 | IO270NPB6V4 | R17 | GDB1/IO152PPB3V4 | U9 | IO222PPB5V3 |
| P4 | IO261NPB6V3 | R18 | GDC1/IO151PDB3V4 | U10 | IO206PDB5V1 |
| P5 | IO249PPB6V1 | R19 | IO138NDB3V3 | U11 | IO202PDB5V1 |
| P6 | IO259PDB6V3 | R20 | VCC | U12 | IO194PDB5V0 |
| P7 | IO259NDB6V3 | R21 | IO130NDB3V2 | U13 | IO176NDB4V2 |
| P8 | VCCIB6 | R22 | IO134PDB3V2 | U14 | IO176PDB4V2 |
| P9 | GND | T1 | IO243PPB6V1 | U15 | VMV4 |
| P10 | VCC | T2 | IO245NDB6V1 | U16 | TCK |
| P11 | VCC | T3 | IO243NPB6V1 | U17 | VPUMP |
| P12 | VCC | T4 | IO241PDB6V0 | U18 | TRST |
| P13 | VCC | T5 | IO241NDB6V0 | U19 | GDA0/IO153NDB3V4 |
| P14 | GND | T6 | GEC1/IO236PPB6V0 | U20 | IO144NDB3V3 |
| P15 | VCCIB3 | T7 | VCOMPLE | U21 | IO140NDB3V3 |
| P16 | GDB0/IO152NPB3V4 | T8 | GNDQ | U22 | IO142PDB3V3 |
| P17 | IO136NDB3V2 | T9 | GEA2/IO233PPB5V4 | V1 | IO239PDB6V0 |
| P18 | IO136PDB3V2 | T10 | IO206NDB5V1 | V2 | IO240NPB6V0 |
| P19 | IO138PDB3V3 | T11 | IO202NDB5V1 | V3 | GND |
| P20 | VMV3 | T12 | IO194NDB5V0 | V4 | GEA1/IO234PDB6V0 |
| P21 | IO130PDB3V2 | T13 | IO186NDB4V4 | V5 | GEA0/IO234NDB6V0 |
| P22 | IO128NDB3V1 | T14 | IO186PDB4V4 | V6 | GNDQ |
| R1 | IO247NDB6V1 | T15 | GNDQ | V7 | GEC2/IO231PDB5V4 |
| R2 | IO245PDB6V1 | T16 | VCOMPLD | V8 | IO222NPB5V3 |
| R3 | VCC | T17 | VJTAG | V9 | IO204NDB5V1 |
| R4 | IO249NPB6V1 | T18 | GDC0/IO151NDB3V4 | V10 | IO204PDB5V1 |
| R5 | IO251NDB6V2 | T19 | GDA1/IO153PDB3V4 | V11 | IO195NDB5V0 |
| R6 | IO251PDB6V2 | T20 | IO144PDB3V3 | V12 | IO195PDB5V0 |
| R7 | GEC0/IO236NPB6V0 | T21 | IO140PDB3V3 | V13 | IO178NDB4V3 |
| R8 | VMV5 | T22 | IO134NDB3V2 | V14 | IO178PDB4V3 |

| FG484 | | FG484 | |
|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| V15 | IO155NDB4V0 | Y7 | IO220PDB5V3 |
| V16 | GDB2/IO155PDB4V0 | Y8 | VCC |
| V17 | TDI | Y9 | VCC |
| V18 | GNDQ | Y10 | IO200PDB5V0 |
| V19 | TDO | Y11 | IO192PDB4V4 |
| V20 | GND | Y12 | IO188NPB4V4 |
| V21 | IO146PDB3V4 | Y13 | IO187PSB4V4 |
| V22 | IO142NDB3V3 | Y14 | VCC |
| W1 | IO239NDB6V0 | Y15 | VCC |
| W2 | IO237PDB6V0 | Y16 | IO164NDB4V1 |
| W3 | IO230PSB5V4 | Y17 | IO164PDB4V1 |
| W4 | GND | Y18 | GND |
| W5 | IO232NDB5V4 | Y19 | IO158PPB4V0 |
| W6 | GEB2/IO232PDB5V4 | Y20 | IO150PDB3V4 |
| W7 | IO231NDB5V4 | Y21 | IO148NPB3V4 |
| W8 | IO214NDB5V2 | Y22 | VCCIB3 |
| W9 | IO214PDB5V2 | | |
| W10 | IO200NDB5V0 | | |
| W11 | IO192NDB4V4 | | |
| W12 | IO184NDB4V3 | | |
| W13 | IO184PDB4V3 | | |
| W14 | IO156NDB4V0 | | |
| W15 | GDC2/IO156PDB4V0 | | |
| W16 | IO154NDB4V0 | | |
| W17 | GDA2/IO154PDB4V0 | | |
| W18 | TMS | | |
| W19 | GND | | |
| W20 | IO150NDB3V4 | | |
| W21 | IO146NDB3V4 | | |
| W22 | IO148PPB3V4 | | |
| Y1 | VCCIB6 | | |
| Y2 | IO237NDB6V0 | | |
| Y3 | IO228NDB5V4 | | |
| Y4 | IO224NDB5V3 | | |
| Y5 | GND | | |
| Y6 | IO220NDB5V3 | | |

FG676



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

| FG676 | | FG676 | | FG676 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| A1 | GND | AA11 | IO153NDB5V2 | AB21 | TCK |
| A2 | GND | AA12 | IO147NDB5V1 | AB22 | TRST |
| A3 | GAA0/IO00NDB0V0 | AA13 | IO139NDB5V0 | AB23 | GDC0/IO108NDB3V2 |
| A4 | GAA1/IO00PDB0V0 | AA14 | IO137NDB5V0 | AB24 | GDC1/IO108PDB3V2 |
| A5 | IO06NDB0V0 | AA15 | IO123NDB4V1 | AB25 | IO104NDB3V2 |
| A6 | IO09NDB0V1 | AA16 | IO123PDB4V1 | AB26 | IO104PDB3V2 |
| A7 | IO09PDB0V1 | AA17 | IO117NDB4V0 | AC1 | IO170PDB6V0 |
| A8 | IO14NDB0V1 | AA18 | IO117PDB4V0 | AC2 | GEB0/IO168NPB6V0 |
| A9 | IO14PDB0V1 | AA19 | GDB2/IO112PDB4V0 | AC3 | IO166NPB5V3 |
| A10 | IO22NDB0V2 | AA20 | GNDQ | AC4 | GNDQ |
| A11 | IO22PDB0V2 | AA21 | TDO | AC5 | GND |
| A12 | IO26NDB0V3 | AA22 | GND | AC6 | IO160PDB5V3 |
| A13 | IO26PDB0V3 | AA23 | GND | AC7 | IO161PDB5V3 |
| A14 | IO30NDB0V3 | AA24 | IO102NDB3V1 | AC8 | IO154PDB5V2 |
| A15 | IO30PDB0V3 | AA25 | IO102PDB3V1 | AC9 | GND |
| A16 | IO34NDB1V0 | AA26 | IO98NDB3V1 | AC10 | IO150NDB5V1 |
| A17 | IO34PDB1V0 | AB1 | IO174NDB6V0 | AC11 | IO155NDB5V2 |
| A18 | IO38NDB1V0 | AB2 | IO171NDB6V0 | AC12 | IO142NDB5V0 |
| A19 | IO38PDB1V0 | AB3 | GEB1/IO168PPB6V0 | AC13 | IO138NDB5V0 |
| A20 | IO41PDB1V1 | AB4 | GEA0/IO167NPB6V0 | AC14 | IO138PDB5V0 |
| A21 | IO44PDB1V1 | AB5 | VCCPLE | AC15 | IO132NDB4V2 |
| A22 | IO49PDB1V2 | AB6 | GND | AC16 | IO129NDB4V2 |
| A23 | IO50PDB1V2 | AB7 | GND | AC17 | IO121NDB4V1 |
| A24 | GBC1/IO55PDB1V3 | AB8 | IO156NDB5V2 | AC18 | IO119PDB4V1 |
| A25 | GND | AB9 | IO156PDB5V2 | AC19 | IO118NDB4V0 |
| A26 | GND | AB10 | IO150PDB5V1 | AC20 | IO118PDB4V0 |
| AA1 | IO174PDB6V0 | AB11 | IO155PDB5V2 | AC21 | IO114PPB4V0 |
| AA2 | IO171PDB6V0 | AB12 | IO142PDB5V0 | AC22 | TMS |
| AA3 | GEA1/IO167PPB6V0 | AB13 | IO135NDB5V0 | AC23 | VJTAG |
| AA4 | GEC0/IO169NPB6V0 | AB14 | IO135PDB5V0 | AC24 | VMV3 |
| AA5 | VCOMPLE | AB15 | IO132PDB4V2 | AC25 | IO106NDB3V2 |
| AA6 | GND | AB16 | IO129PDB4V2 | AC26 | IO106PDB3V2 |
| AA7 | IO165NDB5V3 | AB17 | IO121PDB4V1 | AD1 | IO170NDB6V0 |
| AA8 | GEB2/IO165PDB5V3 | AB18 | IO119NDB4V1 | AD2 | GEA2/IO166PPB5V3 |
| AA9 | IO163PDB5V3 | AB19 | IO112NDB4V0 | AD3 | VMV5 |
| AA10 | IO159NDB5V3 | AB20 | VMV4 | AD4 | GEC2/IO164PDB5V3 |

Package Pin Assignments

| FG676 | | FG676 | | FG676 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| AD5 | IO162PDB5V3 | AE15 | IO134NDB4V2 | AF25 | GND |
| AD6 | IO160NDB5V3 | AE16 | IO133NDB4V2 | AF26 | GND |
| AD7 | IO161NDB5V3 | AE17 | IO127NDB4V2 | B1 | GND |
| AD8 | IO154NDB5V2 | AE18 | IO130NDB4V2 | B2 | GND |
| AD9 | IO148PDB5V1 | AE19 | IO126NDB4V1 | B3 | GND |
| AD10 | IO151PDB5V2 | AE20 | IO124NDB4V1 | B4 | GND |
| AD11 | IO144PDB5V1 | AE21 | IO120NDB4V1 | B5 | IO06PDB0V0 |
| AD12 | IO140PDB5V0 | AE22 | IO116PDB4V0 | B6 | IO04NDB0V0 |
| AD13 | IO143PDB5V1 | AE23 | GDC2/IO113PDB4V0 | B7 | IO07NDB0V0 |
| AD14 | IO141PDB5V0 | AE24 | GDA2/IO111PDB4V0 | B8 | IO11NDB0V1 |
| AD15 | IO134PDB4V2 | AE25 | GND | B9 | IO10NDB0V1 |
| AD16 | IO133PDB4V2 | AE26 | GND | B10 | IO16NDB0V2 |
| AD17 | IO127PDB4V2 | AF1 | GND | B11 | IO20NDB0V2 |
| AD18 | IO130PDB4V2 | AF2 | GND | B12 | IO24NDB0V3 |
| AD19 | IO126PDB4V1 | AF3 | GND | B13 | IO23NDB0V2 |
| AD20 | IO124PDB4V1 | AF4 | GND | B14 | IO28NDB0V3 |
| AD21 | IO120PDB4V1 | AF5 | IO158NPB5V2 | B15 | IO31NDB0V3 |
| AD22 | IO114NPB4V0 | AF6 | IO157NPB5V2 | B16 | IO32PDB1V0 |
| AD23 | TDI | AF7 | IO152NPB5V2 | B17 | IO36PDB1V0 |
| AD24 | GNDQ | AF8 | IO146NDB5V1 | B18 | IO37PDB1V0 |
| AD25 | GDA0/IO110NDB3V2 | AF9 | IO146PDB5V1 | B19 | IO42NPB1V1 |
| AD26 | GDA1/IO110PDB3V2 | AF10 | IO149NDB5V1 | B20 | IO41NDB1V1 |
| AE1 | GND | AF11 | IO149PDB5V1 | B21 | IO44NDB1V1 |
| AE2 | GND | AF12 | IO145NDB5V1 | B22 | IO49NDB1V2 |
| AE3 | GND | AF13 | IO145PDB5V1 | B23 | IO50NDB1V2 |
| AE4 | IO164NDB5V3 | AF14 | IO136NDB5V0 | B24 | GBC0/IO55NDB1V3 |
| AE5 | IO162NDB5V3 | AF15 | IO136PDB5V0 | B25 | GND |
| AE6 | IO158PPB5V2 | AF16 | IO131NDB4V2 | B26 | GND |
| AE7 | IO157PPB5V2 | AF17 | IO131PDB4V2 | C1 | GND |
| AE8 | IO152PPB5V2 | AF18 | IO128NDB4V2 | C2 | GND |
| AE9 | IO148NDB5V1 | AF19 | IO128PDB4V2 | C3 | GND |
| AE10 | IO151NDB5V2 | AF20 | IO122NDB4V1 | C4 | GND |
| AE11 | IO144NDB5V1 | AF21 | IO122PDB4V1 | C5 | GAA2/IO221PDB7V3 |
| AE12 | IO140NDB5V0 | AF22 | IO116NDB4V0 | C6 | IO04PDB0V0 |
| AE13 | IO143NDB5V1 | AF23 | IO113NDB4V0 | C7 | IO07PDB0V0 |
| AE14 | IO141NDB5V0 | AF24 | IO111NDB4V0 | C8 | IO11PDB0V1 |

| FG676 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| C9 | IO10PDB0V1 |
| C10 | IO16PDB0V2 |
| C11 | IO20PDB0V2 |
| C12 | IO24PDB0V3 |
| C13 | IO23PDB0V2 |
| C14 | IO28PDB0V3 |
| C15 | IO31PDB0V3 |
| C16 | IO32NDB1V0 |
| C17 | IO36NDB1V0 |
| C18 | IO37NDB1V0 |
| C19 | IO45NDB1V1 |
| C20 | IO42PPB1V1 |
| C21 | IO46NPB1V1 |
| C22 | IO48NPB1V2 |
| C23 | GBB0/IO56NPB1V3 |
| C24 | VMV1 |
| C25 | GBC2/IO60PDB2V0 |
| C26 | IO60NDB2V0 |
| D1 | IO218NDB7V3 |
| D2 | IO218PDB7V3 |
| D3 | GND |
| D4 | VMV7 |
| D5 | IO221NDB7V3 |
| D6 | GAC0/IO02NDB0V0 |
| D7 | GAC1/IO02PDB0V0 |
| D8 | IO05NDB0V0 |
| D9 | IO08PDB0V1 |
| D10 | IO12NDB0V1 |
| D11 | IO18NDB0V2 |
| D12 | IO17NDB0V2 |
| D13 | IO25NDB0V3 |
| D14 | IO29NDB0V3 |
| D15 | IO33NDB1V0 |
| D16 | IO40PDB1V1 |
| D17 | IO43NDB1V1 |
| D18 | IO47PDB1V1 |

| FG676 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| D19 | IO45PDB1V1 |
| D20 | IO46PPB1V1 |
| D21 | IO48PPB1V2 |
| D22 | GBA0/IO57NPB1V3 |
| D23 | GNDQ |
| D24 | GBB1/IO56PPB1V3 |
| D25 | GBB2/IO59PDB2V0 |
| D26 | IO59NDB2V0 |
| E1 | IO212PDB7V2 |
| E2 | IO211NDB7V2 |
| E3 | IO211PDB7V2 |
| E4 | IO220NPB7V3 |
| E5 | GNDQ |
| E6 | GAB2/IO220PPB7V3 |
| E7 | GAB1/IO01PDB0V0 |
| E8 | IO05PDB0V0 |
| E9 | IO08NDB0V1 |
| E10 | IO12PDB0V1 |
| E11 | IO18PDB0V2 |
| E12 | IO17PDB0V2 |
| E13 | IO25PDB0V3 |
| E14 | IO29PDB0V3 |
| E15 | IO33PDB1V0 |
| E16 | IO40NDB1V1 |
| E17 | IO43PDB1V1 |
| E18 | IO47NDB1V1 |
| E19 | IO54NDB1V3 |
| E20 | IO52NDB1V2 |
| E21 | IO52PDB1V2 |
| E22 | VCCPLB |
| E23 | GBA1/IO57PPB1V3 |
| E24 | IO63PDB2V0 |
| E25 | IO63NDB2V0 |
| E26 | IO68PDB2V1 |
| F1 | IO212NDB7V2 |
| F2 | IO203PPB7V1 |

| FG676 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| F3 | IO213NDB7V2 |
| F4 | IO213PDB7V2 |
| F5 | GND |
| F6 | VCCPLA |
| F7 | GAB0/IO01NDB0V0 |
| F8 | GNDQ |
| F9 | IO03PDB0V0 |
| F10 | IO13PDB0V1 |
| F11 | IO15PDB0V1 |
| F12 | IO19PDB0V2 |
| F13 | IO21PDB0V2 |
| F14 | IO27NDB0V3 |
| F15 | IO35PDB1V0 |
| F16 | IO39NDB1V0 |
| F17 | IO51PDB1V2 |
| F18 | IO53PDB1V2 |
| F19 | IO54PDB1V3 |
| F20 | VMV2 |
| F21 | VCOMPLB |
| F22 | IO61PDB2V0 |
| F23 | IO61NDB2V0 |
| F24 | IO66PDB2V1 |
| F25 | IO66NDB2V1 |
| F26 | IO68NDB2V1 |
| G1 | IO203NPB7V1 |
| G2 | IO207NDB7V2 |
| G3 | IO207PDB7V2 |
| G4 | IO216NDB7V3 |
| G5 | IO216PDB7V3 |
| G6 | VCOMPLA |
| G7 | VMV0 |
| G8 | VCC |
| G9 | IO03NDB0V0 |
| G10 | IO13NDB0V1 |
| G11 | IO15NDB0V1 |
| G12 | IO19NDB0V2 |

Package Pin Assignments

| FG676 | | FG676 | | FG676 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| G13 | IO21NDB0V2 | H23 | IO69PDB2V1 | K7 | IO217NDB7V3 |
| G14 | IO27PDB0V3 | H24 | IO76PDB2V2 | K8 | VCCIB7 |
| G15 | IO35NDB1V0 | H25 | IO76NDB2V2 | K9 | VCC |
| G16 | IO39PDB1V0 | H26 | IO78NDB2V2 | K10 | GND |
| G17 | IO51NDB1V2 | J1 | IO197NDB7V0 | K11 | GND |
| G18 | IO53NDB1V2 | J2 | IO197PDB7V0 | K12 | GND |
| G19 | VCCIB1 | J3 | VMV7 | K13 | GND |
| G20 | GBA2/IO58PPB2V0 | J4 | IO215NDB7V3 | K14 | GND |
| G21 | GNDQ | J5 | IO215PDB7V3 | K15 | GND |
| G22 | IO64NDB2V1 | J6 | IO214PDB7V3 | K16 | GND |
| G23 | IO64PDB2V1 | J7 | IO214NDB7V3 | K17 | GND |
| G24 | IO72PDB2V2 | J8 | VCCIB7 | K18 | VCC |
| G25 | IO72NDB2V2 | J9 | VCC | K19 | VCCIB2 |
| G26 | IO78PDB2V2 | J10 | VCC | K20 | IO65PDB2V1 |
| H1 | IO208NDB7V2 | J11 | VCC | K21 | IO65NDB2V1 |
| H2 | IO208PDB7V2 | J12 | VCC | K22 | IO74PDB2V2 |
| H3 | IO209NDB7V2 | J13 | VCC | K23 | IO74NDB2V2 |
| H4 | IO209PDB7V2 | J14 | VCC | K24 | IO75PDB2V2 |
| H5 | IO219NDB7V3 | J15 | VCC | K25 | IO75NDB2V2 |
| H6 | GAC2/IO219PDB7V3 | J16 | VCC | K26 | IO84PDB2V3 |
| H7 | VCCIB7 | J17 | VCC | L1 | IO195NDB7V0 |
| H8 | VCC | J18 | VCC | L2 | IO198PPB7V0 |
| H9 | VCCIB0 | J19 | VCCIB2 | L3 | GNDQ |
| H10 | VCCIB0 | J20 | IO62PDB2V0 | L4 | IO201PDB7V1 |
| H11 | VCCIB0 | J21 | IO62NDB2V0 | L5 | IO201NDB7V1 |
| H12 | VCCIB0 | J22 | IO70NDB2V1 | L6 | IO210NDB7V2 |
| H13 | VCCIB0 | J23 | IO69NDB2V1 | L7 | IO210PDB7V2 |
| H14 | VCCIB1 | J24 | VMV2 | L8 | VCCIB7 |
| H15 | VCCIB1 | J25 | IO80PDB2V3 | L9 | VCC |
| H16 | VCCIB1 | J26 | IO80NDB2V3 | L10 | GND |
| H17 | VCCIB1 | K1 | IO195PDB7V0 | L11 | GND |
| H18 | VCCIB1 | K2 | IO199NDB7V1 | L12 | GND |
| H19 | VCC | K3 | IO199PDB7V1 | L13 | GND |
| H20 | VCC | K4 | IO205NDB7V1 | L14 | GND |
| H21 | IO58NPB2V0 | K5 | IO205PDB7V1 | L15 | GND |
| H22 | IO70PDB2V1 | K6 | IO217PDB7V3 | L16 | GND |

| FG676 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| L17 | GND |
| L18 | VCC |
| L19 | VCCIB2 |
| L20 | IO67PDB2V1 |
| L21 | IO67NDB2V1 |
| L22 | IO71PDB2V2 |
| L23 | IO71NDB2V2 |
| L24 | GNDQ |
| L25 | IO82PDB2V3 |
| L26 | IO84NDB2V3 |
| M1 | IO198NPB7V0 |
| M2 | IO202PDB7V1 |
| M3 | IO202NDB7V1 |
| M4 | IO206NDB7V1 |
| M5 | IO206PDB7V1 |
| M6 | IO204NDB7V1 |
| M7 | IO204PDB7V1 |
| M8 | VCCIB7 |
| M9 | VCC |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M15 | GND |
| M16 | GND |
| M17 | GND |
| M18 | VCC |
| M19 | VCCIB2 |
| M20 | IO73NDB2V2 |
| M21 | IO73PDB2V2 |
| M22 | IO81PPB2V3 |
| M23 | IO77PDB2V2 |
| M24 | IO77NDB2V2 |
| M25 | IO82NDB2V3 |
| M26 | IO83PDB2V3 |

| FG676 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| N1 | GFB0/IO191NPB7V0 |
| N2 | VCOMPLF |
| N3 | GFB1/IO191PPB7V0 |
| N4 | IO196PDB7V0 |
| N5 | GFA0/IO190NDB6V2 |
| N6 | IO200PDB7V1 |
| N7 | IO200NDB7V1 |
| N8 | VCCIB7 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N15 | GND |
| N16 | GND |
| N17 | GND |
| N18 | VCC |
| N19 | VCCIB2 |
| N20 | IO79PDB2V3 |
| N21 | IO79NDB2V3 |
| N22 | GCA2/IO88PPB3V0 |
| N23 | IO81NPB2V3 |
| N24 | GCA0/IO87NDB3V0 |
| N25 | GCB0/IO86NPB2V3 |
| N26 | IO83NDB2V3 |
| P1 | GFA2/IO189PDB6V2 |
| P2 | VCCPLF |
| P3 | IO193PPB7V0 |
| P4 | IO196NDB7V0 |
| P5 | GFA1/IO190PDB6V2 |
| P6 | IO194PDB7V0 |
| P7 | IO194NDB7V0 |
| P8 | VCCIB6 |
| P9 | VCC |
| P10 | GND |

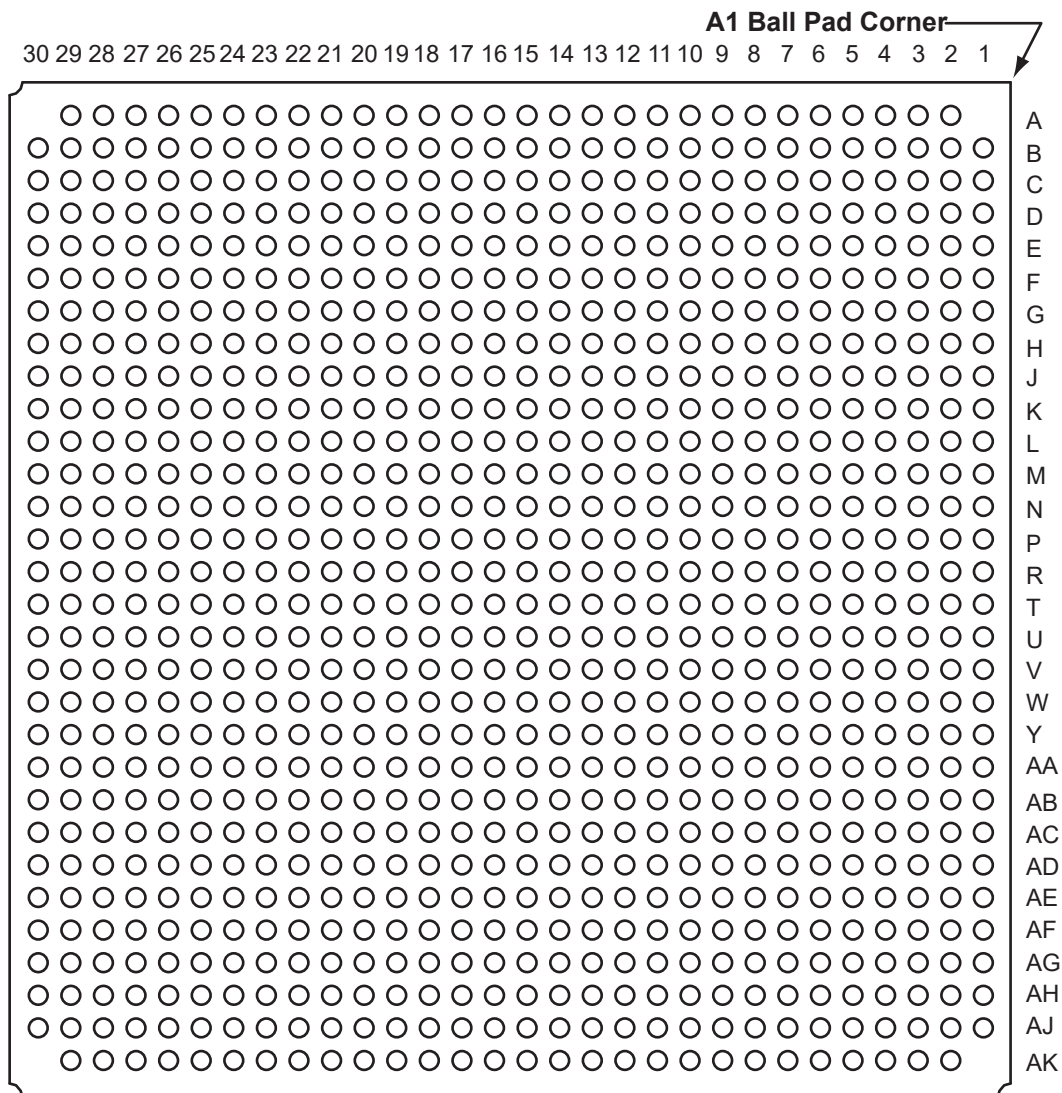
| FG676 | |
|------------|-------------------|
| Pin Number | A3PE1500 Function |
| P11 | GND |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P15 | GND |
| P16 | GND |
| P17 | GND |
| P18 | VCC |
| P19 | VCCIB3 |
| P20 | GCC0/IO85NDB2V3 |
| P21 | GCC1/IO85PDB2V3 |
| P22 | GCB1/IO86PPB2V3 |
| P23 | IO88NPB3V0 |
| P24 | GCA1/IO87PDB3V0 |
| P25 | VCCPLC |
| P26 | VCOMPLC |
| R1 | IO189NDB6V2 |
| R2 | IO185PDB6V2 |
| R3 | IO187NPB6V2 |
| R4 | IO193NPB7V0 |
| R5 | GFC2/IO187PPB6V2 |
| R6 | GFC1/IO192PDB7V0 |
| R7 | GFC0/IO192NDB7V0 |
| R8 | VCCIB6 |
| R9 | VCC |
| R10 | GND |
| R11 | GND |
| R12 | GND |
| R13 | GND |
| R14 | GND |
| R15 | GND |
| R16 | GND |
| R17 | GND |
| R18 | VCC |
| R19 | VCCIB3 |
| R20 | NC |

Package Pin Assignments

| FG676 | | FG676 | | FG676 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function | Pin Number | A3PE1500 Function |
| R21 | IO89NDB3V0 | U5 | IO182PDB6V1 | V15 | VCC |
| R22 | GCB2/IO89PDB3V0 | U6 | IO178PDB6V1 | V16 | VCC |
| R23 | IO90NDB3V0 | U7 | IO178NDB6V1 | V17 | VCC |
| R24 | GCC2/IO90PDB3V0 | U8 | VCCIB6 | V18 | VCC |
| R25 | IO91PDB3V0 | U9 | VCC | V19 | VCCIB3 |
| R26 | IO91NDB3V0 | U10 | GND | V20 | IO107PDB3V2 |
| T1 | IO186PDB6V2 | U11 | GND | V21 | IO107NDB3V2 |
| T2 | IO185NDB6V2 | U12 | GND | V22 | IO103NDB3V2 |
| T3 | GNDQ | U13 | GND | V23 | IO103PDB3V2 |
| T4 | IO180PDB6V1 | U14 | GND | V24 | VMV3 |
| T5 | IO180NDB6V1 | U15 | GND | V25 | IO95NDB3V1 |
| T6 | IO188NDB6V2 | U16 | GND | V26 | IO94PDB3V0 |
| T7 | GFB2/IO188PDB6V2 | U17 | GND | W1 | IO179NDB6V1 |
| T8 | VCCIB6 | U18 | VCC | W2 | IO179PDB6V1 |
| T9 | VCC | U19 | VCCIB3 | W3 | IO177NDB6V1 |
| T10 | GND | U20 | NC | W4 | IO177PDB6V1 |
| T11 | GND | U21 | IO101NDB3V1 | W5 | IO172PDB6V0 |
| T12 | GND | U22 | IO101PDB3V1 | W6 | IO172NDB6V0 |
| T13 | GND | U23 | IO92NDB3V0 | W7 | VCC |
| T14 | GND | U24 | IO92PDB3V0 | W8 | VCC |
| T15 | GND | U25 | IO95PDB3V1 | W9 | VCCIB5 |
| T16 | GND | U26 | IO93NPB3V0 | W10 | VCCIB5 |
| T17 | GND | V1 | IO183PDB6V2 | W11 | VCCIB5 |
| T18 | VCC | V2 | IO183NDB6V2 | W12 | VCCIB5 |
| T19 | VCCIB3 | V3 | VMV6 | W13 | VCCIB5 |
| T20 | IO99PDB3V1 | V4 | IO181PDB6V1 | W14 | VCCIB4 |
| T21 | IO99NDB3V1 | V5 | IO181NDB6V1 | W15 | VCCIB4 |
| T22 | IO97PDB3V1 | V6 | IO176PDB6V1 | W16 | VCCIB4 |
| T23 | IO97NDB3V1 | V7 | IO176NDB6V1 | W17 | VCCIB4 |
| T24 | GNDQ | V8 | VCCIB6 | W18 | VCCIB4 |
| T25 | IO93PPB3V0 | V9 | VCC | W19 | VCC |
| T26 | NC | V10 | VCC | W20 | VCCIB3 |
| U1 | IO186NDB6V2 | V11 | VCC | W21 | GDB0/IO109NDB3V2 |
| U2 | IO184NDB6V2 | V12 | VCC | W22 | GDB1/IO109PDB3V2 |
| U3 | IO184PDB6V2 | V13 | VCC | W23 | IO105NDB3V2 |
| U4 | IO182NDB6V1 | V14 | VCC | W24 | IO105PDB3V2 |

| FG676 | |
|-------------------|--------------------------|
| Pin Number | A3PE1500 Function |
| W25 | IO96PDB3V1 |
| W26 | IO94NDB3V0 |
| Y1 | IO175NDB6V1 |
| Y2 | IO175PDB6V1 |
| Y3 | IO173NDB6V0 |
| Y4 | IO173PDB6V0 |
| Y5 | GEC1/IO169PPB6V0 |
| Y6 | GNDQ |
| Y7 | VMV6 |
| Y8 | VCCIB5 |
| Y9 | IO163NDB5V3 |
| Y10 | IO159PDB5V3 |
| Y11 | IO153PDB5V2 |
| Y12 | IO147PDB5V1 |
| Y13 | IO139PDB5V0 |
| Y14 | IO137PDB5V0 |
| Y15 | IO125NDB4V1 |
| Y16 | IO125PDB4V1 |
| Y17 | IO115NDB4V0 |
| Y18 | IO115PDB4V0 |
| Y19 | VCC |
| Y20 | VPUMP |
| Y21 | VCOMPLD |
| Y22 | VCCPLD |
| Y23 | IO100NDB3V1 |
| Y24 | IO100PDB3V1 |
| Y25 | IO96NDB3V1 |
| Y26 | IO98PDB3V1 |

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Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| A2 | GND | AA9 | GEB1/IO235PPB6V0 | AB15 | IO198PDB5V0 |
| A3 | GND | AA10 | VCC | AB16 | IO192NDB4V4 |
| A4 | IO14NPB0V1 | AA11 | IO226PPB5V4 | AB17 | IO192PDB4V4 |
| A5 | GND | AA12 | VCCIB5 | AB18 | IO178NDB4V3 |
| A6 | IO07NPB0V0 | AA13 | VCCIB5 | AB19 | IO178PDB4V3 |
| A7 | GND | AA14 | VCCIB5 | AB20 | IO174NDB4V2 |
| A8 | IO09NDB0V1 | AA15 | VCCIB5 | AB21 | IO162NPB4V1 |
| A9 | IO17NDB0V2 | AA16 | VCCIB4 | AB22 | VCC |
| A10 | IO17PDB0V2 | AA17 | VCCIB4 | AB23 | VCCPLD |
| A11 | IO21NDB0V2 | AA18 | VCCIB4 | AB24 | VCCIB3 |
| A12 | IO21PDB0V2 | AA19 | VCCIB4 | AB25 | IO150PDB3V4 |
| A13 | IO33NDB0V4 | AA20 | IO174PDB4V2 | AB26 | IO148PDB3V4 |
| A14 | IO33PDB0V4 | AA21 | VCC | AB27 | IO147NDB3V4 |
| A15 | IO35NDB0V4 | AA22 | IO142NPB3V3 | AB28 | IO145PDB3V3 |
| A16 | IO35PDB0V4 | AA23 | IO144NDB3V3 | AB29 | IO143PDB3V3 |
| A17 | IO41NDB1V0 | AA24 | IO144PDB3V3 | AB30 | IO137PDB3V2 |
| A18 | IO43NDB1V0 | AA25 | IO146NDB3V4 | AC1 | IO254PDB6V2 |
| A19 | IO43PDB1V0 | AA26 | IO146PDB3V4 | AC2 | IO254NDB6V2 |
| A20 | IO45NDB1V0 | AA27 | IO147PDB3V4 | AC3 | IO240PDB6V0 |
| A21 | IO45PDB1V0 | AA28 | IO139NDB3V3 | AC4 | GEC1/IO236PDB6V0 |
| A22 | IO57NDB1V2 | AA29 | IO139PDB3V3 | AC5 | IO237PDB6V0 |
| A23 | IO57PDB1V2 | AA30 | IO133NDB3V2 | AC6 | IO237NDB6V0 |
| A24 | GND | AB1 | IO256NDB6V2 | AC7 | VCOMPLE |
| A25 | IO69PPB1V3 | AB2 | IO244PDB6V1 | AC8 | GND |
| A26 | GND | AB3 | IO244NDB6V1 | AC9 | IO226NPB5V4 |
| A27 | GBC1/IO79PPB1V4 | AB4 | IO241PDB6V0 | AC10 | IO222NDB5V3 |
| A28 | GND | AB5 | IO241NDB6V0 | AC11 | IO216NPB5V2 |
| A29 | GND | AB6 | IO243NPB6V1 | AC12 | IO210NPB5V2 |
| AA1 | IO256PDB6V2 | AB7 | VCCIB6 | AC13 | IO204NDB5V1 |
| AA2 | IO248PDB6V1 | AB8 | VCCPLE | AC14 | IO204PDB5V1 |
| AA3 | IO248NDB6V1 | AB9 | VCC | AC15 | IO194NDB5V0 |
| AA4 | IO246NDB6V1 | AB10 | IO222PDB5V3 | AC16 | IO188NDB4V4 |
| AA5 | GEA1/IO234PDB6V0 | AB11 | IO218PPB5V3 | AC17 | IO188PDB4V4 |
| AA6 | GEA0/IO234NDB6V0 | AB12 | IO206NDB5V1 | AC18 | IO182PPB4V3 |
| AA7 | IO243PPB6V1 | AB13 | IO206PDB5V1 | AC19 | IO170NPB4V2 |
| AA8 | IO245NDB6V1 | AB14 | IO198NDB5V0 | AC20 | IO164NDB4V1 |

Package Pin Assignments

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| AC21 | IO164PDB4V1 | AD27 | GDA0/IO153NDB3V4 | AF3 | VCCIB6 |
| AC22 | IO162PPB4V1 | AD28 | GDC0/IO151NDB3V4 | AF4 | IO220NPB5V3 |
| AC23 | GND | AD29 | GDC1/IO151PDB3V4 | AF5 | VCC |
| AC24 | VCOMPLD | AD30 | GND | AF6 | IO228NDB5V4 |
| AC25 | IO150NDB3V4 | AE1 | IO242PPB6V1 | AF7 | VCCIB5 |
| AC26 | IO148NDB3V4 | AE2 | VCC | AF8 | IO230PDB5V4 |
| AC27 | GDA1/IO153PDB3V4 | AE3 | IO239PDB6V0 | AF9 | IO229NDB5V4 |
| AC28 | IO145NDB3V3 | AE4 | IO239NDB6V0 | AF10 | IO229PDB5V4 |
| AC29 | IO143NDB3V3 | AE5 | VMV6 | AF11 | IO214PPB5V2 |
| AC30 | IO137NDB3V2 | AE6 | GND | AF12 | IO208NDB5V1 |
| AD1 | GND | AE7 | GNDQ | AF13 | IO208PDB5V1 |
| AD2 | IO242NPB6V1 | AE8 | IO230NDB5V4 | AF14 | IO200PDB5V0 |
| AD3 | IO240NDB6V0 | AE9 | IO224NPB5V3 | AF15 | IO196NDB5V0 |
| AD4 | GEC0/IO236NDB6V0 | AE10 | IO214NPB5V2 | AF16 | IO186NDB4V4 |
| AD5 | VCCIB6 | AE11 | IO212NDB5V2 | AF17 | IO186PDB4V4 |
| AD6 | GNDQ | AE12 | IO212PDB5V2 | AF18 | IO180NDB4V3 |
| AD7 | VCC | AE13 | IO202NPB5V1 | AF19 | IO180PDB4V3 |
| AD8 | VMV5 | AE14 | IO200NDB5V0 | AF20 | IO168NDB4V1 |
| AD9 | VCCIB5 | AE15 | IO196PDB5V0 | AF21 | IO168PDB4V1 |
| AD10 | IO224PPB5V3 | AE16 | IO190NDB4V4 | AF22 | IO160NDB4V0 |
| AD11 | IO218NPB5V3 | AE17 | IO184PDB4V3 | AF23 | IO158NPB4V0 |
| AD12 | IO216PPB5V2 | AE18 | IO184NDB4V3 | AF24 | VCCIB4 |
| AD13 | IO210PPB5V2 | AE19 | IO172PDB4V2 | AF25 | IO154NPB4V0 |
| AD14 | IO202PPB5V1 | AE20 | IO172NDB4V2 | AF26 | VCC |
| AD15 | IO194PDB5V0 | AE21 | IO166NDB4V1 | AF27 | TDO |
| AD16 | IO190PDB4V4 | AE22 | IO160PDB4V0 | AF28 | VCCIB3 |
| AD17 | IO182NPB4V3 | AE23 | GNDQ | AF29 | GNDQ |
| AD18 | IO176NDB4V2 | AE24 | VMV4 | AF30 | GND |
| AD19 | IO176PDB4V2 | AE25 | GND | AG1 | IO238NPB6V0 |
| AD20 | IO170PPB4V2 | AE26 | GDB0/IO152NDB3V4 | AG2 | VCC |
| AD21 | IO166PDB4V1 | AE27 | GDB1/IO152PDB3V4 | AG3 | IO232NPB5V4 |
| AD22 | VCCIB4 | AE28 | VMV3 | AG4 | GND |
| AD23 | TCK | AE29 | VCC | AG5 | IO220PPB5V3 |
| AD24 | VCC | AE30 | IO149PDB3V4 | AG6 | IO228PDB5V4 |
| AD25 | TRST | AF1 | GND | AG7 | IO231NDB5V4 |
| AD26 | VCCIB3 | AF2 | IO238PPB6V0 | AG8 | GEC2/IO231PDB5V4 |

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| AG9 | IO225NPB5V3 | AH15 | IO195NDB5V0 | AJ21 | IO173PDB4V2 |
| AG10 | IO223NPB5V3 | AH16 | IO185NDB4V3 | AJ22 | IO163NDB4V1 |
| AG11 | IO221PDB5V3 | AH17 | IO185PDB4V3 | AJ23 | IO163PDB4V1 |
| AG12 | IO221NDB5V3 | AH18 | IO181PDB4V3 | AJ24 | IO167NPB4V1 |
| AG13 | IO205NPB5V1 | AH19 | IO177NDB4V2 | AJ25 | VCC |
| AG14 | IO199NDB5V0 | AH20 | IO171NPB4V2 | AJ26 | IO156NPB4V0 |
| AG15 | IO199PDB5V0 | AH21 | IO165PPB4V1 | AJ27 | VCC |
| AG16 | IO187NDB4V4 | AH22 | IO161PPB4V0 | AJ28 | TMS |
| AG17 | IO187PDB4V4 | AH23 | IO157NDB4V0 | AJ29 | GND |
| AG18 | IO181NDB4V3 | AH24 | IO157PDB4V0 | AJ30 | GND |
| AG19 | IO171PPB4V2 | AH25 | IO155NDB4V0 | AK2 | GND |
| AG20 | IO165NPB4V1 | AH26 | VCCIB4 | AK3 | GND |
| AG21 | IO161NPB4V0 | AH27 | TDI | AK4 | IO217PPB5V2 |
| AG22 | IO159NDB4V0 | AH28 | VCC | AK5 | GND |
| AG23 | IO159PDB4V0 | AH29 | VPUMP | AK6 | IO215PPB5V2 |
| AG24 | IO158PPB4V0 | AH30 | GND | AK7 | GND |
| AG25 | GDB2/IO155PDB4V0 | AJ1 | GND | AK8 | IO207NDB5V1 |
| AG26 | GDA2/IO154PPB4V0 | AJ2 | GND | AK9 | IO207PDB5V1 |
| AG27 | GND | AJ3 | GEA2/IO233PPB5V4 | AK10 | IO201NDB5V0 |
| AG28 | VJTAG | AJ4 | VCC | AK11 | IO201PDB5V0 |
| AG29 | VCC | AJ5 | IO217NPB5V2 | AK12 | IO193NDB4V4 |
| AG30 | IO149NDB3V4 | AJ6 | VCC | AK13 | IO193PDB4V4 |
| AH1 | GND | AJ7 | IO215NPB5V2 | AK14 | IO197PDB5V0 |
| AH2 | IO233NPB5V4 | AJ8 | IO213NDB5V2 | AK15 | IO191NDB4V4 |
| AH3 | VCC | AJ9 | IO213PDB5V2 | AK16 | IO191PDB4V4 |
| AH4 | GEB2/IO232PPB5V4 | AJ10 | IO209NDB5V1 | AK17 | IO189NDB4V4 |
| AH5 | VCCIB5 | AJ11 | IO209PDB5V1 | AK18 | IO189PDB4V4 |
| AH6 | IO219NDB5V3 | AJ12 | IO203NDB5V1 | AK19 | IO179PPB4V3 |
| AH7 | IO219PDB5V3 | AJ13 | IO203PDB5V1 | AK20 | IO175NDB4V2 |
| AH8 | IO227NDB5V4 | AJ14 | IO197NDB5V0 | AK21 | IO175PDB4V2 |
| AH9 | IO227PDB5V4 | AJ15 | IO195PDB5V0 | AK22 | IO169NDB4V1 |
| AH10 | IO225PPB5V3 | AJ16 | IO183NDB4V3 | AK23 | IO169PDB4V1 |
| AH11 | IO223PPB5V3 | AJ17 | IO183PDB4V3 | AK24 | GND |
| AH12 | IO211NDB5V2 | AJ18 | IO179NPB4V3 | AK25 | IO167PPB4V1 |
| AH13 | IO211PDB5V2 | AJ19 | IO177PDB4V2 | AK26 | GND |
| AH14 | IO205PPB5V1 | AJ20 | IO173NDB4V2 | AK27 | GDC2/IO156PPB4V0 |

Package Pin Assignments

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| AK28 | GND | C5 | VCCIB0 | D11 | IO11PDB0V1 |
| AK29 | GND | C6 | IO03PDB0V0 | D12 | IO23NDB0V2 |
| B1 | GND | C7 | IO03NDB0V0 | D13 | IO23PDB0V2 |
| B2 | GND | C8 | GAB1/IO01PDB0V0 | D14 | IO27PDB0V3 |
| B3 | GAA2/IO309PPB7V4 | C9 | IO05PDB0V0 | D15 | IO40PDB0V4 |
| B4 | VCC | C10 | IO15NPB0V1 | D16 | IO47NDB1V0 |
| B5 | IO14PPB0V1 | C11 | IO25NDB0V3 | D17 | IO47PDB1V0 |
| B6 | VCC | C12 | IO25PDB0V3 | D18 | IO55NPB1V1 |
| B7 | IO07PPB0V0 | C13 | IO31NPB0V3 | D19 | IO65NDB1V3 |
| B8 | IO09PDB0V1 | C14 | IO27NDB0V3 | D20 | IO65PDB1V3 |
| B9 | IO15PPB0V1 | C15 | IO39NDB0V4 | D21 | IO71NDB1V3 |
| B10 | IO19NDB0V2 | C16 | IO39PDB0V4 | D22 | IO71PDB1V3 |
| B11 | IO19PDB0V2 | C17 | IO55PPB1V1 | D23 | IO73NDB1V4 |
| B12 | IO29NDB0V3 | C18 | IO51PDB1V1 | D24 | IO73PDB1V4 |
| B13 | IO29PDB0V3 | C19 | IO59NDB1V2 | D25 | IO74NDB1V4 |
| B14 | IO31PPB0V3 | C20 | IO63NDB1V2 | D26 | GBB0/IO80NPB1V4 |
| B15 | IO37NDB0V4 | C21 | IO63PDB1V2 | D27 | GND |
| B16 | IO37PDB0V4 | C22 | IO67NDB1V3 | D28 | GBA0/IO81NPB1V4 |
| B17 | IO41PDB1V0 | C23 | IO67PDB1V3 | D29 | VCC |
| B18 | IO51NDB1V1 | C24 | IO75NDB1V4 | D30 | GBA2/IO82PPB2V0 |
| B19 | IO59PDB1V2 | C25 | IO75PDB1V4 | E1 | GND |
| B20 | IO53PDB1V1 | C26 | VCCIB1 | E2 | IO303NPB7V3 |
| B21 | IO53NDB1V1 | C27 | IO64PPB1V2 | E3 | VCCIB7 |
| B22 | IO61NDB1V2 | C28 | VCC | E4 | IO305PPB7V3 |
| B23 | IO61PDB1V2 | C29 | GBA1/IO81PPB1V4 | E5 | VCC |
| B24 | IO69NPB1V3 | C30 | GND | E6 | GAC0/IO02NDB0V0 |
| B25 | VCC | D1 | IO303PPB7V3 | E7 | VCCIB0 |
| B26 | GBC0/IO79NPB1V4 | D2 | VCC | E8 | IO06PPB0V0 |
| B27 | VCC | D3 | IO305NPB7V3 | E9 | IO24NDB0V2 |
| B28 | IO64NPB1V2 | D4 | GND | E10 | IO24PDB0V2 |
| B29 | GND | D5 | GAA1/IO00PPB0V0 | E11 | IO13NDB0V1 |
| B30 | GND | D6 | GAC1/IO02PDB0V0 | E12 | IO13PDB0V1 |
| C1 | GND | D7 | IO06NPB0V0 | E13 | IO34NDB0V4 |
| C2 | IO309NPB7V4 | D8 | GAB0/IO01NDB0V0 | E14 | IO34PDB0V4 |
| C3 | VCC | D9 | IO05NDB0V0 | E15 | IO40NDB0V4 |
| C4 | GAA0/IO00NPB0V0 | D10 | IO11NDB0V1 | E16 | IO49NDB1V1 |

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|------------|-------------------|
| Pin Number | A3PE3000 Function |
| E17 | IO49PDB1V1 |
| E18 | IO50PDB1V1 |
| E19 | IO58PDB1V2 |
| E20 | IO60NDB1V2 |
| E21 | IO77PDB1V4 |
| E22 | IO68NDB1V3 |
| E23 | IO68PDB1V3 |
| E24 | VCCIB1 |
| E25 | IO74PDB1V4 |
| E26 | VCC |
| E27 | GBB1/IO80PPB1V4 |
| E28 | VCCIB2 |
| E29 | IO82NPB2V0 |
| E30 | GND |
| F1 | IO296PPB7V2 |
| F2 | VCC |
| F3 | IO306PDB7V4 |
| F4 | IO297PDB7V2 |
| F5 | VMV7 |
| F6 | GND |
| F7 | GNDQ |
| F8 | IO12NDB0V1 |
| F9 | IO12PDB0V1 |
| F10 | IO10PDB0V1 |
| F11 | IO16PDB0V1 |
| F12 | IO22NDB0V2 |
| F13 | IO30NDB0V3 |
| F14 | IO30PDB0V3 |
| F15 | IO36PDB0V4 |
| F16 | IO48NDB1V0 |
| F17 | IO48PDB1V0 |
| F18 | IO50NDB1V1 |
| F19 | IO58NDB1V2 |
| F20 | IO60PDB1V2 |
| F21 | IO77NDB1V4 |
| F22 | IO72NDB1V3 |

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|------------|-------------------|
| Pin Number | A3PE3000 Function |
| F23 | IO72PDB1V3 |
| F24 | GNDQ |
| F25 | GND |
| F26 | VMV2 |
| F27 | IO86PDB2V0 |
| F28 | IO92PDB2V1 |
| F29 | VCC |
| F30 | IO100NPB2V2 |
| G1 | GND |
| G2 | IO296NPB7V2 |
| G3 | IO306NDB7V4 |
| G4 | IO297NDB7V2 |
| G5 | VCCIB7 |
| G6 | GNDQ |
| G7 | VCC |
| G8 | VMV0 |
| G9 | VCCIB0 |
| G10 | IO10NDB0V1 |
| G11 | IO16NDB0V1 |
| G12 | IO22PDB0V2 |
| G13 | IO26PPB0V3 |
| G14 | IO38NPB0V4 |
| G15 | IO36NDB0V4 |
| G16 | IO46NDB1V0 |
| G17 | IO46PDB1V0 |
| G18 | IO56NDB1V1 |
| G19 | IO56PDB1V1 |
| G20 | IO66NDB1V3 |
| G21 | IO66PDB1V3 |
| G22 | VCCIB1 |
| G23 | VMV1 |
| G24 | VCC |
| G25 | GNDQ |
| G26 | VCCIB2 |
| G27 | IO86NDB2V0 |
| G28 | IO92NDB2V1 |

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|------------|-------------------|
| Pin Number | A3PE3000 Function |
| G29 | IO100PPB2V2 |
| G30 | GND |
| H1 | IO294PDB7V2 |
| H2 | IO294NDB7V2 |
| H3 | IO300NDB7V3 |
| H4 | IO300PDB7V3 |
| H5 | IO295PDB7V2 |
| H6 | IO299PDB7V3 |
| H7 | VCOMPLA |
| H8 | GND |
| H9 | IO08NDB0V0 |
| H10 | IO08PDB0V0 |
| H11 | IO18PDB0V2 |
| H12 | IO26NPB0V3 |
| H13 | IO28NDB0V3 |
| H14 | IO28PDB0V3 |
| H15 | IO38PPB0V4 |
| H16 | IO42NDB1V0 |
| H17 | IO52NDB1V1 |
| H18 | IO52PDB1V1 |
| H19 | IO62NDB1V2 |
| H20 | IO62PDB1V2 |
| H21 | IO70NDB1V3 |
| H22 | IO70PDB1V3 |
| H23 | GND |
| H24 | VCOMPLB |
| H25 | GBC2/IO84PDB2V0 |
| H26 | IO84NDB2V0 |
| H27 | IO96PDB2V1 |
| H28 | IO96NDB2V1 |
| H29 | IO89PDB2V0 |
| H30 | IO89NDB2V0 |
| J1 | IO290NDB7V2 |
| J2 | IO290PDB7V2 |
| J3 | IO302NDB7V3 |
| J4 | IO302PDB7V3 |

Package Pin Assignments

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| J5 | IO295NDB7V2 | K11 | IO04PPB0V0 | L17 | VCC |
| J6 | IO299NDB7V3 | K12 | VCCIB0 | L18 | VCC |
| J7 | VCCIB7 | K13 | VCCIB0 | L19 | VCC |
| J8 | VCCPLA | K14 | VCCIB0 | L20 | VCC |
| J9 | VCC | K15 | VCCIB0 | L21 | IO78NPB1V4 |
| J10 | IO04NPB0V0 | K16 | VCCIB1 | L22 | IO104NPB2V2 |
| J11 | IO18NDB0V2 | K17 | VCCIB1 | L23 | IO98NDB2V2 |
| J12 | IO20NDB0V2 | K18 | VCCIB1 | L24 | IO98PDB2V2 |
| J13 | IO20PDB0V2 | K19 | VCCIB1 | L25 | IO87PDB2V0 |
| J14 | IO32NDB0V3 | K20 | IO76PPB1V4 | L26 | IO87NDB2V0 |
| J15 | IO32PDB0V3 | K21 | VCC | L27 | IO97PDB2V1 |
| J16 | IO42PDB1V0 | K22 | IO78PPB1V4 | L28 | IO101PDB2V2 |
| J17 | IO44NDB1V0 | K23 | IO88NDB2V0 | L29 | IO103PDB2V2 |
| J18 | IO44PDB1V0 | K24 | IO88PDB2V0 | L30 | IO119NDB3V0 |
| J19 | IO54NDB1V1 | K25 | IO94PDB2V1 | M1 | IO282NDB7V1 |
| J20 | IO54PDB1V1 | K26 | IO94NDB2V1 | M2 | IO282PDB7V1 |
| J21 | IO76NPB1V4 | K27 | IO85PDB2V0 | M3 | IO292NDB7V2 |
| J22 | VCC | K28 | IO85NDB2V0 | M4 | IO292PDB7V2 |
| J23 | VCCPLB | K29 | IO93PDB2V1 | M5 | IO283NDB7V1 |
| J24 | VCCIB2 | K30 | IO93NDB2V1 | M6 | IO285PDB7V1 |
| J25 | IO90PDB2V1 | L1 | IO286NDB7V1 | M7 | IO287PDB7V1 |
| J26 | IO90NDB2V1 | L2 | IO286PDB7V1 | M8 | IO289PDB7V1 |
| J27 | GBB2/IO83PDB2V0 | L3 | IO298NDB7V3 | M9 | IO289NDB7V1 |
| J28 | IO83NDB2V0 | L4 | IO298PDB7V3 | M10 | VCCIB7 |
| J29 | IO91PDB2V1 | L5 | IO283PDB7V1 | M11 | VCC |
| J30 | IO91NDB2V1 | L6 | IO291NDB7V2 | M12 | GND |
| K1 | IO288NDB7V1 | L7 | IO291PDB7V2 | M13 | GND |
| K2 | IO288PDB7V1 | L8 | IO293PDB7V2 | M14 | GND |
| K3 | IO304NDB7V3 | L9 | IO293NDB7V2 | M15 | GND |
| K4 | IO304PDB7V3 | L10 | IO307NPB7V4 | M16 | GND |
| K5 | GAB2/IO308PDB7V4 | L11 | VCC | M17 | GND |
| K6 | IO308NDB7V4 | L12 | VCC | M18 | GND |
| K7 | IO301PDB7V3 | L13 | VCC | M19 | GND |
| K8 | IO301NDB7V3 | L14 | VCC | M20 | VCC |
| K9 | GAC2/IO307PPB7V4 | L15 | VCC | M21 | VCCIB2 |
| K10 | VCC | L16 | VCC | M22 | NC |

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| M23 | IO104PPB2V2 | N29 | IO107PDB2V3 | R5 | GFB0/IO274NPB7V0 |
| M24 | IO102PDB2V2 | N30 | IO107NDB2V3 | R6 | IO271NDB6V4 |
| M25 | IO102NDB2V2 | P1 | IO276NDB7V0 | R7 | GFB2/IO271PDB6V4 |
| M26 | IO95PDB2V1 | P2 | IO278NDB7V0 | R8 | IO269PDB6V4 |
| M27 | IO97NDB2V1 | P3 | IO280NDB7V0 | R9 | IO269NDB6V4 |
| M28 | IO101NDB2V2 | P4 | IO284NDB7V1 | R10 | VCCIB7 |
| M29 | IO103NDB2V2 | P5 | IO279NDB7V0 | R11 | VCC |
| M30 | IO119PDB3V0 | P6 | GFC1/IO275PDB7V0 | R12 | GND |
| N1 | IO276PDB7V0 | P7 | GFC0/IO275NDB7V0 | R13 | GND |
| N2 | IO278PDB7V0 | P8 | IO277PDB7V0 | R14 | GND |
| N3 | IO280PDB7V0 | P9 | IO277NDB7V0 | R15 | GND |
| N4 | IO284PDB7V1 | P10 | VCCIB7 | R16 | GND |
| N5 | IO279PDB7V0 | P11 | VCC | R17 | GND |
| N6 | IO285NDB7V1 | P12 | GND | R18 | GND |
| N7 | IO287NDB7V1 | P13 | GND | R19 | GND |
| N8 | IO281NDB7V0 | P14 | GND | R20 | VCC |
| N9 | IO281PDB7V0 | P15 | GND | R21 | VCCIB2 |
| N10 | VCCIB7 | P16 | GND | R22 | GCC0/IO112NDB2V3 |
| N11 | VCC | P17 | GND | R23 | GCB2/IO116PDB3V0 |
| N12 | GND | P18 | GND | R24 | IO118PDB3V0 |
| N13 | GND | P19 | GND | R25 | IO111PPB2V3 |
| N14 | GND | P20 | VCC | R26 | IO122PPB3V1 |
| N15 | GND | P21 | VCCIB2 | R27 | GCA0/IO114NPB3V0 |
| N16 | GND | P22 | GCC1/IO112PDB2V3 | R28 | VCOMPLC |
| N17 | GND | P23 | IO110PDB2V3 | R29 | GCB1/IO113PPB2V3 |
| N18 | GND | P24 | IO110NDB2V3 | R30 | IO115NPB3V0 |
| N19 | GND | P25 | IO109PPB2V3 | T1 | IO270NDB6V4 |
| N20 | VCC | P26 | IO111NPB2V3 | T2 | VCCPLF |
| N21 | VCCIB2 | P27 | IO105PDB2V2 | T3 | GFA2/IO272PPB6V4 |
| N22 | IO106NDB2V3 | P28 | IO105NDB2V2 | T4 | GFA1/IO273PDB6V4 |
| N23 | IO106PDB2V3 | P29 | GCC2/IO117PDB3V0 | T5 | IO272NPB6V4 |
| N24 | IO108PDB2V3 | P30 | IO117NDB3V0 | T6 | IO267NDB6V4 |
| N25 | IO108NDB2V3 | R1 | GFC2/IO270PDB6V4 | T7 | IO267PDB6V4 |
| N26 | IO95NDB2V1 | R2 | GFB1/IO274PPB7V0 | T8 | IO265PDB6V3 |
| N27 | IO99NDB2V2 | R3 | VCOMPLF | T9 | IO263PDB6V3 |
| N28 | IO99PDB2V2 | R4 | GFA0/IO273NDB6V4 | T10 | VCCIB6 |

Package Pin Assignments

| FG896 | | FG896 | | FG896 | |
|------------|-------------------|------------|-------------------|------------|-------------------|
| Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function | Pin Number | A3PE3000 Function |
| T11 | VCC | U17 | GND | V23 | IO128NDB3V1 |
| T12 | GND | U18 | GND | V24 | IO132PDB3V2 |
| T13 | GND | U19 | GND | V25 | IO130PPB3V2 |
| T14 | GND | U20 | VCC | V26 | IO126NDB3V1 |
| T15 | GND | U21 | VCCIB3 | V27 | IO129NDB3V1 |
| T16 | GND | U22 | IO120PDB3V0 | V28 | IO127NDB3V1 |
| T17 | GND | U23 | IO128PDB3V1 | V29 | IO125NDB3V1 |
| T18 | GND | U24 | IO124PDB3V1 | V30 | IO123PDB3V1 |
| T19 | GND | U25 | IO124NDB3V1 | W1 | IO266NDB6V4 |
| T20 | VCC | U26 | IO126PDB3V1 | W2 | IO262NDB6V3 |
| T21 | VCCIB3 | U27 | IO129PDB3V1 | W3 | IO260NDB6V3 |
| T22 | IO109NPB2V3 | U28 | IO127PDB3V1 | W4 | IO252NDB6V2 |
| T23 | IO116NDB3V0 | U29 | IO125PDB3V1 | W5 | IO251NDB6V2 |
| T24 | IO118NDB3V0 | U30 | IO121NDB3V0 | W6 | IO251PDB6V2 |
| T25 | IO122NPB3V1 | V1 | IO268NDB6V4 | W7 | IO255NDB6V2 |
| T26 | GCA1/IO114PPB3V0 | V2 | IO262PDB6V3 | W8 | IO249PPB6V1 |
| T27 | GCB0/IO113NPB2V3 | V3 | IO260PDB6V3 | W9 | IO253PDB6V2 |
| T28 | GCA2/IO115PPB3V0 | V4 | IO252PDB6V2 | W10 | VCCIB6 |
| T29 | VCCPLC | V5 | IO257NPB6V2 | W11 | VCC |
| T30 | IO121PDB3V0 | V6 | IO261NPB6V3 | W12 | GND |
| U1 | IO268PDB6V4 | V7 | IO255PDB6V2 | W13 | GND |
| U2 | IO264NDB6V3 | V8 | IO259PDB6V3 | W14 | GND |
| U3 | IO264PDB6V3 | V9 | IO259NDB6V3 | W15 | GND |
| U4 | IO258PDB6V3 | V10 | VCCIB6 | W16 | GND |
| U5 | IO258NDB6V3 | V11 | VCC | W17 | GND |
| U6 | IO257PPB6V2 | V12 | GND | W18 | GND |
| U7 | IO261PPB6V3 | V13 | GND | W19 | GND |
| U8 | IO265NDB6V3 | V14 | GND | W20 | VCC |
| U9 | IO263NDB6V3 | V15 | GND | W21 | VCCIB3 |
| U10 | VCCIB6 | V16 | GND | W22 | IO134PDB3V2 |
| U11 | VCC | V17 | GND | W23 | IO138PDB3V3 |
| U12 | GND | V18 | GND | W24 | IO132NDB3V2 |
| U13 | GND | V19 | GND | W25 | IO136NPB3V2 |
| U14 | GND | V20 | VCC | W26 | IO130NPB3V2 |
| U15 | GND | V21 | VCCIB3 | W27 | IO141PDB3V3 |
| U16 | GND | V22 | IO120NDB3V0 | W28 | IO135PDB3V2 |

| FG896 | |
|-------------------|--------------------------|
| Pin Number | A3PE3000 Function |
| W29 | IO131PDB3V2 |
| W30 | IO123NDB3V1 |
| Y1 | IO266PDB6V4 |
| Y2 | IO250PDB6V2 |
| Y3 | IO250NDB6V2 |
| Y4 | IO246PDB6V1 |
| Y5 | IO247NDB6V1 |
| Y6 | IO247PDB6V1 |
| Y7 | IO249NPB6V1 |
| Y8 | IO245PDB6V1 |
| Y9 | IO253NDB6V2 |
| Y10 | GEB0/IO235NPB6V0 |
| Y11 | VCC |
| Y12 | VCC |
| Y13 | VCC |
| Y14 | VCC |
| Y15 | VCC |
| Y16 | VCC |
| Y17 | VCC |
| Y18 | VCC |
| Y19 | VCC |
| Y20 | VCC |
| Y21 | IO142PPB3V3 |
| Y22 | IO134NDB3V2 |
| Y23 | IO138NDB3V3 |
| Y24 | IO140NDB3V3 |
| Y25 | IO140PDB3V3 |
| Y26 | IO136PPB3V2 |
| Y27 | IO141NDB3V3 |
| Y28 | IO135NDB3V2 |
| Y29 | IO131NDB3V2 |
| Y30 | IO133PDB3V2 |

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the ProASIC3E datasheet.

Table 1 •

| Revision | Changes | Page |
|---------------------------------|---|--------------|
| Revision 16 (November 2019) | Updated the template change with Microchip-Microsemi logo across the document. | NA |
| | Removed PQ208 from the A3PE600 device and its related information across the document. | NA |
| Revision 15 (June 2015) | Updated " ProASIC3E Ordering Information ". Interchanged the positions of Y-Security Feature and I- Application (Temperature Range) (SAR 67296). Added Note "Only devices with package size greater than or equal to 5x5 are supported". Updated Commercial and Industrial Junction Temperatures (SAR 67588). | 1-III |
| | Added the A3PE3000 package to Table 2-5 (SARs 52320 and 58737). | 2-5 |
| | Updated " VCCIBx I/O Supply Voltage " (SAR 43323). | 3-1 |
| | | |
| Revision 14 (May 2014) | Added 2 mA and 6 mA I/O short currents values in " I/O Short Currents IOSH/IOSL " (SAR 56295). | 2-23 2-25 |
| | Added 2 mA and 6 mA minimum and maximum DC input and output levels in " Minimum and Maximum DC Input and Output Levels "(SAR 56295). | 2-26 2-26 |
| | Added 3.3 V LVTTTL / 3.3 V LVCMOS High Slew Commercial-Case Conditions for 2 mA and 6 mA in " 3.3 V LVTTTL / 3.3 V LVCMOS High Slew " (SAR 56295). | |
| | Added 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew Commercial-Case Conditions for 2 mA and 6 mA in " 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew " (SAR 56295). | |
| Revision 13 (January 2013) | In the " Features and Benefits " section, updated the Clock Conditioning Circuit (CCC) and PLL Wide Input Frequency Range from '1.5 MHz to 200 MHz' to '1.5MHz to 350 MHz' based on Table 2-98 (SAR 22196). | 1-1 |
| | The " ProASIC3E Ordering Information " section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43220). | 1-III |
| | Added a note to " Recommended Operating Conditions ¹ " table (SAR 42716): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to $85^{\circ}C$. | 2-2 |
| | The note in " ProASIC3E CCC/PLL Specification " table referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42571). | 2-73 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40285). Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 12 (September 2012) | The " Security " section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-1 |

Table 1 •

| Revision | Changes | Page |
|---|--|---|
| Revision 11 (August 2012) | Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions ¹ (SAR 38322). | 2-1 3-1 2-1 |
| | The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924): "Summary of Maximum and Minimum DC Input and Output Levels" table "Summary of I/O Timing Characteristics—Software Default Settings" table "I/O Output Buffer Maximum Resistances ¹ " table "Minimum and Maximum DC Input and Output Levels" table "Minimum and Maximum DC Input and Output Levels" table Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714). | 2-17 2-20 2-21 2-40 2-42 |
| | "Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934). | 2-23 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796): "It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error. | 2-31 |
| | Revision 11 (continued) | Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889). |
| In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222). | | 2-54 |
| Figure 2-47 and Figure 2-48 are new (SAR 34848). | | 2-82 |
| The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | | 3-1 |

Table 1 •

| Revision | Changes | Page |
|-----------------------------|---|------------|
| Revision 10 (March 2012) | The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34669). | I, 1-1 |
| | The Y security option and Licensed DPA Logo were added to the "ProASIC3E Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34727). | III |
| | The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface" (SAR 34689). | 1-3 |
| | The "Specifying I/O States During Programming" section is new (SAR 34699). | 1-6 |
| | VCCPLL in Table 2-2 • Recommended Operating Conditions ¹ was corrected from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 33851). The T _J symbol was added to the table and notes regarding T _A and T _J were removed. The second of two parameters in the VCCI and VMV row, called "3.3 V DC supply voltage," was corrected to "3.0 V DC supply voltage" (SAR 37227). | 2-2 |
| | The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P _{CLOCK} " section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the <i>ProASIC3E FPGA Fabric User's Guide</i> (SAR 34735). | 2-10 |
| | t _{DOUT} was corrected to t _{DIN} in Figure 2-3 • Input Buffer Timing Model and Delays (example) (SAR 37109). | 2-14 |
| | The typo related to the values for 3.3 V LVCMOS Wide Range in Table 2-17 • Summary of I/O Timing Characteristics—Software Default Settings was corrected (SAR 37227). | 2-20 |
| | The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section and "3.3 V LVCMOS Wide Range" section and tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 μA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34763). | 2-19, 2-28 |

Table 1 •

| Revision | Changes | Page |
|----------------------------|--|--|
| Revision 10 (continued) | <p>"TBD" for 3.3 V LVCMOS Wide Range in Table 2-19 • I/O Output Buffer Maximum Resistances¹ and Table 2-21 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33853).</p> <p>3.3 V LVCMOS Wide Range information was separated from regular 3.3 V LVCMOS and placed into its own new section, "3.3 V LVCMOS Wide Range". Values of IOSH and IOSL were added in Table 2-29 • Minimum and Maximum DC Input and Output Levels (SAR 33853).</p> <p>The formulas in the table notes for Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34755).</p> <p>The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).</p> <p>The titles and subtitles for Table 2-31 • 3.3 V LVCMOS Wide Range High Slew and Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew were corrected (SAR 37227).</p> <p>The following notes were removed from Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34812): $\pm 5\%$ Differential input voltage = ± 350 mV</p> <p>Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36957).</p> <p>A note was added to Table 2-98 • ProASIC3E CCC/PLL Specification indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34824).</p> <p>The following figures were deleted. Reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs, which covers these cases in detail (SAR 34872). Figure 2-44 • Write Access after Write onto Same Address Figure 2-45 • Read Access after Write onto Same Address Figure 2-46 • Write Access after Read onto Same Address</p> <p>The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-49 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35750).</p> <p>The "Pin Descriptions and Packaging" chapter is new (SAR 34771).</p> <p>Package names used in the "Package Pin Assignments" section were revised to match standards given in Package Mechanical Drawings (SAR 34771).</p> <p>Pin E6 for the FG256 package was corrected from VvB0 to VCCIB0 (SARs 30364, 31597, 26243).</p> | <p>2-21, 2-28</p> <p>2-22</p> <p>2-25</p> <p>2-29, 2-30</p> <p>2-52</p> <p>2-71</p> <p>2-73</p> <p>2-77, 2-78, 2-82, 2-85</p> <p>3-1</p> <p>4-1</p> <p>4-9</p> |
| July 2010 | <p>The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3E Device Status" table on page II indicates the status for each device in the device family.</p> | N/A |

| Revision | Changes | Page | | | | | | | | | | | | | | |
|---|--|---|-------------------|-----|------------|-----|------------|----|-------------|----|-------------|----|------------------|----|-------------|------|
| Revision 9 (Aug 2009) Product Brief v1.2 | All references to speed grade –F have been removed from this document. | N/A | | | | | | | | | | | | | | |
| DC and Switching Characteristics v1.3 | The "Pro I/Os with Advanced I/O Standards" section was revised to add definitions of hot-swap and cold-sparing. | 1-6 | | | | | | | | | | | | | | |
| | 3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data. | N/A | | | | | | | | | | | | | | |
| | IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables. | N/A | | | | | | | | | | | | | | |
| | –F was removed from the datasheet. The speed grade is no longer supported. | N/A | | | | | | | | | | | | | | |
| | In the Table 2-2 • Recommended Operating Conditions ¹ "3.0 V DC supply voltage" and note 4 are new. | 2-2 | | | | | | | | | | | | | | |
| | The Table 2-4 • Overshoot and Undershoot Limits ¹ table was updated. | 2-3 | | | | | | | | | | | | | | |
| | The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated. | 2-6 | | | | | | | | | | | | | | |
| | There are new parameters and data was updated in the Table 2-99 • RAM4K9 table. | 2-79 | | | | | | | | | | | | | | |
| There are new parameters and data was updated in the Table 2-100 • RAM512X18 table. | 2-80 | | | | | | | | | | | | | | | |
| Revision 8 (Feb 2008) Product Brief v1.1 | Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new. | 1-II | | | | | | | | | | | | | | |
| Revision 7 (Jun 2008) DC and Switching Characteristics v1.2 | The title of Table 2-4 • Overshoot and Undershoot Limits ¹ was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted. | 2-3 | | | | | | | | | | | | | | |
| | Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated. | 2-52 | | | | | | | | | | | | | | |
| Revision 6 (Jun 2008) | The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table. | 4-25 | | | | | | | | | | | | | | |
| Revision 5 (Jun 2008) Packaging v1.4 | The naming conventions changed for the following pins in the "FG484" for the A3PE600: <table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;">Pin Number</th> <th style="text-align: left;">New Function Name</th> </tr> </thead> <tbody> <tr> <td>J19</td> <td>IO45PPB2V1</td> </tr> <tr> <td>K20</td> <td>IO45NPB2V1</td> </tr> <tr> <td>M2</td> <td>IO114NPB6V1</td> </tr> <tr> <td>N1</td> <td>IO114PPB6V1</td> </tr> <tr> <td>N4</td> <td>GFC2/IO115PPB6V1</td> </tr> <tr> <td>P3</td> <td>IO115NPB6V1</td> </tr> </tbody> </table> | Pin Number | New Function Name | J19 | IO45PPB2V1 | K20 | IO45NPB2V1 | M2 | IO114NPB6V1 | N1 | IO114PPB6V1 | N4 | GFC2/IO115PPB6V1 | P3 | IO115NPB6V1 | 4-20 |
| Pin Number | New Function Name | | | | | | | | | | | | | | | |
| J19 | IO45PPB2V1 | | | | | | | | | | | | | | | |
| K20 | IO45NPB2V1 | | | | | | | | | | | | | | | |
| M2 | IO114NPB6V1 | | | | | | | | | | | | | | | |
| N1 | IO114PPB6V1 | | | | | | | | | | | | | | | |
| N4 | GFC2/IO115PPB6V1 | | | | | | | | | | | | | | | |
| P3 | IO115NPB6V1 | | | | | | | | | | | | | | | |
| Revision 4 (Apr 2008) Product Brief v1.0 | The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | N/A | | | | | | | | | | | | | | |
| | Packaging v1.3 | The "FG324" package diagram was replaced. | 4-10 | | | | | | | | | | | | | |

| Revision | Changes | Page |
|---|--|-----------|
| Revision 3 (Apr 2008) Packaging v1.2 | The following pins had duplicates and the extra pins were deleted from the "PQ208" A3PE3000 table: 36, 62, 171 Note: There were no pin function changes in this update. | 4-2 |
| | The following pins had duplicates and the extra pins were deleted from the "FG324" table: E2, E3, E16, E17, P2, P3, T16, U17 Note: There were no pin function changes in this update. | 4-10 |
| | The "FG256" pin table was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version. | 4-7 |
| | The "FG484" was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version. | 4-20 |
| | The following pins had duplicates and the extra pins were deleted from the "FG896" table: AD6, AE5, AE28, AF29, F5, F26, G6, G25 Note: There were no pin function changes in this update. | 4-39 |
| Revision 2 (Mar 2008) Product Brief rev. 1 | The FG324 package was added to the "ProASIC3E Product Family" table, the "I/Os Per Package1" table, and the "Temperature Grade Offerings" table for A3PE3000. | I, II, IV |
| Revision 1 (Feb 2008) DC and Switching Characteristics v1.1 | In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature 1 , Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2 |
| | The " PLL Behavior at Brownout Condition " section is new. | 2-4 |
| | In the " PLL Contribution—PPLL " section, the following was deleted: FCLKIN is the input clock frequency. | 2-11 |
| | In Table 2-14 • Summary of Maximum and Minimum DC Input Levels , the note was incorrect. It previously said T _J and it was corrected and changed to T _A . | 2-18 |
| | In Table 2-98 • ProASIC3E CCC/PLL Specification , the SCLK parameter and note 1 are new. | 2-73 |
| | Table 2-103 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-83 |
| Revision 1 (cont'd) Packaging v1.1 | The "PQ208" pin table for A3PE3000 was updated. | 4-2 |
| | The "FG324" pin table for A3PE3000 is new. | 4-11 |
| | The "FG484" pin table for A3PE3000 is new. | 4-15 |
| | The "FG896" pin table for A3PE3000 is new. | 4-39 |
| Revision 0 (Jan 2008) | This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0. | N/A |
| v2.1 (July 2007) | CoreMP7 information was removed from the " Features and Benefits " section. | 1-1 |
| | The M1 device part numbers have been updated in ProASIC3E Product Family, "Packaging Tables", "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix". | 1-1 |

| Revision | Changes | Page |
|---|--|------|
| v2.1 (continued) | The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections. | 1-1 |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | 1-1 |
| | The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)." | 2-9 |
| | The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added. | 3-2 |
| | The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up. | 2-15 |
| v2.0 (April 2007) | In the "Temperature Grade Offerings" section, Ambient was deleted. | iii |
| | Ambient was deleted from "Temperature Grade Offerings". | iii |
| | Ambient was deleted from the "Speed Grade and Temperature Grade Matrix". | iv |
| | The "PLL Macro" section was updated to include power-up information. | 2-15 |
| | Table 2-13 • ProASIC3E CCC/PLL Specification was updated. | 2-30 |
| | Figure 2-19 • Peak-to-Peak Jitter Definition is new. | 2-18 |
| | The "SRAM and FIFO" section was updated with operation and timing requirement information. | 2-21 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled. | 2-28 |
| | In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4. | 2-34 |
| | Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated. | 2-64 |
| | Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7. | 2-40 |
| | The "VCCPLF PLL Supply Voltage" section was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" section was updated. | 2-50 |
| | The "GL Globals" section was updated to include information about direct input into quadrant clocks. | 2-51 |
| | VJTAG was deleted from the "TCK Test Clock" section. | 2-51 |
| | In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated. | 2-51 |
| | Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45". | 3-2 |
| | Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os). | 3-2 |
| In EQ 3-2, 150 was changed to 110 and the result changed to 5.88. | 3-5 | |

| Revision | Changes | Page |
|--|---|--------------|
| v2.0 (continued) | Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated. | 3-5 |
| | Table 3-5 • Package Thermal Resistivities was updated. | 3-5 |
| | Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated. | 3-8 |
| | t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18. | 3-74 to 3-74 |
| | The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated. | 3-23 |
| | Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new. | 3-71 to 3-73 |
| | Figure 3-53 • Timing Diagram was updated. | 3-80 |
| | Notes were added to the package diagrams identifying if they were top or bottom view. | N/A |
| | The A3PE1500 "208-Pin PQFP" table is new. | 4-4 |
| | The A3PE1500 "484-Pin FBGA" table is new. | 4-18 |
| | The A3PE1500 "A3PE1500 Function" table is new. | 4-24 |
| Advance v0.6 (January 2007) | In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages. | ii |
| Advance v0.5 (April 2006) | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-8 • Very-Long-Line Resources was updated. | 2-8 |
| | The footnotes in Figure 2-27 • CCC/PLL Macro were updated. | 2-28 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-8 • Very-Long-Line Resources was updated. | 2-8 |
| | The footnotes in Figure 2-27 • CCC/PLL Macro were updated. | 2-28 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| The "WCLK and RCLK" section was updated. | 2-25 | |

| Revision | Changes | Page |
|-----------------------------|--|------|
| Advance v0.5 (continued) | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | The "Introduction" of the "Introduction" section was updated. | 2-28 |
| | PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards | 2-29 |
| | Table 2-35 • ProASIC3E I/O Features was updated. | 2-54 |
| | The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature. | 2-32 |
| | The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information. | 2-35 |
| | Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices. | 2-64 |
| | The notes in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices were updated. | 2-64 |
| | The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new. | 2-41 |
| | A footnote was added to Table 2-37 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in ProASIC3E Devices (maximum drive strength and high slew selected). | 2-55 |
| | Table 2-48 • ProASIC3E I/O Attributes vs. I/O Standard Applications | 2-81 |
| | Table 2-55 • ProASIC3 I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings | 2-85 |
| | The "x" was updated in the "Pin Descriptions" section. | 2-50 |
| | The "VCC Core Supply Voltage" pin description was updated. | 2-50 |
| | The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected. | 2-50 |
| | EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-13 • ProASIC3E CCC/PLL Specification. | 2-30 |
| | EXTFB was removed from Figure 2-27 • CCC/PLL Macro. | 2-28 |
| | The LVPECL specification in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated. | 2-64 |
| | Table 2-15 • Levels of Hot-Swap Support was updated. | 2-34 |
| | The "Cold-Sparing Support" section was updated. | 2-34 |
| | "Electrostatic Discharge (ESD) Protection" section was updated. | 2-35 |
| | The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section. | 2-50 |
| | The "VJTAG JTAG Supply Voltage" pin description was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground. | 2-50 |

| Revision | Changes | Page |
|--------------------------------|--|----------------------|
| Advance v0.5 (continued) | The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused. | 2-50 |
| | The "JTAG Pins" section was updated to include information on what happens when the pin is unused. | 2-51 |
| | The "Programming" section was updated to include information concerning serialization. | 2-53 |
| | The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information. | 2-54 |
| | The "DC and Switching Characteristics" chapter was updated with new information. | Starting on page 3-1 |
| | Table 3-6 was updated. | 3-5 |
| | In Table 3-10, PAC4 was updated. | 3-8 |
| | Table 3-19 was updated. | 3-20 |
| | The note in Table 3-24 was updated. | 3-23 |
| | All Timing Characteristics tables were updated from LVTTL to Register Delays | 3-26 to 3-64 |
| | The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated. | 3-74 to 3-79 |
| | F_{TCKMAX} was updated in Table 3-98. | 3-80 |
| Advance v0.4 (October 2005) | The "Packaging Tables" table was updated. | ii |
| Advance v0.3 | Figure 2-11 was updated. | 2-9 |
| | The "Clock Resources (VersaNets)" section was updated. | 2-9 |
| | The "VersaNet Global Networks and Spine Access" section was updated. | 2-9 |
| | The "PLL Macro" section was updated. | 2-15 |
| | Figure 2-27 was updated. | 2-28 |
| | Figure 2-20 was updated. | 2-19 |
| | Table 2-5 was updated. | 2-25 |
| | Table 2-6 was updated. | 2-25 |
| | The "FIFO Flag Usage Considerations" section was updated. | 2-27 |
| | Table 2-33 was updated. | 2-51 |
| | Figure 2-24 was updated. | 2-31 |
| | The "Cold-Sparing Support" section is new. | 2-34 |
| | Table 2-45 was updated. | 2-64 |
| | Table 2-48 was updated. | 2-81 |
| | Pin descriptions in the "JTAG Pins" section were updated. | 2-51 |
| | The "Pin Descriptions" section was updated. | 2-50 |
| | Table 3-7 was updated. | 3-6 |

| Revision | Changes | Page |
|-----------------------------|--|------|
| Advance v0.3 (continued) | The "Methodology" section was updated. | 3-9 |
| | The A3PE3000 "208-Pin PQFP" pin table was updated. | 4-6 |

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "[ProASIC3E Device Status](#)" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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