



# RF Power LDMOS Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

This 63 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2300 to 2400 MHz.

### 2300 MHz

- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 30$  Vdc,  $I_{DQA} = 500$  mA,  $V_{GSB} = 0.7$  Vdc,  $P_{out} = 63$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

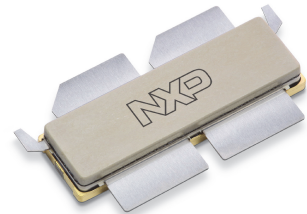
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
2300 MHz	15.6	49.3	8.4	-30.1
2350 MHz	16.1	48.7	8.5	-31.9
2400 MHz	16.1	48.0	8.2	-32.7

### Features

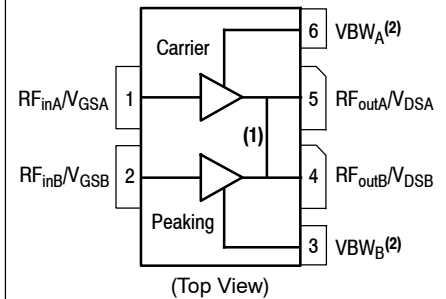
- Advanced high performance in-package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate-source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for digital predistortion error correction systems

**A3T23H300W23SR6**

**2300–2400 MHz, 63 W AVG., 30 V  
 AIRFAST RF POWER LDMOS  
 TRANSISTOR**



**ACP-1230S-4L2S**



**Figure 1. Pin Connections**

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device can operate with  $V_{DD}$  current supplied through pin 3 and pin 6.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +150	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ when DC current is fed through pin 3 and pin 6 Derate above $25^\circ\text{C}$	CW	180 1.2	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature $73^\circ\text{C}$ , 63 W Avg., W-CDMA, 30 Vdc, $I_{DQA} = 500\text{ mA}$ , $V_{GSB} = 0.7\text{ Vdc}$ , 2350 MHz	$R_{\theta JC}$	0.17	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics (4)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	5	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics - Side A, Carrier**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 140\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage ( $V_{DD} = 30\text{ Vdc}$ , $I_{DA} = 500\text{ mAdc}$ , Measured in Functional Test)	$V_{GSA(Q)}$	2.2	2.6	3.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.4\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

**On Characteristics - Side B, Peaking**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 320\ \mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.2\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1,2,3)</sup> (In NXP Doherty Test Fixture, 50 ohm system) $V_{DD} = 30\text{ Vdc}$ , $I_{DQA} = 500\text{ mA}$ , $V_{GSB} = 0.7\text{ Vdc}$ , $P_{out} = 63\text{ W Avg.}$ , $f = 2300\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	14.4	15.6	16.8	dB
Drain Efficiency	$\eta_D$	46.7	49.3	—	%
$P_{out}$ @ 3 dB Compression Point, CW	P3dB	55.3	56.2	—	dBm
Adjacent Channel Power Ratio	ACPR	—	-29.0	-26.0	dBc

**Load Mismatch** <sup>(3)</sup> (In NXP Doherty Test Fixture, 50 ohm system)  $I_{DQA} = 500\text{ mA}$ ,  $V_{GSB} = 0.7\text{ Vdc}$ ,  $f = 2350\text{ MHz}$ , 12  $\mu\text{sec(on)}$ , 10% Duty Cycle

VSWR 10:1 at 32 Vdc, 360 W Pulsed CW Output Power (3 dB Input Overdrive from 210 W Pulsed CW Rated Power)	No Device Degradation
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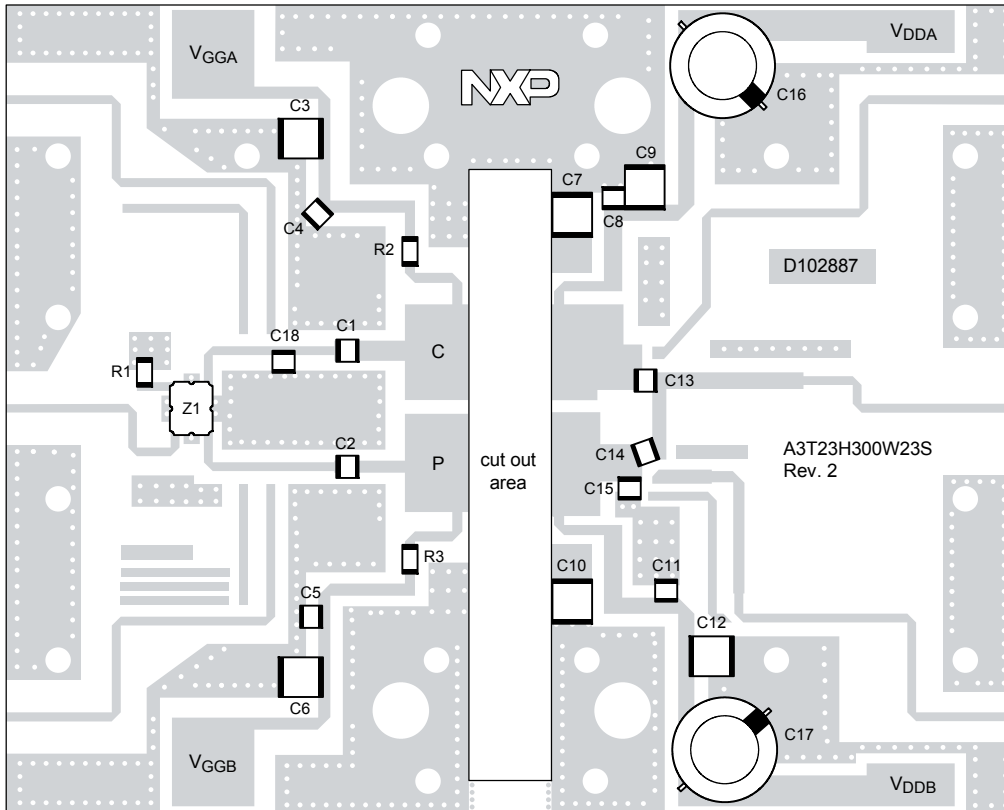
**Typical Performance** <sup>(3)</sup> (In NXP Doherty Test Fixture, 50 ohm system)  $V_{DD} = 30\text{ Vdc}$ ,  $I_{DQA} = 500\text{ mA}$ ,  $V_{GSB} = 0.7\text{ Vdc}$ , 2300–2400 MHz Bandwidth

$P_{out}$ @ 3 dB Compression Point <sup>(4)</sup>	P3dB	—	410	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300–2400 MHz bandwidth)	$\Phi$	—	-18	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	230	—	MHz
Gain Flatness in 100 MHz Bandwidth @ $P_{out} = 63\text{ W Avg.}$	$G_F$	—	0.4	—	dB
Gain Variation over Temperature (-40°C to +85°C)	$\Delta G$	—	0.007	—	dB/°C
Output Power Variation over Temperature (-40°C to +85°C)	$\Delta P_{1dB}$	—	0.003	—	dB/°C

**Table 5. Ordering Information**

Device	Tape and Reel Information	Package
A3T23H300W23SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	ACP-1230S-4L2S

- $V_{DDA}$  and  $V_{ddb}$  must be tied together and powered by a single DC power supply.
- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- P3dB =  $P_{avg} + 7.0\text{ dB}$  where  $P_{avg}$  is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note:  $V_{DDA}$  and  $V_{DDB}$  must be tied together and powered by a single DC power supply.

aaa-030921

**Figure 2. A3T23H300W23SR6 Test Circuit Component Layout**

**Table 6. A3T23H300W23SR6 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C2, C4, C5, C8, C11, C14	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C3, C6, C7, C9, C10, C12	10 $\mu$ F Chip Capacitor	C5750X7S2A106M230KB	TDK
C13	3.3 pF Chip Capacitor	ATC100B3R3CT500XT	ATC
C15	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C16, C17	470 $\mu$ F, 63 V Electrolytic Capacitor	MCGPR63V477M13X26	Multicomp
C18	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
R1	50 $\Omega$ , 30 W Termination Resistor	RFP-375375N6Z50-2	Anaren
R2, R3	3.6 $\Omega$ , 1/4 W Chip Resistor	CRCW12063R60FKEA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D102887	MTL

### PACKAGE DIMENSIONS



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	STANDARD: NON-JEDEC	
	SOT1800-4	21 JUN 2017

A3T23H300W23SR6

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

5. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

6. DATUM H IS LOCATED AT THE BOTTOM OF THE LEAD FRAME AND IS COINCIDENT WITH THE LEAD WHERE THE LEADS EXIT THE PLASTIC BODY.

7. DIMENSIONS M AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .012 INCH (0.30 MM) PER SIDE. DIMENSIONS M AND S DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

8. DIMENSIONS D, U AND K DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .010 INCH (0.25 MM) TOTAL IN EXCESS OF THE D, U AND K DIMENSION AT MAXIMUM MATERIAL CONDITION.

9. DATUM A AND B TO BE DETERMINED AT DATUM T.

DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	U	.035	.045	0.89	1.14
CC	.160	.190	4.06	4.83	V1	.640	.655	16.26	16.64
D	.455	.465	11.56	11.81	W1	.105	.115	2.67	2.92
E	.062	.069	1.57	1.75	W2	.135	.145	3.43	3.68
F	.004	.007	0.10	0.18	W3	.245	.255	6.22	6.48
H1	.082	.090	2.08	2.29	W4	.265	.281	6.73	7.14
H2	.078	.094	1.98	2.39	Y	0.695 BSC		17.65 BSC	
K	.175	.195	4.45	4.95	Z1	R.000	R.040	R0.00	R1.02
L	0.270 BSC		6.86 BSC		Z2	.060	.100	1.52	2.54
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
N	1.218	1.242	30.94	31.55	bbb	.010		0.25	
R	.365	.375	9.27	9.53	ccc	.020		0.51	

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REV: A

STANDARD: NON-JEDEC

SOT1800-4

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## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- .s2p File

### Development Tools

- Printed Circuit Boards

### To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2018	<ul style="list-style-type: none"><li>• Initial release of data sheet</li></ul>