A5931

Three-Phase Sensorless Fan Driver IC

FEATURES AND BENEFITS

- AEC-Q100 qualified (K version)
- Closed-loop speed control
- Speed curve configuration via EEPROM
- I^2C serial port
- Sinusoidal modulation for reduced audible noise and low vibration
- Sensorless (no Hall sensors required)
- Low $R_{DS(ON)}$ power MOSFETs—3 A capability
- Minimal external components
- PWM speed input
- FG speed output
- RD rotor lock output
- Lock detection
- Soft start
- Standby mode
- Shorted load protection

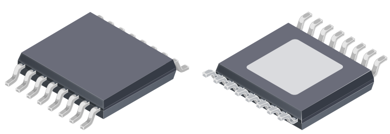
DESCRIPTION

The A5931 three-phase motor driver IC incorporates sensorless sinusoidal drive to minimize vibration for high speed server fans. Sensorless control eliminates the requirement for Hall sensors for server fan applications.

A flexible closed-loop speed control system is integrated into the IC. EEPROM is used to tailor the common functions of the fan speed curve to a specific application. This eliminates the requirement for a microprocessor-based system and minimizes programming requirements.

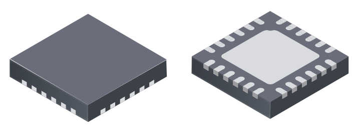
The A5931 is available in a 24-contact 4 mm × 4 mm QFN with exposed thermal pad (suffix ES), and a 16-lead TSSOP with exposed thermal pad (suffix LP). These packages are lead (Pb) free, with 100% matte-tin leadframe plating.

PACKAGES:



16-lead TSSOP
with exposed thermal pad
(LP package)

Not to scale



24-contact QFN
with exposed thermal pad
4 mm × 4 mm × 0.75 mm
(ES package)

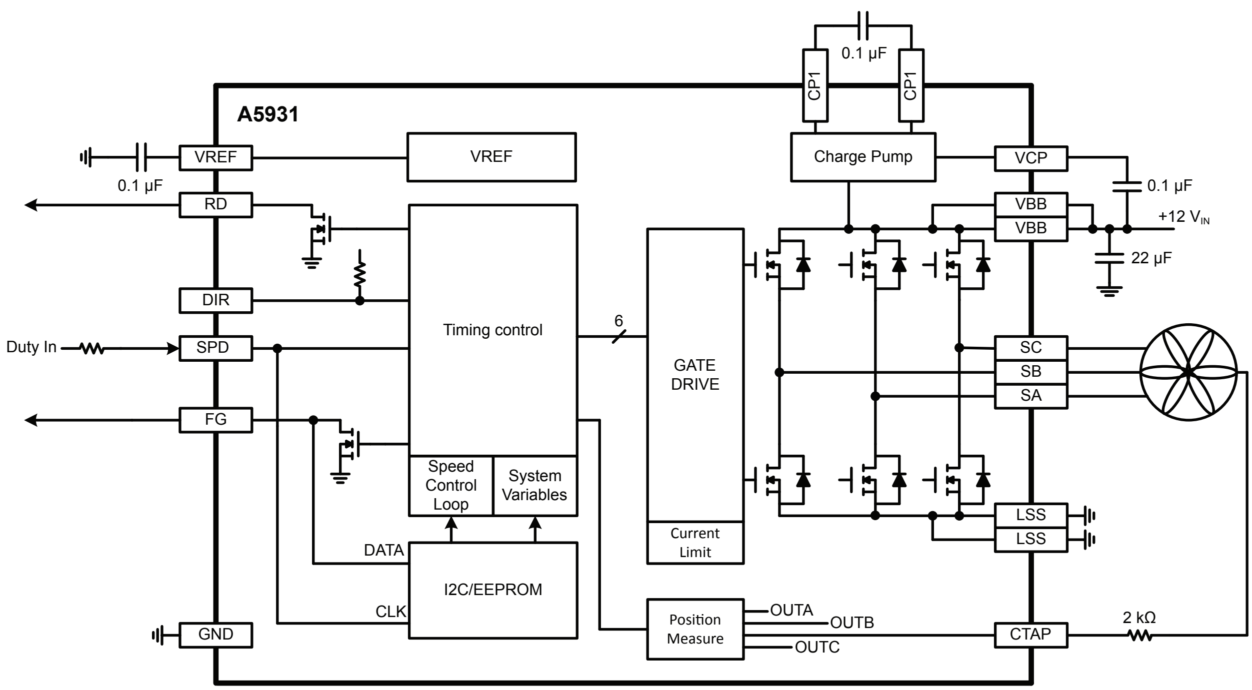


Figure 1: Typical Application

SPECIFICATIONS

SELECTION GUIDE

Part Number	Operating Temperature Range (T_A) (°C)	Packaging	Packing
A5931GESTR-T	–40 to 105	24-contact QFN with exposed thermal pad	1500 pieces per 7-inch reel
A5931GLPTR-T	–40 to 105	16-lead TSSOP with exposed thermal pad	4000 pieces per 13-inch reel
A5931KLPTR-T	–40 to 125	16-lead TSSOP with exposed thermal pad	4000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}	DC	18	V
		t_w < 10 ms	20	V
Logic Input Voltage Range	V_{IN}	SPD, DIR	–0.3 to 6	V
Logic Output	V_O	FG, RD	V_{BB}	V
Output Current	I_{OUT}		internally limited	A
Output Voltage	V_{OUT}		V_{BB} + 1	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C
		Range K	–40 to 125	°C

RECOMMENDED OPERATIONAL RANGE

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Supply Voltage	V_{BB}	DC	5	12	16	V
Logic Input Voltage Range	V_{IN}	PWM	–0.3	–	6	V
Motor Current	I_{OUT}	Motor phase current – sinusoidal running mode	–	–	3000	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	24-contact QFN (package ES), on 2-sided PCB 1-in.^{2} copper	45	°C/W
		16-lead TSSOP (package LP), on 2-sided PCB 1-in.^{2} copper	35	°C/W

*Additional thermal information available on the Allegro website.

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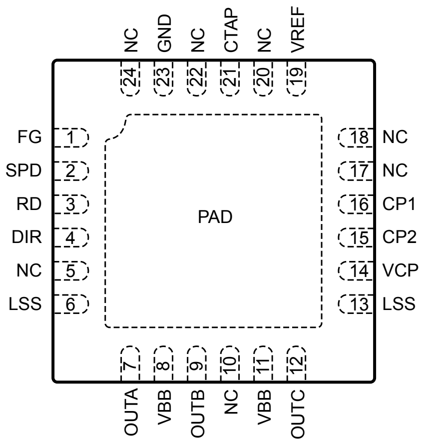
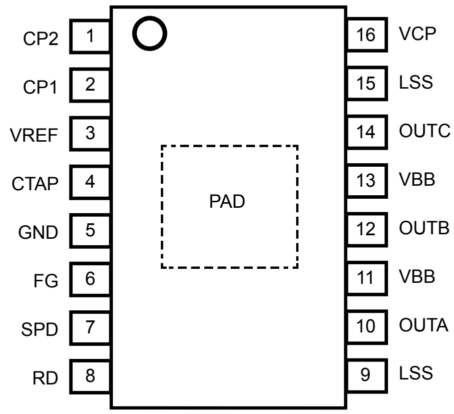
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



ES Package Pinouts



LP Package Pinouts

Terminal List Table

Terminal Number		Name	Function
ES Package	LP Package		
1	6	FG	Output signal
2	7	SPD	Logic input – speed demand
3	8	RD	Logic output signal
4	–	DIR	Logic input
5	–	NC	No connect
6	9	LSS	Low-side source connection
7	10	OUTA	Motor terminal
8	11	VBB	Input supply
9	12	OUTB	Motor terminal
10	–	NC	No connect
11	13	VBB	Input supply
12	14	OUTC	Motor terminal
13	15	LSS	Low-side source connection
14	16	VCP	Charge pump capacitor
15	1	CP2	Charge pump capacitor
16	2	CP1	Charge pump capacitor
17	–	NC	No connect
18	–	NC	No connect
19	3	VREF	Reference voltage output
20	–	NC	No connect
21	4	CTAP	Motor terminal
22	–	NC	No connect
23	5	GND	Ground
24	–	NC	No connect
–	–	PAD	Exposed pad for enhanced thermal dissipation

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ELECTRICAL CHARACTERISTICS: Valid for T_A = –40°C to 105°C (G version) or T_A = –40°C to 125°C (K version), and V_{BB} = 5 to 16 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Supply Current	I_{BB}	Active mode (PWM duty < DC_ON)	–	8.5	13	mA
	I_{BBS}	V_{BB} = 12 V, standby mode	–	–	100	μA
Reference Voltage	V_{REF}	I = 0 to 10 mA	2.75	2.85	2.95	V
POWER DRIVER						
Total Driver On-Resistance (Sink + Source) [2]	$R_{DS(ON)}$	I_{OUT} = 1.5 A, T_J = 25°C, V_{BB} = 12 V, G Version	–	210	250	mΩ
		I_{OUT} = 1.5 A, T_J = 25°C, V_{BB} = 12 V, K Version	–	225	265	mΩ
		I_{OUT} = 1.5 A, T_J = 125°C, V_{BB} = 12 V, G Version	–	300	360	mΩ
		I_{OUT} = 1.5 A, T_J = 125°C, V_{BB} = 12 V, K Version	–	320	380	mΩ
		Source Driver, T_J = 25°C, G Version	–	105	–	mΩ
		Sink Driver, T_J = 25°C, G Version	–	105	–	mΩ
Motor PWM Frequency	f_{PWM}		23.4	24.4	25.4	kHz
SPEED CONTROL						
PWM Input Frequency Range	f_{PWMIN}		6 [3]	–	100	kHz
Duty Cycle On Threshold	DC_{ON}	Relative to target	–0.5	–	0.5	%
Duty Cycle Off Threshold	DC_{OFF}	Relative to target	–0.5	–	0.5	%
Speed Setpoint	F_{SPD}	PWM mode	–5	–	5	%
SPD Standby Threshold (Analog)	V_{SPDTH}	A5931KLPTR-T only	–	0.7	0.8	V
SPD On Threshold	V_{SPDON}	DC_{ON} = 10%, A5931KLPTR-T only	–	300	–	mV
SPD On Threshold	V_{SPDOFF}	DC_{OFF} = 8%, A5931KLPTR-T only	–	258	–	mV
SPD ADC Resolution	V_{SPDLSB}	A5931KLPTR-T only	–	4.82	–	mV
SPD ADC Code Offset	SPD_{OFF}	A5931KLPTR-T only	–	12	–	LSB
SPD ADC Accuracy [4]	SPD_{ACC}	V_{SPD} = 0.2 to 2.5 V, relative to equation, A5931KLPTR-T only	–20	–	20	LSB
PROTECTION CIRCUITS						
Lock Timing	t_{OFF}	Relative to target	–10	–	10	%
VBB Undervoltage Threshold	V_{BBUVLO}	V_{BB} rising	–	4.3	4.5	V
VBB Undervoltage Hysteresis	V_{BBHYS}		160	300	480	mV
Overcurrent Protection	I_{OCP}		4.2	6.5	8.5	A
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.
[2] $R_{DS(ON)}$ difference due to bond wire material, copper (G version) versus gold (K version).
[3] Refer to description for SPD pin.
[4] SPD Analog mode is not tested for A5931GES-T or A5931GLP-T.

Continued on next page...

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ELECTRICAL CHARACTERISTICS (continued): Valid for T_A = –40°C to 105°C (G version) or T_A = –40°C to 125°C (K version), and V_{BB} = 5 to 16 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC/INPUT OUTPUT/I²C						
Logic Input Low Level	V_{IL}		–	–	0.8	V
Logic Input High Level	V_{IH}		2	–	–	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Logic Input Current	I_{IN}	SPD	–10	<1	10	µA
		DIR, V_{IN} = 0 V, 100 kΩ pull-up	–	28	–	µA
Output Saturation Voltage (FG, RD)	V_{SAT}	I = 5 mA	–	–	0.3	V
Output Leakage (FG, RD)	I_O	V = 16 V, switch OFF	–	–	5	µA
I²C TIMING						
SCL Clock Frequency	f_{CLK}		3	–	400	kHz
Bus Free-Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	ms

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

Basic Operation

The A5931 targets high-speed fan applications to meet the objectives of minimal vibration, high efficiency, and ability to customize the IC to the speed control specification.

In typical systems, an MCU is required to meet each application specification. The A5931 integrates the basic closed-loop speed control function, thus allowing elimination of the cost, PCB space, and programming requirements of a custom MCU.

For each specific application, the EEPROM settings can be created with the Allegro EVB and software. Contact Allegro sales to order the custom IC. (Minimum volume requirements will apply).

The speed of the fan is typically controlled by variable duty cycle PWM input. The duty cycle is measured and converted to a 9-bit number. This 9-bit "demand" is translated to a speed signal based on settings that are configured via EEPROM.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

Standby mode can be achieved by holding SPD pin low for longer than the programmed lock off-time. In specific speed curve options, the motor will never turn off, if speed is set to run at a minimum value with 0% duty cycle applied. In this type of configuration, standby mode is not available.

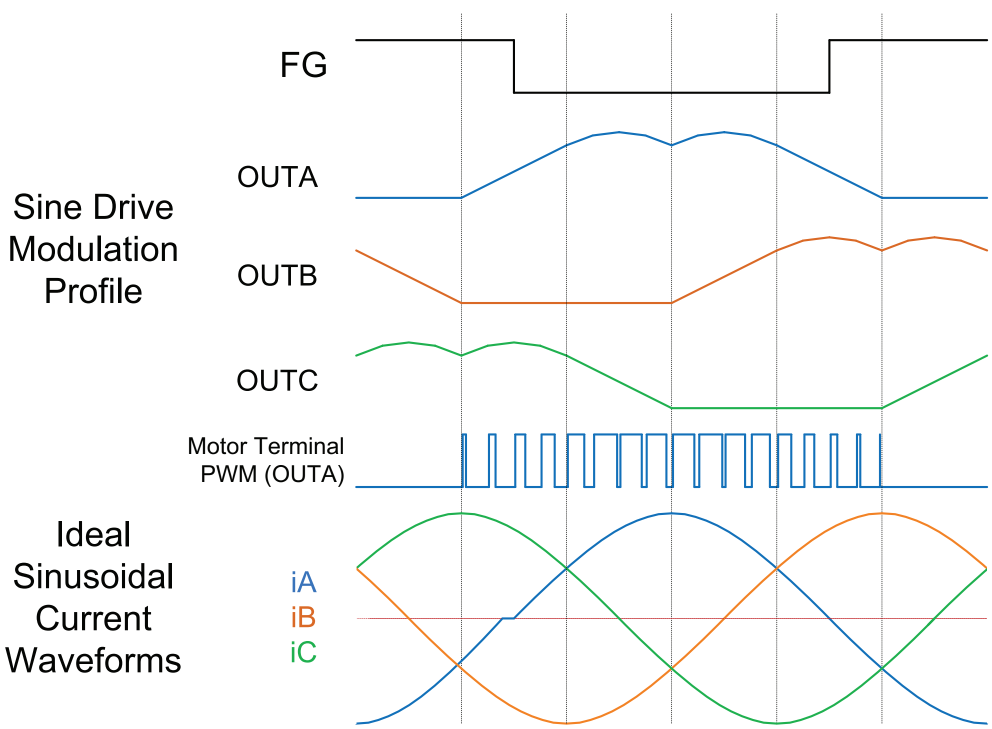

Figure 2: Sinusoidal Drive Sequence for DIR = HI

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FG. Open-drain output, represents the speed of the motor for normal operation. Additionally, the FG pin serves as the data line, (SDA) for I^2C communication.

The FG output signal typically represents two periods per mechanical revolution. f_{FGOUT} may not be same as electrical frequency:

$$f_{ELEC} = f_{FGOUT} \times NumberOfPolePairs / 2$$

$$f_{FGOUT} = f_{ELEC} \times 2 / NumberOfPolePairs$$

$$RPM = 30 \times f_{FGOUT}$$

$$RPM = f_{ELEC} \times 60 / NumberOfPolePairs$$

RD. Open-drain output, logic high indicates a rotor fault condition as defined by EEPROM variables. RD function can be disabled via EEPROM. When function is disabled, RD pin goes high to indicate end of open-loop starting sequence.

SPD. Speed Demand input pin. Choice of analog voltage control or PWM duty control is determined by EEPROM selection.

Duty cycle control. The input Duty cycle signal is measured with logic circuit. The calculated output number is translated to a speed Demand signal with a resolution of 0.2%.

The maximum input PWM frequency is 100 kHz. To avoid interaction with the I^2C circuitry, which share the FG and SPD inputs, the minimum PWM frequency may be limited based on the maximum frequency of the speed output pin FG.

$f_{PWM(min)}$ is the larger number of 2.5 × $f_{FGOUT(max)}$ or 100 Hz.

$f_{FGOUT(max)}$ is the maximum speed under all operating conditions.

Note: f_{FGOUT} (Hz) depends on selection of pole-pair in EEPROM, typically equals RPM / 30.

Analog control (A5931KLP only). Voltage applied will increase speed demand. An internal 9-bit A/D converter will translate the input to a speed demand.

$$Code = V_{IN(SPD)} / 4.82\text{ mV} – 12 \text{ where code} = [0…511]$$

$$Applied\ Duty\ (\%) = Code / 511.$$

CTAP. This analog input is an optional connection for motor common (Wye motors). It is required to insert a 2 kΩ resistor in series with the pin. If not used, as in case of Delta wound motor, then pin must be left open circuit.

LOCK DETECT. A5931 will turn off for the programmed time (t_{OFF}) when the rotor is in a locked condition.

DIR (ES package only). Login input to control direction of motor. Logic "1" moves the outputs in sequence A→B→C. To reverse direction, logic "0" will sequence A→C→B. If the DIR pin changes while motor is running, the motor coasts for the programmed time, t_{LOCK}. After t_{LOCK} timeout, a normal startup sequence occurs. If motor is still moving opposite of intended direction, resynchronization logic will stop the motor before standard startup sequence.

DIR is pulled up internally with 100 kΩ resistor. To avoid any concern with PCB noise, it is recommended to connect pin to GND or VREF externally.

OCP. Overcurrent protection is intended to protect the IC from application conditions of shorted load, motor short to ground, and motor short to battery. The OCP protection monitors the drain-to-source voltage (VDS) across any source or sink driver when the output is turned on. The OCP level is approximately 6.5 A. If the OCP threshold is exceeded for 640 nanoseconds, all drivers are shut off. This fault mode can be reset by PWM ON/OFF or timeout of t_{LOCK}, depending on EEPROM bit OCPOPT.

Pin shorts to GND (low inductance) on PCB should be avoided. It is possible during startup that the applied duty can be set below the blank time of the OCP circuit. For this scenario, there can be multiple pulses of high current that may overstress the IC before the OCP shutdown can occur.

OCL. An optional overcurrent limit function can be set to four different levels via EEPROM. In general, current limit should be set to a value beyond the maximum expected run current. If current limit occurs during normal operation, audible noise or motor stalling could potentially be observed. The current limit circuit monitors the VDS of the sink-side MOSFET and turns off the source driver(s) for the remainder of the PWM cycle. Current limit needs to be enabled via EEROM bit OCLD set low. If enabled, then OCL bits in the EEPROM control the level as follows:

Table 1: Overcurrent Limit

Code	I_{OCL} (A)
00	3.2
01	2.6
10	1.8
11	1

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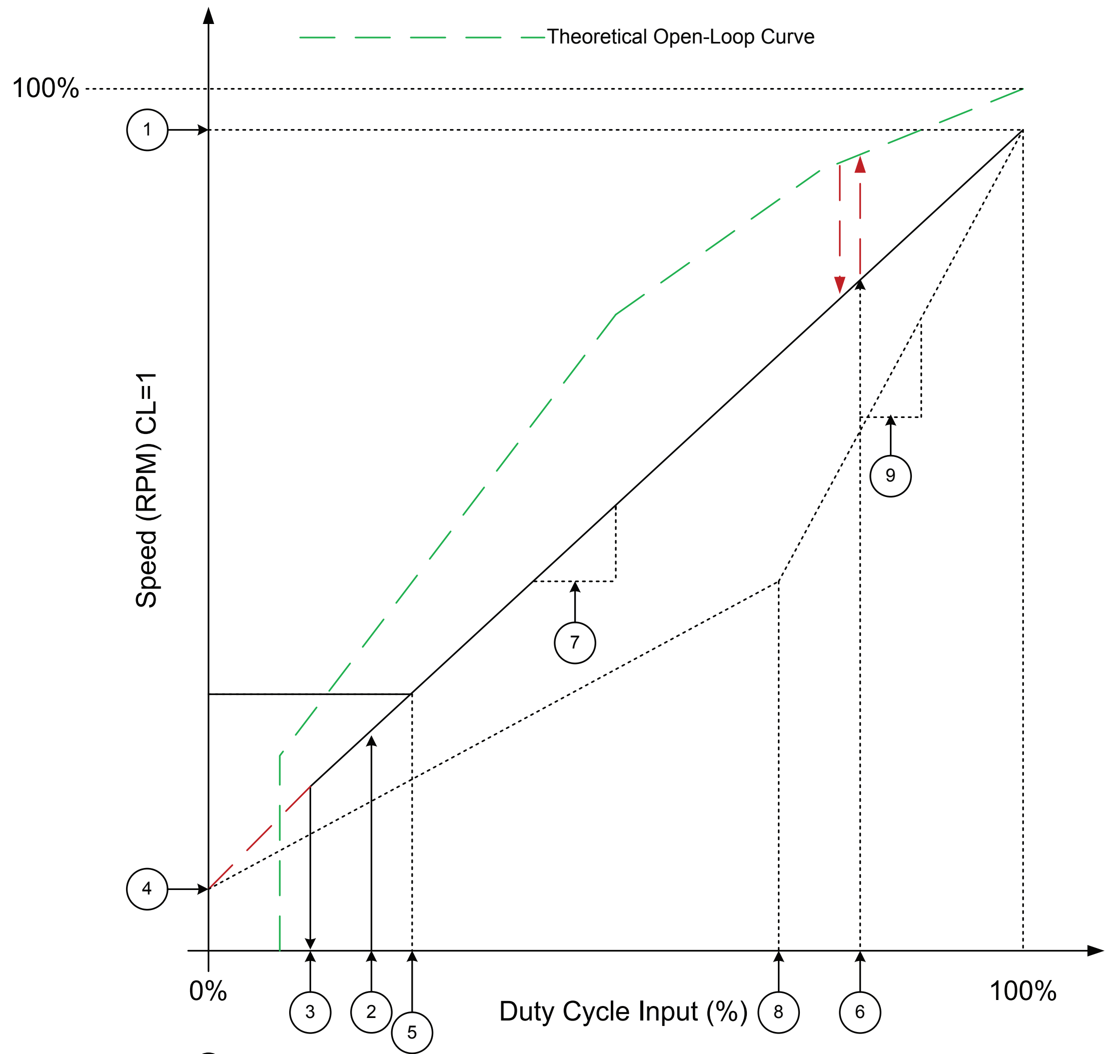
SPEED CURVE PARAMETERS



1 Maximum Speed (calculated from Slope of line AND Offset)

2 Duty On (DC_{ON}/511)

3 Duty Off (DC_{OFF}/511)

4 MINSPD

5 Min Duty Clamp

6 Max Duty Threshold and Hystersis

7 Slope (based on SPDSLP variable)

8 Slope Switch Duty

9 Slope 2 Option

Figure 3: Speed Curve Parameters

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Speed Curve Parameters (continued)

Refer to "Figure 3: Speed Curve Parameters" on page 9 for items below.

Minimum Speed Setpoint. The minimum speed is defined by the value stored in EEPROM variable MINSPD. The resolution is 1 rpm.

MINSPD (rpm) = 0..4095

Maximum Speed Setpoint. The A5931 calculates the maximum speed based on line equation $y = mx + B$. The maximum speed is defined as the speed with input duty = 100%.

The desired maximum speed is used to set the EEPROM variable SPDSLP1.

$$SPDSLP1 = 64 \times (Maximum\ Speed\ (rpm) - MINSPD) / 511$$

Example: Max Speed = 25000, Min Speed = 3000.

$$SPDSLP1 = 64 \times 22000 / 511 = 2755$$

where SPDSLP1 = 0..8192

$$Motor\ Speed\ (rpm) = Slope \times DutyIN + MINSPD.$$

where Slope = SPDSLP1 × 511 / 64 and DutyIN expressed in %.

Duty In Enable Threshold. EEPROM variable DCON defines the input duty signal that enables the drive. DCON is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

$$Duty\ On\ (\%) = 100 \times DCON / 511$$

If DCON is set to "0", motor will turn on with 0% duty cycle input.

Duty In Disable Threshold. EEPROM variable DCOFF defines the input duty signal that disables the drive. DCOFF is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

$$Duty\ Off(\%) = DCOFF / 511$$

DCOFF should always be set to a lower number than DCON.

Duty Cycle Invert. To create mirror image of speed curve, set duty cycle invert bit to "1".

Minimum Duty Clamp. Minimum speed can be clamped to a value to allow motor to run at defined low-level speed. This is achieved by ignoring the duty cycle input if below the programmed MINDTY level.

$$Min\ Duty\ Clamp\ (\%) = 100 \times MINDTY / 511$$

Therefore the minimum speed will be defined by:

$$MinSpeedClamp(rpm) = Slope \times MinDutyClamp + MINSPD$$

Setting MINDTY to 0 disables the function.

MINDTY = 0..255.

Maximum Duty Clamp. EEPROM variable DTYMAX defines a duty level at which the motor will change operation from closed-loop curve. The change of operation would depend on MAXDTYOPT setting. If MAXDTYOP = 0, open-loop operation will result. If MAXDTYOPT = 1, then operation will remain closed-loop; however, the speed will be clamped at the value calculated by DTYMAX level.

4 bits are used for this setting at resolution of 1.6% to cover the range 76.5% to 100%.

$$Maximum\ Duty\ (\%) = 100 \times (511 - MAXDTY \times 8) / 511$$

MAXDTY = 0..15; if MAXDTY = 0, then function is disabled.

Hysteresis is needed to prevent motor from going back and forth between open- and closed-loop mode.

MAXDTYHYS = 0...15.

Hys(%) = (MAXDTYHYS + 1) × 0.4

Dual Slope Option. Two different slopes can be selected by setting variable SLPSWDTY greater than 0.

Slope2 = (MAXSPEED – SLPSWRPM) / (100% – SLPSWDTY)

Slope1 = (SLPSWRPM – MINSPEED) / SLPSWDTY

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RD FUNCTION

Rotor lock output RD can be used to indicate motor is not running as expected. A high level on RD will indicate a fault.

Refer to the following four timing diagrams and Table 2 for understanding of the RD function and flexibility to adjust parameters via EEPROM.

Table 2

EEPROM Parameter	Range	Resolution	Comment
LOCKEVT	0/1		0 = RD triggered at lock event count of 2 1 = Use RDBLANK for lock events
RDHIGH (rpm)	0 to 4080	16 rpm	If set to 0; RD function disabled
RDLOW (rpm)	0 to 4080	16 rpm	Must be programmed lower than RD_high
RDDLY	0 to 15	1 second	
RDBLANK	0.1 to 25.4	100 milliseconds	
TLOCK	0.1 to 25.4	100 milliseconds	

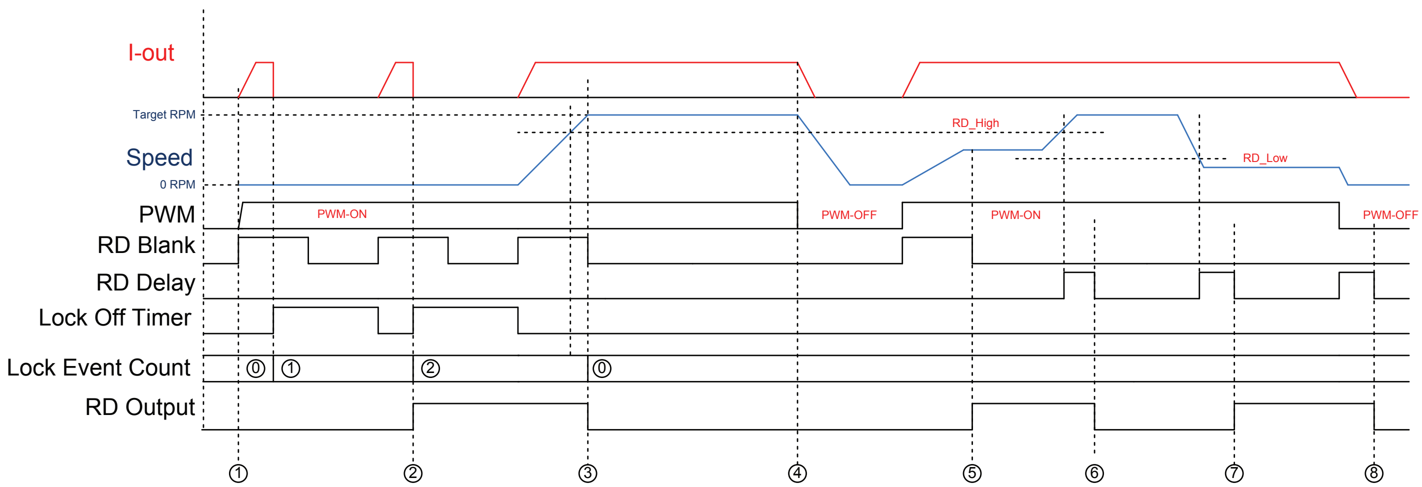

Figure 4: RD Timing Diagram (LOCKEVT = 0)

1. Power on with rotor locked condition
2. RD is high after 2nd lock event
3. RD resets low after RD Blank if Speed > RD_High; Lock Event Count reset to zero
4. PWM off – RD is low since normal condition
5. RD is high after RD Blank if Speed < RD_High
6. RD is low if Speed > RD_High after RD Delay
7. RD is high if Speed < RD_Low after RD Delay
8. PWM off – RD goes low after RD Delay low since normal condition

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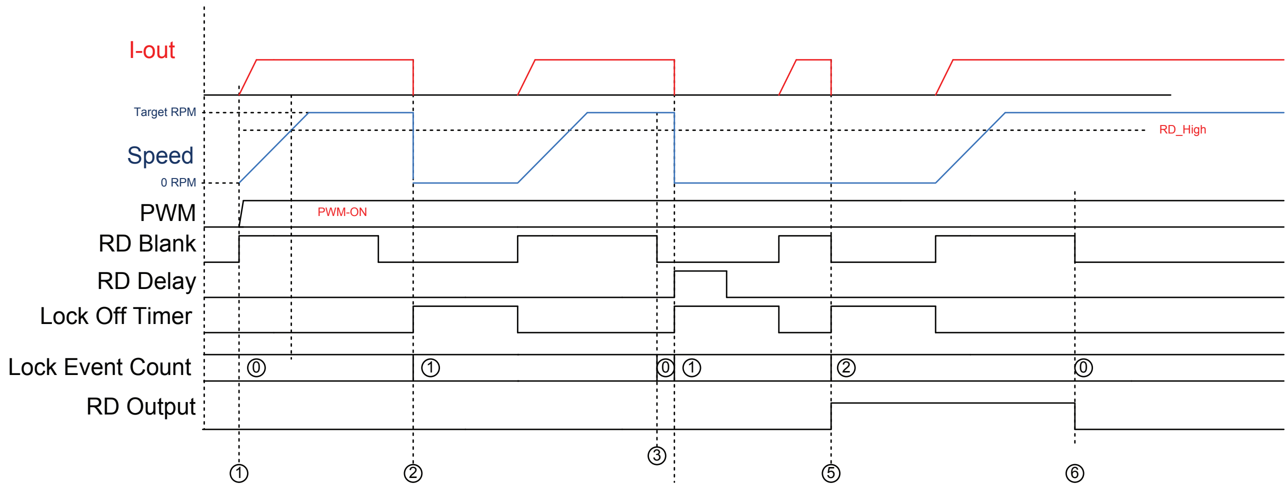

Figure 5: RD Timing Diagram (LOCKEVT = 0); lock condition while running

1. Power on with PWM normal startup
2. Rotor locked while running – Lock Event Counter is one
3. If Speed > RD_high after RD Blank, Lock Event count reset to zero
4. Rotor locked while running – Lock Event Counter is one
5. RD is high after 2nd lock event
6. RD reset to low after RD Blank if (Speed > RD_High); Lock Event Count reset to zero

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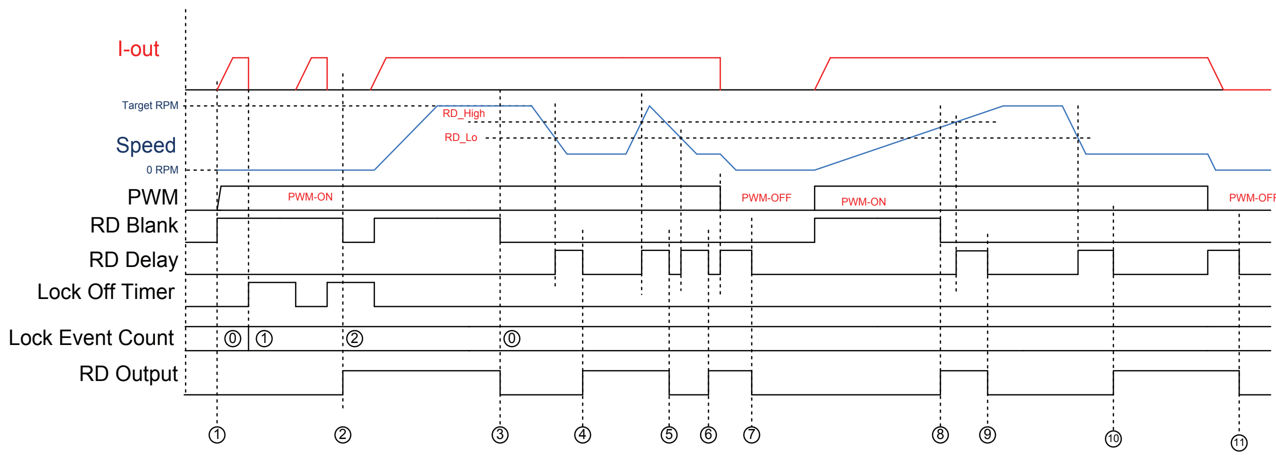

Figure 6: RD Timing Diagram (LOCKEVT = 1)

1. Power on with rotor locked condition
2. RD is high after RD Blank if Speed < RD_High
3. RD resets low after RD Blank if Speed > RD_High
4. RD changes to high if Speed < RD_Low after RD Delay
5. RD changes to low if Speed > RD_High after RD Delay
6. RD changes to high if Speed < RD_Low after RD Delay
7. RD changes to low when PWM goes off after RD Delay
8. RD changes to high after RD Blank if Speed < RD_High even if Speed > RD_Low
9. RD changes to low if Speed > RD_High after RD Delay
10. RD changes to high if Speed < RD_Low after RD Delay
11. RD changes to low when PWM goes off after RD Delay

Note: RD Blank should be programmed longer than the time is take to accelerate to the RD_High level. Startup time + time to accelerate to RD_High.

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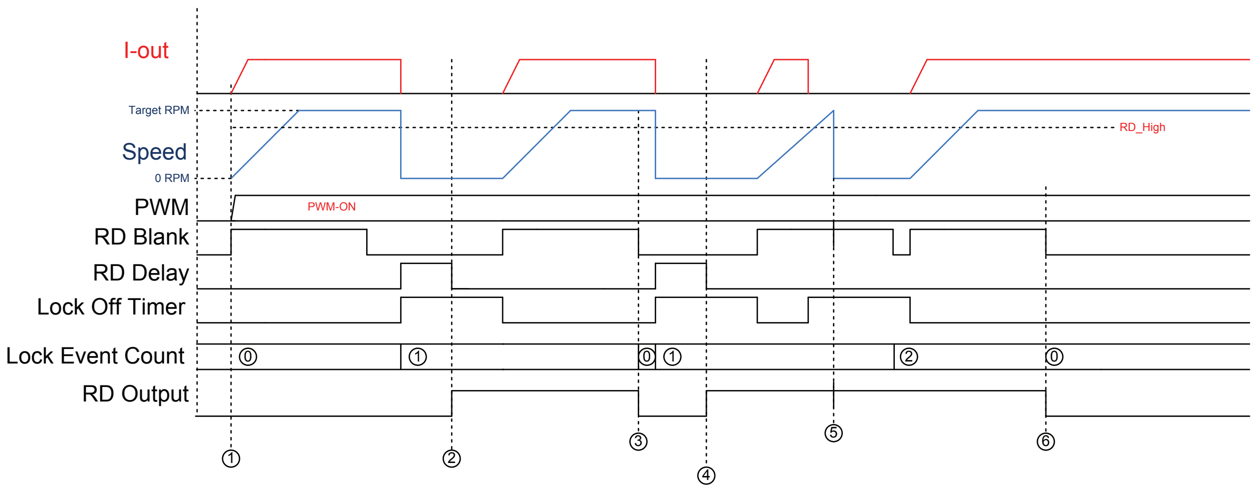

Figure 7: RD Timing Diagram (LOCKEVT = 1); lock condition while running

1. Power on with PWM normal startup
2. Rotor locked while running – RD changes to high after RD Delay if Speed < RD_Low
3. RD changes to low if Speed > RD_high after RD Blank
4. Rotor locked while running – RD changes to high after RD Delay if Speed < RD_Low
5. RD remains high, even if Speed is OK, since RD Blank has not timed out
6. RD reset to low after RD Blank if Speed > RD_High

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EEPROM MAP

Table 3: EEPROM Map

ADDR	Bits	Name	Description	Default Setting	Default Value (decimal)
0	15:0	Dev1	Device information for customer use	n/a	0
1	11:0	MINSPD	Range = 0 to 4095, LSB = 1 rpm	2000	2000
	12	DUTYINV	0 = normal, 1 = invert	0	0
	13	MAXOFF	0 = normal, 1 = max speed when duty < DC_Off	0	0
	14	MAXDTYOPT	0 = run at open loop, 1 = run at MAXDTYCLP	1	1
	15	Unused			
2	13:0	SPDSLP1	Calculated slope of speed curve	set for 19909 rpm	2243
	15:14	Unused		0	0
3	7:0	DCON	Range = 0 to 49.9%, LSB = 0.2%	10%	97
	15:8	DCOFF	Range = 0 to 49.9%, LSB = 0.2%	7.4%	79
4	3:0	MAXDTYCLP	Range = 100% to 76.5%, LSB = 1.6%	0	0
	7:4	MAXDTYHYS	Range = 0 to 5.9%, LSB = 0.4%	0	0
	14:8	MINDTYCLP	Range = 0 to 49.9%, LSB = 0.39%	0	0
	15	Unused			
5	7:0	STRTDMD	Range = 0 to 16 V, LSB = 63 mV	945 mV	15
	15:8	DMDPOST	Range = 0 to 100%, LSB = 0.39%	100%	255
6	7:0	ALIGNT	Range = 0 to 20.4 seconds, LSB = 80 ms	480 ms	6
	15:8	ASLOPE	Range = 160 ms to 40 seconds	511 ms	80
7	7:0	STRTF	Range = 0 to 20.4 seconds, LSB = 80 ms	2 Hz	32
	15:8	ACCEL	Range = 0 to 99.6 Hz/s, LSB = 0.78	42 Hz/s	107
8	7:0	ACCELT	Range = 0 to 20.4 seconds, LSB = 80 ms	480 ms	6
	15:8	RMOT	Phase to Phase Motor Resistance [1]	1.3	13
9	3:0	DMDRMPAL	Range = 3.8 to 63.8 ms/count, LSB = 3.8	23.8 ms/count	5
	7:4	DMDRMPAH	Range = 3.8 to 63.8 ms/count, LSB = 3.8	7.8 ms/count	1
	11:8	DMDRMPDL	Range = 3.8 to 63.8 ms/count, LSB = 3.8	15.8 ms/count	3
	15:12	DMDRMPDH	Range = 3.8 to 63.8 ms/count, LSB = 3.8	15.8 ms/count	3
10	15:0	Dev2	Device information	n/a	n/a
11	7:0	MAXSPD	Maximum electrical frequency	1061 Hz	23
	15:8	TLOCK	Range = 0 to 25.5 seconds	5 seconds	50
12	7:0	RDLOW	Range = 0 to 4095, LSB = 16 rpm	0	0
	15:8	RDHIGH	Range = 0 to 4095, LSB = 16 rpm	0	0
13	7:0	RDBLANK	Range = 0 to 25.5 seconds, LSB = 100 ms	0	0
	12:8	RDDLY	Range = 0 to 15 seconds, LSB = 1 second	0	0
14	11:0	PHASLP	Calculated slope for linear phase advance	set for 11°@20000 rpm	367
	15:12	SOWLIN	Window width with linear phase advance	28°	15

[1] RMOT is for GUI use; it does not change operation of the IC

Continued on next page...

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EEPROM MAP (continued)

ADDR	Bits	Name	Description	Default Setting	Default Value (decimal)
15	0	PCDLY	Post-coast delay: 0 = 100 ms, 1 = 500 ms	500 ms	1
	1	STBYDIS	Standby Mode: 0 = Enable, 1 = Disable	0	0
	3:2	PWMF	Motor PWM selection	24 or 48 kHz	2
	5:4	BEMFFILT	Bemf Comparator filter	4 µs	0
	6	TCENB	Temperature compensation: 0 = Off, 1 = On	0	0
	8:7	WINDM	Windmill option	0	0
	12:9	SPDCLP	Minimum clamp is speed control mode	4.6%	2
	14:13	OCL	Set overcurrent limit level	0	0
	15	OCLD	1 = disable overcurrent limit	0	0
16	0	CL	Speed Control Mode: 0 = open loop, 1 = closed	enabled	1
	1	PHA	Running Mode: 0 = auto, 1 = linear phase advance	0	0
	2	LOCKEVT	RD function mode select	0	0
	3	SPDSEL	Speed control select: 0 = PWM duty, 1 = analog	0	0
	6:4	PP	Pole pair = PP + 1	2 pp	1
	7	NOCOAST	1 = no coast, 0 = coast	1	1
	8	ALIGNMODE	0 = align, 1 = one cycle	one cycle	1
	10:9	QCKSTRT	0 = disable, 1 = enable	0	0
	11	FGSTRT	0 = FG disabled during startup, 1 = FG enabled	0	0
	13:12	BEMFHYS	BEMF hysteresis level for startup	40 mV	1
	14	SOWAUTO	Initial value of window	21°	1
	15	OCPOPT	0 = reset after TLOCK, 1 = after PWM on/off	TLOCK	0
17	7:0	KP	Closed loop	16	16
	15:8	KI	Closed loop	2	2
18	7:0	SLPSWDTY	Duty at which slope changes	0	0
	15:8	Unused			
19	14:0	SLPSWRPM	Range 0 to 16384, LSB = 1 rpm	2000 rpm	2000
	15	Unused			
20	13:0	SPDSLP2	Calculated slope	0	0
	15:14	Unused			
21	15:0	Allegro	Allegro use only	n/a	
22	15:0	Dev3	Device information	n/a	
23	15:0	Allegro	Allegro use only	n/a	

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SERIAL PORT CONTROL OPTION

Normally the IC is controlled by duty cycle input and uses the EEPROM data that is stored to create the speed curve profile. However, it is possible to use direct serial port control to avoid programming EEPROM.

When using direct control, the input duty cycle command is replaced by writing a 9-bit number to register 165.

Example:

REGADDR[data]: (in decimal)

165[511] → Duty = 100%

165[102] → Duty = 102 / 511 = 20%

Upon power up, the IC defaults to duty cycle input mode. To use serial port mode, the internal registers should be programmed before turning the part on. The sequence to use serial port mode is:

1. Drive FG and SPD pins low *
2. Power-up IC
3. Program registers for parameter setting that correspond to each of the EEPROM memory locations.
   A. REGADDR = 64 + EEPROM ADDR.
   B. Program register addresses 65 to 84 corresponding to EEPROM addresses 1 to 20.
   C. It may be helpful to use the GUI text file to help define the hex data for each of the EEPROM addresses.
4. Write to register 165 to start motor

* Note: If SPD is not driven low before power up, motor will try to start immediately as the default high value will demand 100% on signal.

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Serial Port

The A5931 uses standard fast mode I^{2}C serial port format to program the EEPROM or to control the IC speed serially. The SPD pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running, the FG may then pull the data line low while trying to initialize into serial port mode. Once an I^{2}C command is sent, the SPD input is ignored, and the motor will turn off as if a PWM duty command of 0% was sent.

The A5931 7-bit slave address is 0x55.

I^{2}C Timing Diagrams

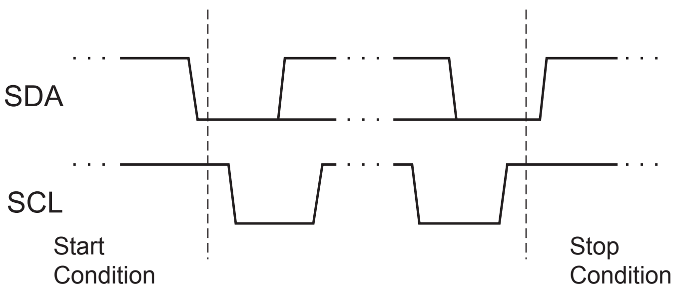

Figure 8: Start and Stop Conditions

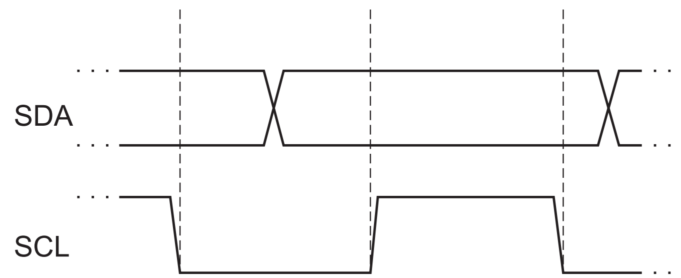

Figure 9: Clock and Data Bit Synchronization

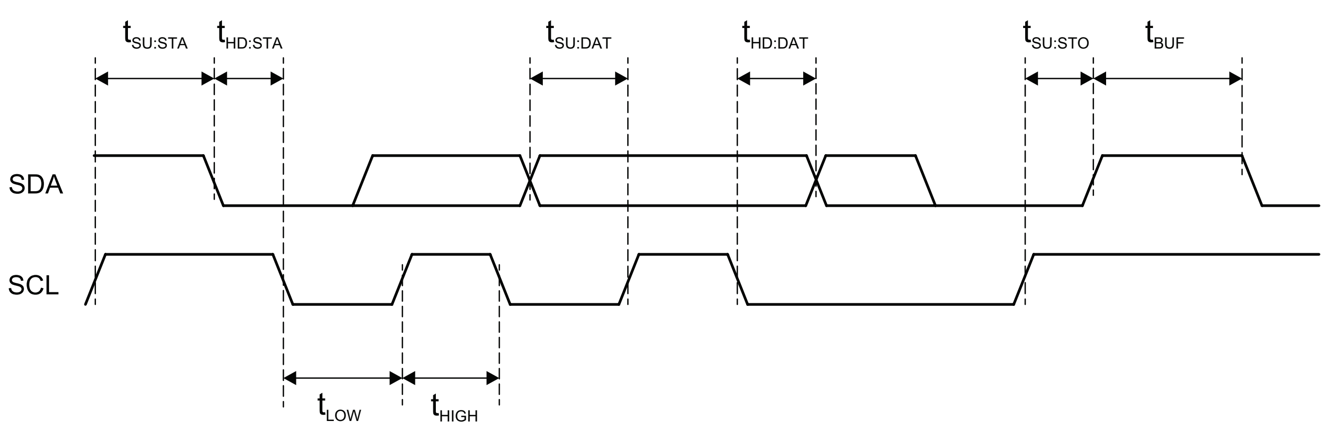

Figure 10: I^{2}C-Compatible Timing Requirements

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Write Command

1. Start Condition
2. 7-bit I2C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address
4. 2 data bytes, MSB first
5. Stop Condition

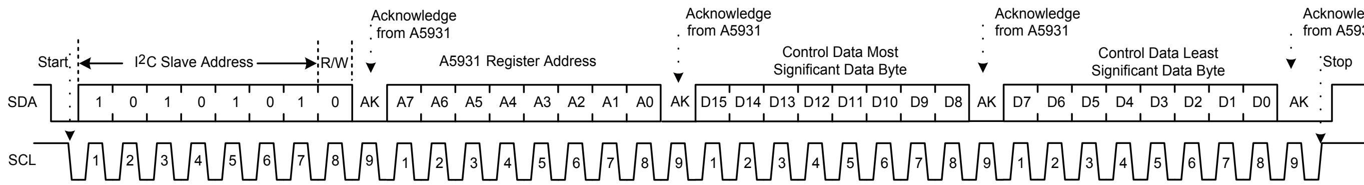

Figure 11: Write Command

Read Command

1. Start Condition
2. 7-bit I2C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address to be read
4. Stop Condition
5. Start Condition
6. 7-bit I2C Slave Address (Device ID) 1010101, R/W Bit = 1
7. Read 2 data bytes
8. Stop Condition

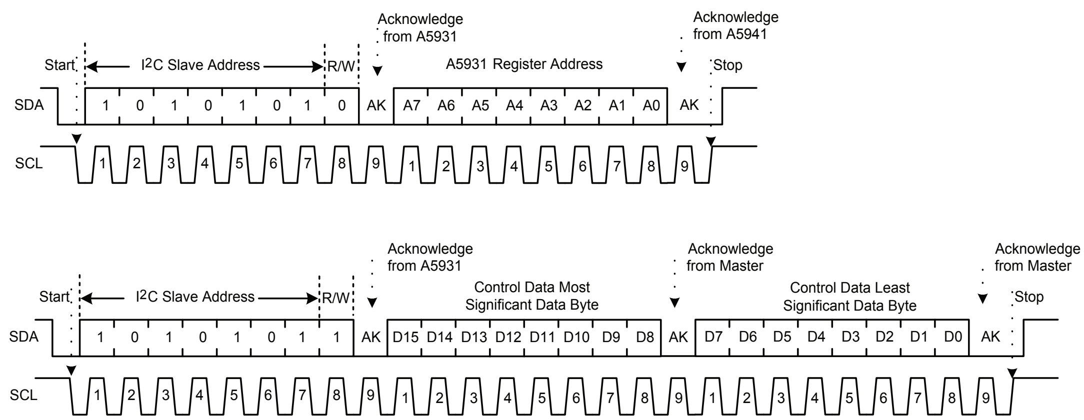

Figure 12: Read Command

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Programming EEPROM

The A5931 contains 24 words of 16-bit length. The EEPROM is controlled with the following I^2C registers. Refer to application note for EEPROM definition.

Table 4: EEPROM Control – Register 161 (Used to control programming of EEPROM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEPROM voltage required for writing or erasing
1	ER	Sets mode to erase
2	WR	Sets mode to write
3	RD	Sets mode to read
15:4	n/a	Do not use; always set to zero during programming process

Table 5: EEPROM Address – Register 162 (Used to set the EEPROM address to be altered)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
4:0	eeADDRESS	Used to specify EEPROM address to be changed.
15:5	n/a	Do not use; always set to zero during programming process

Table 6: EEPROM DataIn – Register 163 (Used to set the EEPROM new data to be programmed)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed

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Table 7: DataOUT – Register 164 (Used for read operations)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAout															

Bit	Name	Description
15:0	eeDATAout	Used to readback EEPROM data from address defined in register 162

There are 3 basic commands: Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 10 ms per word.

Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (0x0105)

1) Erase the word

	I^2C Write REGADDR[Data]	; comment
a.	162[5]	; set EEPROM address to erase
b.	163[0]	; set 0000 as Data In
c.	161[3]	; set control to Erase and trigger high-voltage pulse
d.	Wait 15 ms	; wait for pulse to end
e.	161[0]	; clear voltage

2) Write the new data

a.	162[5]	; set EEPROM address to write
b.	163[261]	; set Data In = 261
c.	161[5]	; set control to Write and trigger high-voltage pulse
d.	Wait 15 ms	; wait for pulse to end
e.	161[5]	; clear voltage

Example #2: Read EEPROM address 5 to confirm correct data properly programmed

1) Read the word

a.	5[I^2C Read]	; read register 5; this will be the contents of EEPROM

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APPLICATION INFORMATION

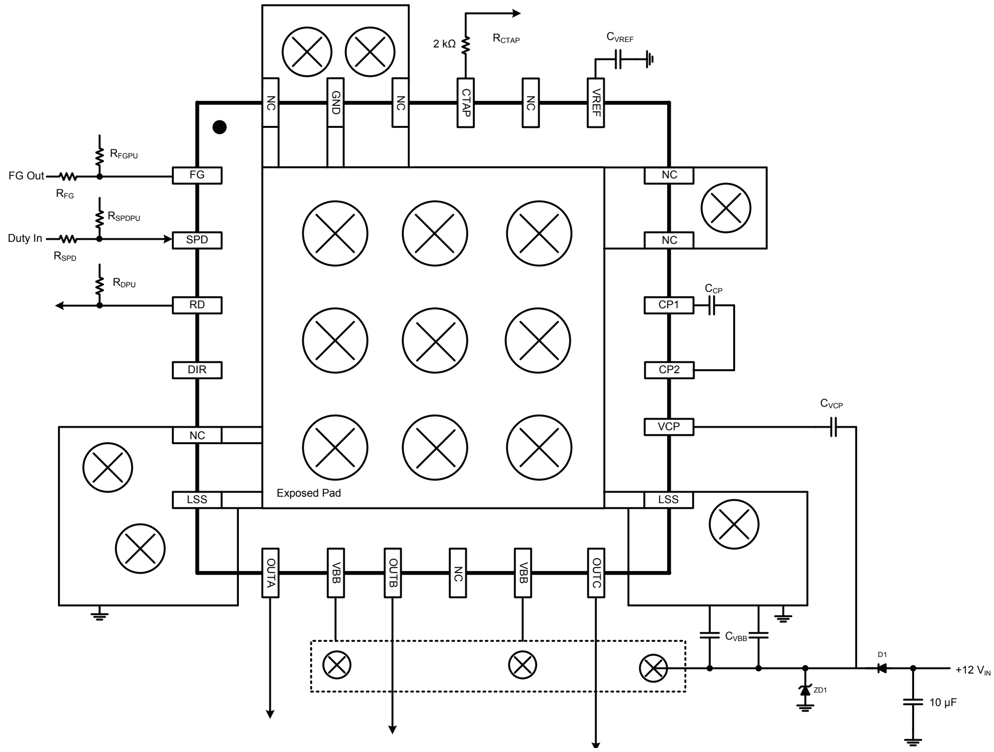

Figure 13: Typical Application Circuit

Table 8: Typical Application Components

Name	Suggested Value	Comment
C_{VREF}	0.1 µF / X5R / 10 V	Ceramic capacitor required
C_{VBB}	10 to 100 µF	Power supply stabilization – electrolytic or ceramic OK.
C_{VCP}	0.1 µF	Ceramic capacitor required
C_{CP}	0.1 µF	Ceramic capacitor required
D1	Not installed	May be required to isolate motor from system or for reverse polarity protection
ZD1	SMBJ14A	TVS to limit max V_{BB} due to transients due to motor generation on power line. Suggested to clamp below 16 V.
R_{CTAP}	2 kΩ	2 kΩ series resistance; not required if pin left O/C
R_{FG}	500 Ω	Optional – If FG wired to connector – R_{FG} will isolate IC pin from noise or overvoltage transients or protect from connector issues
R_{FGPU}	10 kΩ	Open-drain pull-up resistor – required if using pin for I^2C
R_{SPD}	500 Ω	Optional – If PWM wired to connector – R_{SPD} will isolate IC pin from noise or overvoltage transients or protect from connector issues
R_{SPDPU}	10 kΩ	Open-drain pull-up resistor – required if using pin for I^2C
R_{RD}	10 kΩ	Open-drain pull-up resistor – optional for RD function or test use

Layout Notes:
1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place C_{VREF} and C_{VBB} as close as possible to IC, connected to GND plane.

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PIN DIAGRAMS

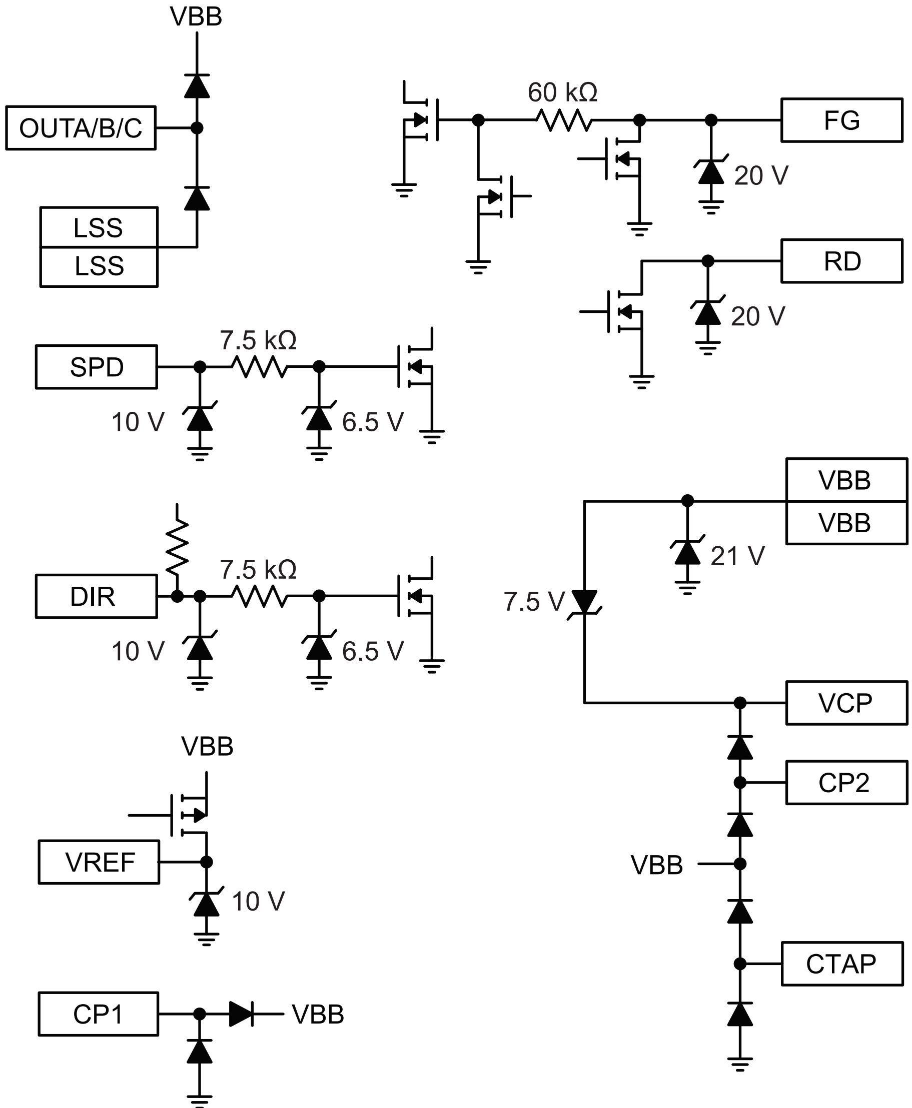

Figure 14: Pin Diagrams

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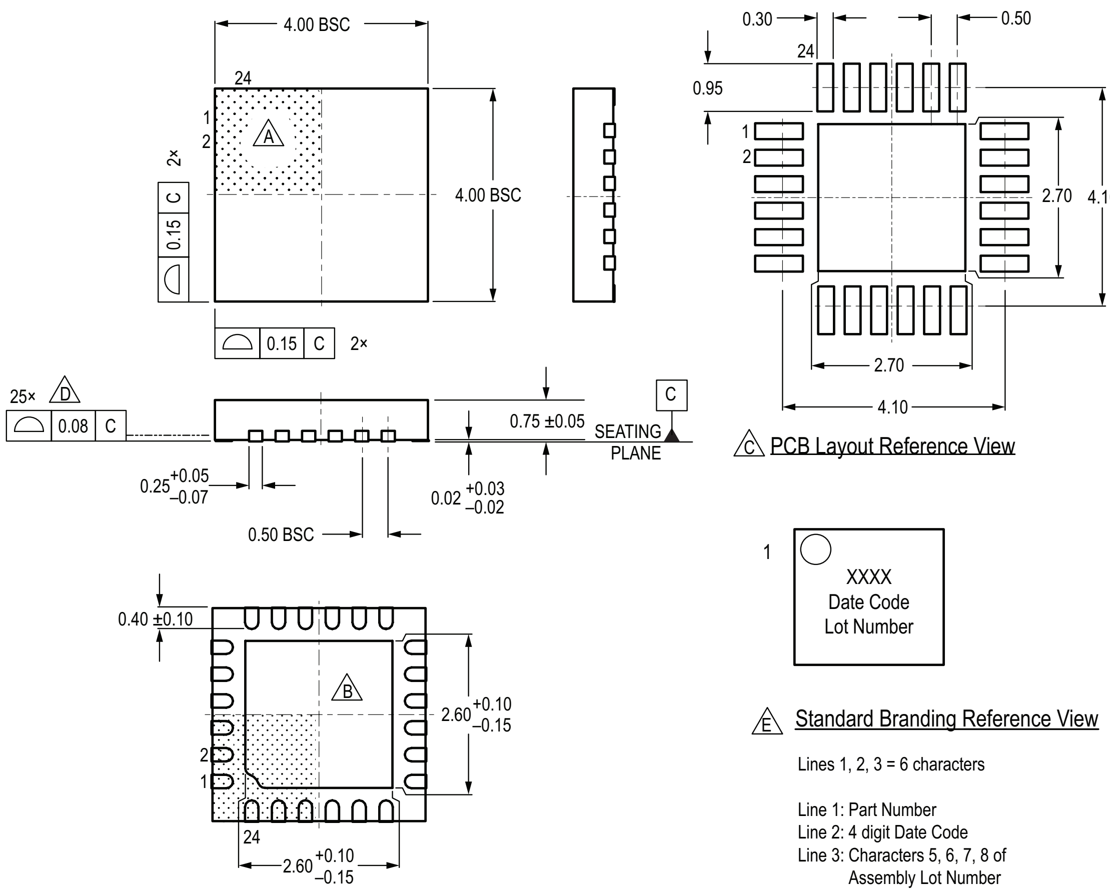
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD.)
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.



Lines 1, 2, 3 = 6 characters

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

- A Terminal #1 mark area
- B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).
- C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- D Coplanarity includes exposed thermal pad and terminals
- E Branding scale and appearance at supplier discretion.

Figure 15: Package ES, 24-Contact QFN with Exposed Pad

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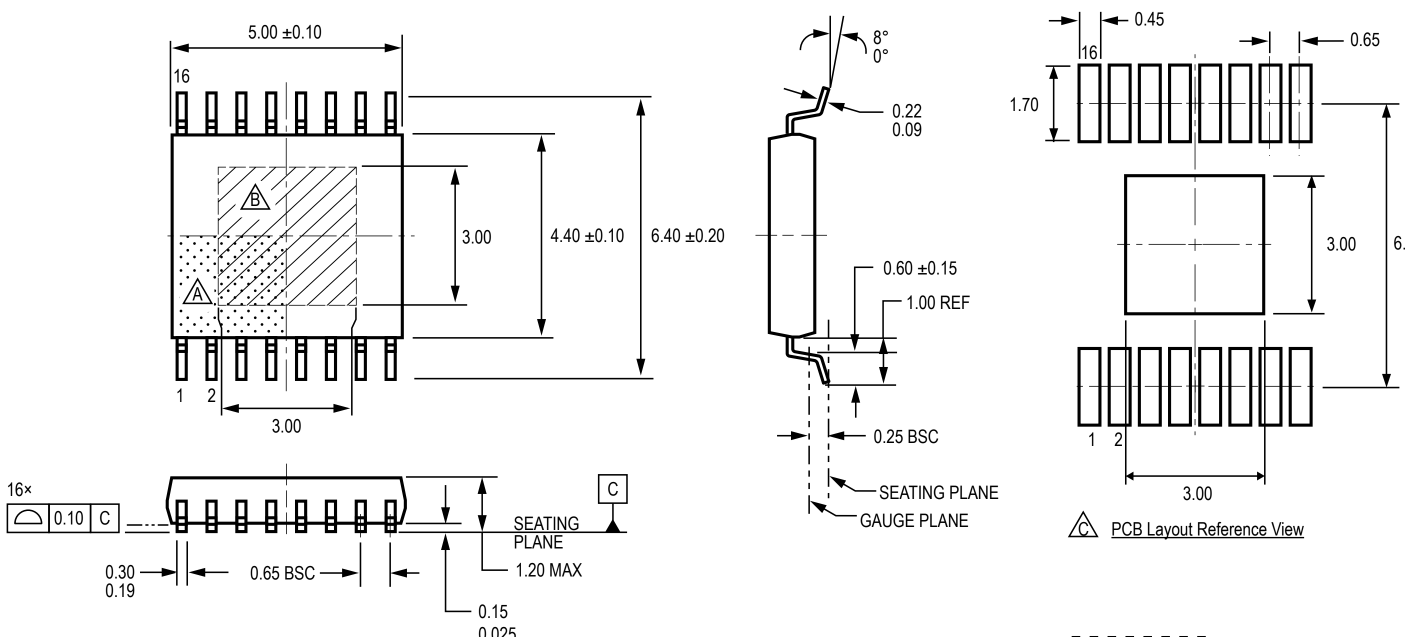
For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

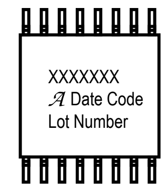


A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion



D Standard Branding Reference View

Line 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 16: Package LP, 16-Lead TSSOP with Exposed Pad

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