A5G26S004N

Airfast RF Power GaN Transistor

Rev. 2 — January 2022 Data Sheet: Technical Data

This 24 dBm RF power GaN transistor is designed for cellular base station applications covering the frequency range of 2496 to 2690 MHz.

2600 MHz

- Typical Single- Carrier W- CDMA Reference Circuit Performance: V_{DD} = 48 Vdc, I_{DQ} = 10 mA, P_{out} = 24 dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2515 MHz	18.7	18.8	10.2	–39.6
2595 MHz	19.6	20.5	9.8	–42.0
2675 MHz	18.9	20.6	9.7	–44.7

1. All data measured in reference circuit with device soldered to printed circuit board.

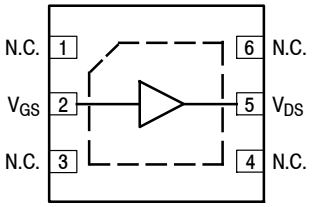
Features

- High terminal impedances for optimal broadband performance
- Designed for low complexity analog or digital linearization systems
- Universal broadband driver
- Optimized for massive MIMO active antenna systems for 5G base stations

A5G26S004N

2496–2690 MHz, 24 dBm Avg., 48 V AIRFAST RF POWER GaN TRANSISTOR

DFN 4.5 × 4 PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain- Source Voltage	V_{DSS}	125	Vdc
Gate- Source Voltage	V_{GS}	–8, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current @ T_C = 25°C	I_{GMAX}	0.74	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–55 to +150	°C
Maximum Channel Temperature	T_{CH}	225	°C

Table 2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Operating Voltage	V_{DD}	48	Vdc

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface- to- Case Case Temperature 115°C, P_D = 1.1 W	$R_{\theta JC}$ (IR)	9.5 (1)	°C/W
Thermal Resistance by Finite Element Analysis, Channel- to- Case Case Temperature 115°C, P_D = 1.1 W	$R_{\theta CHC}$ (FEA)	32 (2)	°C/W

Table 4. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS- 001- 2017)	1B
Charge Device Model (per JS- 002- 2014)	C3

Table 5. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22- A113, IPC/JEDEC J- STD- 020	3	260	°C

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Off- State Drain Leakage (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	0.74	mAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 0.74 mAdc)	$V_{GS(th)}$	–4.9	–2.6	–1.9	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_D = 10 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	–2.9	–2.5	–2.0	Vdc
Gate- Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –12 Vdc)	I_{GSS}	–0.74	—	—	mAdc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the channel temperature in degrees Celsius, *A* = –11.1 and *B* = 8366.

(continued)

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQ} = 10 mA, P_{out} = 24 dBm Avg., f = 2690 MHz, 1-tone CW.					
Power Gain	G_{ps}	18.0	20.9	24.0	dB
Drain Efficiency	η_D	20.0	22.4	—	%
P_{out} @ 6 dB Compression Point	P6dB	35.0	37.4	—	dBm
Wideband Ruggedness (2) (In NXP Reference Circuit, 50 ohm system) I_{DQ} = 10 mA, f = 2595 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 0.64 W Avg. Modulated Output Power (3 dB Input Overdrive from 0.3 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (2) (In NXP Reference Circuit, 50 ohm system) V_{DD} = 48 Vdc, I_{DQ} = 10 mA, 2515–2675 MHz Bandwidth					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	250	—	MHz
Gain Flatness in 160 MHz Bandwidth @ P_{out} = 24 dBm Avg.	G_F	—	0.9	—	dB
Fast CW, 27 ms Sweep					
P_{out} @ 6 dB Compression Point	P6dB	—	4.0	—	W
AM/PM (Maximum value measured at the P6dB compression point across the 2515–2675 MHz bandwidth)	Φ	—	–16	—	°
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP6dB	—	0.002	—	dB/°C

Table 7. Ordering Information

Device	Tape and Reel Information	Package
A5G26S004NT6	T6 Suffix = 5,000 Units, 12 mm Tape Width, 13-inch Reel	DFN 4.5 × 4

1. Part internally input matched.
2. All data measured in reference circuit with device soldered to printed circuit board.

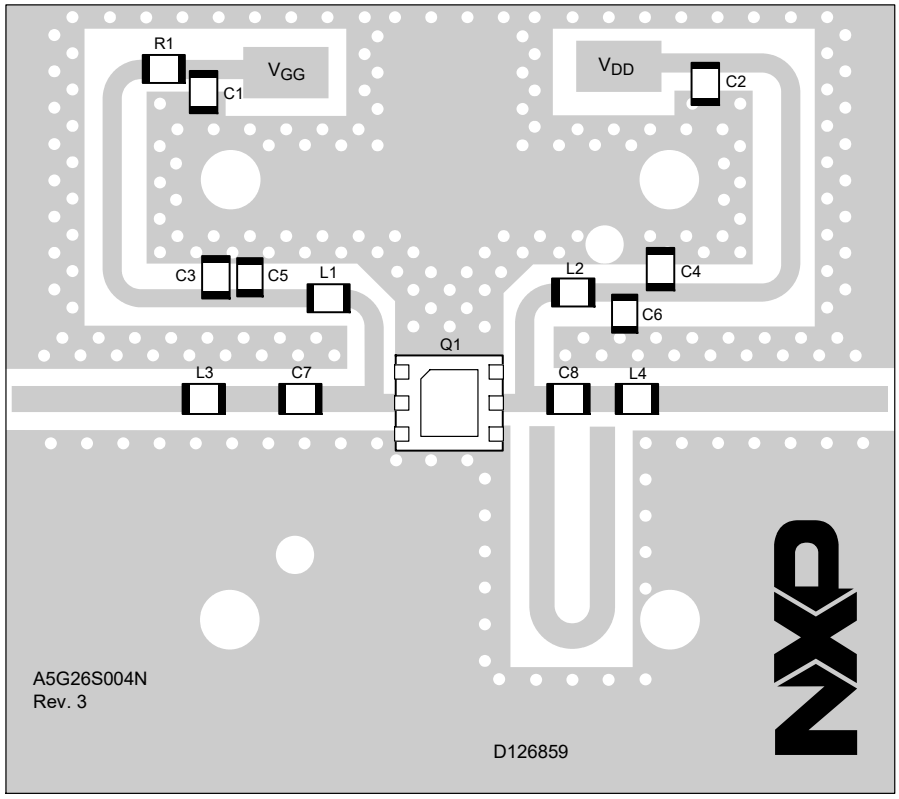
NOTE: Correct Biasing Sequence for GaN Depletion Mode Transistors

Turning the device ON

1. Set V_{GS} to the pinch-off voltage, typically –5 V.
2. Turn on V_{DS} to nominal supply voltage (+48 V).
3. Increase V_{GS} until I_{DS} current is attained.
4. Apply RF input power to desired level.

Turning the device OFF

1. Turn RF power off.
2. Reduce V_{GS} down to the pinch-off voltage, typically –5 V.
3. Adjust drain voltage V_{DS} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Turn off V_{GS}.



Note: All data measured in reference circuit with device soldered to printed circuit board. *aaa-039741*

Figure 2. A5G26S004N Reference Circuit Component Layout

Table 8. A5G26S004N Reference Circuit Component Designations and Values

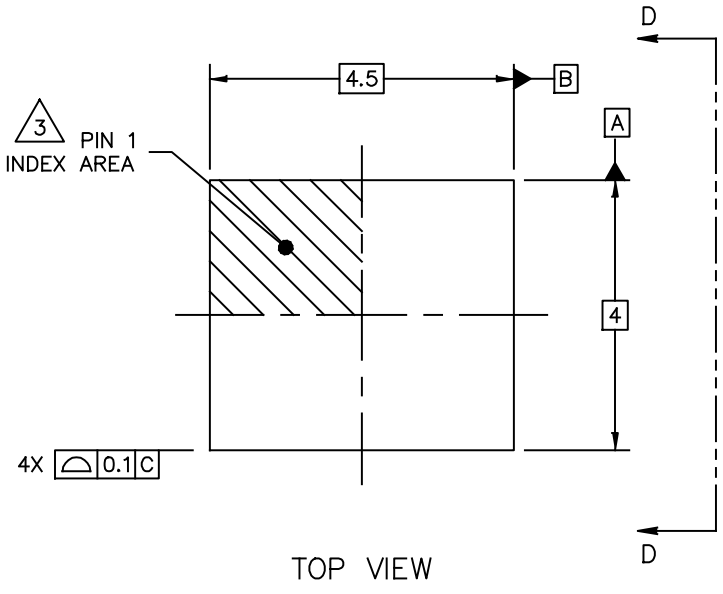
Part	Description	Part Number	Manufacturer
C1, C2	2.2 μF Chip Capacitor	GRM32ER72A225KA35L	Murata
C3, C4	1 μF Chip Capacitor	GRM31MR71H105KA88L	Murata
C5, C6, C7, C8	8.2 pF Chip Capacitor	GQM2195C2E8R2BB12D	Murata
L1	3.9 nH Chip Inductor	0603HP-3N9XJLW	Coilcraft
L2, L3	1.6 nH Chip Inductor	0603HP-1N6XJLW	Coilcraft
L4	4.7 nH Chip Inductor	0603HP-4N7XJLW	Coilcraft
Q1	RF Power GaN Transistor	A5G26S004N	NXP
R1	10 Ω, 1/8 W Chip Resistor	CRCW080510R0FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D126859	MTL

Figure 3. Product Marking

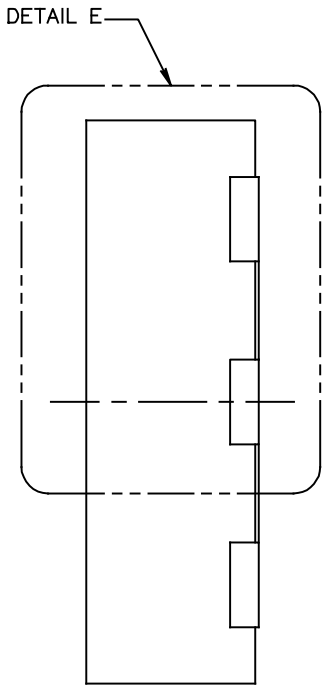
Package Information

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

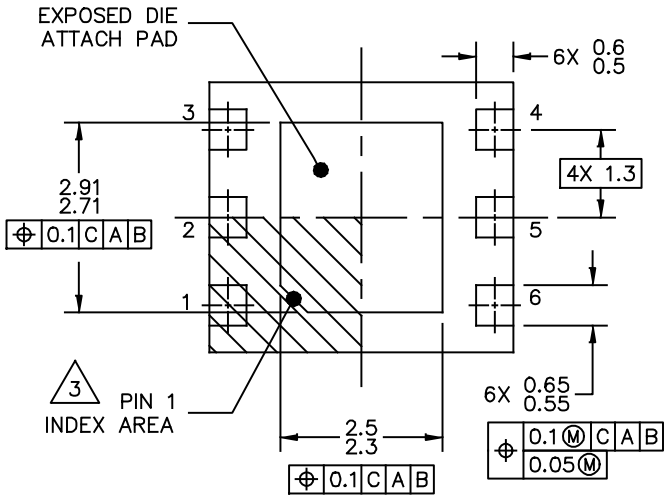
SOT2040–1



TOP VIEW



VIEW D–D



BOTTOM VIEW

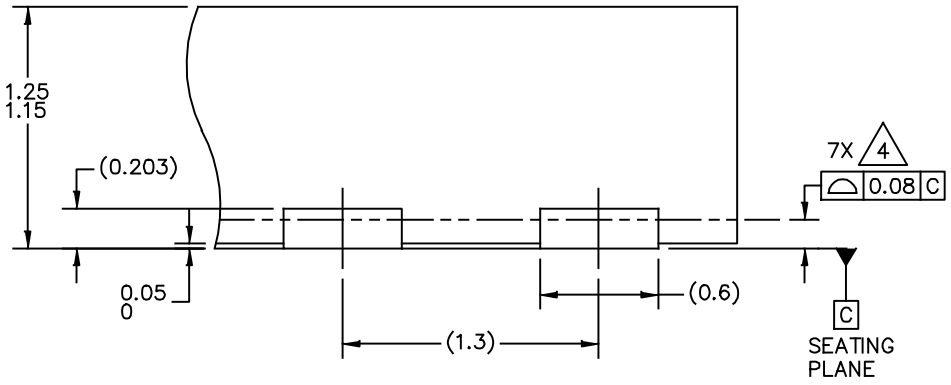
RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 1 OF 6

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



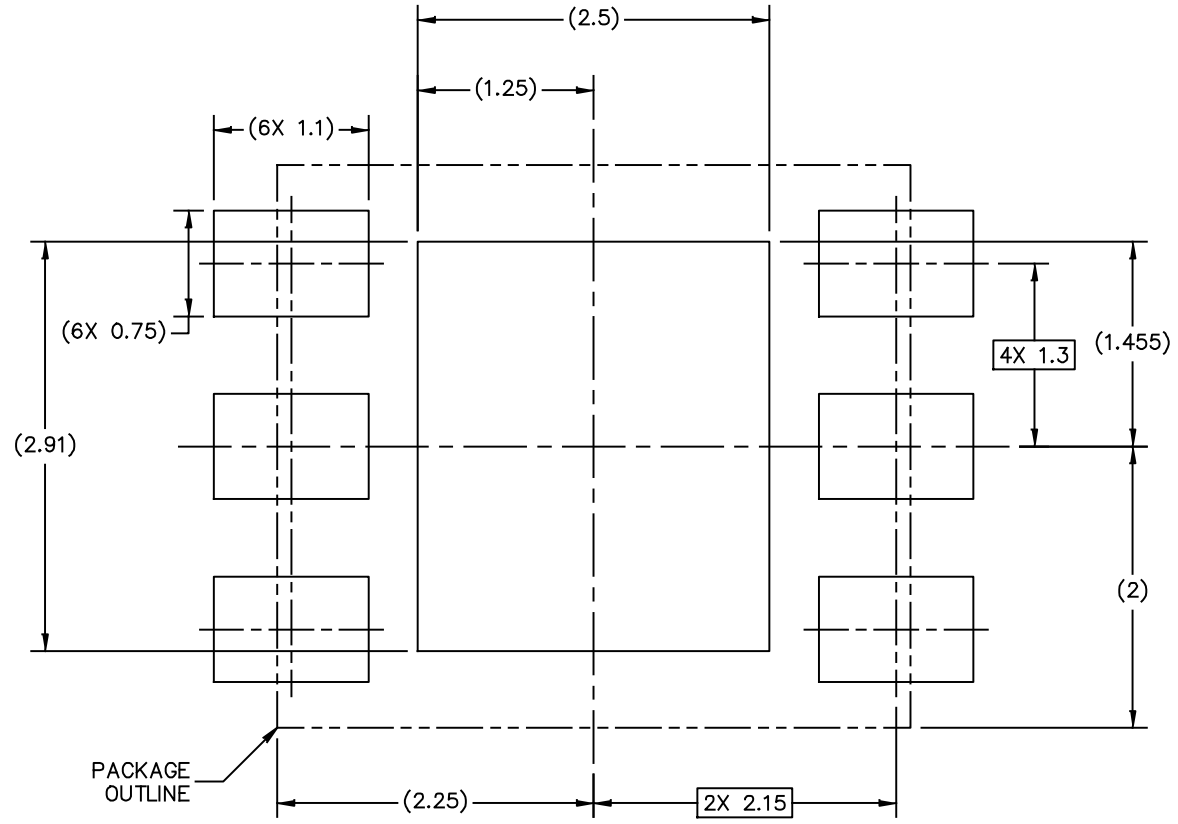
DETAIL E
VIEW ROTATED 90°CW

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 2

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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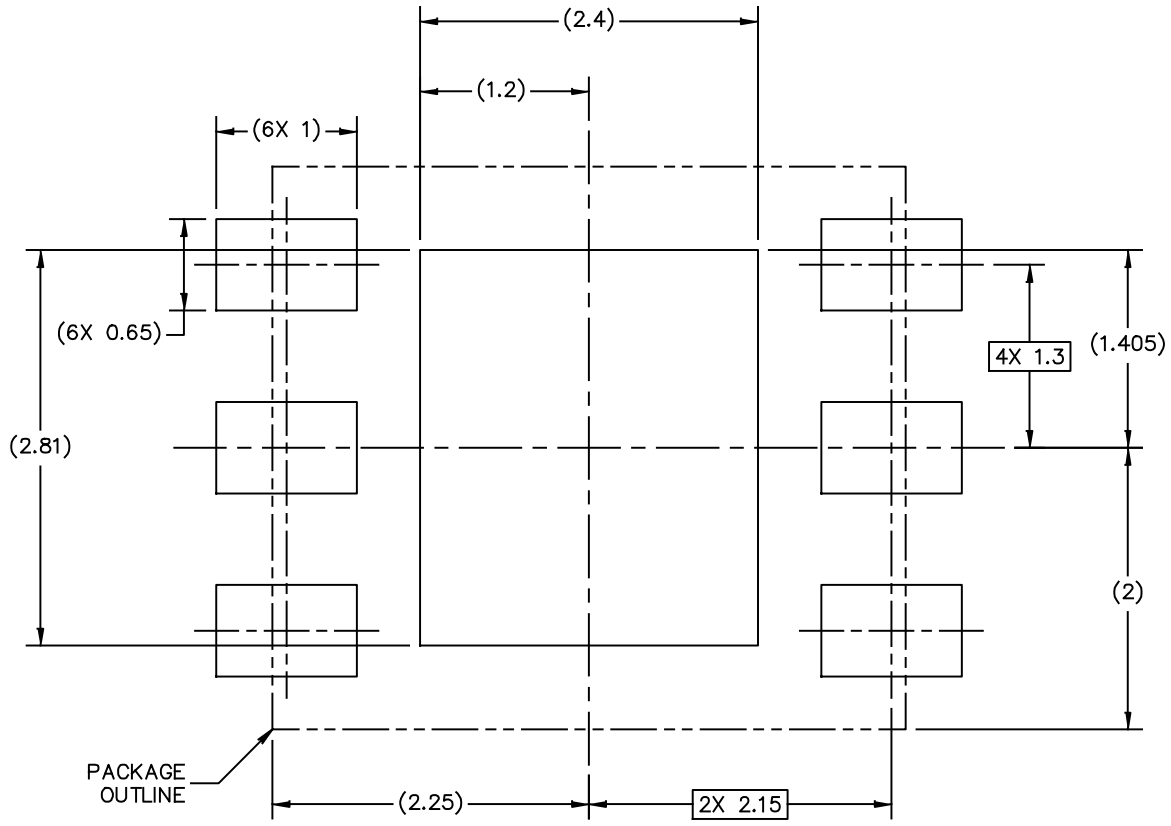
H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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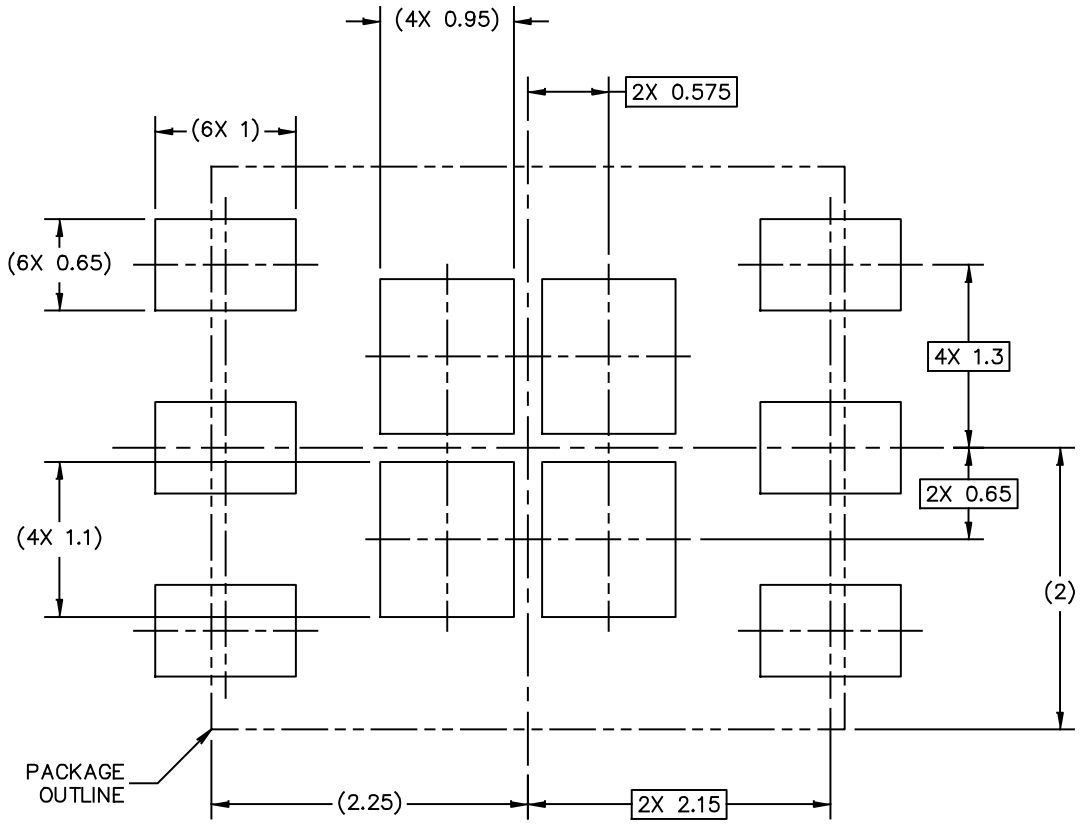
H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 5

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

DATE: 01 AUG 2019

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Product Documentation, Software and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2020	• Initial release of data sheet
1	Jan. 2021	• Table 1, Maximum Ratings: updated operating voltage for complete data sheet standardization, p. 2 • Table 2, Recommended Operating Conditions: added to data sheet, p. 2
2	Jan. 2022	• Table 6, DC On Characteristics, $V_{GS(th)}$: Min, Typ and Max values updated to match production test values, p. 2