A80803

Multi-Topology Synchronous LED Controller with PWM Dimming and High/Low Intensity Modes

FEATURES AND BENEFITS

- Wide 5 to 37 V input voltage range
  - □ 40 V absolute maximum for load dump
  - □ 4.5 V UVLO falling for idle stop
- Wide output voltage, up to 70 V OVP rating
- Single-ended topology controller with internal gate drivers for low-side and high-side external MOSFETs
  - □ Topology options including boost and buck-boost
  - □ Unique topology changeover option for high/low beam
  - □ Unique slew rate control to minimize current overshoot/undershoot during high/low transition
- Complementary gate drivers for high/low beam applications
- Options for SPI control or programmable EEPROM for design parameters, eliminates need for local microcontroller
- Internal PWM generator and driver to control external dimming MOSFET
- Fixed frequency operation with programmable dithering for EMC mitigation
- Constant current regulation
- Extensive fault detection and reporting through SPI or hardwired fault signals
- Analog dimming options for LED binning, input voltage foldback, and temperature foldback via NTC
- 5 V / 50 mA linear regulator to power external circuitry
- Four programmable current settings to adapt to LED binning

DESCRIPTION

The A80803 is a switch-mode, constant-current DC/DC controller for high-power LED automotive lighting applications. The controller is based on a programmable fixed frequency, peak current mode control architecture and can be configured in multiple different switching topologies to suit different application requirements.

Both a low-side and high-side gate driver are included to control the external power MOSFETs. Two additional gate drivers are integrated to enable/disable part of the LED string to simplify high/low beam applications.

Diagnostics can be reported through SPI or via the two fault pins. The SPI interface can also be used to control many configuration options of the A80803. Alternatively, these options can be factory-programmed and stored in EEPROM to remove the need for a local microcontroller.

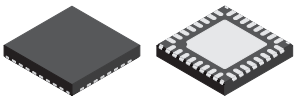
LED brightness can be controlled by a PWM signal on the EN/PWM pin or by an internal PWM signal configured via SPI. An internal driver controls a MOSFET in series with the LED string to optimize dimming. The PWMOUT driver strength is programmable via SPI to optimize LED current during PWM transitions. LED current foldback is provided for low input voltage and thermal events.

The A80803 is available in a thermally enhanced 32-pin 5 mm × 5 mm QFN package with wettable flank.

APPLICATIONS

- Automotive lighting applications

PACKAGE



32-pin 5 mm × 5 mm QFN with exposed thermal pad and wettable flank (suffix ET)

Not to scale

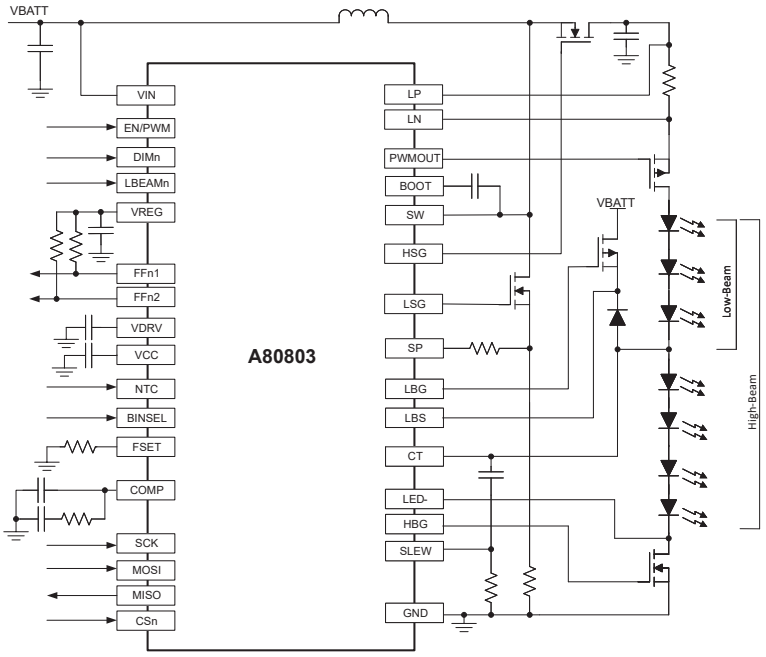


Figure 1: Simplified Block Diagram

SELECTION GUIDE

Part Number	Package	Packing [1]
A80803KETASR	32-pin 5 mm × 5 mm QFN with exposed thermal pad and wettable flank	6000 pieces per 13-inch reel

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN/PWM, DIMn, LBEAMn			–0.3 to 40	V
BOOT, HSG			–0.3 to 90	V
		t < 250 ns	–2 to 90	V
		t < 50 ns	–6 to 90	V
Boot with respect to SW	$V_{BOOT-SW}$		6.6	V
LP, LN, PWMOUT, LED–, SW, LBS, LBG, CT, SLEW			–0.3 to 80	V
LP with respect to LN	V_{LP-LN}		–0.5 to 0.5	V
PWMOUT with respect to LP	$V_{PWMOUT-LP}$		–6.6	V
LBG with respect to LBS	$V_{LBG-LBS}$		–6.6	V
HSG with respect to SW	V_{HSG-SW}		–6.6	V
VCC, BINSEL, COMP, SP			–0.3 to 3.8	V
All other pins			–0.3 to 6.6	V
Junction Temperature	T_J		–40 to 150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	°C/W

[3] Additional thermal information available on the Allegro website.

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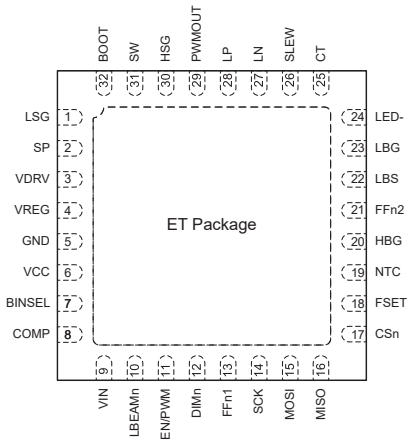
TERMINAL DIAGRAM AND TERMINAL LIST



ET-32 Package Terminals

Terminal List

Number	Name	Function
1	LSG	Low side gate driver to drive main switching MOSFET in all topologies.
2	SP	Current sense input and slope comp for current mode control of regulator.
3	VDRV	Output of internal LDO used as power supply for internal gate drivers. Use a 2.2 µF ceramic capacitor from V_{DRV} to ground. This pin should not be used to power external circuitry.
4	VREG	Output of 5 V / 50 mA LDO. Place a 2.2 µF capacitor on this pin for stability.
5	GND	Ground pin
6	VCC	Voltage rail for internal circuits. Place a 1 µF capacitor here. This pin should only be used for a voltage divider to BINSEL pin and should not drive external circuitry.
7	BINSEL	Binning pin with four binning levels. Selects reference value for current regulation
8	COMP	Compensation pin to stabilize the regulation loop.
9	VIN	Input voltage pin
10	LBEAMn	Low/High beam control. LBEAMn = 0 sets low-beam operation, LBEAMn = 1 sets high-beam operation.
11	EN/PWM	Input for external PWM pulses. PWMOUT can be controlled by this pin in external PWM mode. Pin can also be used as chip enable. A80803 is disabled if this pin is held low for longer than $t_{DIS,EN/PWM}$.
12	DIMn	Selects internal or external PWM dimming. External PWM is used when DIMn is high.
13	FFn1	Open drain active low signal. Pulls low when any fault is detected.
14	SCK	Serial interface clock signal.
15	MOSI	Serial interface input.
16	MISO	Serial interface output.
17	CSn	Chip Select, active low.
18	FSET	Switching frequency programming pin. Connect a resistor form this pin to GND to set the converter switching frequency.
19	NTC	Temperature-controlled analog dimming pin. A voltage on this pin controls the regulated output current.
20	HBG	Gate driver output for high-beam boost topology NFET. Driver is with respect to GND pin.
21	FFn2	Open drain active low signal. Pulls low when selected faults are detected.
22	LBS	Source connection of low-beam buck-boost topology PFET. Tie to VIN if not used.
23	LBG	Gate driver output for low-beam buck-boost topology PFET. Driver is with respect to LBS pin.
24	LED-	Negative end of high-beam LED string (total string).
25	CT	Negative end of low-beam LED string, center tap (partial string).
26	SLEW	Filter connection for control of slew rate on topology switch over MOSFETs, LBG, and HBG.
27	LN	LED current negative sense voltage. A resistor placed between LP and LN sets the current in the LED string.
28	LP	LED current positive sense voltage. A resistor placed between LP and LN sets the current in the LED string.
29	PWMOUT	PWM output to drive high side PFET for PWM dimming of LED string.
30	HSG	High side gate driver to drive synchronous MOSFET.
31	SW	Regulator switch node connect to node.
32	BOOT	BOOT voltage for high side gate driver. Place a 0.1 µF capacitor between BOOT and SW for gate drive current.
–	PAD	Tie to GND plane for optimal thermal performance.

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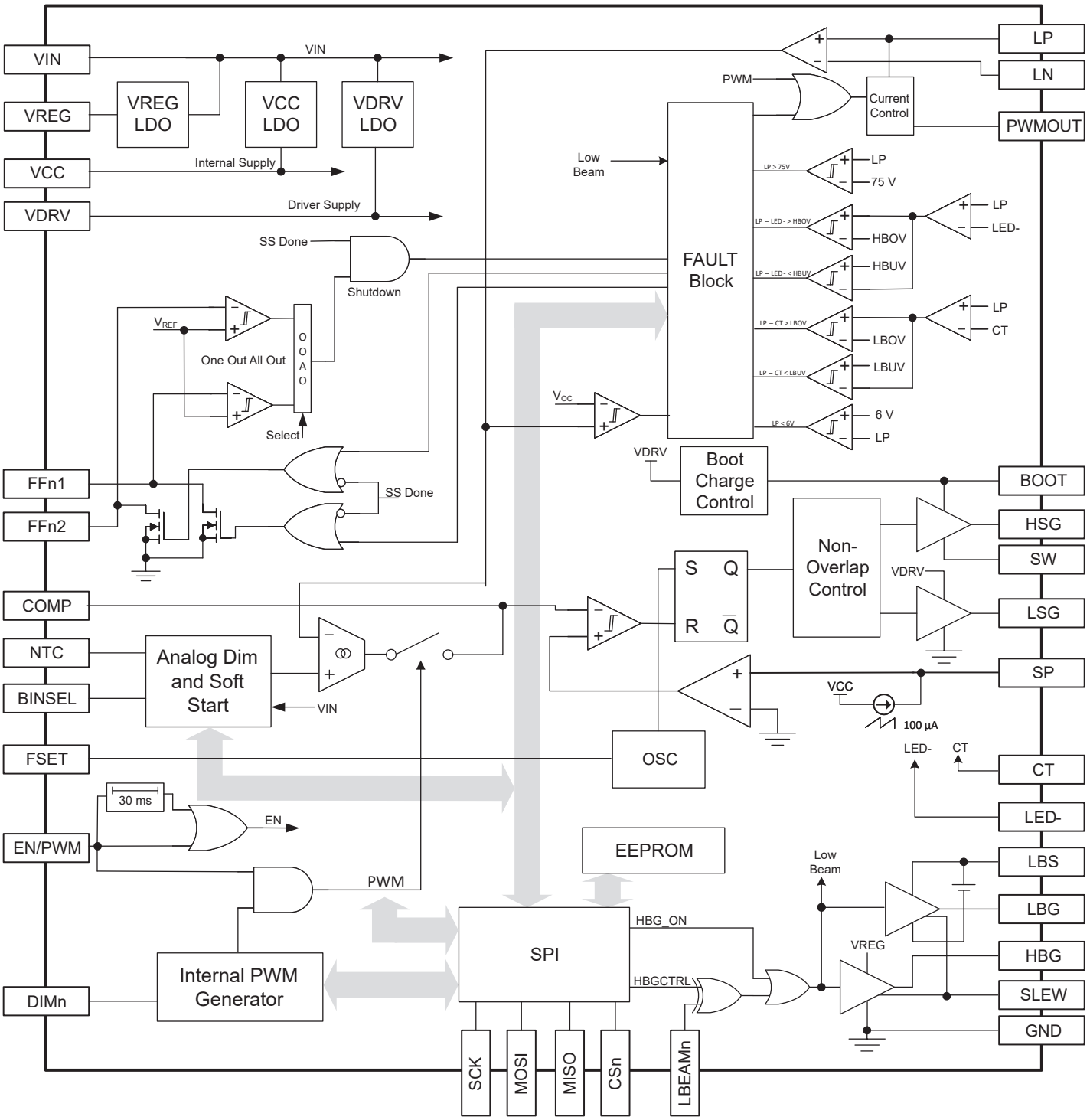
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS [1]: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL INPUTS						
Operating Input Voltage Range	V_{VIN}		5	–	37	V
Programmable Input Switching Threshold	$V_{VIN,UV,H}$	V_{VIN} rising, V_{INUV} = Code 0	5.40	5.65	5.90	V
	$V_{VIN,UV,TOL}$	V_{INUV} = Code 0	–0.25	–	+0.25	V
	$V_{VIN,UV,L}$	V_{VIN} falling, V_{INUV} = Code 0	4.50	4.75	5.00	V
Input VCC and VREG Undervoltage	$V_{VIN,VCC,ON}$	V_{VIN} rising, VCC and VREG start up	4.2	4.5	4.8	V
	$V_{VIN,VCC,OFF}$	V_{VIN} falling, VCC and VREG start up	3.9	4.2	4.5	V
	$V_{VIN,VCC,HYS}$	V_{VIN} hysteresis when VCC and VREG shutdown	–	0.3	–	V
Input Overvoltage	$V_{VIN,OV,H}$	V_{INOV} = Code 7 (35 V is selected)	–	35	–	V
Input Overvoltage Tolerance	$V_{VIN,OV,TOL}$	V_{INOV} = x (all possible voltages)	–1.3	–	+1.3	V
Input Overvoltage Hysteresis	$V_{VIN,OV,HYS}$	V_{INOV} = x (all possible voltages)	–	1	–	V
Operating Input Current	$I_{VIN,OP}$	Operating, no switching, EN/PWM = 1	–	8	–	mA
Standby Input Current [3]	$I_{VIN,STANDBY}$	Standby mode, EN/PWM = 0, VREG_EN = 0, V_{VIN} = 14 V	–	–	160	µA
		T_J = 25°C	–	90	120	µA
Input Switching UV Deglitch Timer	$t_{UV,FLT}$		9	10	11	ms
Startup Fault Blank Time	t_{FB}	SFST = Code 3	–	21.5	–	ms
LINEAR REGULATOR (VREG)						
VREG Output Voltage	V_{VREG}	I_{VREG} = 0 to 50 mA, 6 V ≤ V_{VIN} ≤ 18 V	4.9	–	5.1	V
VREG Dropout	$V_{VREG,DROP}$	I_{VREG} = 50 mA, V_{VIN} = 5 V	–	–	0.3	V
VREG Overcurrent Limit	$I_{VREG,OC}$	V_{VREG} = 4.85 V, 7 V ≤ V_{VIN} ≤ 18 V	55	–	80	mA
VREG Foldback Current	$I_{VREG,FB}$	V_{VREG} = 0 V, 5 V ≤ V_{VIN} ≤ 18 V	–	16	–	mA
VREG Undervoltage	$V_{VREG,UV}$		–	4.5	–	V
VREG Undervoltage Hysteresis	$V_{VREG,UV,HYS}$		–	240	–	mV
DRIVER POWER SUPPLY (VDRV)						
VDRV Output Voltage	V_{VDRV}	I_{VDRV} = 20 mA, 6.5 V ≤ V_{VIN} ≤ 18 V	5.8	–	6.2	V
VDRV Dropout	$V_{VDRV,DROP}$	I_{VDRV} = 20 mA, V_{VIN} = 6 V	–	–	0.6	V
INTERNAL REGULATOR (VCC)						
VCC Output Voltage	V_{VCC}	I_{VCC} = 0 to 5 mA, 6 V ≤ V_{VIN} ≤ 18 V	3.2	–	3.4	V
OSCILLATOR						
Oscillator Frequency	f_{OSC}	R_{FSET} = 100 kΩ	315	350	385	kHz
MAIN REGULATOR (LSG, HSG, BOOT, SW)						
Gate Driver Turn On Time [3]	t_r	C_{LOAD} = 1 nF, 20% to 80%	–	7.5	–	ns
Gate Driver Turn Off Time [3]	t_f	C_{LOAD} = 1 nF, 80% to 20%	–	5	–	ns
LSG Minimum Off Time	$t_{off,MIN}$		–	–	135	ns
LSG Minimum On Time	$t_{on,MIN}$		–	–	135	ns

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[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MAIN REGULATOR (LSG, HSG, BOOT, SW) (continued)						
LSG to GND High Voltage	V_{LSG}	6 V ≤ V_{VIN} ≤ 18 V	5.7	–	6.2	V
Low Side Gate Driver Source Current	$I_{LSG,H}$	V_{VDRV} = 6 V, V_{LSG} = 1.5 V	–	1.4	–	A
Low Side Gate Driver Sink Current	$I_{LSG,L}$	V_{VDRV} = 6 V, V_{LSG} = 2.0 V	–	1.6	–	A
HSG to SW High Voltage	$V_{HSG,SW}$	V_{BOOT} – V_{SW} = 5.3 V	–	5.3	–	V
High-Side Gate Driver Source Current	$I_{HSG,H}$	V_{VDRV} = 6 V, V_{BOOT} – V_{SW} = 5.3 V, $V_{HSG,SW}$ = 1.5 V	–	1.3	–	A
High Side Gate Driver Sink Current	$I_{HSG,L}$	V_{VDRV} = 6 V, V_{BOOT} – V_{SW} = 5.3 V, V_{HSG} = 2.0 V	–	1.5	–	A
INNER CURRENT LOOP CONTROL (SP, COMP)						
Current Sense Input (SP) Bias Current	I_{BIAS}	V_{SP} = 300 mV	–	–20	–	µA
Current Sense (SP) Overload Switch Threshold Voltage	$V_{SP,OL}$		370	400	440	mV
Switch Current Overload Filter Time	$t_{SC,OL}$		–	64	–	Clock cycles
Switch Current Sense Amplifier Voltage Gain	A_{CS}		–	2.25	–	V/V
Slope Compensation Peak Current	I_{SLOPE}		–116	–	–93	µA
OUTER CURRENT LOOP CONTROL (LP, LN)						
Input Bias Current LN	I_{LN}	V_{LP} = V_{LN} = 14 V	–	500	–	nA
Input Bias Current LP	I_{LP}	V_{LP} = V_{LN} = 14 V	–	1	–	mA
Differential Sense Voltage	$K_{BIN}V_{IDL}$	EN/PWM = 1, V_{IDL} = V_{LP} – V_{LN}, k_{BINx} = k_{VIN} = k_{NTC} = 1	196	200	204	mV
		EN/PWM = 1, V_{IDL} = V_{LP} – V_{LN}, k_{BINx} = 0.625, k_{VIN} = k_{NTC} = 1	119	125	131	mV
		k_{BINx} = k_{NTC} = 1, k_{VIN} = 0.2	–	40	–	mV
Input Common Mode Range	$V_{LP,CM}$		6	–	70	V
Error Amplifier Open Loop DC Gain [3]	A_{VEA}		–	62	–	dB
Transconductance	g_{mCOMP}		1100	1500	1900	µA/V
COMP Sink Current	$I_{COMP,sink}$	V_{COMP} = 0.8 V, V_{LP} – V_{LN} = 250 mV	–	1	–	mA
COMP Source Current	$I_{COMP,source}$	V_{COMP} = 0.8 V, V_{LP} – V_{LN} = 150 mV	–	–105	–	µA
COMP Leakage Current	$I_{LCOMP,LKG}$	V_{COMP} = 1 V, No switching	–	±200	–	nA
Overcurrent Threshold	$V_{IDL,OC}$	LP wrt LN	260	320	380	mV
Overcurrent Hysteresis	$V_{IDL,OC,HYS}$		–	30	–	mV
LED Output Overcurrent Filter Time	t_{OPI}	OCFILT = Code 0	–	2	–	clock cycles
LED Output Undervoltage Filter Time	t_{OPV}		–	30	–	clock cycles
Hiccup Shutdown Period	t_{HIC}	LED overcurrent or output undervoltage or overvoltage or switch overload	9	10	11	ms
THERMAL PROTECTION						
Overtemperature Shutdown Threshold	T_{JF}	Temperature increasing	155	170	–	°C
Overtemperature Hysteresis	ΔT_J	Recovery = T_{JF} – ΔT_J	–	20	–	°C

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM DIMMING AND ENABLE (EN/PWM, PWMOUT, DIMN)						
Disable Time	$t_{DISEPWM}$	EN/PWM = 0	24.8	30	35	ms
EN/PWM Low Voltage	$V_{EN/PWML}$		–	–	0.3	V
EN/PWM High Voltage	$V_{EN/PWMH}$		2	–	–	V
EN/PWM to PWMOUT Propagation Delay	$t_{prop,DLY}$	V_{LP} = 10 V	–	2.6	–	µs
PWMOUT Low Voltage	V_{PWMLO}	PFET on, PWMOUT wrt LP, VLP = 10V	–6.6	–5.5	–4.5	V
Peak Pull-Up Current	I_{PULLUP}	EN/PWM = 0, PWMOUT wrt LP = 0 V, PWM_DRV = Code 0	–	–25	–	mA
Peak Pull-Down Current	$I_{PULLDOWN}$	EN/PWM = 1, PWMOUT wrt LP = –5.5 V, PWM_ DRV = Code 0	–	25	–	mA
Internal PWM Clock Frequency Tolerance	$f_{PWM,int}$		–10	–	+10	%
External PWM Frequency	$f_{PWM,ext}$		100	–	1000	Hz
External PWM Duty Cycle	$D_{PWM,ext}$	$f_{PWM,ext}$ = 500 Hz	5	–	95	%
LP Undervoltage PWMOUT Turn-On	$V_{PWMUVON}$	Measured at LP wrt GND	–	–	6.3	V
LP Undervoltage PWMOUT Turn-Off	$V_{PWMUVOFF}$	Measured at LP wrt GND	5.5	–	–	V
DIMn Low Voltage	V_{DIMnL}		–	–	0.3	V
DIMn High Voltage	V_{DIMnH}		2	–	–	V
DIMn Deglitch Time	$t_{deglitch,DIMn}$		90	100	110	µs
LOW/HIGH BEAM (LBEAMN, LBG, LBS, HBG)						
LBEAMn Low Voltage	$V_{LBEAMnLO}$		–	–	0.3	V
LBEAMn High Voltage	$V_{LBEAMnHi}$		2	–	–	V
LBEAMn Deglitch Time	$t_{deglitch,LBEAMn}$		90	100	110	µs
LBG to LBS Low Voltage	$V_{LBG,LO}$	LBEAMn = 0, LBG wrt LBS, V_{LBS} = 10 V	–6.5	–5.5	–4.5	V
LBG Peak Pull-Up Current	$I_{LBG,PULLUP}$	LBEAMn = 1, LBG wrt LBS = 0 V, V_{LBS} = 10 V	–	–0.24	–	mA
LBG Peak Pull-Down Current	$I_{LBG,PULLDOWN}$	LBEAMn = 0, LBG wrt LBS = –5 V, V_{LBS} = 10 V	–	0.24	–	mA
HBG to GND High Voltage	$V_{HBG,LO}$	LBEAMn = 1, HBG wrt GND, V_{VIN} = 10 V	V_{VREG} – 0.1	–	V_{VREG}	V
HBG Peak Pull-Up Current	$I_{HBG,PULLUP}$	LBEAMn = 1, HBG wrt GND = 0 V	–	–0.24	–	mA
HBG Peak Pull-Down Current	$I_{HBG,PULLDOWN}$	LBEAMn = 0, HBG wrt GND = V_{VREG}	–	0.24	–	mA
PROTECTION FEATURES						
Output Over/Undervoltage Tolerance	$V_{OV/UVTOL}$		–1 V – 1% OV/UV	–	1 V + 1% OV/UV	V
Output Overvoltage Hysteresis	V_{OVHYS}		–	0.5	–	V
Fixed Overvoltage Protection	$V_{OV,FIXED}$	Measured between LP and GND when rising	72	75	78	V
Fixed Overvoltage Hysteresis	$V_{OV,HYS}$	Measured between LP and GND when falling	–	1	–	V
Strong Short Protection	$V_{STG,SHT}$	Measure between LP and GND	–	1	–	V
CT Undervoltage Protection	$V_{CT,UV}$	Measured between CT and GND when falling	–	2	–	V
CT Undervoltage Hysteresis	$V_{CT,UV,HYS}$	Measured between CT and GND when rising	–	0.4	–	V

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FAULT REPORTING (FFN1, FFN2)						
FFnx Output (Open Drain)	$V_{FFn,OL}$	I_{OL} = 1 mA, Fault asserted	–	–	0.4	V
FFnx Output Leakage Current	$I_{FFn,OH}$	V_{FFnx} = 5.5 V, fault not asserted	–1	–	1	µA
SERIAL COMMUNICATION (MOSI, MISO, SCK, CS)						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input Low Voltage	V_{IH}	All logic inputs	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	250	550	–	mV
Input Pull-Down MOSI, SCK	R_{PDS}	0 < V_{IN} < 5 V	–	50	–	kΩ
Input Pull-Up Current to VCC	I_{PU}	$\overline{SS}$	–	100	–	µA
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	0.2	0.4	V
Output Low Voltage	V_{OH}	I_{OL} = –1 mA [1]	2.4	V_{VCC} – 0.2	–	V
Output Leakage [1]	I_{OH}	0 V < V_{SDO} < 5.5 V, $\overline{SS}$ = 1	–1	–	1	µA
Clock High Time [3]	t_{SCKH}	A in Figure 2	50	–	–	ns
Clock Low Time [3]	t_{SCKL}	B in Figure 2	50	–	–	ns
Strobe Lead Time [3]	t_{STLD}	C in Figure 2	30	–	–	ns
Strobe Lag Time [3]	t_{STLG}	D in Figure 2	30	–	–	ns
Strobe High Time [3]	t_{STRH}	E in Figure 2	300	–	–	ns
Data Out Enable Time [3]	t_{SDOE}	F in Figure 2	–	–	40	ns
Data Out Disable Time [3]	t_{SDOD}	G in Figure 2	–	–	30	ns
Data Out Valid Time From Clock Falling [3]	t_{SDOV}	H in Figure 2	–	–	40	ns
Data Out Hold Time From Clock Falling [3]	t_{SDOH}	J in Figure 2	5	–	–	ns
Data In Set-Up Time To Clock Rising [3]	t_{SDIS}	K in Figure 2	15	–	–	ns
Data In Hold Time From Clock Rising [3]	t_{SDIH}	L in Figure 2	10	–	–	ns

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[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Ensured by design and characterization, not production tested.

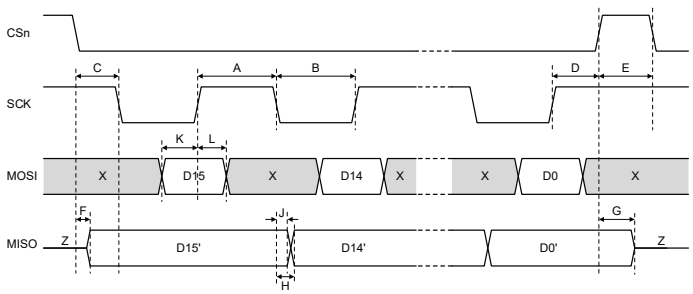

Figure 2: Serial Interface Timing Diagram

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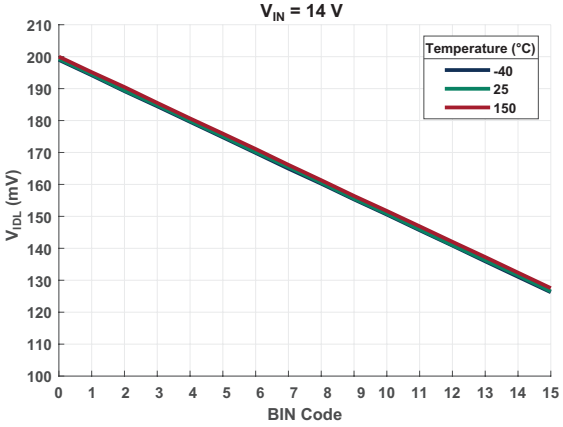
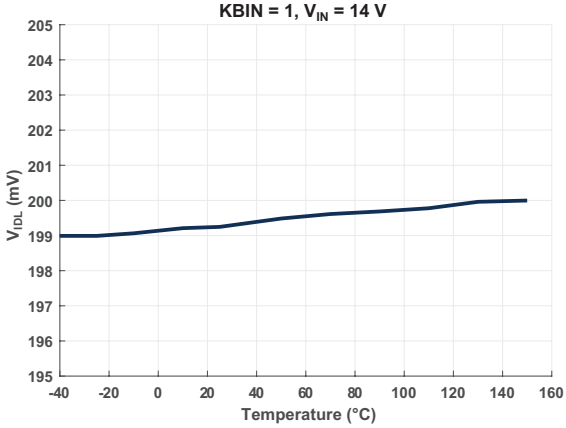
TYPICAL OPERATING CHARACTERISTICS

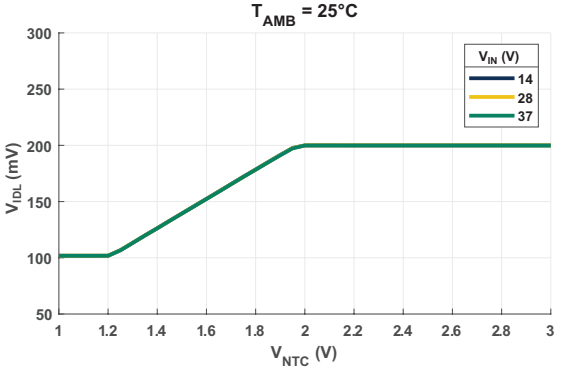
V_{IDL} (LP - LN) vs. BIN Code
V_{IN} = 14 V



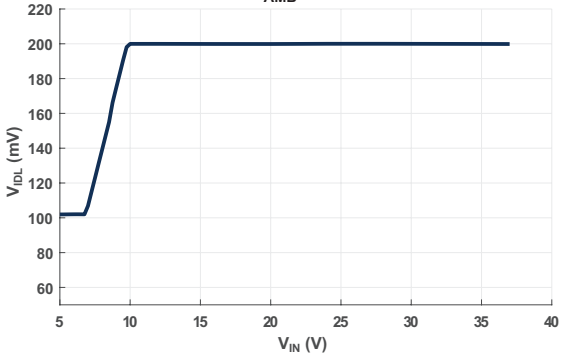
V_{IDL} (LP - LN) vs. Temperature
KBIN = 1, V_{IN} = 14 V



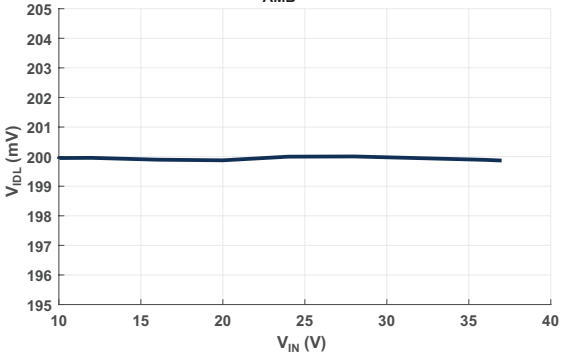
V_{IDL} (LP - LN) vs. V_{NTC}
KBIN = 1, KNTC = 0.5
V_{NTC1} = 2 V, SF1NTC = 0.672
T_{AMB} = 25°C



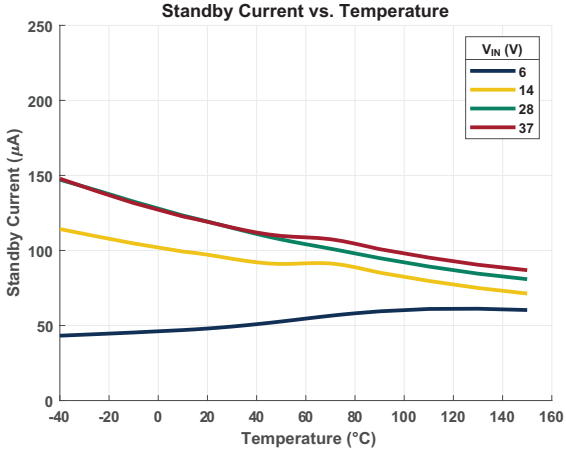
V_{IDL} (LP - LN) vs. V_{IN}
KBIN = 1, KVIN = 0.5
V_{IN1} = 10 V, SF1VIN = 0.1625
T_{AMB} = 25°C



V_{IDL} (LP - LN) vs. V_{IN}
KBIN = 1, KVIN = 0.5
V_{IN1} = 10 V, SF1VIN = 0.1625
T_{AMB} = 25°C



Standby Current vs. Temperature



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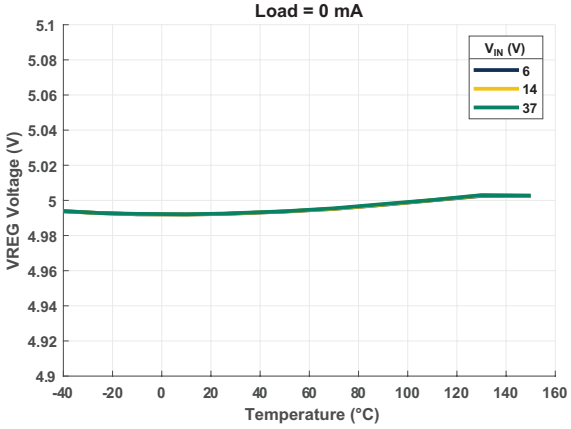
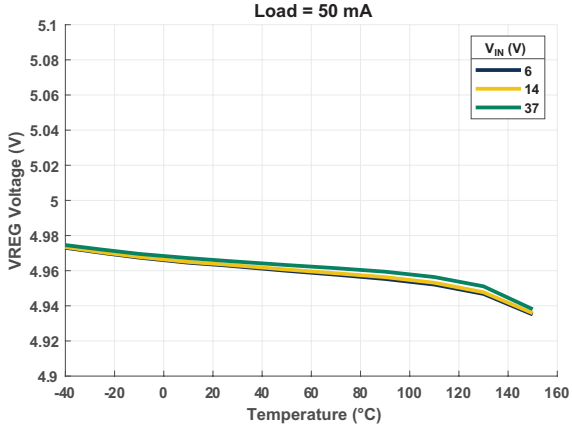
TYPICAL OPERATING CHARACTERISTICS (continued)

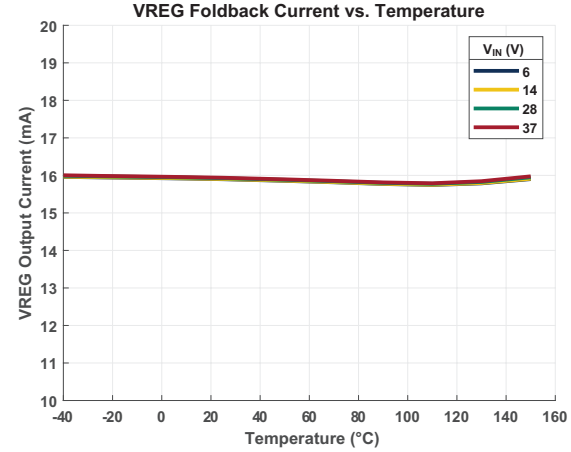
V_{REG} Voltage vs. Temperature
Load = 0 mA



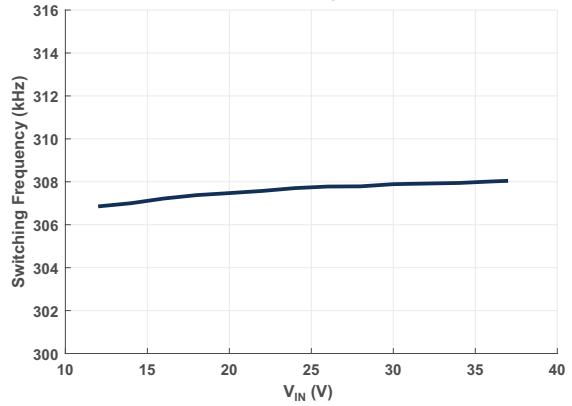
VREG Voltage vs. Temperature
Load = 50 mA



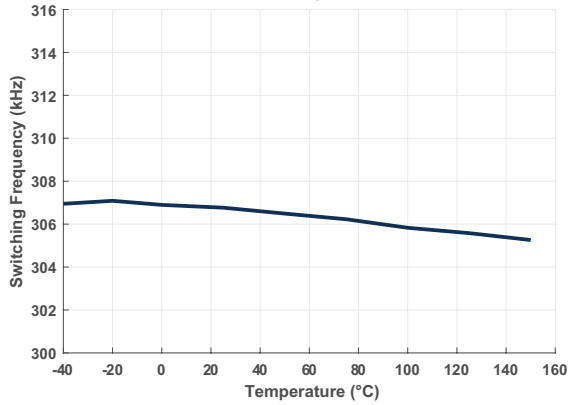
VREG Foldback Current vs. Temperature



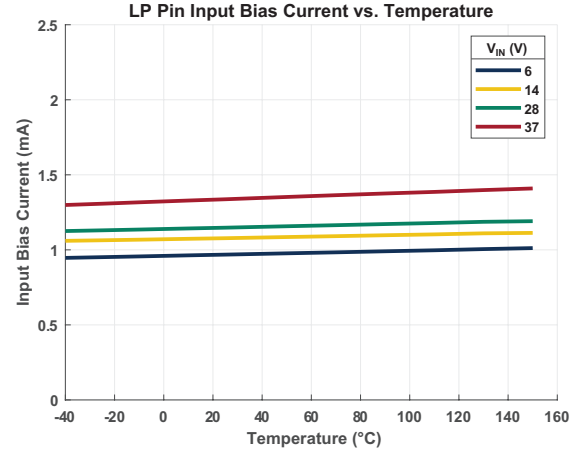
Switching Frequency vs. V_{IN}
T_{AMB} = 25°C, R_{FSET} = 115 kΩ



Switching Frequency vs. Temperature
V_{IN} = 14 V, R_{FSET} = 115 kΩ



LP Pin Input Bias Current vs. Temperature



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FUNCTIONAL DESCRIPTION

The A80803 is a switch-mode, constant-current controller for high-power LED automotive lighting applications. The controller is based on a programmable fixed-frequency, peak current mode control architecture. The switching power supply can be configured in multiple different switching topologies to suit different application requirements. For each configuration, the appropriate loop compensation and slope compensation passive components must be selected for optimal performance.

The A80803 integrates all necessary control elements to provide a cost-effective solution for a DC-DC controller using external MOSFETs. The maximum LED current is programmable by external sense resistor selection. The LED current can be modulated by an internal PWM signal or can sync to an external PWM signal for direct PWM control on the EN/PWM pin.

The maximum LED current can be adjusted based on one of four binning levels on the BINSEL pin and further derated at low input voltage, high temperature, or both.

The A80803 handles several hardware fault conditions and reports fault status on the active low FFn1 and FFn2 pins. FFn2 can be configured to report or ignore fault conditions and has a programmable assertion delay.

Power Converter Operation

The A80803 provides the necessary blocks to create a switch mode power supply with a single low-side control MOSFET and optionally a high-side synchronous MOSFET, including output current sense, error amplifier with external compensation, resistor programmable switching frequency, and two gate drivers. The EN/PWM pin is a dual function pin, acting as enable if held high, and acting as the PWM input for LED dimming if pulsed with an off-time less than $t_{DIS,EN/PWM}$.

Switching Frequency

The oscillator for the main power converter is programmable using a resistor to ground and is programmable from 70 to 700 kHz. The relationship between the switching frequency and the programming resistor is shown in Figure 3 and Equation 1 below. Keep R_{FSET} within the range of 50 to 500 kΩ as beyond this range the A80803 detects R_{FSET} open and short faults.

Equation 1:

$$R_{FSET} = 35000 / f_{SW}$$

where R_{FSET} is in kΩ and f_{SW} is in kHz

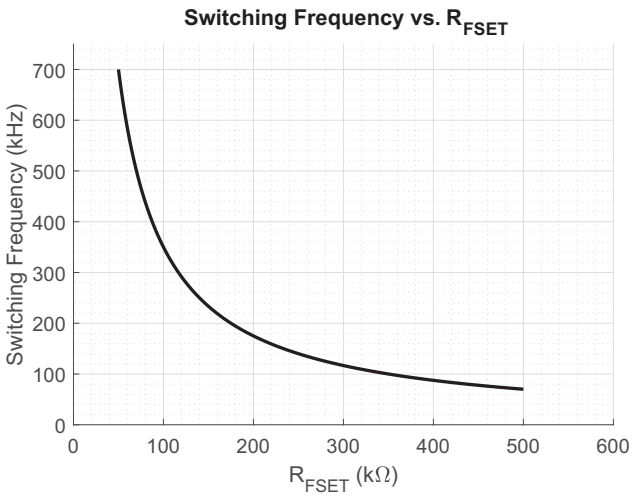

Figure 3: Switching Frequency vs. FSET Resistor

Frequency Dithering

The oscillator also includes dithering which reduces EMI of the power converter. By default, dithering is set to a 10% frequency sweep with 10 kHz modulation. Additional frequency dithering values are available through the SPI interface by accessing the DITH_FRNG and DITH_MOD fields in CONFIG0.

Table 1: Dithering Frequency

Dithering Frequency	DITH_FRNG[1:0]
Off	00
±5%	01
±10%	10
±15%	11

Table 2: Dithering Modulation

Dithering Modulation	DITH_MOD[1:0]
10 kHz	00
5 kHz	01
15 kHz	10
22 kHz	11

Power Stage Gate Drivers

The two main power converter gate drivers provide drive signals to external NMOS devices. The low-side gate driver controls the power flow in the converter. The high-side gate driver allows for efficient delivery of inductor current to the load.

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The A80803 includes a boot circuit that allows the use of an NMOS device for the high-side switch. The boot circuit operates at the main converter switching frequency.

Soft Start

Soft start can be programmed from 5 to 20 ms in 5 ms steps using the SFST field in the CONFIG1 register.

Table 3: Soft Start Time

Soft Start Time	SFST[1:0]
5 ms	00
10 ms	01
15 ms	10
20 ms	11

During the soft soft time, the A80803 operates asynchronously. This prevents reverse conduction through the high-side power switch in the event of starting into a pre-biased output. Upon the completion of soft start, the A80803 automatically switches to synchronous operation to improve efficiency.

Current Sensing

The control loop depends on two current sense circuits. The inner current-sense loop provides the inductor current information for peak current mode control. A series resistor in this circuit allows the user to program the slope compensation to ensure a stable loop under all operating conditions. The outer loop uses an external current sense resistor to control the DC current in the load.

Switch Current Sensing

The current through the inner loop is measured by the external sense resistor, R_{SP}, and the amplifier at the SP pin. The SP pin provides peak-current information to determine duty cycle for the switching converter and a cycle-by-cycle current limit for the switching MOSFET. A resistor at the input of the SP pin, R_{SLOPE}, sets the slope compensation to prevent subharmonic oscillations at duty cycles greater than 50%.

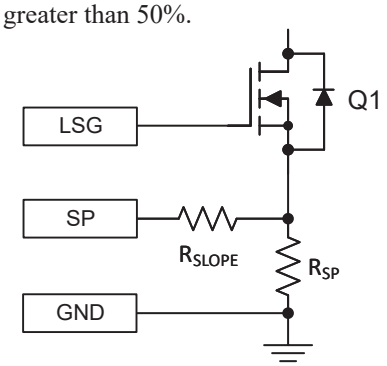

Figure 4

The current limit of the inner loop is set by the input limit of the sense amplifier, V_{IDS}, the maximum switch current that has been determined, and the effects of the slope compensation must be taken into account. The operating duty cycle must be calculated at maximum load and minimum operating input voltage. The amount of slope compensation can be calculated for this operating point and can then be added to the actual current-sense signal to determine the maximum signal amplitude before cycle-by-cycle current limiting takes effect. The term di_{SLOPE}/dt is the required slope compensation as selected during the design process and programmed with R_{SLOPE} as described in section Slope Compensation.

Equation 2:

$$R_{SP} = \frac{V_{IDS,MIN}}{1.2\left[I_{LP} + \left(\frac{di_{SLOPE}}{dt} \times \frac{D_{MAX}}{f_{SW}}\right)\right]}$$

Note that the minimum value of V_{IDS} is used with an additional 20% on the peak current to allow for margin. I_{LP} is the peak current in the inductor.

Slope Compensation

Slope compensation can be added to the MOSFET current-sense signal on pin SP to prevent subharmonic oscillations where the peak-to-average control error becomes increasingly larger at duty cycles in excess of 50%. A current source is provided at the SP pin as a sawtooth from 0 to 100 µA. An external resistor, R_{SLOPE}, connected between the SP pin and the source connection of the MOSFET, is used to program the appropriate voltage level to scale the slope compensation for correct use with the appropriate topology and set up conditions that have been adopted.

Equation 3:

$$R_{SLOPE} = \frac{\frac{di_{SLOPE}}{dt} \times R_{SP}}{I_{SLOPE} \times f_{SW}}$$

di_{SLOPE}/dt, is the required slope compensation based on design parameters.

Low-Side Switch Current Limit (inner loop)

Cycle-by-cycle current protection is provided through the low-side MOSFET. If an overcurrent occurs for longer than 64 switching clock cycles, the high-side MOSFET drive (PWMOUT) and the low-side MOSFET drive (HSG) are disabled, FFn1 and FFn2 are set low, and the hiccup timer, t_{HIC}, is initiated for a period of 10 ms. After the hiccup period, an auto-restart is performed under control of the soft-start timer.

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LED Current Sense Resistor

The main outer loop uses an external current sense resistor to control the DC current in the load.

The initial LED current, $I_{LED,SET}$, is programmed by the LED sense resistor, R_{SL}, according to:

Equation 4:

$$R_{SL} = \frac{V_{IDL}}{I_{LED,SET}}$$

V_{IDL} is the differential LED current sense voltage ($V_{LP} - V_{LN}$). See Outer Current Loop Control (LP, LN) section in Electrical Characteristics table. Typical V_{IDL} = 200 mV.

LED PWM Dimming

The LED current can be pulse-width modulated to control the LED brightness while maintaining the same current level through the LEDs during the on-time.

When the EN/PWM pin is driven low for less than $t_{DIS,EN/PWM}$, the PWMOUT signal disables the PWM PMOS to open the LED string and the LSG and HSG signals are set to their off-state to stop switching. If the EN/PWM pin is driven low for more than $t_{DIS,EN/PWM}$ the A80803 enters standby.

PWM Dimming Source

Two options are available for PWM dimming: apply an external PWM signal to the EN/PWM pin or use internal PWM dimming. Select internal or external PWM dimming by controlling the state of the DIMn pin or toggling the PWM_EN bit in the CONFIG14 register. Note that if the PWM_EN bit is set it will override the DIMn pin to select internal dimming. Tie the DIMn pin high to control the dimming mode through SPI. The PWM_EN bit defaults to 0, so if SPI is not used the DIMn pin controls dimming selection; see Table 4 for all combinations of DIMn and PWM_EN. For the best performance, the minimum recommended PWM dimming duty cycle is 5%.

Table 4: PWM Dimming Source Selection

DIMn Pin	PWM_EN Bit	Dimming Source
0	0	Internal
0	1	Internal
1	0	External
1	1	Internal

PWMOUT

PWMOUT is used to drive a PMOS in series with the LEDs to turn the current through the LEDs on or off. When the PWM signal is high, the PWMOUT pin will drive 5.5 V below the regulator output voltage. When the PWM signal is low, the PWMOUT signal will drive to the regulator output voltage. Connect PWMOUT to the gate of the PWM PMOS to turn the LEDs on when PWM is high and off when PWM is low. There is an undervoltage detect circuit to ensure sufficient regulator output voltage is available to switch the PMOS on. The current drive to the PWM PMOS is configurable through SPI by setting the PWM_DRV field in CONFIG14. Allegro recommends configuring the PWM_DRV field to control the PMOS gate drive instead of using a series resistor. This feature provides programmable control of the LED current edge rate while PWM dimming. The PWMOUT current drive setting applies for both external and internal PWM dimming. The PWMOUT pin can drive the gate of the PWM PMOS on and off without a gate-source pullup resistor. If a pullup resistor is required to support system safety requirements, use at least 100 kΩ for the pullup resistance.

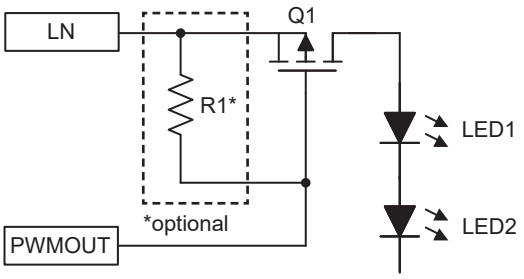

Figure 5: PWM PMOS circuit with optional gate-source pullup resistor, if required

Table 5: PWMOUT Pull-Up/Down Current Configuration

Gate Drive Current	PWM_DRV [1:0]	Code
25 mA	00	0
2 mA	01	1
0.5 mA	10	2
1 mA	11	3

External PWM Dimming

Drive the DIMn pin high to enable external PWM dimming. If SPI is used in the application, the PWM_EN bit must be set to 0.

Apply a PWM signal to EN/PWM within the specifications in the PWM Dimming and Enable section of the Electrical Characteristics table.

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Internal PWM Dimming

To enable internal PWM dimming drive EN/PWM high to keep the A80803 out of standby, and drive DIMn low or set PWM_EN bit to 1. If PWM_EN is set to 1 the state of the DIMn pin is ignored. EN/PWM should be treated as an enable pin when using internal PWM dimming, do not apply a PWM signal.

Four internal PWM frequency options are available and the internal PWM duty cycle is configurable from 0% to 100% in 0.5% steps. See Table 6 for the internal PWM frequency options and CONFIG14-CONFIG15 in Table 41: Register Map for all internal PWM options.

Table 6: Internal PWM Frequency Configuration

Internal PWM Frequency	PWM_FREQ [1:0]	Code
200 Hz	00	0
250 Hz	01	1
300 Hz	10	2
350 Hz	11	3

LED Analog Dimming

Three analog dimming methods to adjust the maximum LED current are provided within the A80803: LED binning, input voltage derating, and thermal derating. The threshold levels and behavior of these pins are programmed through SPI.

The maximum LED current, I_{LED}, is set using the external current sense resistor, R_{CS}, and scaled by adjusting the reference voltage to maintain across R_{CS}.

When LED binning is used, I_{LED} is derated by the programmed gain for the selected bin. When input voltage derating is used, I_{LED} will be scaled by the programmed input voltage foldback gain. When thermal derating is used, I_{LED} will be scaled by the programmed NTC foldback gain. The three current derating factors are k_{BINx}, k_{VIN} and k_{NTC}. The maximum LED current is the minimum of k_{BIN}, k_{VIN}, and k_{NTC} at the system operating voltage and temperature for the active bin.

LED Binning

LED binning applies one of four scaling factors to I_{LED} and allows for better matching. Drive the BINSEL pin to one of four voltage regions relative to V_{CC} to select a bin. See Table 7 for the voltage ranges on the BINSEL pin that correspond to each bin. The A80803 will regulate the LED current to $I_{LED(BINx)}$, where:

Equation 5:

$$I_{LED(BINx)} = k_{BINx} \times I_{LED}$$

Table 7: BINSEL Voltage Ranges (V_{CC})

BINx	$V_{BINSEL(MIN)}$	$V_{BINSEL(MAX)}$
1	0.62 × V_{CC}	V_{CC}
2	0.45 × V_{CC}	0.6 × V_{CC}
3	0.25 × V_{CC}	0.4 × V_{CC}
4	GND	0.2 × V_{CC}

The resistor divider from VCC should draw less than 1 mA. If resistor values that would draw more than 1 mA are required, the voltage divider can be tied to VREG using the following table to account for the difference between V_{REG} and V_{CC}.

Table 8: BINSEL Voltage Ranges (V_{REG})

BINx	$V_{BINSEL(MIN)}$	$V_{BINSEL(MAX)}$
1	0.41 × V_{REG}	0.66 × V_{REG}
2	0.30 × V_{REG}	0.40 × V_{REG}
3	0.17 × V_{REG}	0.27 × V_{REG}
4	GND	0.13 × V_{REG}

Each bin has its own 4-bit register field to store its scaling factor, k_{BINx}, in the CONFIG2 and CONFIG3 registers. The scale factors are programmable through SPI from 100% to 62.5% of I_{LED} in 2.5% steps. See Table 9 for examples of BINx codes to achieve a k_{BINx} scale factor. Calculate the bin gain, k_{BINx}, with the following equation:

Equation 6:

$$k_{BINx} = 1 - 0.025 \times code$$

$$\text{for } 0 \le code \le 15$$

Or, to find the code for a specific gain:

Equation 7:

$$code = (1 - k_{BINx}) / 0.025$$

$$\text{for } 0.625 \le k_{BINx} \le 1$$

Table 9: BINx Scale Factor

k_{BINx}	BINx [3:0]	Code
1	0000	0
0.975	0001	1
0.950	0010	2
…	…	…
0.650	1110	14
0.625	1111	15

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Input Voltage Derating

The LED current, I_{LED}, can be scaled down linearly as input voltage decreases up to a maximum derating set by k_{VIN}, programmable from a gain of 1 to a gain of 0.2 in CONFIG13. The shape of the input voltage derating is defined by the bin gain, k_{BIN}, a voltage level to start derating, V_{IN1}, a voltage level to stop derating, V_{IN2}, and the derating gain at V_{IN2}, k_{VIN}. The derating term definitions are shown in Figure 6. V_{IN2} should be 2 to 5 V lower than V_{IN1}. See Table 11 for available values of k_{VIN} and Table 12 for available values for V_{IN1}, or CONFIG13 in the register map.

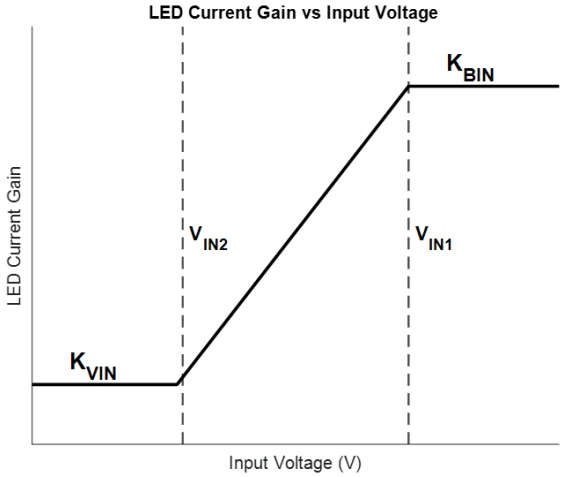

Figure 6: Input Voltage Derating Definitions

The A80803 stores the value for V_{IN1} as register field VIN1 in CONFIG13. Instead of storing V_{IN2} directly it stores the slope-factor to achieve the desired V_{IN2}, SFxVIN in CONFIG9 - CONFIG12. See Figure 7 for the voltage derating definition terms used in the A80803 registers, where "x" represents the bin number.

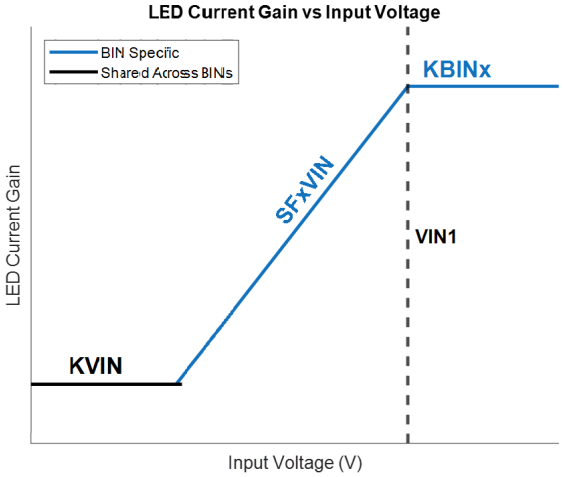

Figure 7: Input Voltage Derating Programming Definitions

All bins share a common V_{IN1} and k_{VIN}, while each bin has a separate slope-factor field, allowing different bins to have different derating slopes, as shown in Figure 8.

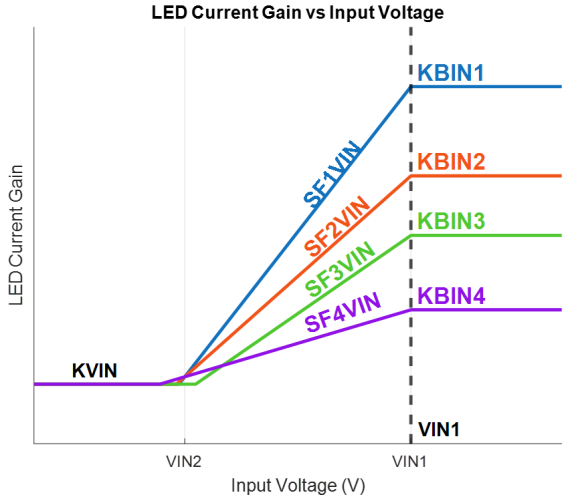

Figure 8: Input Voltage Derating Programming For Multiple Bins

Calculate the slope-factor from the following equation:

Equation 8:

$$slope = \frac{k_{BIN} - k_{VIN}}{V_{IN1} - V_{IN2}}$$

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Calculate register field SFxVIN from Equation 9 or find the closest available value in Table 16 to the calculated slope-factor.

Equation 9:

$$SFxVIN = round\left(\frac{slope}{0.0125} - 1\right)$$

Using the selected slope-factor, SFxVIN, the actual V_{IN2} voltage can be found with the following equation:

Equation 10:

$$V_{IN2(Actual)} = V_{IN1} - \frac{k_{BIN} - k_{VIN}}{SF}$$

When input voltage, V_{IN}, is greater than V_{IN1}, I_{LED} is only scaled by the selected bin. When V_{IN} is less than V_{IN2}, I_{LED} is scaled by k_{VIN}. When $V_{IN2} < V_{IN} < V_{IN1}$, the LED current is scaled by the slope-factor and V_{IN}. Table 10 shows the LED current scaling factor based on input voltage.

Table 10: Input Voltage Derating LED Current Scale Factor

Input Voltage (V_{IN})	I_{LED} Scale Factor
$V_{IN} > V_{IN1}$	k_{BIN}
$V_{IN2} < V_{IN} < V_{IN1}$	k_{VIN} + [SFxVIN × (V_{IN} – V_{IN2})]
$V_{IN} < V_{IN2}$	k_{VIN}

Table 11: Values for k_{VIN}

k_{VIN}	KVIN[2:0]	Code
1	000	0
0.8	001	1
0.7	010	2
0.6	011	3
0.5	100	4
0.4	101	5
0.3	110	6
0.2	111	7

Table 12: Values for V_{IN1}

V_{IN1}	VIN1[2:0]	Code
7.5 V	000	0
8.0 V	001	1
8.5 V	010	2
9.0 V	011	3
9.5 V	100	4
10.0 V	101	5
10.5 V	110	6
11.0 V	111	7

Thermal Derating

The LED current, I_{LED}, can be scaled down linearly as the voltage at the NTC pin decreases, up to a maximum derating set by k_{NTC}. This feature is intended to be used with a voltage divider at the NTC pin between a resistor and a negative temperature coefficient thermistor as shown in Figure 9. Applications that do not require thermal derating should tie the NTC pin to a voltage higher than the programmed VNTC1, such as tying to VREG.

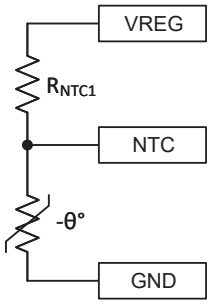

Figure 9: NTC Derating Application Circuit

The shape of the derating is defined by the bin gain, k_{BIN}, a voltage level to start derating, V_{NTC1}, a voltage level to stop derating, V_{NTC2}, and the derating gain at V_{NTC2}, k_{NTC}. The derating term definitions are shown in Figure 10.

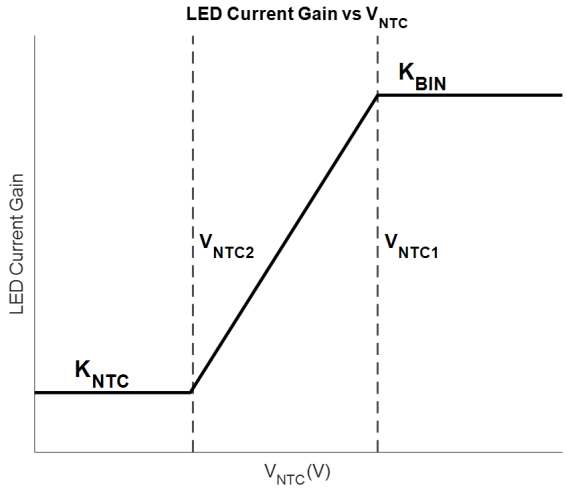

Figure 10: NTC Derating Definitions

The voltage levels V_{NTC1} and V_{NTC2} represent the temperature to start derating and the temperature to stop derating respectively, based on the voltage at the NTC pin when used with a thermistor in the circuit shown in Figure 9. The exact values of V_{NTC1} and V_{NTC2} depend on the properties of the selected thermistor. See the Thermal Derating Example section for more details on calculating V_{NTC1} and V_{NTC2} for a given thermistor.

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The A80803 stores the value for V_{NTC1} as register field V_{NTC1} in CONFIG4, and instead of storing V_{NTC2} directly, it stores the slope factor to achieve the desired V_{NTC2}, SFxNTC in CONFIG5 – CONFIG8. The gain term k_{NTC} is stored as KNTC in CONFIG4. See Figure 7 for the voltage derating definition terms used in the A80803 registers.

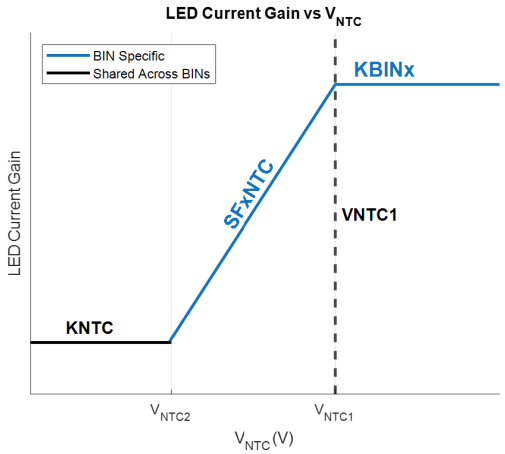

Figure 11: NTC Derating Programming Definitions

For proper operation, k_{NTC} should be less than k_{BINx} and V_{NTC2} should be at least 0.5 V lower than V_{NTC1}. See Table 14 for available values for k_{NTC}, and Table 15 and Equation 14 for available values of V_{NTC1}.

All bins share a common V_{NTC1} and k_{NTC}, while each bin has a separate slope factor field, SFxNTC, allowing different bins to have different derating slopes to reach the same final derated value, as shown in Figure 4.

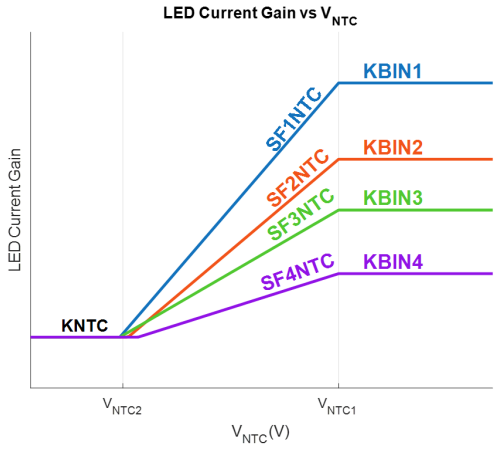

Figure 12: NTC Derating Programming for Multiple Bins

Calculate the slope factor for NTC derating of a specific bin from the following equation:

Equation 11:

$$slope = \frac{k_{BIN} - k_{NTC}}{V_{NTC1} - V_{NTC2}}$$

Calculate the register field SFxNTC from Equation 12 or the closest available value in Table 17 to the calculated slope-factor.

Equation 12:

$$SFxNTC = round\left(\frac{slope}{0.032} - 1\right)$$

Using the selected slope-factor, SFxNTC, the actual V_{NTC2} voltage can be found with the following equation:

Equation 13:

$$V_{NTC2(Actual)} = V_{NTC1} - \frac{k_{BIN} - k_{NTC}}{SF}$$

where SF is the selected slope-factor.

When the voltage at the NTC pin, V_{NTC}, is greater than V_{NTC1}, I_{LED} is only scaled by the selected bin. When V_{NTC} is less than V_{NTC2}, I_{LED} is scaled by k_{NTC}. When $V_{NTC2} < V_{NTC} < V_{NTC1}$, the LED current is scaled by the slope-factor and V_{NTC}. Table 13 shows the LED current scaling factor based on NTC pin voltage.

Table 13: NTC Derating LED Current Scale Factor

NTC Pin Voltage (V_{NTC})	I_{LED} Scale Factor
$V_{NTC} > V_{NTC1}$	k_{BIN}
$V_{NTC2} < V_{NTC} < V_{NTC1}$	k_{NTC} + [SFxNTC × (V_{NTC} – V_{NTC2})]
$V_{NTC} < V_{NTC2}$	k_{NTC}

Table 14: Values for k_{NTC}

k_{NTC}	K_{NTC}[1:0]	Code
0.8	00	0
0.7	01	1
0.6	01	2
0.5	11	3

Table 15: Values for VNTC1

V_{NTC1}	V_{NTC1}[4:0]	Code
1.20	00000	0
1.25	00001	1
1.30	00010	2
…	…	…
2.70	11110	30
2.75	11111	31

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Equation 14:

$$V_{NTC1} = 1.2 + 0.05 \times code \quad \text{for } 0 \leq code \leq 31$$

Combined Analog Dimming

All three analog dimming functions work together to regulate the LED current to the minimum of the active bin gain, the input voltage derating gain, and the NTC derating gain.

Equation 15:

$$I_{LED} = \min([I_{LED(BIN)}, I_{LED(VIN)}, I_{LED(NTC)}])$$

where:

$I_{LED(BIN)}$ is I_{LED} for the active BIN,
$I_{LED(VIN)}$ is I_{LED} for the current V_{IN},
$I_{LED(NTC)}$ is I_{LED} for the current V_{NTC}.

Figure 13 shows the effect of the combined analog dimming at three different temperatures with varied input voltage. At Temperature 1, I_{LED} is only limited by input voltage. At Temperature 2, I_{LED} is limited by temperature until it meets the input voltage derating limit. Finally, at Temperature 3, the LED current is limited by temperature at all input voltages.

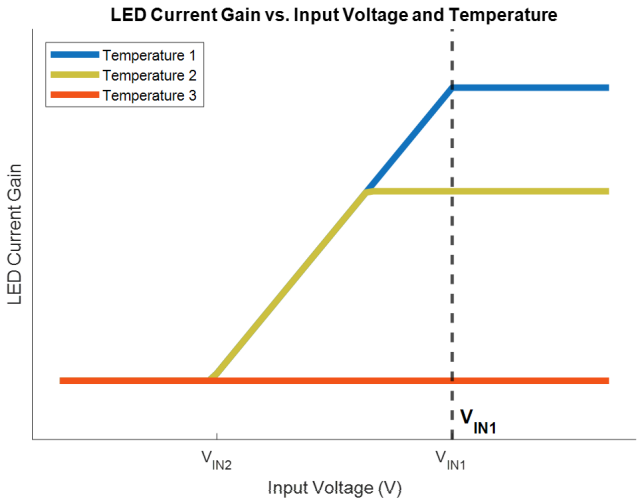

Figure 13: Effect of Combined Analog Dimming

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Table 16: Slope-Factors for Input Voltage Derating

Slope Factor	SFxVIN[4:0]	Code
0.0125	00000	0
0.0250	00001	1
0.0375	00010	2
0.0500	00011	3
0.0625	00100	4
0.0750	00101	5
0.0875	00110	6
0.1000	00111	7
0.1125	01000	8
0.1250	01001	9
0.1375	01010	10
0.1500	01011	11
0.1625	01100	12
0.1750	01101	13
0.1875	01110	14
0.2000	01111	15
0.2125	10000	16
0.2250	10001	17
0.2375	10010	18
0.2500	10011	19
0.2625	10100	20
0.2750	10101	21
0.2875	10110	22
0.3000	10111	23
0.3125	11000	24
0.3250	11001	25
0.3375	11010	26
0.3500	11011	27
0.3625	11100	28
0.3750	11101	29
0.3875	11110	30
0.4000	11111	31

Table 17: Slope-Factors for NTC Derating

Slope Factor	SFxNTC[4:0]	Code
0.032	00000	0
0.064	00001	1
0.096	00010	2
0.128	00011	3
0.160	00100	4
0.192	00101	5
0.224	00110	6
0.256	00111	7
0.288	01000	8
0.320	01001	9
0.352	01010	10
0.384	01011	11
0.416	01100	12
0.448	01101	13
0.480	01110	14
0.512	01111	15
0.544	10000	16
0.576	10001	17
0.608	10010	18
0.640	10011	19
0.672	10100	20
0.704	10101	21
0.736	10110	22
0.768	10111	23
0.800	11000	24
0.832	11001	25
0.864	11010	26
0.896	11011	27
0.928	11100	28
0.960	11101	29
0.992	11110	30
1.024	11111	31

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Input Voltage Derating Example

The design parameters for an application with four BINs, input voltage derating from 10 V to 5 V, and LED current gain of 0.5 at the minimum input voltage are shown in Table 16.

Table 18: Example Input Voltage Derating Parameters

Parameter	Value	Description
k_{BIN1}	1	BIN1 gain
k_{BIN2}	0.85	BIN2 gain
k_{BIN3}	0.75	BIN3 gain
k_{BIN4}	0.7	BIN4 gain
V_{IN1}	10 V	V_{IN} to start derating
V_{IN2}	5 V	V_{IN} for maximum derating
k_{VIN}	0.5	Maximum V_{IN} derating gain

Start by finding the gain factors for each bin from Equation 7. Next, calculate the slope-factors, SFxVIN, for each bin from Equation 8 and find the closest value in Table 16 or use Equation 9. Calculate $V_{IN2(Actual)}$ from Equation 10 to verify the actual level where k_{VIN} will take full effect. See Table 19 for the results for this design; Figure 14 shows the effect on I_{LED} for this example graphically (shown with a typical $V_{VIN,UV,L}$ of 4.75 V).

Table 19: Solved Example for Input Voltage Derating

Parameter	BIN1	BIN2	BIN3	BIN4
BIN Gain	1	0.85	0.75	0.7
V_{IN1} (V)	10	10	10	10
V_{IN2} (V) (target)	5	5	5	5
Calculated Slope	0.1	0.07	0.05	0.04
Closest Slope Factor	0.1	0.075	0.05	0.0375
KBINx (Code)	0	6	10	12
KVIN (Code)	4	4	4	4
VIN1 (Code)	5	5	5	5
SFxVIN (Code)	7	5	3	2
$V_{IN2(Actual)}$, typical (V)	5.0	5.3	5	4.67

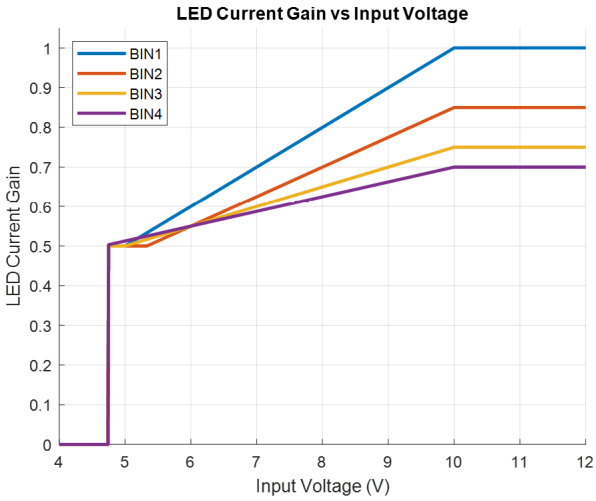

Figure 14: Example LED Current Gain with Input Voltage Derating for Multiple Bins

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Thermal Derating Example

This example implements thermal derating starting at 90°C and reaching a maximum thermal derating gain of 0.6 at 130°C. The thermistor used in this example is a Vishay NTCS0603E-3103FHT with a base value of 10 kΩ and a beta value of 3960. The design parameters for this example are shown in Table 20.

Table 20: Example Thermal Foldback Design Parameters

Parameter	Value	Description
k_{BIN1}	1	BIN1 gain
k_{BIN2}	0.85	BIN2 gain
k_{BIN3}	0.75	BIN3 gain
k_{BIN4}	0.7	BIN4 gain
T_{DER1}	90°C	Temperature to start derating
T_{DER2}	130°C	Temperature for maximum derating
k_{NTC}	0.6	Maximum temperature derating gain
R_0	10 kΩ	Value of thermistor at 25°C
β	3960	Thermistor beta constant

Using the thermistor beta equation as shown in Equation 16 and the circuit in Figure 9, set R_{NTC1} to 2.21 kΩ to keep the voltage at the NTC pin away from the extremes of the voltage divider rails while in the derating temperature range. See Figure 11 for the resistance change of the thermistor and the corresponding voltage change at the NTC pin (output of the voltage divider) as temperature changes.

Equation 16:

$$R = R_0 e^{\beta\left(\frac{1}{T}-\frac{1}{T_0}\right)}$$

where:

R_0: Thermistor resistance at T_0 Ω
T_0: Baseline thermistor temperature Kelvin
T: Thermistor temperature Kelvin
β: Thermistor Beta constant

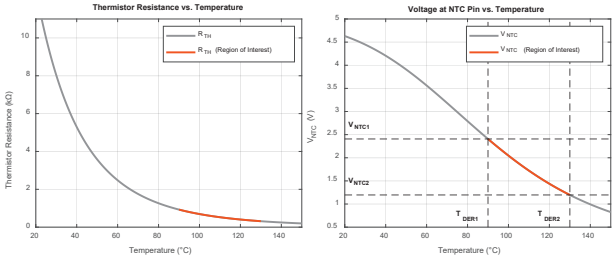

Figure 15: Thermistor and NTC Voltage Change with Temperature

Start by finding the gain factors for each bin from Equation 7. Next, calculate the slope factor, SFxNTC, for each bin using Equation 11 and find the closest value in Table 17 or use Equation 12. Calculate $V_{NTC2(Actual)}$ from Equation 13 to verify the actual level where k_{NTC} will take full effect. See Table 21 for the results for this design; Figure 16 shows the effect on I_{LED} for this example graphically.

Table 21: Solved Example for Thermal Derating

Parameter	BIN1	BIN2	BIN3	BIN4
BIN Gain	1	0.85	0.75	0.7
V_{NTC1} (V)	2.406	2.406	2.406	2.406
V_{NTC2} (V) (target)	1.196	1.196	1.196	1.196
Calculated Slope	0.332	0.208	0.125	0.083
Closest Slope Factor	0.320	0.192	0.128	0.096
KBINx (Code)	0	6	10	12
KNTC (Code)	2	2	2	2
VNTC1 (Code)	24	24	24	24
SFxNTC (Code)	9	5	3	2
$V_{NTC2(Actual)}$, typical (V)	1.15	1.098	1.228	1.358

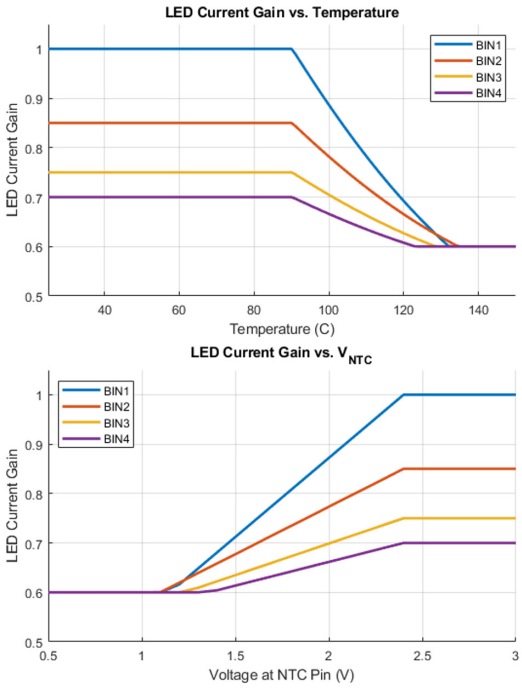

Figure 16: Example of LED Current Gain with NTC Derating

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Low and High Beam Control

The A80803 is designed to support low/high-beam applications and can simply and smoothly transition from low-beam to high-beam LED lighting conditions. The A80803 has a unique slew-control feature to minimize the LED current overshoot and undershoot while transitioning between low-beam and high-beam, see the Low/High-Beam Transition Slew Control section.

Buck-Boost/Boost Low/High-Beam Control

The A80803 can switch between low-beam and high-beam operating modes by controlling two MOSFETs with its integrated MOSFET drivers at the LBG (low-beam gate) and HBG (high-beam gate) pins. Set the operating mode by driving the LBEAMn pin low for low-beam mode or high for high-beam mode. While in low-beam mode, the A80803 operates as a buck-boost converter, and in high-beam mode, the A80803 operates as a boost converter.

Two external MOSFETs are required to switch between low-beam and high-beam modes. The low-beam PMOS should have its gate connected to the LBG pin, its source connected to the LBS pin, and its drain connected to the input voltage, VIN. The high-beam NMOS should have its gate connected to the HBG pin, its source connected to GND, and its drain connected to the bottom of the LED string. Connect a 2 kΩ resistor with 5% (or better) tolerance and 4.7 nF capacitor with 10% (or better) tolerance from the gate to the drain for both the NMOS and the PMOS for stability of the beam transition circuit. Refer to Figure 17 for a circuit diagram of low/high beam application.

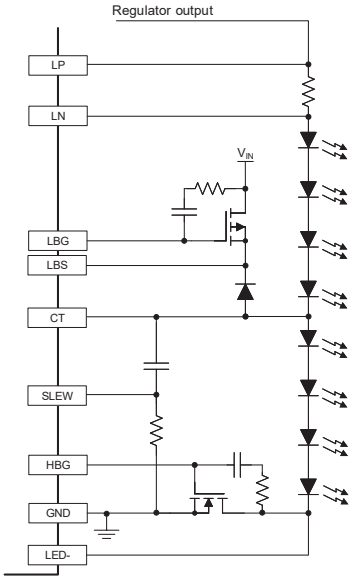

Figure 17: Low/High-Beam Application Circuit

When in low-beam mode, LBG drives the PMOS gate 5.5 V below VIN to turn it on, connecting VIN to CT (through a diode), and HBG drives the NMOS gate low to disconnect the LEDs between CT and GND. The current path is from the regulated output through the top LEDs and into VIN as shown in Figure 18.

When in high-beam mode, LBG drives the PMOS gate up to VIN to disconnect VIN from CT, and HBG drives the NMOS gate high to connect the full LED string to GND, as shown in Figure 19.

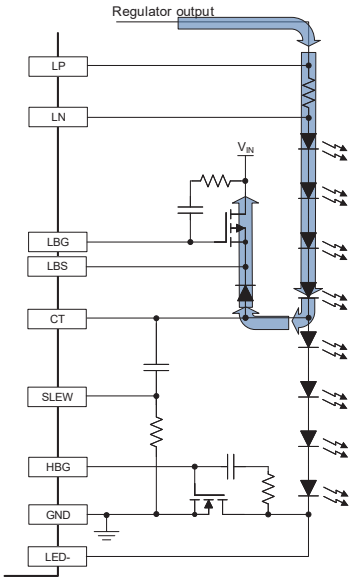

Figure 18: Low-Beam LED Current Flow (Buck-Boost)

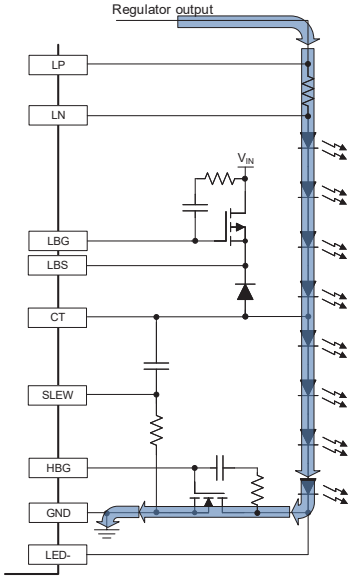

Figure 19: High-Beam LED Current Flow (Boost)

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Low/High Beam Control Methods

Two options are available for low/high beam selection: apply an external signal to the LBEAMn pin or write to the HBG_ON bit in the CONFIG16 register via SPI. Note that if the HBG_ON bit is set, it will override the LBEAMn pin to select high-beam mode. Tie the LEAMn pin low to control the dimming mode through SPI. Set the HBG_ON bit to 0 to use the LBEAMn pin to control low/high-beam selection. Also note that the HBGCTRL bit in CONFIG16 should be 0 to use the topology change application. Both HBG_ON and HBGCTRL default to 0. The HB_UV and HB_OV faults are ignored while in low-beam mode, and the LB_UV and LB_OV faults are ignored while in high-beam mode. The low-beam to high-beam transition is designed to be used at 100% PWM dimming.

Table 22: Low/High-Beam Control for Topology Switch Control

LBEAMn Pin	HBG_ON Bit	HBGCTRL Bit	LBG / HBG	Low/High-Beam
0	0	0	ON / OFF	Low-Beam
0	1	0	OFF / ON	High-Beam
1	0	0	OFF / ON	High-Beam
1	1	0	OFF / ON	High-Beam

Boost Low/High-Beam Control

The A80803 can also be configured to transition between low/high-beam operation with a single NMOS in a boost topology. Connect the NMOS gate to HBG, source to GND, and drain to CT, as shown in Figure 20. In this configuration, the NMOS will short the high-beam LEDs when HBG is high to enter low-beam operation, the opposite polarity of the topology change circuit. In this configuration where the power converter is strictly a boost converter the input voltage must always be less than both the low-beam and high-beam output voltage.

Set the HBGCTRL bit to 1 to invert the polarity of the LBEAMn pin, driving HBG high when LBEAMn is low. The HBGCTRL bit also inverts which low-beam/high-beam UV/OV circuits are monitored to align with the LBEAMn polarity. The LBG and LBS pins are not used in the single MOSFET configuration.

Table 23: Low/High-Beam Control for Single MOSFET Control

LBEAMn Pin	HBG_ON Bit	HBGCTRL Bit	LBG / HBG	Low/High-Beam
0	0	1	X / ON	Low-Beam
0	1	1	X / ON	Low-Beam
1	0	1	X / OFF	High-Beam
1	1	1	X / ON	Low-Beam

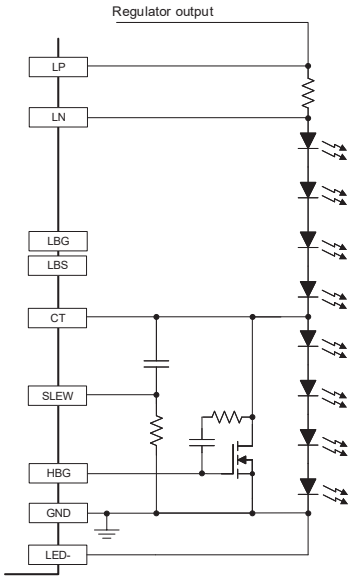

Figure 20: Low/High-Beam Control with Single MOSFET

Low/High-Beam Transition Slew Control

The A80803 minimizes the LED current overshoot and undershoot seen during low/high-beam transitions. The minimal LED current overshoot and undershoot is shown for a 1 A LED current application in Figure 21.

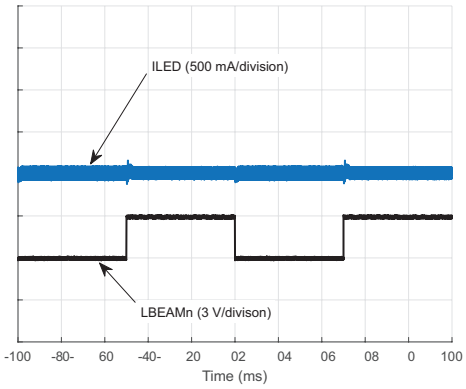

Figure 21: Minimum LED Current Under/Overshoot for 1 A LED Current Application

This feature is controlled by an external resistor and capacitor at the SLEW pin as shown in Figure 17. Most applications use a 1 V/ms slew rate at the CT pin with a 5.36 kΩ resistor and 47 nF capacitor. The slew rate can be adjusted with Equation 17 while keeping R_{SLEW} between 3.6 kΩ and 7.5 kΩ.

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Equation 17:

$$C_{SLEW} = \frac{250\ mV \times dt}{R_{SLEW} \times dV}$$

When VIN is greater than the voltage at the CT node, V_{CT}, the low/high-beam transition follows the state changes shown in Figure 22. When V_{IN} is less than V_{CT}, the low/high-beam transition follows the state changes shown in Figure 23.

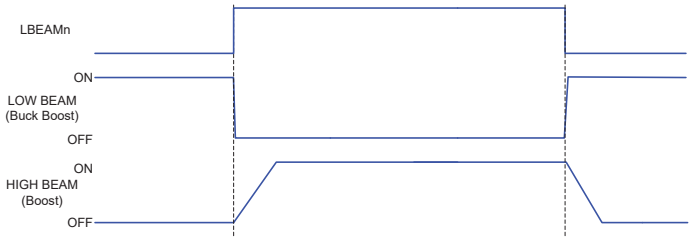

Figure 22: Low/High/Low-Beam Transitions when $V_{IN} > V_{CT}$

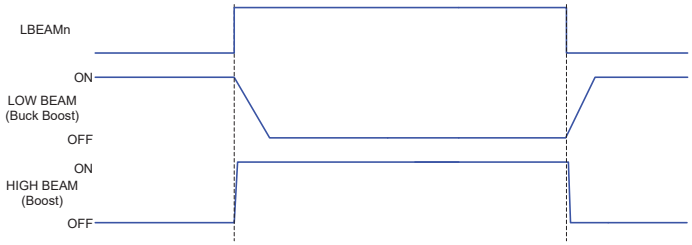

Figure 23: Low/High/Low-Beam Transitions when $V_{IN} < V_{CT}$

Input UVLO

The A80803 input UVLO rising edge is programmable via SPI. The default value is typically 5.65 V with 0.9 V hysteresis. This allows the A80803 to maintain full operation down to $V_{IN,MIN}$ of 5 V. Therefore, end equipment can operate to battery voltages of 6 V and allow 1 V drop for reverse protection or filtering.

The A80803 requires a higher voltage than $V_{IN,MIN,H}$ to start operating. The falling undervoltage shut down is just below $V_{IN,MIN}$.

Table 24: V_{IN} Undervoltage Lockout Programmable Options

$V_{IN,MIN,H}$ Typical	$V_{IN,MIN,L}$ Typical	VIN_UV[1:0]
5.65 V	4.75 V	00
6.0 V	5.1 V	01
6.5 V	5.6 V	10
7.0 V	6.1 V	11

Linear Regulator

The A80803 provides a 5 V linear regulator, V_{REG}, that can source up to 50 mA for general use. The user can select, through SPI, if this regulator remains on when the A80803 is in standby mode while EN/PWM is held low, or if the linear regulator shuts down when EN/PWM is held low.

Table 25: VREG Configurable State Options

VREG Status	VREG_EN[0]
Disabled	0
Always on	1

When VREG_EN is high and EN/PWM is low, the A80803 behaves like a 5 V linear regulator with fault reporting through FFn1 and communication through SPI.

If VREG_EN and EN/PWM are set to zero, the startup phase will include a time to load the registers from SPI. When VIN is applied, VCC will be enabled so the registers can be loaded. If both EN/PWM and VREG_EN are 0, then VCC will turn off and the A80803 will go into standby mode. It remains in standby mode until EN/PWM goes high or VIN is power cycled. See the Startup Timing Diagrams in Figure 26, Figure 27, and Figure 28.

Linear regulator power loss is directly proportional to the input voltage.

The power dissipation of the VREG regulator can be calculated with:

Equation 18:

$$P_D = (V_{IN} - V_{LDO}) \times I_{OUT}$$

where V_{IN} is the input voltage to the A80803, V_{LDO} is 5 V, and I_{OUT} is the current drawn from VREG.

The temperature rise can be calculated with:

Equation 19:

$$T_{rise} = P_D \times R_{\theta JA}$$

See Thermal Characteristics section for details about $R_{\theta JA}$.

The VDRV regulator is also a factor in total temperature rise of the A80803. The current draw from the VDRV regulator follows:

Equation 20:

$$I_{VDRV} = f_{SW}(Q_{LSG} + Q_{HSG})$$

Use Equation 18 and Equation 19 to calculate the temperature rise due to VDRV, where V_{LDO} is 6 V for the VDRV linear regulator.

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Standby Power

Standby power is the power consumed by the A80803 when the input voltage is applied but the IC is in standby mode by pulling the enable pin low. Automotive lighting applications are often powered from a switched battery connection or have a pass transistor for overcurrent protection, eliminating the concern for standby power consumption since the IC will be fully disabled when the lighting system is powered down. Applications that require a reduced standby current can implement a circuit similar to the one shown below to disable the A80803 when the lighting system is not in use.

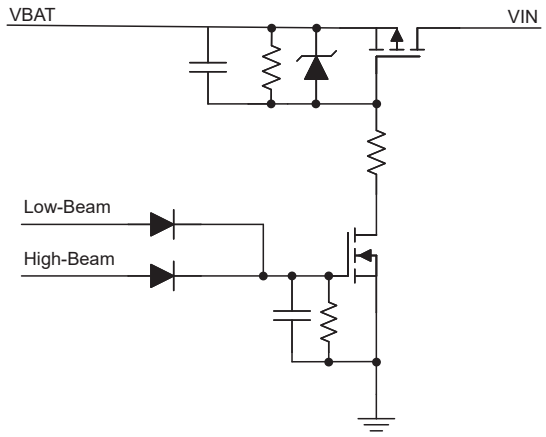

Figure 24: Input Disconnect

Fault Handling and Reporting

The A80803 can handle the following fault conditions: input under/overvoltage, VREG and VDRV undervoltage, low-side switch current limit, output overvoltage, output overcurrent, output undervoltage, FSET open/short-to-ground, as well as LED fault conditions for open LED, short LED or output undervoltage, and LED string short.

Faults are reported through two active-low fault flag pins and through SPI. The fault flag pin FFn1 reports all faults detected by the A80803. The fault flag FFn2 only reports the faults that are selected through SPI. If a second fault occurs while the flag is low, the flag status remains unchanged. The flag will not go high until all faults are corrected.

During shutdown, the fault flag goes low when VIN drops below its UV threshold, irrespective of the state of other fault reporting circuits.

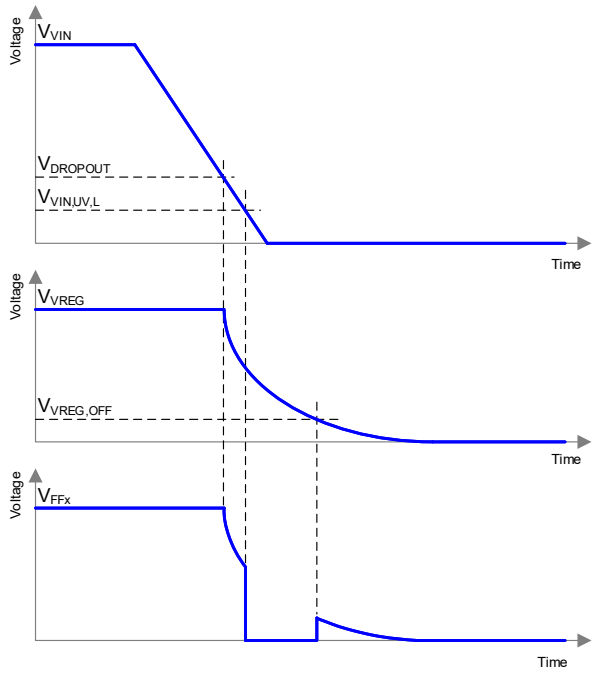

Figure 25: FFn1 and FFn2 behavior during shutdown when pulled up to VREG

Table 26: Faults selectable on FFn2 output

Fault Name	Description
OPENLED	Open LED
STRSHORT	Shorted LED string
OUT_OV	Output Overvoltage
OUT_UV	Output Undervoltage
OUT_OC	Output Overcurrent
TEMP	Overtemperature
VREG_UV	VREG Fault
HB_F	High-Beam Fault

Fault flag two, FFn2, includes a programmable blanking time before reporting the fault; see the FF2DLY field in CONFIG22 or Table 27 for programming options.

Table 27: Fault Flag 2 Blanking Time

Fault Flag 2 Delay	FF2DLY[1:0]	Code
50 ms	00	0
100 ms	01	1
1000 ms	10	2
2000 ms	11	3

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The two fault flag pins can also be configured as bidirectional to be used as inputs to turn off the A80803 regulation loop, which can be useful in applications that require a one-out-all-out condition where two or more A80803 devices are used. The one-out-all-out mode can be configured via SPI; see the OOAO field in CONFIG22 or for programming options.

Table 28: One-Out-All-Out Behavior

One-Out-All-Out Mode	OOAO[1:0]	Code
Disabled	00	0
FFn1 as bidirectional	01	1
FFn2 as bidirectional	10	2
FFn1 and FFn2 are bidirectional	11	3

Input Undervoltage

If input voltage drops below programmed input undervoltage threshold $V_{VIN,UV,L}$ for more than input UV deglitch time $t_{UV,FLT}$, the A80803 stops switching and turns off the PWM MOSFET. The fault flag signals the fault if it is pulled up to VREG or VCC. Once input voltage rises beyond UV rising threshold, device performs auto soft-start. The input undervoltage setting is programmable via SPI; see the VINUV field in CONFIG1 for all options. If an input undervoltage fault occurs, the FLT_VIN_UV bit is set in DIAG1 and the FF bit is set in DIAG0.

Input Overvoltage

If input voltage rises beyond programmed overvoltage threshold, the device stops switching and turns off PWM MOSFET. The fault flag signals the fault condition. If input voltage drops at least 1.0 V below overvoltage threshold, the device performs auto soft-start. The input overvoltage setting is programmable via SPI; see the VINOV field in CONFIG1 for all options. If an input overvoltage fault occurs, the FLT_VIN_OV bit is set in DIAG1 and the FF bit is set in DIAG0.

VREG Undervoltage

The A80803 monitors the VREG voltage and signals a fault condition if the VREG voltage falls below 4.15 V (typ.), the device stops switching and turns off the PWM MOSFET. If VREG rises above 4.4 V (typ.), and the input voltage is above switching UV rising threshold, the A80803 auto-restarts with soft-start. If a VREG undervoltage fault occurs, the FLT_VREG_UV bit is set in DIAG1 and the FF bit is set in DIAG0.

Low-Side Switch Current Limit

The A80803 provides pulse-by-pulse current limit protection to protect the low-side MOSFET from large currents. During pulse-by-pulse current limit operation, the device waits for 64 switching cycles before turning off the switching MOSFETs (LSG and HSG) and PWM MOSFET. After turning off the MOSFETs, the device waits for a hiccup cooldown period t_{HIC} and performs auto-restart with soft-start. Although the device enforces pulse-by-pulse current protection during soft-start, hiccup operation is disabled until soft-start is finished. If a low-side switch current limit fault occurs, the FLT_LSG_OC bit is set in DIAG1 and the FF bit is set in DIAG0.

FSET Open/Short-to-GND

The FSET pin is monitored for open or shorted-to-GND faults. If an FSET fault occurs, the internal oscillator forces the switching frequency to 350 kHz. The device resumes switching with the set frequency when the fault is removed. If an FSET fault occurs, the FLT_FSET bit is set in DIAG1 and the FF bit is set in DIAG0.

Overtemperature

If the junction temperature of A80803 exceeds Thermal Shutdown (TSD) temperature, the device shuts down VREG and the LED driver, but VCC remains operational so all registers retain their contents and SPI remains operational while in thermal shutdown. Once the temperature drops below the TSD temperature and hysteresis level, the A80803 auto-restarts. If an overtemperature fault occurs, the FLT_TEMP bit is set in DIAG1 and the FF bit is set in DIAG0.

Output Overvoltage

Three overvoltage detection circuits are incorporated in the A80803. The high-beam overvoltage circuit monitors the voltage between the regulator output (LP pin) and LED-, and compares to the programmed level in the OV_HB field in CONFIG17. The low-beam overvoltage circuit monitors the voltage between the regulator output (LP pin) and CT pin, and compares to the programmed level in the OV_LB field in CONFIG18. The third overvoltage circuit monitors the voltage between regulator output (LP pin) and GND pin and its trip level is fixed at 75 V. For best results set the OV_LB and OV_HB levels to about 5 V higher than the nominal low-beam and high-beam voltage levels for the application.

Table 29: Output Overvoltage Fault Scenarios

ID	Failure Mode
1	Output current sense resistor open
2	PWM MOSFET open
3	LED open
4	Current sense negative input (LN) open
5	Current sense positive input (LP) open
6	Input voltage greater than required output voltage, in boost mode

When an overvoltage is detected, the low-side and high-side MOSFETs turn off, immediately waiting for the next switching cycle.

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The behavior after an output overvoltage event can be programmed by the OVB field in CONFIG17. The options are to regulate the output at the OV level with $V_{OV,HYS}$ hysteresis, or turn off the regulator and PWM MOSFET immediately and enter hiccup mode where the output stays off for t_{HIC} seconds followed by an auto-restart with soft-start. The options are summarized in Table 30.

Table 30: Overvoltage Behavior

OV Behavior	OVB[0]
Hysteretic LED Voltage Regulation at OV level	0
Turn off PWM MOSFET and enter hiccup mode	1

The default behavior is for the driver to regulate the output voltage at the overvoltage trip point with some hysteresis. This may cause the current in the LEDs to increase. If the OV event is caused by modes 4, 5, or 6 in the table above, then the user may prefer to also open the PWM MOSFET to protect the LED string.

The high-beam OV level, OV_HB, can be set between 20.4 to 70.0 V in 1.6 V steps. The low-beam OV level, OV_LB, can be set between 10.4 and 60 V in 1.6 V steps. See CONFIG17 and CONFIG18. If an output overvoltage fault occurs, the FLT_OUT_OV bit and FF bit are set in DIAG0.

Output Undervoltage

A80803 reports output undervoltage faults, if any, due to partial LED string short or low input voltage caused by cold cranking the battery. Two UV detect circuits are included to report faults during high or low-beam operation. One detection circuit senses the voltage across the high-beam LED string between LP and LED-, and the other circuit senses the voltage across the low-beam LED string between LP and CT. If the voltage across the high-beam string drops below $V_{UV,HB}$ or the voltage across the low-beam string drops below $V_{UV,LB}$, the fault flag will be pulled low. The two undervoltage detect levels are programmable through SPI. Upon undervoltage detection, the A80803 continues to operate with reduced light output if the one-out-all-out feature is not enabled. If one-out-all-out feature is enabled, the device stops switching during an undervoltage event. During regular startup, UV faults are masked for an additional 50 ms duration after soft-start is finished. Undervoltage faults are also masked while PWM MOSFET is open.

In addition to the above two UV detect circuits, a fixed output UV detect circuit monitors the output voltage at the LP pin with respect to ground and triggers PWMOUT undervoltage fault if the output voltage is less than 6 V. This detection circuit is disabled when low-beam mode is in operation or PWM dimming MOSFET is off. If an output undervoltage event occurs, the FLT_OUT_UV bit and FF bit are set in DIAG0.

Low-Beam/High-Beam OV/UV Comparators

The high-beam undervoltage and overvoltage faults are monitored or ignored according to the HBG on/off state. When HBGCTL = 0, the device is in high-beam mode while HBG is on (LBEAMn is high or HBG_ON = 1). When HBGCTL = 1, the device is in high-beam while HBG is off (LBEAMn is high and HBG_ON = 0). In both cases, the high-beam under/overvoltage comparators are ignored while in low-beam, and the low-beam comparators are ignored while in high-beam.

Table 31: Low/High-Beam and UV/OV Comparator State

HBGCTRL Bit	LBEAMn	HBG_ON	HBG	Low/High-Beam
0	0	0	Off	Low
0	0	1	On	High
0	1	0	On	High
0	1	1	On	High
1	0	0	On	Low
1	0	1	On	Low
1	1	0	Off	High
1	1	1	On	Low

Output Overcurrent

If the voltage across the LP and LN pins exceeds the V_{OC} voltage, then an overcurrent event is detected. The LSG and PWMOUT signals turn off their respective MOSFETs and the fault flag is set low. The MOSFETs remain off for t_{HIC}. After t_{HIC}, the regulator will go through soft-start to try to regulate the output. If the overcurrent still exists, the device will enter another hiccup cycle based on the programmed number of allowable overcurrent clock cycles. Four different clock cycle durations are programmable via the OCFILT field in CONFIG22, shown in Table 32. If an output overcurrent event occurs, the FLT_OUT_OC bit and FF bit are set in DIAG0.

Table 32: Overcurrent Clock Cycle Filter Options

Overcurrent Clock Cycles	OCFILT[1:0]	Code
2	00	0
4	01	1
8	10	2
16	11	3

Open LED

An open LED is detected by an overvoltage event and zero current flowing in the current sense resistor, R_{CS}. If open LED is detected while in low-beam, the A80803 signals the fault flag and responds to overvoltage event. If open LED is detected in

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high-beam, the A80803 will signal this as a high-beam fault; see High-Beam Fault. Note that open LED detection in low-beam is based on the low-beam overvoltage comparator. If the A80803 is operating in low-beam buck-boost mode, the regulated output voltage is referenced to VIN meaning a high OV_LB setting may not trip the low-beam OV comparator if VIN + OV_LB is greater than 75 V. If the fixed 75 V LP-to-GND comparator trips, then the A80803 does not check for open LED. For best results, set the OV level to about 5 V higher than the nominal voltage levels for the application. If open LED is detected, the FLT_OPENLED bit and FF bit are set in DIAG0.

High-Beam Fault

A high-beam fault occurs when the A80803 is operating in high-beam mode and there is an open LED event or if the difference between CT and ground is less than 2 V. When a high-beam fault occurs, the device transitions to low-beam operation, holds the fault pin FFn1 and optionally FFn2 low, and sets the FF and FLT_HBF bits in DIAG0. To resume high-beam operation, the fault must be removed from the system and the FLT_HBF bit must be cleared by writing a 1 to bit D5 in DIAG1.

LED String Short

The A80803 detects complete LED string short fault if the voltage between LP and CT drops below 1 V while the PWM MOSFET is on. Upon fault detection, the A80803 turns off the low-side gate (LSG), high-side gate (HSG), and PWM MOSFET (PWMOUT) after two switching cycles and pulls the fault flag low. After turning off, the FETs, the device waits for hiccup cool down period t_{HIC} before auto-restarting with soft-start. If an LED string short is detected, the FLT_STRSHORT bit and FF bit are set in DIAG0.

LED Short

The A80803 detects a shorted LED in the string when the output voltage is below the programmed low-beam undervoltage level or high-beam undervoltage level. Set the LEDSC bit high in CONFIG1 to enable the LED short fault flag. If LEDSC is set to 1 and an LED short is detected, the FLT_LEDSHORT bit and FF bit are set in DIAG0.

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Table 33: Fault Table Summary

Fault	Action
Input Undervoltage	Low-Side Gate (LSG), High-Side Gate (HSG), and PWM MOSFET (PWMOUT) turn off after $t_{UV,FLT}$ and fault flag FFn1 goes low assuming there is sufficient drive to the flag. Once input voltage rises above the VIN switching UV rising threshold, device performs auto soft-start.
Input Overvoltage	Low-Side Gate (LSG), High-Side Gate (HSG), and PWM MOSFET (PWMOUT) turn off immediately and fault flag FFn1 goes low. Once input voltage drops below the VIN OV threshold, minus hysteresis, device performs auto soft-start.
VREG Undervoltage	Low-Side Gate (LSG), High-Side Gate (HSG), and PWM MOSFET (PWMOUT) turns off immediately and fault flag FFn1 goes low. Once VREG voltage rises above the $VREG_{min}$ threshold, plus hysteresis, device performs auto soft-start.
VDRV Undervoltage	Low-Side Gate (LSG), High-Side Gate (HSG), High-Beam Gate (HBG), and PWM MOSFET (PWMOUT) turn off immediately and fault flag FFn1 goes low. Once VDRV voltage rises above the $VDRV_{min}$ threshold, plus hysteresis, device performs auto soft-start.
Low-Side Switch Current Limit	When fault occurs, device operates with cycle-by-cycle current limit. If fault > 64 switching cycles: Low-Side Gate (LSG), High-Side Gate (HSG), and PWM MOSFET (PWMOUT) turn off and fault flag FFn1 goes low. After t_{HIC} period, device performs auto soft-start.
Thermal Shutdown	VDRV, LED driver shuts down immediately and fault flag FFn1 goes low. Auto-restart with soft start occurs after the temperature drops below the TSD minus hysteresis level.
Programmable Output Overvoltage	Low-Side Gate (LSG) and High-Side Gate (HSG) turn off immediately. Fault flag FFn1 goes low. If OVB = 0, output voltage regulates at OV level with OV/UVHYS hysteresis If OVB = 1, PWM MOSFET (PWMOUT) also turns off. After hiccup period (t_{HIC}), driver auto-restarts with soft-start.
Output Overcurrent	Low-Side Gate (LSG), High-Side Gate (HSG), and PWM MOSFET (PWMOUT) turn off after programmable number of switching cycles. Switching cycles can be programmed through SPI. Fault flag FFn1 goes low. After hiccup period (t_{HIC}), driver auto-restarts with soft-start.
LED Short or Output Undervoltage	Fault flag FFn1 goes low after 30 switching cycles. Device continues to operate normally if one out all out feature is not selected. LED Driver stops switching if one out all out feature is selected.
LP PWMOUT Undervoltage	PWM MOSFET (PWMOUT) turns off immediately. Low-side Gate (LSG) and High-Side Gate (HSG) continue switching to pump up output voltage. Once output rises above $V_{PWMUVON}$, PWMOUT is re-activated.
LED Open	Low-Side Gate (LSG) and High-Side Gate turn off immediately. Fault flag FFn1 goes low. If OVB = 0, output voltage regulates at OV level with OV/UVHYS hysteresis. If OVB = 1, PWM MOSFET (PWMOUT) also turns off. After hiccup period (t_{HIC}), driver auto-restarts with soft-start.
High Beam Fault	Fault flag FFn1 goes low. Device transitions to low-beam mode. Restart device or write one to D5 bit of Diag 1 register to clear the fault.
FSET Pin Open/Short Fault	Fault flag FFn1 goes low. The oscillator outputs default frequency of 350 kHz.
LED String Short	Low-Side Gate (LSG), High-Side Gate (HSG), and PWM MOSFET (PWMOUT) turn off after two switching cycles. Fault flag FFn1 goes low. Switching ceases for hiccup cool down period (t_{HIC}) before driver auto-restarts with soft-start.

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Startup Timing Diagrams

For all timing diagrams, LED current is linear during soft-start once regulator output voltage is higher than LED forward bias voltage.

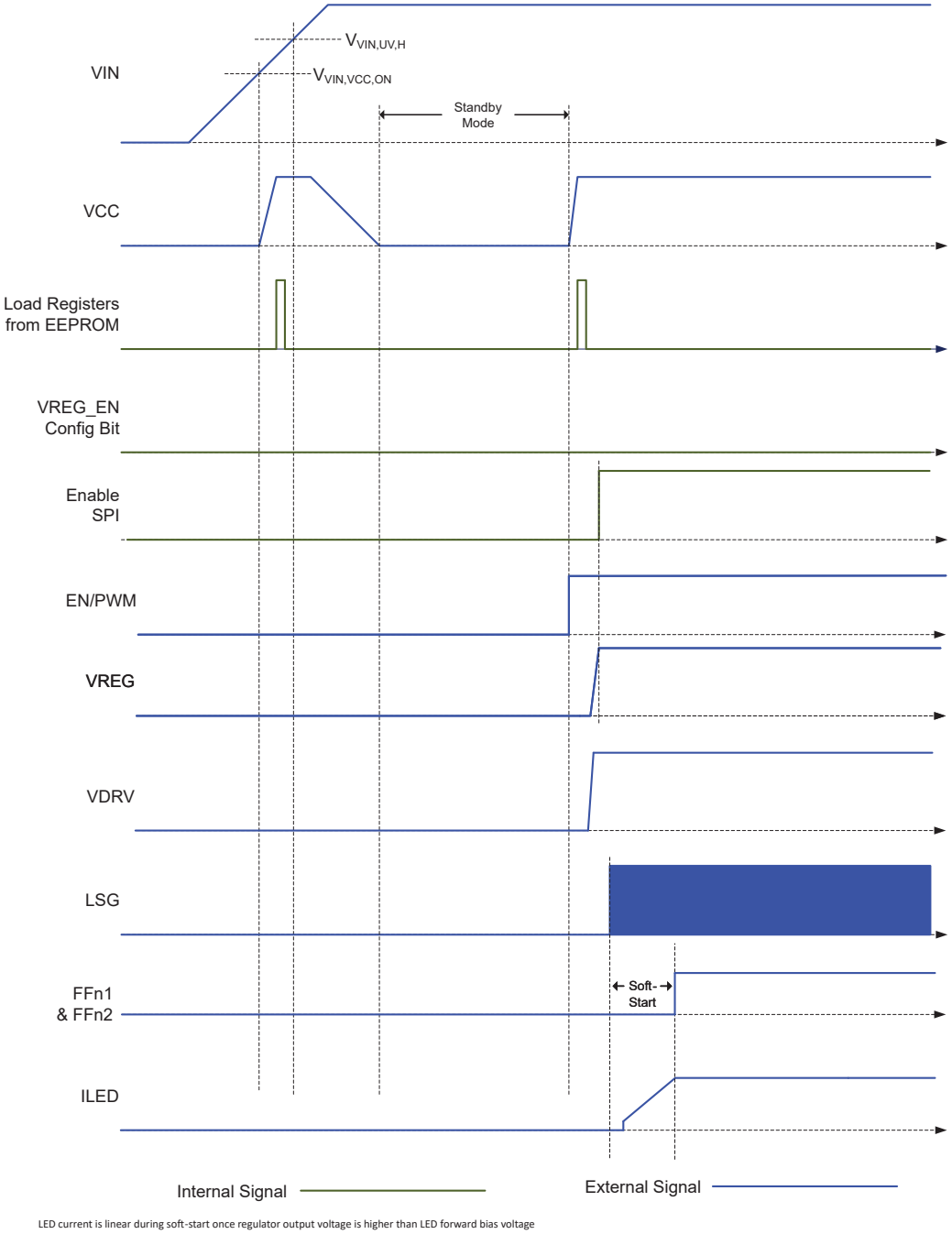

Figure 26: Startup with VREG_EN = 0 for Standby Mode Operation. Device enters normal operation after EN/PWM is High.

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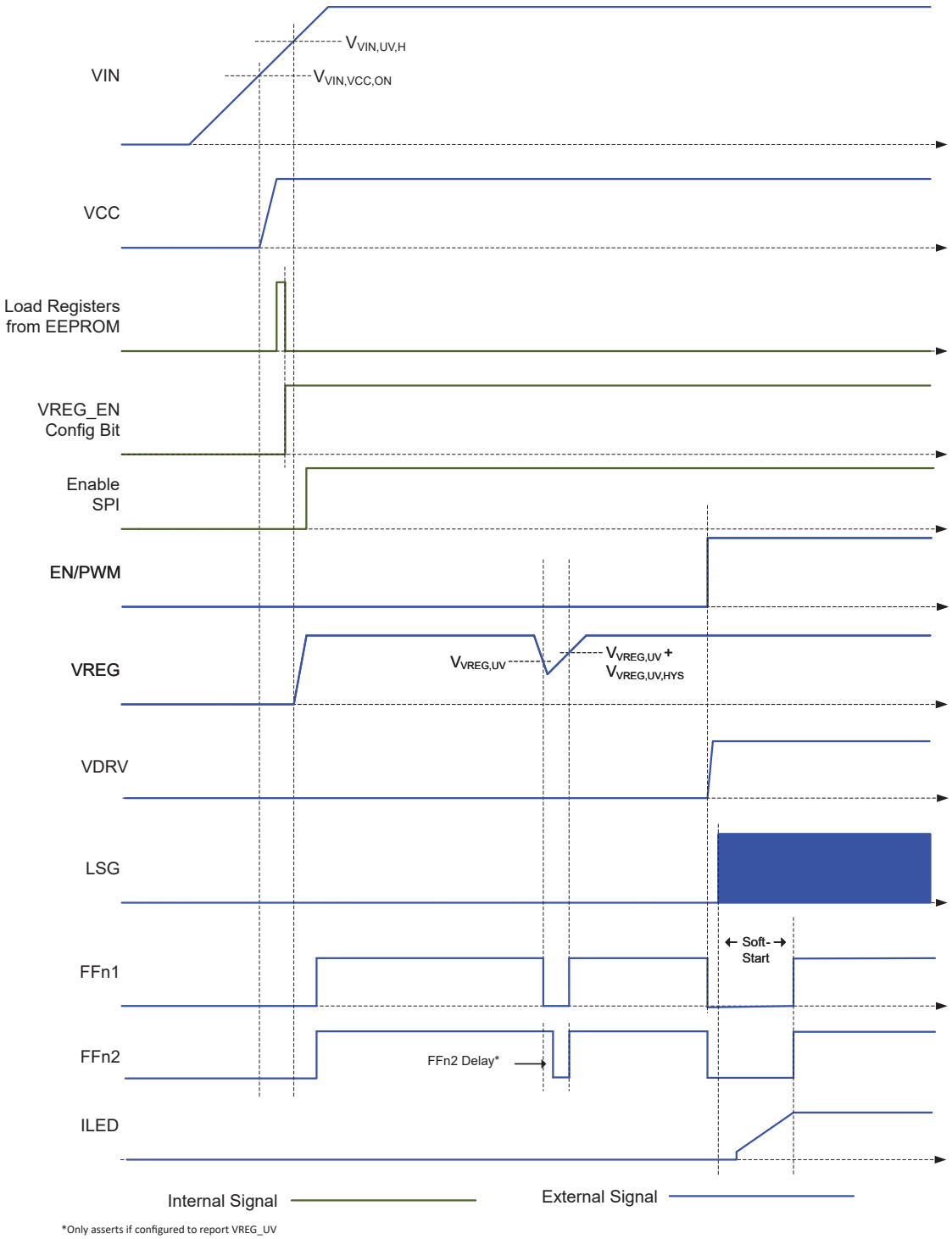

Figure 27: Startup with VREG_EN = 1 for Linear Regulator Operation. Device enters normal operation after EN/PWM is High.

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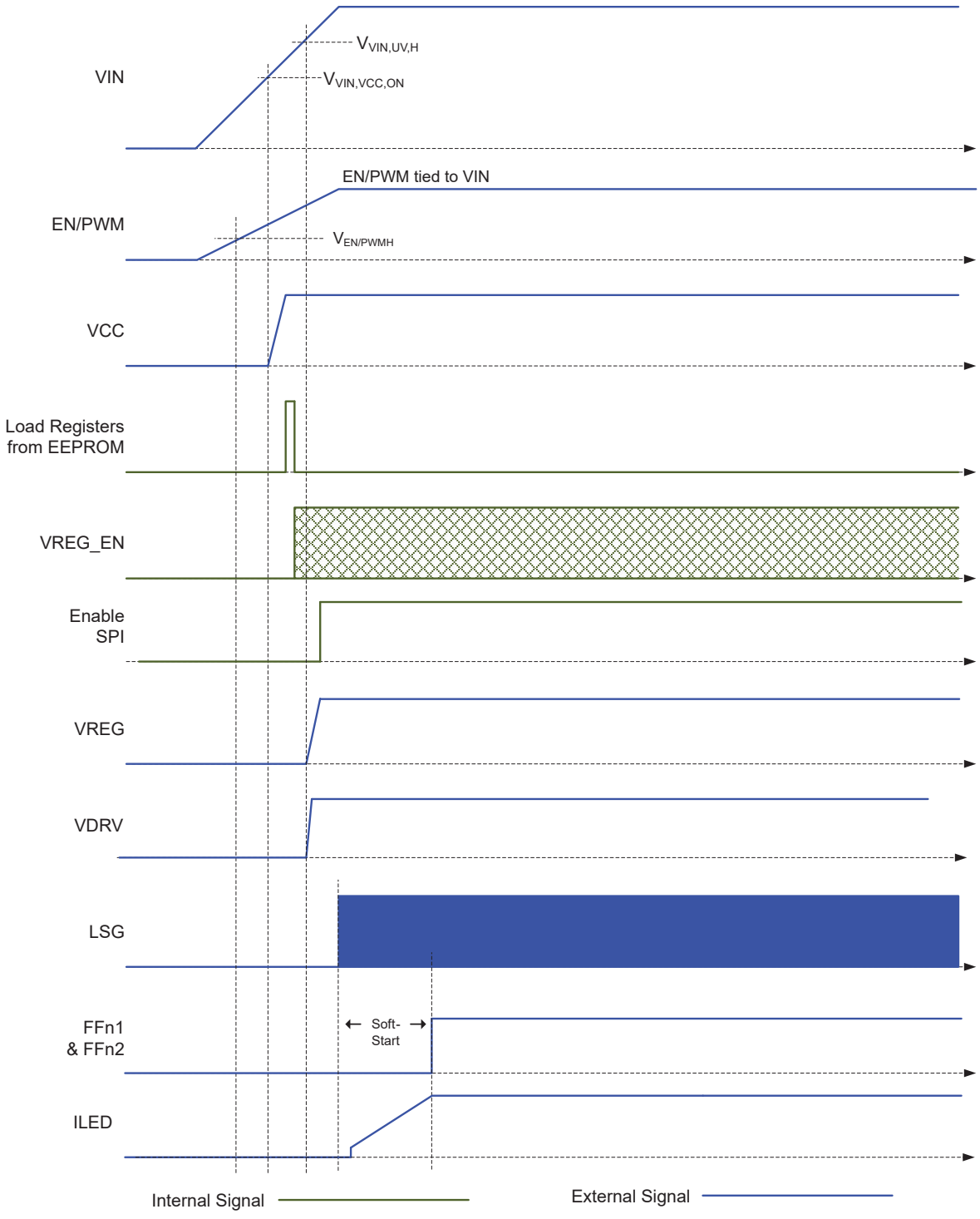

Figure 28: Startup with EN/PWM = VIN.
Device enters normal operation after VIN is above input undervoltage threshold.

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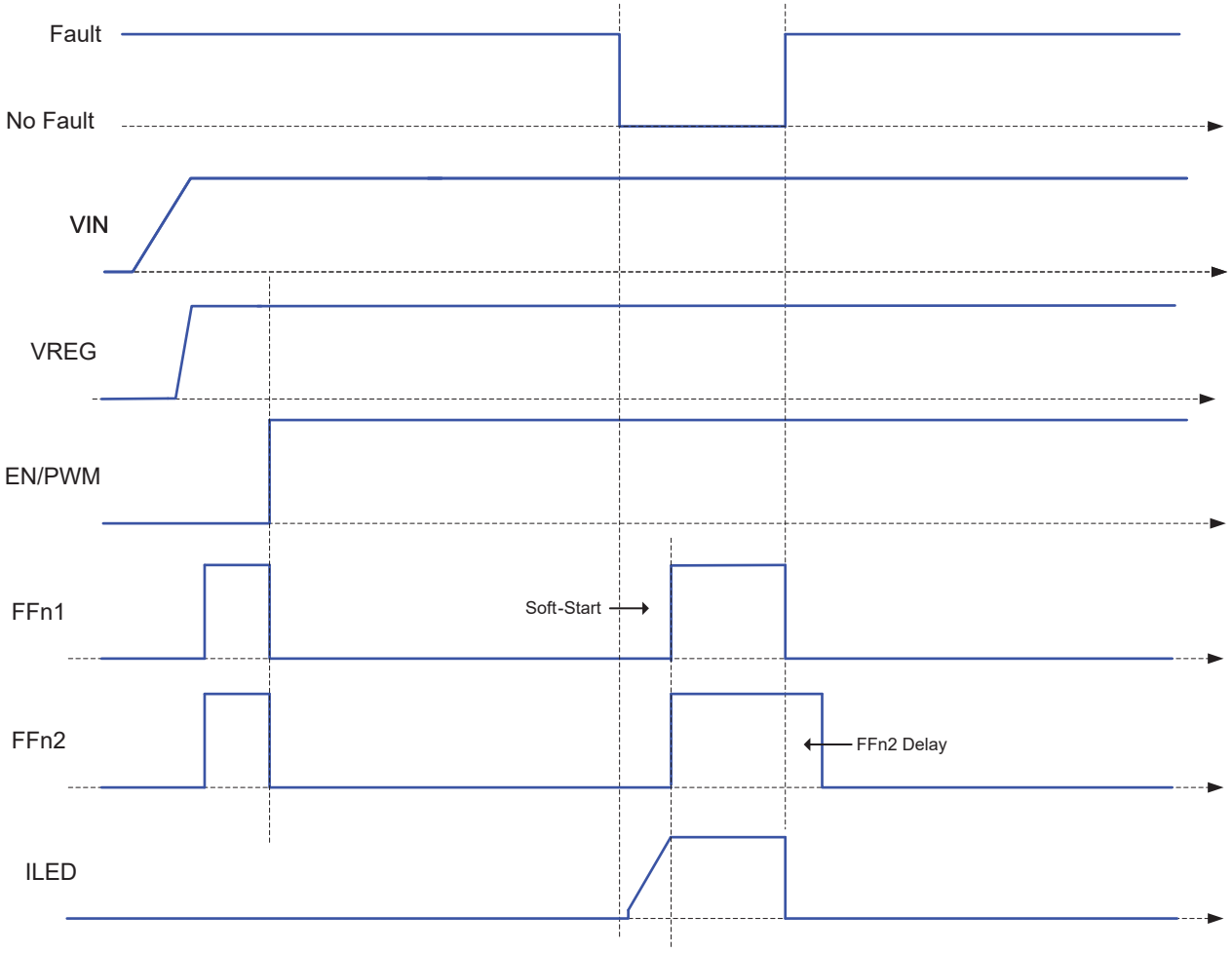

Figure 29: Startup into fault condition with FFn2 configured to report the fault (VREG_EN = 1)

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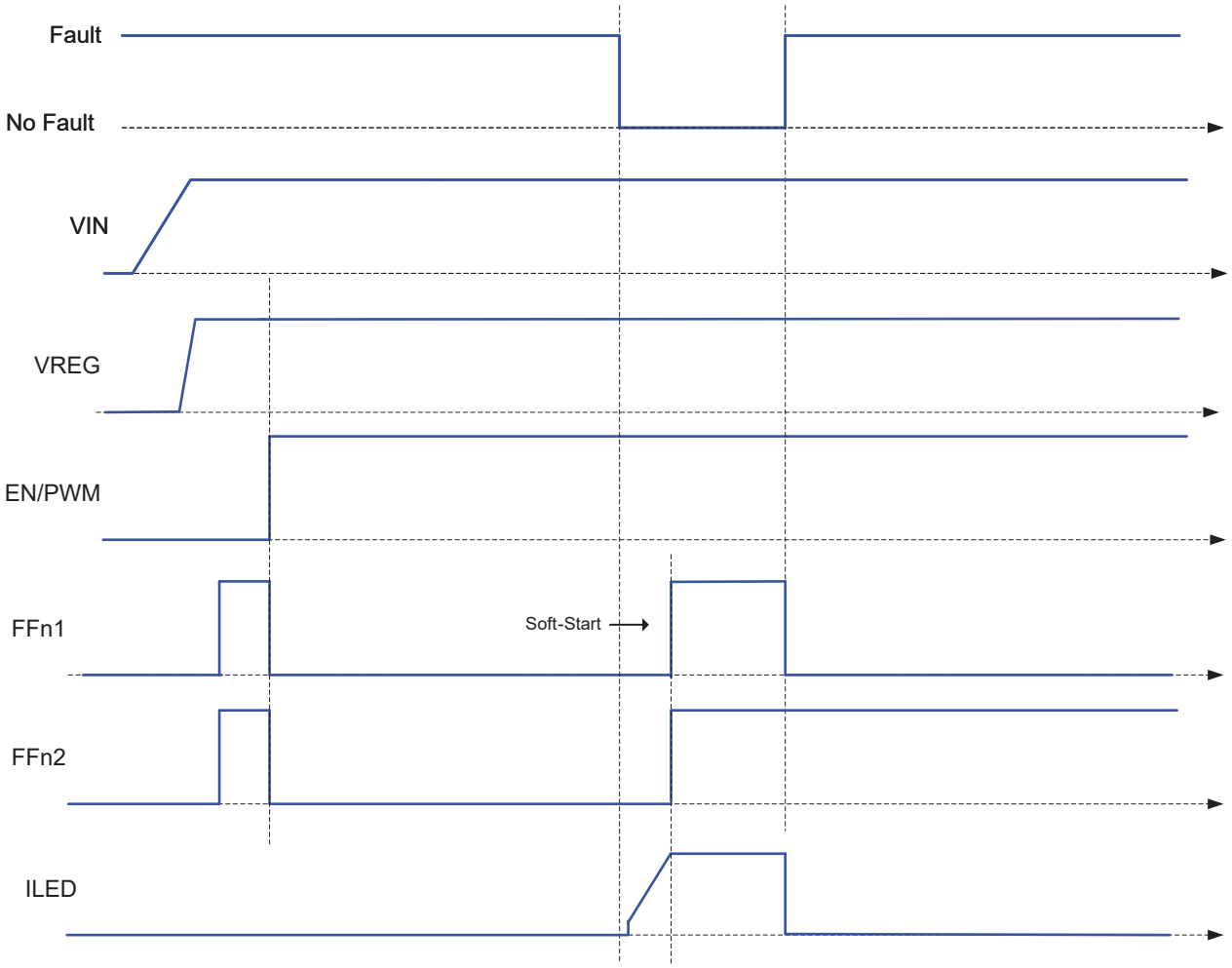

Figure 30: Startup into fault condition with FFn2 configured to not report the fault (VREG_EN = 1)

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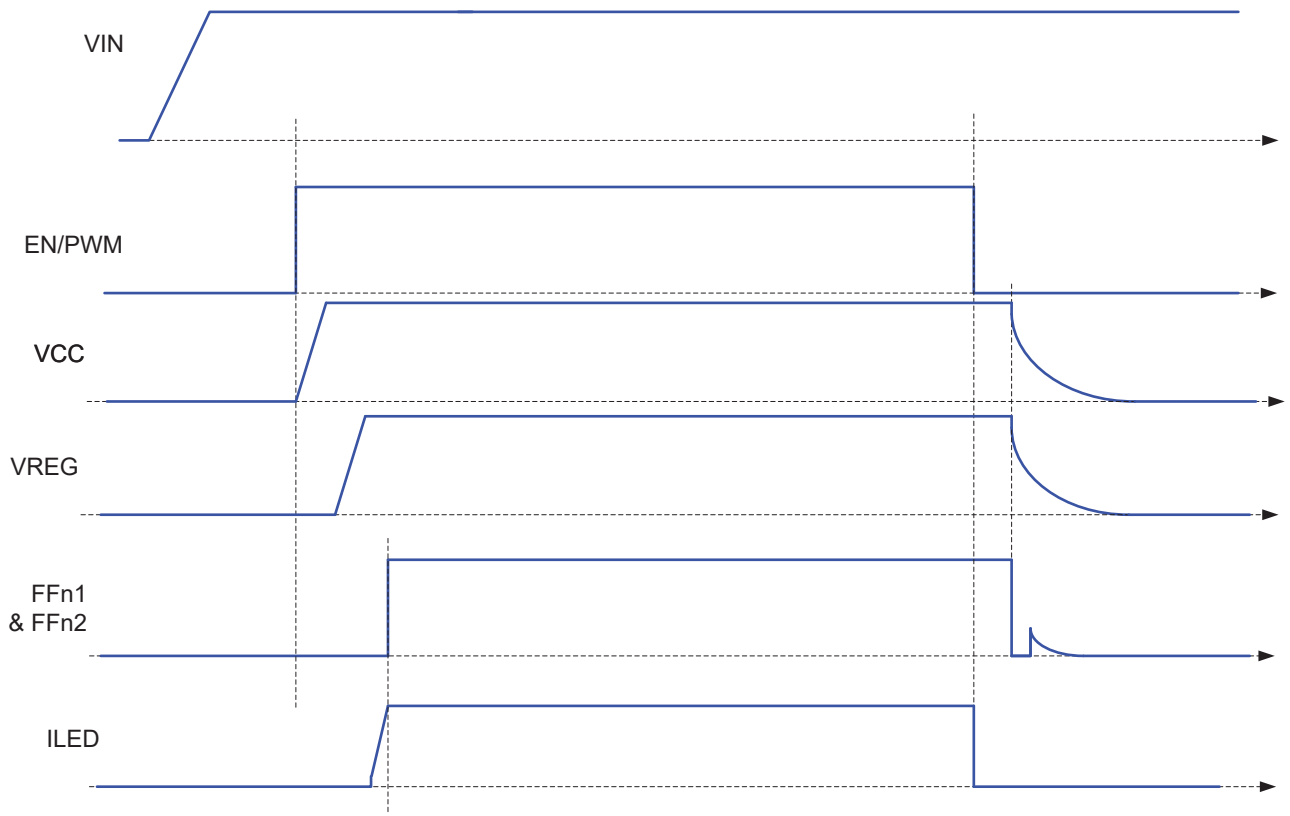

Figure 31: Startup and Shutdown with VREG_EN = 0

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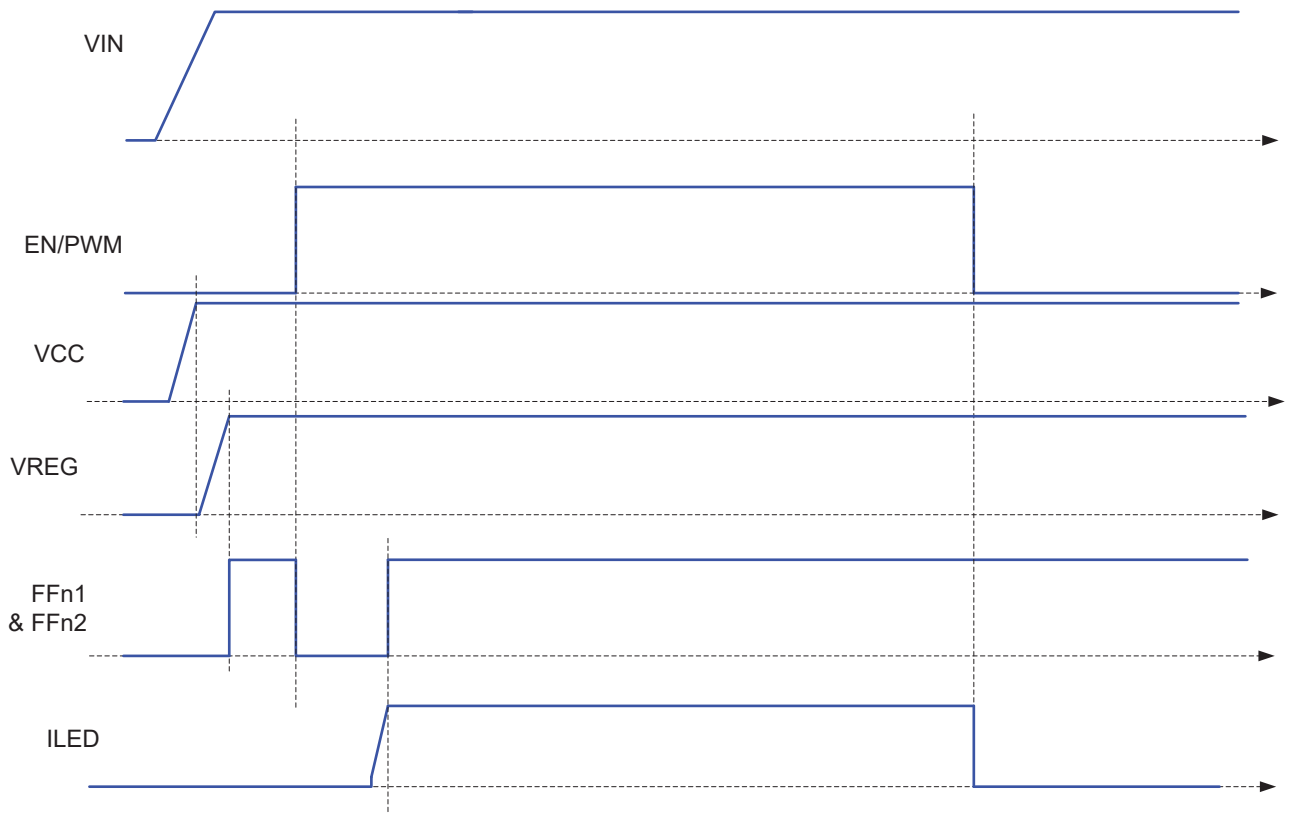

Figure 32: Startup and Shutdown with VREG_EN = 1

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Serial Communication

The A80803 provides the user with a three-wire synchronous serial interface that is compatible with SPI (Serial Peripheral Interface). A fourth wire can be used to provide diagnostic feedback and read back of the register content. The MOSI (Master Out Slave In), SCK (Serial Clock), and CSn (Slave Select) pins are used by the serial interface of the A80803. The MISO (Master In Slave Out) pin can be used to read back from the device.

The serial interface timing requirements are specified in the electrical characteristics table and illustrated in Figure 2. Serial data is received at the A80803 MOSI pin and clocked into a shift register on the rising edge of the clock signal on the SCK pin. The CSn pin should be held high and only driven low during a serial transfer. No data is clocked through the shift register when CSn is high allowing multiple devices to share the MOSI, MISO, and SCK signals. Each slave device requires an independent CSn signal from the master.

A graphical user interface (GUI) software tool is available for download to demonstrate interacting with the configuration registers.

SPI Pins

MOSI: Serial data logic input with pull-down. 16-bit serial word, input MSB first.

SCK: Serial clock logic input with pull-down. Data is latched in from MOSI on the rising edge of SCK. There must be 16 rising edges per write and SCK must be held high when CSn changes.

CSn: Serial data strobe and serial access enable logic input with pull-up. When CSn is high, any activity on SCK or MOSI is ignored and MISO is high impedance, allowing multiple MOSI slaves to have common MOSI, SCK, and MISO connections.

MISO: Serial data output. High impedance when CSn is high. Output bit 15 of the status register, the fault flag (FF), as soon as CSn goes low.

Start a transaction by driving the CSn pin low. After 16 bits have been clocked in to the MOSI pin CSn must be driven high to latch the data into the selected register. The internal control circuits then act on the new data.

If there are more than 16 rising edges on SCK or if CSn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset and the SE (serial error) bit will be set to indicate a data transfer error. The value of the SE bit is from the previous transaction.

The A80803 reports diagnostic and configuration register data on the MISO terminal MSB first while CSn is low, and updates to the next bit on each falling edge of SCK. The first bit, which is always the FF (fault flag) bit from the Diagnostic register, is output as soon as CSn goes low.

SPI Data Frames

To write to any of the write-accessible registers, transfer a 16-bit data frame starting with a 5-bit address, 1 write/read bit, 8 data bits and 1 parity bit as the LSB. See Table 34.

Table 34: SPI MOSI Pin During Read or Write

D15	D14	D13	D12	D11	D10	D9	D8
Register Address [4:0]					W/R	X	Data [7]
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data [6:0]							P

The register address (bits 15:11) specifies which register to write data to or read data from.

To read data from the specified address, set W/$\overline{R}$ to 0. The data bits (bits 9 to 1) are ignored during a read and the register content is clocked out onto the MOSI pin with some diagnostic information, as shown in Table 35. The A80803 cannot transmit data for a read if $V_{REG} < 2$ V.

Table 35: SPI MISO Pin During Read

D15	D14	D13	D12	D11	D10	D9	D8
FF	EE	SE	OUT_OV	OUT_UV	OPENLED	VREG_UV	Data [7]
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data [6:0]							P

To write data to the specific address, set W/$\overline{R}$ to 1. The data bits (bits 9 to 1) will be written to the register when the transaction completes and CSn goes high. During the write transaction the MOSI pin will report diagnostic information, taking advantage of the unused read-back bits to show additional information. See Table 36.

Table 36: SPI MISO Pin During Write

D15	D14	D13	D12	D11	D10	D9	D8
FF	EE	SE	OUT_OV	OUT_UV	OPENLED	VREG_UV	OUT_OC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FSET_FLT	0	LSG_FLT	TEMP_FLT	0	0	0	P

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The parity bit (bit 0, least significant bit) must be calculated for each transaction to ensure odd parity, meaning the sum of the total number of logical high bits is an odd number.

The MISO output updates to the next bit on each falling edge of the SCK. The first bit is always the FF bit from the status register and is output as soon as CS goes low. If an EEPROM Error (EE) occurs, it is reported on MISO after every read or write. A bad parity bit on a write will cancel the write and set the Serial Error (SE) bit in the MISO output. A bad parity bit on a read will also set the SE bit.

Reading and Writing Diagnostic Registers

DIAG0 and DIAG1 are directly addressable for reads and writes. To read DIAG0 or DIAG1 build a SPI transfer as shown in Table 34. Fault status bits are cleared when the fault is removed. Write a 1 to a fault diagnostic field to clear the fault; write 0xFF to both DIAG0 and DIAG1 to clear any faults.

Reading and Writing Configuration Registers

CONFIG0 – CONFIG22 are indirect access registers. Perform a write of the indirect address to register 0x03 to load the contents of a bank of three configuration registers into registers 0x05, 0x06, and 0x07, denoted as CONFIG_X, CONFIG_Y, and CONFIG_Z in Table 37. Use Table 38 to find the indirect register address for a particular configuration register. Read or write registers 0x05, 0x06, 0x07 with normal SPI transfers. Write 0x00 to 0x04 to latch any changes and update the corresponding configuration registers.

Table 37: Indirect Register Access

0x03	0x04	0x05	0x06	0x07
Indirect Address	Write to Latch	CONFIG_X	CONFIG_Y	CONFIG_Z

Table 38: Indirect Register Bank Addresses

Indirect Address	CONFIG_X	CONFIG_Y	CONFIG_Z
0x18	Config_2	Config_1	Config_0
0x19	Config_5	Config_4	Config_3
0x1A	Config_8	Config_7	Config_6
0x1B	Config_11	Config_10	Config_9
0x1C	Config_14	Config_13	Config_12
0x1D	Config_17	Config_16	Config_15
0x1E	Config_20	Config_19	Config_18
0x1F	N/A	Config_22	Config_21

Reading EEPROM

The EEPROM registers are 32 bits wide and each EEPROM register represents three Config registers in bits [23:0]. The EEPROM registers are read the same way as the configuration registers but have a different initial address offset, as shown in Table 39. The indirect address of the EEPROM_CFGx registers are offset from a group of three Config_x registers it represents by 0x10, so EEPRROM_CFG1 represents Config_2 in bits [23:16], Config_1 in bits [15:8] and Config_0 in bits [7:0].

Table 39: EEPROM Registers

0x03	0x04 [31:24]	0x05 [23:16]	0x06 [15:8]	0x07 [7:0]
0x08	Write 0x00 to latch a change	EEPROM_CFG1		
0x09		EEPROM_CFG2		
0xA		EEPROM_CFG3		
0xB		EEPROM_CFG4		
0xC		EEPROM_CFG5		
0xD		EEPROM_CFG6		
0xE		EEPROM_CFG7		
0xF		EEPROM_CFG8		

Writing EEPROM

Writing EEPROM is similar to writing to the configuration registers except it must be unlocked to accept writes. There are seven unlock keys, each 20 bits wide, that must be sent in succession, and the unlock sequence must be the first SPI transfer after a power-on. The unlock keys are shown in Table 40.

Table 40: EEPROM Write Unlock Sequence

Key	Code
0	0x7C339
1	0x71C7D
2	0x650FE
3	0x9E0E1
4	0x7A13F
5	0x5B393
6	0x60604

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Table 41: Register Map

Register	Description	Access	Default	D7	D6	D5	D4	D3	D2	D1	D0
Diag 0	Fault Reporting 1	R, W1C	0x00	FF	FLT _VDRV_UV	FLT_OUT_OV	FLT_OUT_UV	FLT_OUT_OC	FLT_OPENLED	FLT_LEDSHORT	FLT_STRSHORT
Diag 1	Fault Reporting 2	R, W1C	0x00	FLT_VIN_OV	FLT_VIN_UV	FLT_HBF	FLT_FSET	0	FLT_LSG_OC	FLT_VREG_UV	FLT_TEMP
Config 0	Frequency Dither	RW	0x08	RESERVED	DRVR_OFF	VREG_EN	DITH_F RNG		DITH_MOD		RESERVED
Config 1	Soft-start, Input UV and OV	RW	0xF0	VINOV			LEDSC	SFST		VINUV	
Config 2	Output Current for Binning	RW	0x50	KBIN1				KBIN2			
Config 3	Output Current for Binning	RW	0xCF	KBIN3				KBIN4			
Config 4	Thermal foldback	RW	0x26	RESERVED	KNTC		VNTC				
Config 5	Thermal foldback	RW	0x0E	RESERVED			SF1NTC				
Config 6	Thermal foldback	RW	0x08	RESERVED			SF2NTC				
Config 7	Thermal foldback	RW	0x03	RESERVED			SF3NTC				
Config 8	Thermal foldback	RW	0x00	RESERVED			SF4NTC				
Config 9	Input voltage LED current foldback	RW	0x07	RESERVED			SF1VIN				
Config 10	Input voltage LED current foldback	RW	0x05	RESERVED			SF2VIN				
Config 11	Input voltage LED current foldback	RW	0x02	RESERVED			SF3VIN				
Config 12	Input voltage LED current foldback	RW	0x01	RESERVED			SF4VIN				
Config 13	Input voltage LED current foldback	RW	0x13	RESERVED		KVIN			VIN1		
Config 14	PWM dimming	RW	0x00	PWM_EN	PWM_FREQ		RESERVED			PWM_DRV	
Config 15	PWM dimming	RW	0x00	PWM_DUTY							
Config 16	High Low Beam Control & Deadtime	RW	0x00	RESERVED				TDEAD		HBGCTRL	HBG_ON
Config 17	High Beam LED Overvoltage	RW	0x1F	RESERVED		OVB	OV_HB				
Config 18	Low Beam LED Overvoltage	RW	0x1F	RESERVED			OV_LB				
Config 19	High Beam LED Undervoltage	RW	0x00	RESERVED			UV_HB				
Config 20	Low Beam LED Undervoltage	RW	0x00	RESERVED			UV_LB				
Config 21	Fault Flag Behavior 1	RW	0x1F	RESERVED		F F2_VREG_UV	F F2_OUT_OV	FF2_OUT_UV	FF2_OUT_OC	FF2_OPENLED	FF2_STRSHORT
Config 22	Fault Flag Behavior 2	RW	0x03	OOAO		OCFILT		FFN2DLY		FF2_HBF	FF2_TEMP

R = Read
W = Write
W1C = Write 1 to clear
Write 0 to all RESERVED fields.

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Register Descriptions

DIAG0

Indirect Address		N/A	
Direct Address		0x00	
Field	**Bit**	**Default**	**Description**
FF	[7]	0	Fault Flag status bit. This bit is set while any of the status or diagnostic bits are set.
FLT_VDRV_UV	[6]	0	VDRV undervoltage fault status bit
FLT_OUT_OV	[5]	0	Output overvoltage fault diagnostic bit
FLT_OUT_UV	[4]	0	Output undervoltage fault diagnostic bit
FLT_OUT_OC	[3]	0	Output overcurrent fault diagnostic bit
FLT_OPENLED	[2]	0	Open LED fault diagnostic bit
FLT_LEDSHORT	[1]	0	Short LED fault diagnostic bit
FLT_STRSHORT	[0]	0	Short LED string fault diagnostic bit

DIAG1

Indirect Address		N/A	
Direct Address		0x01	
Field	**Bit**	**Default**	**Description**
FLT_VIN_OV	[7]	0	Input overvoltage fault diagnostic bit
FLT_VIN_UV	[6]	0	Input undervoltage fault status bit
FLT_HBF	[5]	0	High-beam fault diagnostic bit
FLT_FSET	[4]	0	FSET fault diagnostic bit
RESERVED	[3]	0	This field is reserved
FLT_LSG_OC	[2]	0	Low-side switching stage overcurrent fault diagnostic bit
FLT_VREG_UV	[1]	0	VREG undervoltage fault status bit
FLT_TEMP	[0]	0	Overtemperature fault status bit

Fault diagnostic bits are latched until cleared. Write a 1 to clear a latched diagnostic field. The diagnostic bit will remain set if the fault state is still active. Fault status bits indicate an active fault and are automatically cleared when the fault is removed.

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CONFIG0

Indirect Address		0x18	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
RESERVED	[7]	0	RESERVED
DRVR_OFF	[6]	0	LED Driver State 0 = LED Driver enabled (default) 1 = LED Driver disabled
VREG_EN	[5]	0	VREG Enable State 0 = VREG off when A80803 in standby mode (default) 1 = VREG on when A80803 in standby mode
DITH_FRNG	[4:3]	0x2	Dithering Frequency Range 00 = Off 01 = ±5% 10 = ±10% (default) 11 = ±15%
DITH_MOD	[2:1]	0	Dithering Modulation 00 = 10 kHz (default) 01 = 5 kHz 10 = 15 kHz 11 = 22 kHz
RESERVED	[0]	0	RESERVED.

CONFIG1

Indirect Address		0x18	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
VINOV	[7:5]	0x7	Input Overvoltage Level 0 = Disabled (default) 1 = 18 V 2 = 19 V 3 = 20 V 4 = 21 V 5 = 33 V 6 = 34 V 7 = 35 V
LEDSC	[4]	0x1	LED Short Detection 0 = LED short detect disabled 1 = LED short detect enabled (default)
SFST	[3:2]	0	Soft-Start time 0 = 5 ms (default) 1 = 10 ms 2 = 15 ms 3 = 20 ms
VINUV	[1:0]	0	Input voltage UVLO 0 = 5.65 V rising, 4.75 V falling (default) 1 = 6.0 V rising, 5.1 V falling 2 = 6.5 V rising, 5.6 V falling 3 = 7.0 V rising, 6.1 V falling

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CONFIG2

Indirect Address		0x18	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
KBIN1	[7:4]	0x5	BIN1 output current multiplier 0 = Gain of 1 1 LSB = –0.025 15 = Gain of 0.625 5 = 0.875 (default)
KBIN2	[3:0]	0	BIN2 output current multiplier 0 = Gain of 1 (default) 1 LSB = –0.025 15 = Gain of 0.625

CONFIG3

Indirect Address		0x19	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
KBIN3	[7:4]	0xC	BIN1 output current multiplier 0 = Gain of 1 1 LSB = –0.025 15 = Gain of 0.625 12 = 0.7 (default)
KBIN4	[3:0]	0xF	BIN2 output current multiplier 0 = Gain of 1 1 LSB = –0.025 15 = Gain of 0.625 (default)

CONFIG4

Indirect Address		0x19	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
KNTC	[6:5]	0x2	NTC Output Current Multiplier 0 = 0.8 1 = 0.7 2 = 0.6 (default) 3 = 0.5
VNTC1	[4:0]	0x06	NTC pin voltage to start current foldback 0 = 1.2 V 1 LSB = 0.05 V 31 = 2.75 V 6 = 1.5 V (default)

CONFIG5

Indirect Address		0x19	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF1NTC	[4:0]	0xE	Slope Factor for BIN1 NTC Foldback

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CONFIG6

Indirect Address		0x1A	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF2NTC	[4:0]	0x08	Slope Factor for BIN2 NTC Foldback

CONFIG7

Indirect Address		0x1A	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF3NTC	[4:0]	0x03	Slope Factor for BIN3 NTC Foldback

CONFIG8

Indirect Address		0x1A	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF4NTC	[4:0]	0	Slope Factor for BIN4 NTC Foldback

CONFIG9

Indirect Address		0x1B	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF1VIN	[4:0]	0x07	Slope Factor for BIN1 VIN Foldback

CONFIG10

Indirect Address		0x1B	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF2VIN	[4:0]	0x05	Slope Factor for BIN2 VIN Foldback

CONFIG11

Indirect Address		0x1B	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF3VIN	[4:0]	0x02	Slope Factor for BIN3 VIN Foldback

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CONFIG12

Indirect Address		0x1C	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
SF4VIN	[4:0]	0x01	Slope Factor for BIN4 VIN Foldback

CONFIG13

Indirect Address		0x1C	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:6]	0	RESERVED
KVIN	[5:3]	0x4	Output current derating for VIN foldback 0 = 1 (Off) 1 = 0.8 2 = 0.7 3 = 0.6 4 = 0.5 (default) 5 = 0.4 6 = 0.3 7 = 0.2
VIN1	[2:0]	0x3	Input voltage to start VIN foldback derating 0 = 7.5 V 1 = 8 V 2 = 8.5 V 3 = 9 V (default) 4 = 9.5 V 5 = 10 V 6 = 10.5 V 7 = 11 V

CONFIG14

Indirect Address		0x1C	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
PWM_EN	[7]	0	Enable Internal PWM Dimming 0 = Force Internal PWM Off (default) 1 = Force Internal PWM On (overrides DIMn pin state)
PWM_FREQ	[6:5]	0	Internal PWM Frequency 0 = 200 Hz (default) 1 = 250 Hz 2 = 300 Hz 3 = 350 Hz
RESERVED	[4:2]	0	RESERVED
PWM_DRV	[1:0]	0	PWM MOSFET gate drive current 0 = 25 mA (default) 1 = 2 mA 2 = 0.5 mA 3 = 1 mA

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CONFIG15

Indirect Address		0x1D	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
PWM_DUTY	[7:0]	0	Internal PWM Dimming Duty Cycle 0 = 0% 1 LSB = 0.5% 200 = 100%

CONFIG16

Indirect Address		0x1D	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:4]	0	RESERVED
TDEAD	[3:2]	0	Additional dead time between LSG and HSG 0 = 0 ns (default) 1 = 10 ns 2 = 20 ns 3 = 40 ns
HBGCTRL	[1]	0	LBEAMn pin polarity 0 = HBG low (off) when LBEAMn low (default) 1 = HBG high (on) when LBEAMn low
HBG_ON	[0]	0	Force the high-beam gate on 0 = HBG follows LBEAMn pin (default) 1 = HBG forced on

CONFIG17

Indirect Address		0x1D	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:6]	0	RESERVED
OVB	[5]	0	Set driver operation during overvoltage event 0 = LED voltage is regulated to configured OV level (default) 1 = PWM MOSFET is turned Off
OV_HB	[4:0]	0x1F	High-Beam Overvoltage Trip Level 0 = 20.4 V 1 LSB = 1.6 V 31 = 70 V (default)

CONFIG18

Indirect Address		0x1E	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
OV_LB	[4:0]	0x1F	Low-Beam Overvoltage Trip Level 0 = 10.4 V 1 LSB = 1.6 V 31 = 60 V (default)

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CONFIG19

Indirect Address		0x1E	
Direct Address		0x06	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
UV_HB	[4:0]	0	High-Beam Undervoltage Trip Level 0 = 10.4 V (default) 1 LSB = 1.6 V 31 = 60 V

CONFIG20

Indirect Address		0x1E	
Direct Address		0x05	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:5]	0	RESERVED
UV_LB	[4:0]	0	Low-Beam Undervoltage Trip Level 0 = 2.4 V (default) 1 LSB = 1.6 V 31 = 52 V

CONFIG21

Indirect Address		0x1F	
Direct Address		0x07	
Field	**Bit**	**Default**	**Description**
RESERVED	[7:6]	0	RESERVED
FF2_VREG_UV	[5]	1	VREG_UV reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)
FF2_OUT_OV	[4]	1	OUT_OV reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)
FF2_OUT_UV	[3]	1	OUT_UV reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)
FF2_OUT_OC	[2]	1	OUT_OC reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)
FF2_OPENLED	[1]	1	OPENLED reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)
FF2_STRSHORT	[0]	1	STRSHORT reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)

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CONFIG22

Indirect Address		0x1F		
Direct Address		0x06		
Field	**Bit**	**Access**	**Default**	**Description**
OOAO	[7:6]	R/W	0	One-Out-All-Out Behavior 0 = Disabled (default) 1 = FFn1 becomes bidirectional enable/fault flag 2 = FFn2 becomes bidirectional enable/fault flag 3 = FFn1 and FFn2 become bidirectional enable/fault flag
OCFILT	[5:4]	R/W	0	Overcurrent detect filter delay 0 = 2 clock cycles (default) 1 = 4 clock cycles 2 = 8 clock cycles 3 = 16 clock cycles
FF2DLY	[3:2]	R/W	0	FF2 reporting delay 0 = 50 ms (default) 1 = 100 ms 2 = 1000 ms 3 = 2000 ms
FF2_HBF	[1]	R/W	1	High-Beam Fault reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)
FF2_TEMP	[0]	R/W	1	Overtemperature reported on FFn2 0 = Not reported on FFn2 1 = Reported on FFn2 (default)

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APPLICATIONS INFORMATION

Three Brightness Level DRL Headlamp Application

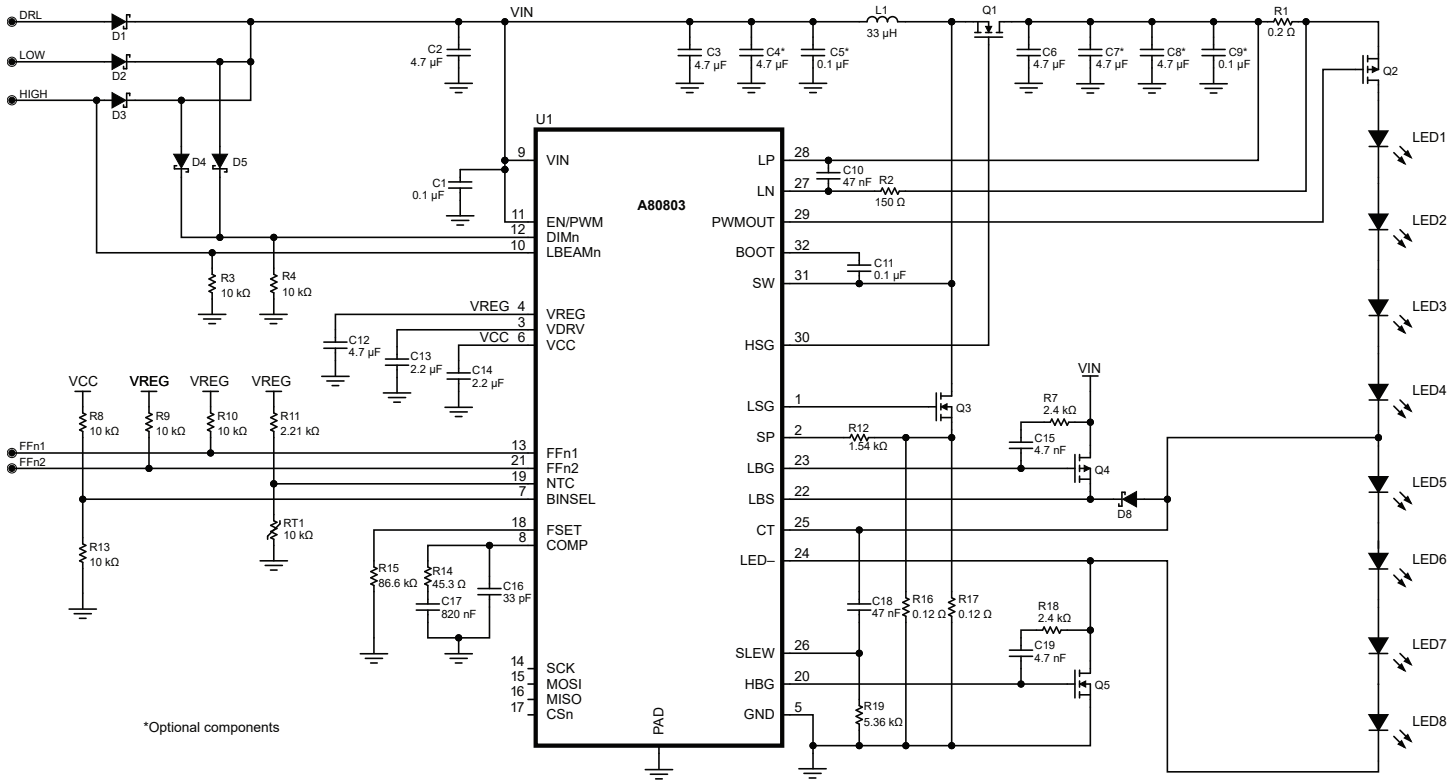

Figure 33: DRL, Low, High Tri-Level Lighting Application

Table 42: DRL Headlight Application Brightness Levels

Input Signal	EN/PWM	DIMn	LBEAMn	Switching Topology	LED Lighting Level
DRL	High	Low	Low	Buck-Boost	Internal PWM dimming from EEPROM
Low-Beam	High	High	Low	Buck-Boost	100% dimming for low-beam LEDs
High-Beam	High	High	High	Boost	100% dimming for all LEDs

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Table 43: Three Brightness Level DRL Headlamp Application Bill of Materials

Designator	Description	Quantity	Manufacturer	Manufacturer P/N
U1	A80803 in the QFN-32	1		
C1	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0603	1		
C2, C3, C4*	Capacitor, Ceramic, 4.7 µF, 50 V, X7R, 1210	3	Murata	GCM32ER71H475KA55K
C5*, C9*	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0805	2		
C6, C7*, C8*	Capacitor, Ceramic, 4.7 µF, 100 V, X7R, 1210	3	TDK	CNA6P1X7R2A475K250AE
C10	Capacitor, Ceramic, 47 nF, 25 V, X7R, 0402	1		
C11	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 0402	1		
C12	Capacitor, Ceramic, 4.7 µF, 16 V, X7R, 0805	1		
C13, C14	Capacitor, Ceramic, 2.2 µF, 16 V, X7R, 0805	2		
C15, C19	Capacitor, Ceramic, 4.7 nF, 50 V, X7R, 0402	2		
C16	Capacitor, Ceramic, 33 pF, 50 V, C0G, 0603	1		
C17	Capacitor, Ceramic, 820 nF, 25 V, X7R, 0603	1		
C18	Capacitor, Ceramic, 47 nF, 50 V, X7R, 0603	1		
D1, D2, D3, D4, D5	Diode, Schottky, 60 V, 5 A, SOD-128	5	Nexperia	PMEG60T50ELPX
D8	Diode, Schottky, 100 V, 2 A, SOD123W	1		
L1	Inductor, 33 µH, ±20%, 8 A (sat), 85.5 mΩ (max)	1	Eaton	HCMA1305-330-R
LED1 … LED8	White LED	8		
Q1, Q3	MOSFET, N-Channel, 30 A, 100 V, LFPAK56,	2	Nexperia	PSMN038-100YL
Q2, Q4	MOSFET, P-Channel, 100 V, 15 A, TO252-3	2	Infineon	SPD15P10PLGBTMA1
Q5	MOSFET, N-Channel, 14.8 A, 100 V, LFPAK56	1	Nexperia	BUK9Y104-100B
R1	Resistor, 0.2 Ω, 1 W, 1%, 2512	1		
R2	Resistor, 150 Ω, 1/16 W, 1%, 0402	1		
R3, R4, R8, R9, R10, R13	Resistor, 10 kΩ, 1/16 W, 1%, 0402	6		
R7, R18	Resistor, 2.4 kΩ, 1/16 W, 1%, 0402	2		
R11	Resistor, 2.21 kΩ, 1/16 W, 1%, 0402	1		
R12	Resistor, 1.54 kΩ, 1/16 W, 1%, 0402	1		
R14	Resistor, 45.3 Ω, 1/10 W, 1%, 0603	1		
R15	Resistor, 86.6 kΩ, 1/16 W, 1%, 0402	1		
R16, R17	Resistor, 0.12 Ω, 1 W, 1%, 2512	2		
R19	Resistor, 5.36 kΩ, 1/16 W, 1%, 0402	1		
RT1	Thermistor, NTC, 10 kΩ, 0603	1	Vishay	NTCS0603E3103FHT

* C4, C5, C7, C8, C9 are optional components.

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Two Brightness Level Lighting Application with Single MOSFET for Low/High-Beam

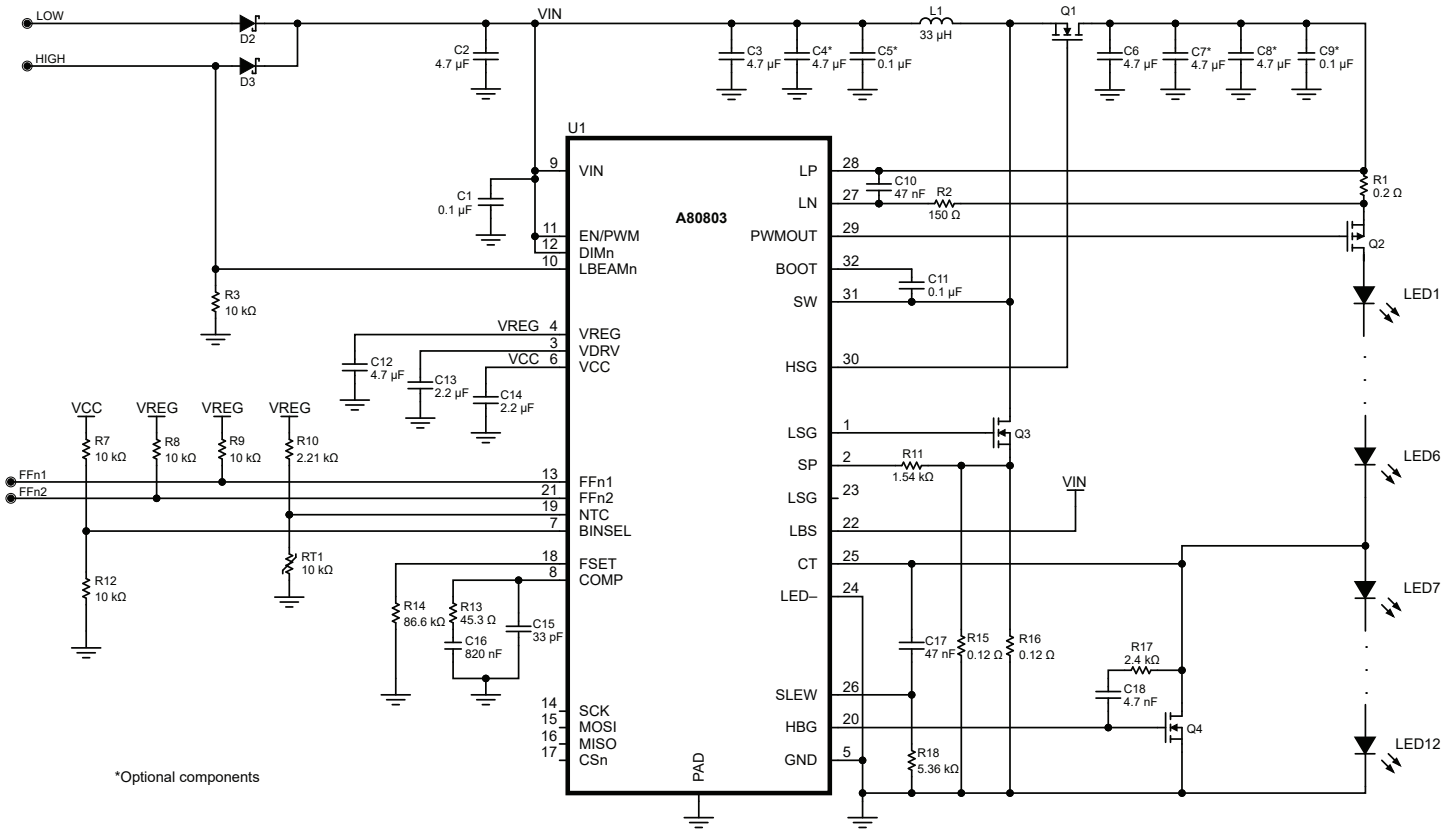

Figure 34: Two Brightness Level Boost LED Controller

Table 44: Boost LED Controller LED Brightness Levels

Input Signal	EN/PWM	DIMn	LBEAMn	Switching Topology	LED Lighting Level
Low-Beam	High	High	Low	Boost	100% dimming for low-beam LEDs
High-Beam	High	High	High	Boost	100% dimming for all LEDs

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Table 45: Two Brightness Level Lighting Application with Single MOSFET for Low/High-Beam Bill of Materials

Designator	Description	Quantity	Manufacturer	Manufacturer P/N
U1	A80803 in the QFN-32	1		
C1	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0603	1		
C2, C3, C4*	Capacitor, Ceramic, 4.7 µF, 50 V, X7R, 1210	3	Murata	GCM32ER71H475KA55K
C5*, C9*	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0805	2		
C6, C7*, C8*	Capacitor, Ceramic, 4.7 µF, 100 V, X7R, 1210	3	TDK	CNA6P1X7R2A475K250AE
C10	Capacitor, Ceramic, 47 nF, 25 V, X7R, 0402	1		
C11	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 0402	1		
C12	Capacitor, Ceramic, 4.7 µF, 16 V, X7R, 0805	1		
C13, C14	Capacitor, Ceramic, 2.2 µF, 16 V, X7R, 0805	2		
C15	Capacitor, Ceramic, 33 pF, 50 V, C0G, 0603	1		
C16	Capacitor, Ceramic, 820 nF, 25 V, X7R, 0603	1		
C17	Capacitor, Ceramic, 47 nF, 50 V, X7R, 0603	1		
C18	Capacitor, Ceramic, 4.7 nF, 50 V, X7R, 0402	1		
D2, D3	Diode, Schottky, 60 V, 5 A, SOD-128	2	Nexperia	PMEG60T50ELPX
L1	Inductor, 33 µH, ±20%, 8 A (sat), 85.5 mΩ (max)	1	Eaton	HCMA1305-330-R
LED1…LED12	White LED	12		
Q1, Q3	MOSFET, N-Channel, 30 A, 100 V, LFPAK56	2	Nexperia	PSMN038-100YL
Q2	MOSFET, P-Channel, 100 V, 15 A, TO252-3	1	Infineon	SPD15P10PLGBTMA1
Q4	MOSFET, N-Channel, 14.8 A, 100 V, LFPAK56	1	Nexperia	BUK9Y104-100B
R1	Resistor, 0.2 Ω, 1 W, 1%, 2512	1		
R2	Resistor, 150 Ω, 1/16 W, 1%, 0402	1		
R3, R7, R8, R9, R12	Resistor, 10 kΩ, 1/16 W, 1%, 0402	5		
R10	Resistor, 2.21 kΩ, 1/16 W, 1%, 0402	1		
R11	Resistor, 1.54 kΩ, 1/16 W, 1%, 0402	1		
R13	Resistor, 45.3 Ω, 1/10 W, 1%, 0603	1		
R14	Resistor, 86.6 kΩ, 1/16 W, 1%, 0402	1		
R15, R16	Resistor, 0.12 Ω, 1 W, 1%, 2512	2		
R17	Resistor, 2.4 kΩ, 1/16 W, 1%, 0402	1		
R18	Resistor, 5.36 kΩ, 1/16 W, 1%, 0402	1		
RT1	Thermistor, NTC, 10 kΩ, 0603	1	Vishay	NTCS0603E3103FHT

* C4, C5, C7, C8, C9 are optional components.

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Single LED String Boost Controller with Configurable Internal PWM Dimming

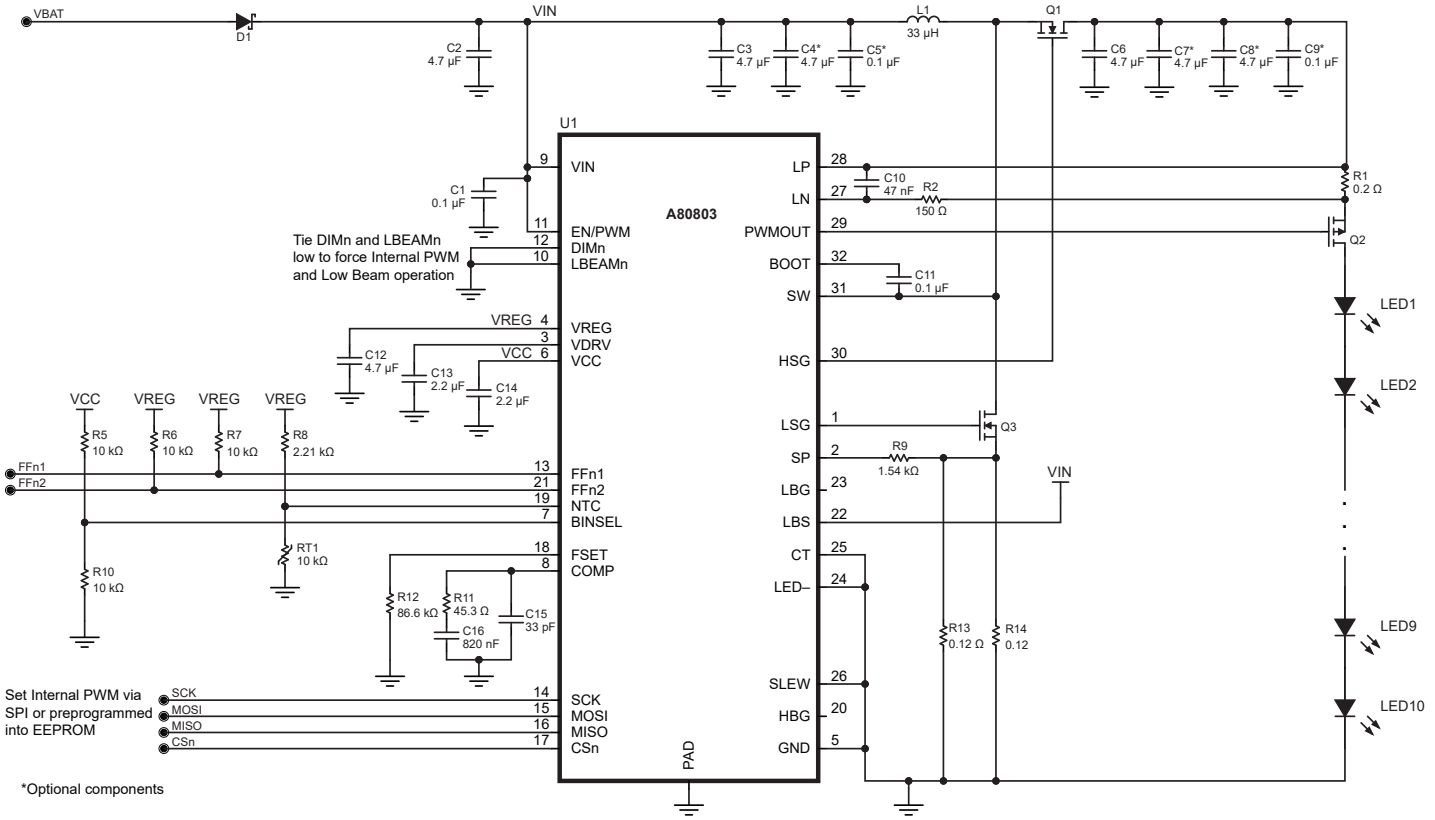

Figure 35: Boost LED Controller with Internal PWM Dimming

Table 46: Boost LED Controller Brightness Levels

Input Signal	EN/PWM	DIMn	LBEAMn	Switching Topology	LED Lighting Level
VIN	High	Low	Low	Boost	Set via PWM_DUTY field in CONFIG15

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Table 47: Single LED String Boost Controller with Configurable Internal PWM Dimming Bill of Materials

Designator	Description	Quantity	Manufacturer	Manufacturer P/N
U1	A80803 in the QFN-32	1		
C1	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0603	1		
C2, C3, C4*	Capacitor, Ceramic, 4.7 µF, 50 V, X7R, 1210	3	Murata	GCM32ER71H475KA55K
C5*, C9*	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0805	2		
C6, C7*, C8*	Capacitor, Ceramic, 4.7 µF, 100 V, X7R, 1210	3	TDK	CNA6P1X7R2A475K250AE
C10	Capacitor, Ceramic, 47 nF, 25 V, X7R, 0402	1		
C11	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 0402	1		
C12	Capacitor, Ceramic, 4.7 µF, 16 V, X7R, 0805	1		
C13, C14	Capacitor, Ceramic, 2.2 µF, 16 V, X7R, 0805	2		
C15	Capacitor, Ceramic, 33 pF, 50 V, C0G, 0603	1		
C16	Capacitor, Ceramic, 820 nF, 25 V, X7R, 0603	1		
D1	Diode, Schottky, 60 V, 5 A, SOD-128	1	Nexperia	PMEG60T50ELPX
L1	Inductor, 33 µH, ±20%, 8 A (sat), 85.5 mΩ (max)	1	Eaton	HCMA1305-330-R
LED1 … LED10	White LED	10		
Q1, Q3	MOSFET, N-Channel, 30 A, 100 V, LFPAK56	2	Nexperia	PSMN038-100YL
Q2	MOSFET, P-Channel, 100 V, 15 A, TO252-3	1	Infineon	SPD15P10PLGBTMA1
R1	Resistor, 0.2 Ω, 1 W, 1%, 2512	1		
R2	Resistor, 150 Ω, 1/16 W, 1%, 0402	1		
R5, R6, R7, R10	Resistor, 10 kΩ, 1/16 W, 1%, 0402	4		
R8	Resistor, 2.21 kΩ, 1/16 W, 1%, 0402	1		
R9	Resistor, 1.54 kΩ, 1/16 W, 1%, 0402	1		
R11	Resistor, 45.3 Ω, 1/10 W, 1%, 0603	1		
R12	Resistor, 86.6 kΩ, 1/16 W, 1%, 0402	1		
R13, R14	Resistor, 0.12 Ω, 1 W, 1%, 2512	2		
RT1	Thermistor, NTC, 10 kΩ, 0603	1	Vishay	NTCS0603E3103FHT

* C4, C5, C7, C8, C9 are optional components.

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Single LED String Buck-Boost LED Controller with External PWM

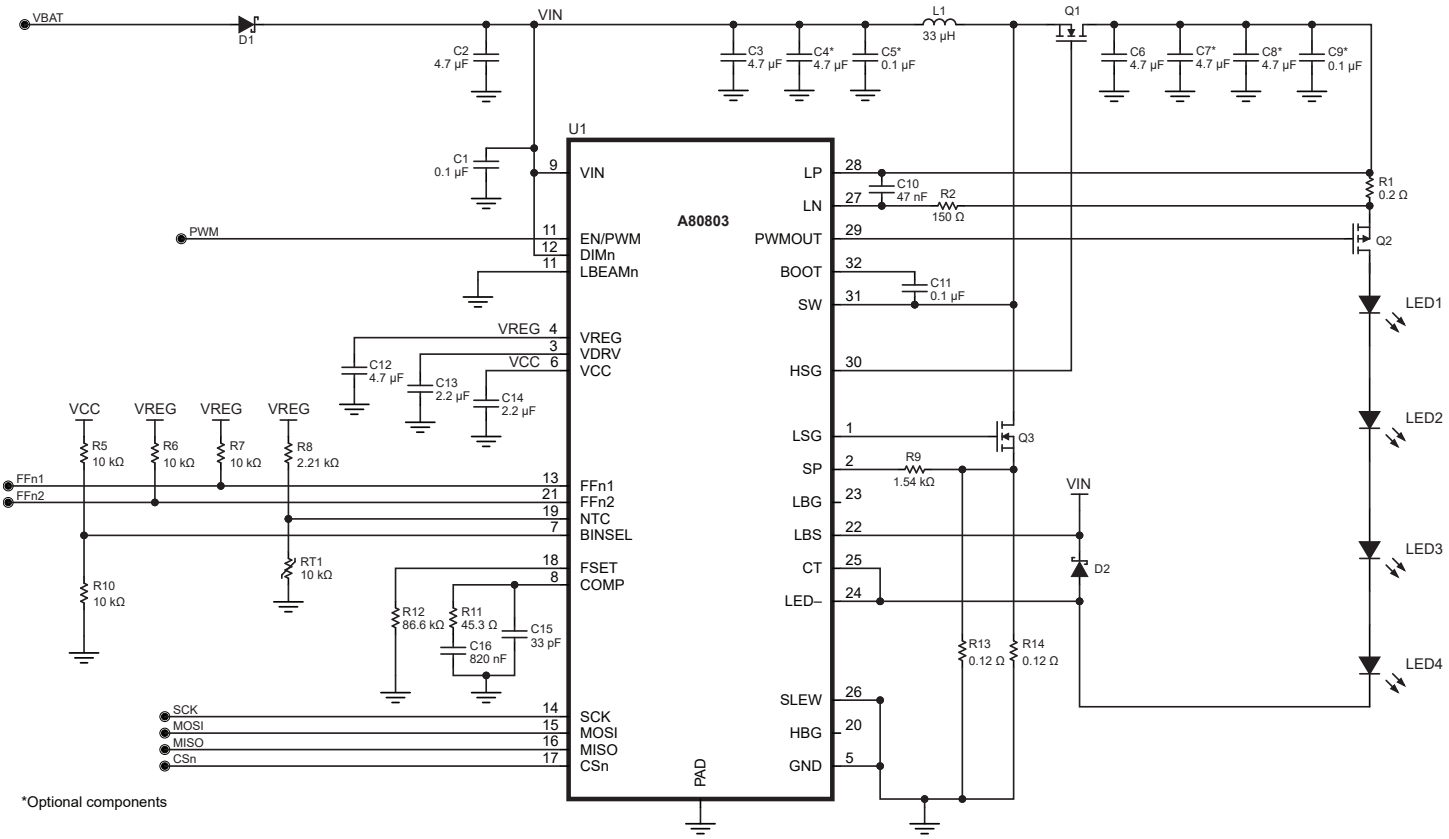

Figure 36: Buck-Boost LED Controller with External PWM

Table 48: Boost LED Controller Brightness Levels

Input Signal	EN/PWM	DIMn	LBEAMn	Switching Topology	LED Lighting Level
VIN	External Signal	High	Low	Buck-Boost	Set via external PWM signal on EN/PWM pin

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Table 49: Single LED String Buck-Boost LED Controller with External PWM Bill of Materials

Designator	Description	Quantity	Manufacturer	Manufacturer P/N
U1	A80803 in the QFN-32	1		
C1	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0603	1		
C2, C3, C4*	Capacitor, Ceramic, 4.7 µF, 50 V, X7R, 1210	3	Murata	GCM32ER71H475KA55K
C5*, C9*	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0805	2		
C6, C7*, C8*	Capacitor, Ceramic, 4.7 µF, 100 V, X7R, 1210	3	TDK	CNA6P1X7R2A475K250AE
C10	Capacitor, Ceramic, 47 nF, 25 V, X7R, 0402	1		
C11	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 0402	1		
C12	Capacitor, Ceramic, 4.7 µF, 16 V, X7R, 0805	1		
C13, C14	Capacitor, Ceramic, 2.2 µF, 16 V, X7R, 0805	2		
C15	Capacitor, Ceramic, 33 pF, 50 V, C0G, 0603	1		
C16	Capacitor, Ceramic, 820 nF, 25 V, X7R, 0603	1		
D1	Diode, Schottky, 60 V, 5 A, SOD-128	1	Nexperia	PMEG60T50ELPX
D2	Diode, Schottky, 100 V, 2 A, SOD-123W	1	Nexperia	PMEG10020ELRX
L1	Inductor, 33 µH, ±20%, 8 A (sat), 85.5 mΩ (max)	1	Eaton	HCMA1305-330-R
LED1, LED2, LED3, LED4	White LED	4		
Q1, Q3	MOSFET, N-Channel, 30 A, 100 V, LFPAK56	2	Nexperia	PSMN038-100YL
Q2	MOSFET, P-Channel, 100 V, 15 A, TO252-3	1	Infineon	SPD15P10PLGBTMA1
R1	Resistor, 0.2 Ω, 1 W, 1%, 2512	1		
R2	Resistor, 150 Ω, 1/16 W, 1%, 0402	1		
R5, R6, R7, R10	Resistor, 10 kΩ, 1/16 W, 1%, 0402	4		
R8	Resistor, 2.21 kΩ, 1/16 W, 1%, 0402	1		
R9	Resistor, 1.54 kΩ, 1/16 W, 1%, 0402	1		
R11	Resistor, 45.3 Ω, 1/10 W, 1%, 0603	1		
R12	Resistor, 86.6 kΩ, 1/16 W, 1%, 0402	1		
R13, R14	Resistor, 0.12 Ω, 1 W, 1%, 2512	2		
RT1	Thermistor, NTC, 10kohm, 0603	1	Vishay	NTCS0603E3103FHT

* C4, C5, C7, C8, C9 are optional components.

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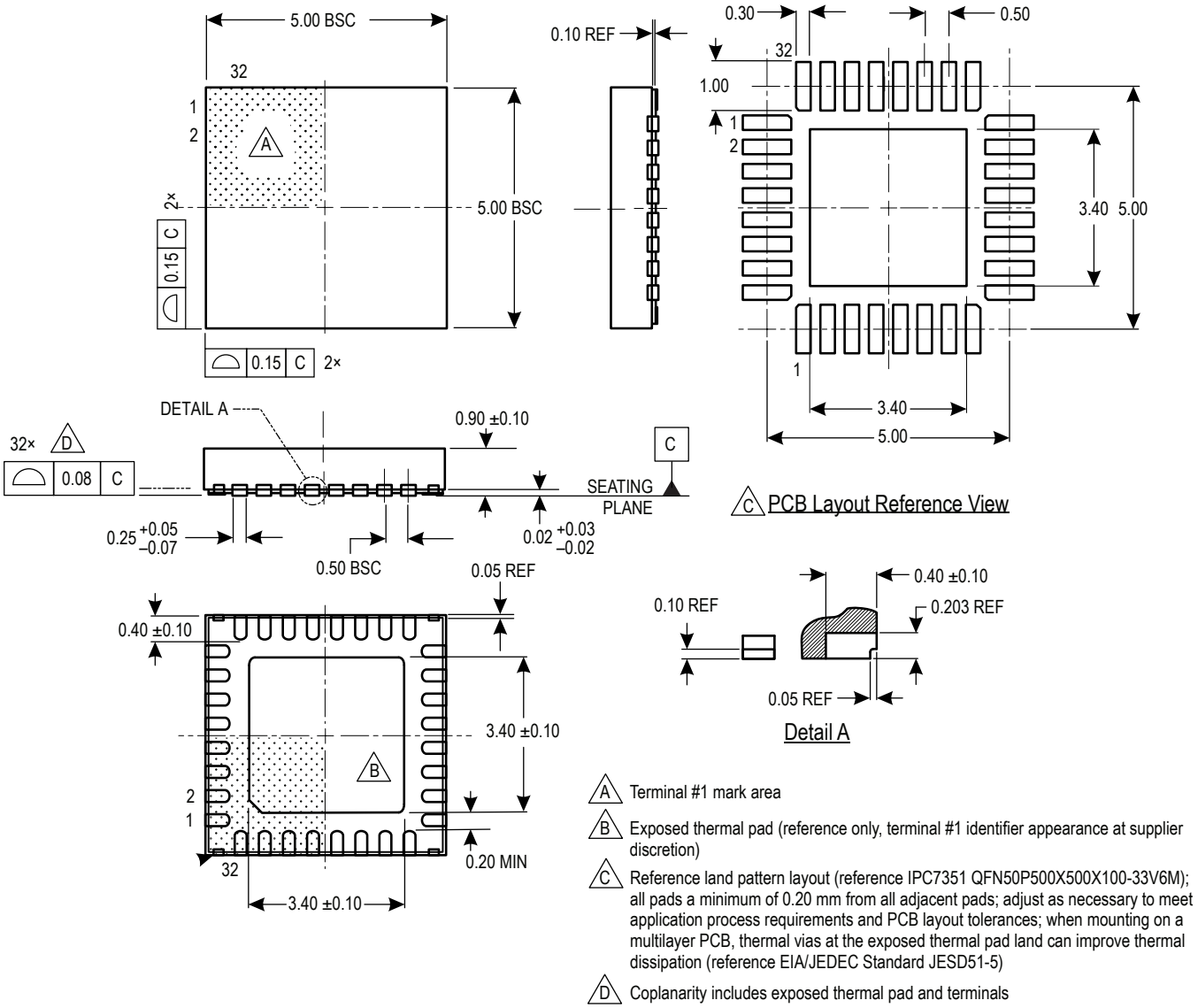
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 and JEDEC MO-220VHHD-5)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 37: 32-Pin 5 mm × 5 mm QFN with exposed thermal pad and wettable flank (suffix ET)

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