



HSMC SATA RAID board [AB12-HSMCRAID] Manual [Ver1.0E]

Introduction

Thank you for choosing HSMC SATA RAID board [Part Number: AB12-HSMCRAID] ("RAID board" in this manual.) The RAID board is compliant with HSMC standard of Altera and provides 8 SATA channels at maximum by high speed serial interface in HSMC so that user can build SATA RAID prototype system.

The RAID board can directly connect with 8 pcs of 2.5"-SATA drive. User can supply power to the connected SATA drive via 4-pin ATX Standard power connector.

On-board 150MHz low-jitter differential oscillator will supply high-quality reference SATA clock to the refclk input of FPGA via HSMC I/F (CLKIN2p/n).

Board Appearance

The RAID board size is 78mm width and 90mm length.

Following figure-1 and figure-2 shows component side and solder side appearance respectively.

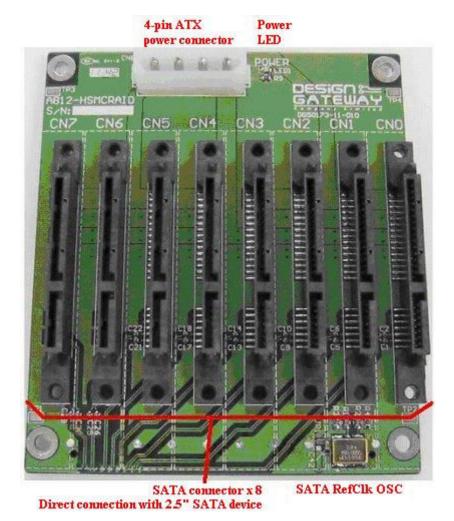
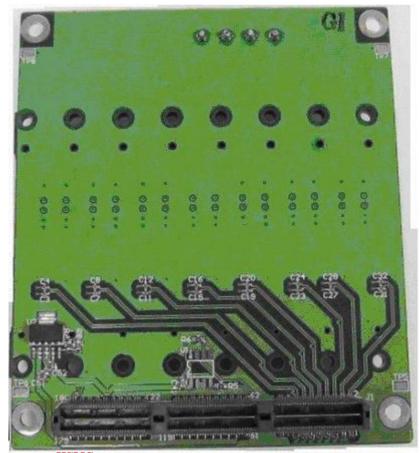


Figure-1: AB12-HSMCRAID component side







HSMC connector (Samtec QTH-090-01-L-D-A)

Figure-2: AB12-HSMCRAID solder side

Connection to the FPGA board

Connect the RAID board with HSMC connector on the FPGA board.

For 2.5"-SATA drive connection, user can directly connect SATA drive with CN0 – CN7 SATA connector on the RAID board.

Use 4-pin ATX Standard power connector for SATA drive power supply.

User must check that all SATA drives, RAID board and FPGA board are powered off when remove or connect.

To connect 3.5"-SATA drive, use SATA general extention cable. Following general extention cable is suitable for 3.5" usage.

Vendor: AREA (Setagaya Denki) Product Number: AR-S005S

URL: http://www.area-powers.jp/denki/cable/s005s.htm

Vendor: AINEX

Product Number: SAT-15EXPA

URL: http://www.ainex.jp/products/sat-15expa.htm

When user want to assign SATA channel of the RAID board as a SATA Device to connect with SATA Host-PC, use above extention cable along with the following crossover adapter provided from DesignGateway.

Vendor: DesignGateway

Product Number: AB02-CROSSOVER

URL: http://www.design-gateway.com/ABseries.html

Copyright©2011 Design Gateway Co,.Ltd. All rights reserved.





Pin Assignment

Pin assignment of HSMC on the RAID board is listed following table-1.

HSMC	Samtec	HSMC	Signal	RAID Bd connection
Pin# (*1)	Pin#	definition	Name	destination
1 111111 (1)	(*1)	deminion	ranic	destination
	(1)			
1	1	TX P7	HT7P	CN7-S2 (TX Pos)
2		RX P7	HR7P	CN7-S6 (RX Pos)
3		TX N7	HT7N	CN7-S3 (TX Neg)
4		RX N7	HR7N	CN7-S5 (RX Neg)
				(======================================
5	7	TX P6	HT6P	CN6-S2 (TX Pos)
6	8	RX P6	HR6P	CN6-S6 (RX Pos)
7	9	TX N6	HT6N	CN6-S3 (TX Neg)
8		RX N6	HR6N	CN6-S5 (RX Neg)
		_		· · ·
9	13	TX_P5	HT5P	CN5-S2 (TX Pos)
10	14	RX_P5	HR5P	CN5-S6 (RX Pos)
11	15	TX_N5	HT5N	CN5-S3 (TX Neg)
12	16	RX N5	HR5N	CN5-S5 (RX Neg)
13	19	TX P4	HT4P	CN4-S2 (TX Pos)
14	20	RX_P4	HR4P	CN4-S6 (RX Pos)
15	21	TX N4	HT4N	CN4-S3 (TX Neg)
16	22	RX N4	HR4N	CN4-S5 (RX Neg)
		_		, o,
17	25	TX P3	HT3P	CN3-S2 (TX Pos)
18	26	RX P3	HR3P	CN3-S6 (RX Pos)
19	27	TX N3	HT3N	CN3-S3 (TX Neg)
20	28	RX N3	HR3N	CN3-S5 (RX Neg)
21	31	TX_P2	HT2P	CN2-S2 (TX Pos)
22	32	RX_P2	HR2P	CN2-S6 (RX Pos)
23	33	TX_N2	HT2N	CN2-S3 (TX Neg)
24	34	RX_N2	HR2N	CN2-S5 (RX Neg)
25		TX_P1	HT1P	CN1-S2 (TX Pos)
26	38	RX_P1	HR1P	CN1-S6 (RX Pos)
27	39	TX_N1	HT1N	CN1-S3 (TX Neg)
28	40	RX_N1	HR1N	CN1-S5 (RX Neg)
29		TX_P0	HT0P	CN0-S2 (TX Pos)
30	44	RX_P0	HR0P	CN0-S6 (RX Pos)
31	45	TX_N0	HT0N	CN0-S3 (TX Neg)
32	46	RX_N0	HR0N	CN0-S5 (RX Neg)
156	176	CLKIN2P	SCKN	(via R1) X1-5 (*2)
158	178	CLKIN2N	SCKP	(via R2) X1-4 (*2)

Table1: HSMC pin assignment of AB12-HSMCRAID board

Note

- (*1) HSMC Pin# is pin number defined in HSMC standard, while Samtec Pin# is pin number of connector specification.
- (*2) 150MHz SATA reference clock of CLKIN2P/N is reversed in its polarity due to the board trace, however, this polarity invertion is no problem because differential clock waveform is symmetrical.





Disclaimer

DesignGateway is exempted from any damage to the connected SATA device or FPGA board. DesignGateway does not guarantee transfer speed performance.

[Inquiry]

URL: http://www.design-gateway.com/ Email: mailto:sales@design-gateway.com

Revision History

Revision	Date	Description	
1.0E	13-Jul-2012	Release English manual	