ACFL-5211U

Bi-directional Wide Operating Temperature 1MBd Digital Optocoupler with R^{2}Coupler^{TM} Isolation in a Stretched 12-Pin Surface Mount Plastic Package

Data Sheet

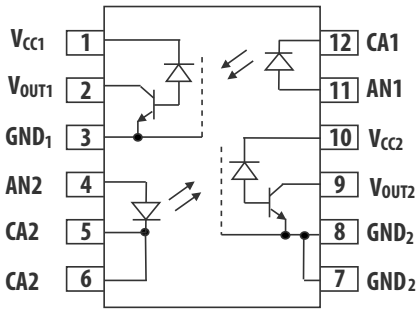
Description

The ACFL-5211U is a dual channel, bi-directional, high speed 1MBd digital optocoupler. The stretched SO-12 stretched package outline is designed to be compatible with standard surface mount processes and occupies the same land area as the stretched SO8 package.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output. Each channel is also galvanically isolated from the other with no cross-talk.

Avago R^{2}Coupler provides with reinforced insulation and reliability that delivers safe signal isolation critical in high temperature industrial applications.

Functional Diagram



Note: The connection of a 1 µF bypass capacitor between pins 1 and 3 and pins 8 and 10 is recommended.

Truth Table

LED	VO
ON	LOW
OFF	HIGH

Features

- Wide Temperature Range: -40°C to +125°C
- Ultra low LED drive current for status feedback at I_F = 0.8mA or 1.5mA
- High speed (1MBd) operation at I_F = 10mA with low propagation delay: 1µs (max.)
- Low standby leakage:
  - I_{CCH}: 2.5µA (max.)
  - I_{OH}: 5µA (max.)
- 30 kV/µs High Common-Mode Rejection at V_{CM} = 1500 V (typ)
- Compact, Auto-Insertable Stretched SO12 Packages
- Worldwide Safety Approval:
  - UL 1577 recognized, 5kV_{RMS}/1 min.
  - CSA Component Acceptance Notice#5A
  - IEC/EN/DIN EN 60747-5-5

Applications

- Low Speed Digital Signal Isolation Interface
- Inverter Fault Feedback Signal Isolation
- Switching Power Supplies Feedback Circuit

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.

Pin Description

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	VCC1	Primary Side Power Supply	7	GND2	Secondary Side Ground
2	VOUT1	Output 1	8	GND2	Secondary Side Ground
3	GND1	Primary Side Ground	9	VOUT2	Output 2
4	AN2	Anode 2	10	VCC2	Secondary Side Power Supply
5	CA2	Cathode 2	11	AN1	Anode 1
6	CA2	Cathode 2	12	CA1	Cathode 1

Ordering Information

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACFL-5211U	-000E	Stretched SO-12	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

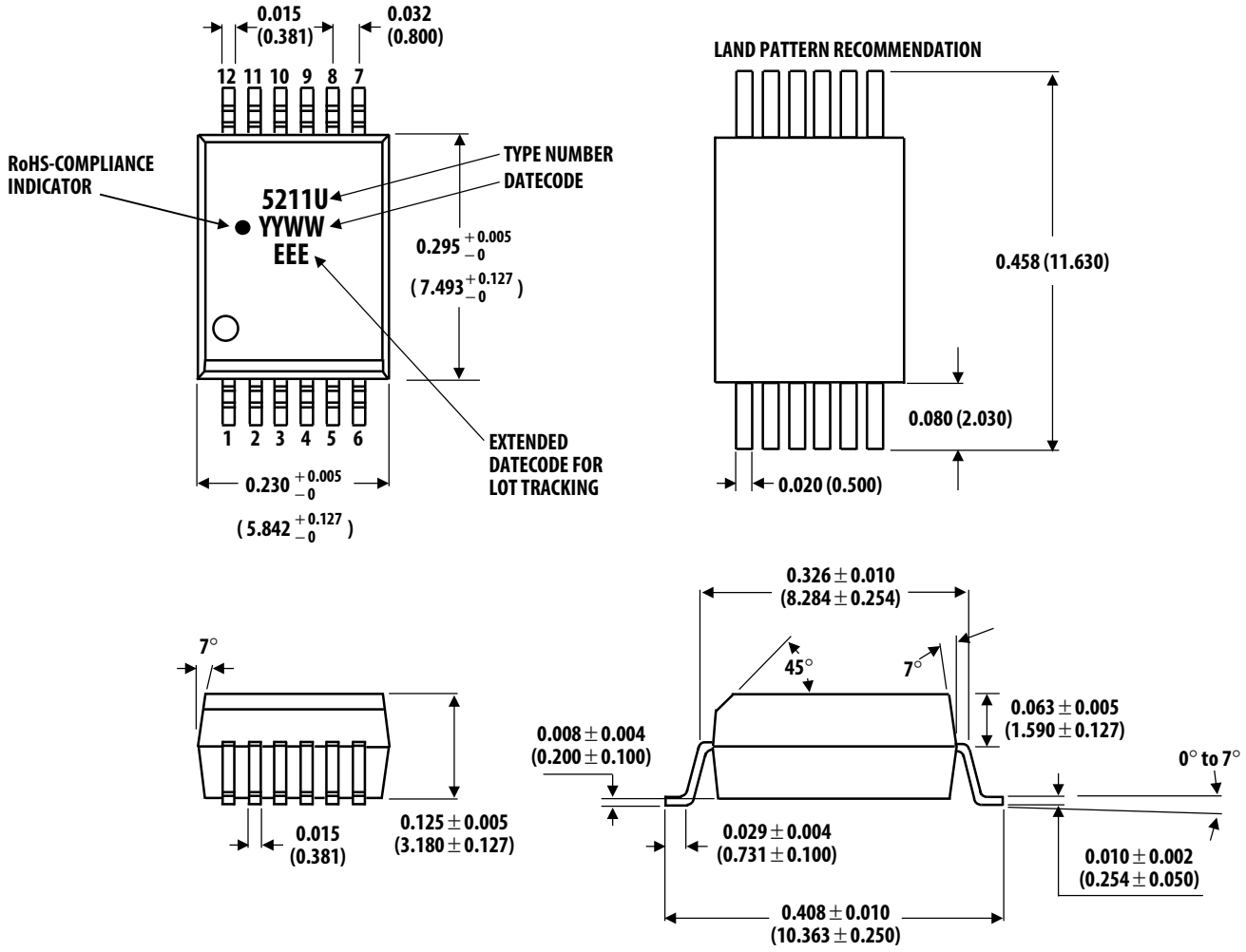
Example 1:

ACFL-5211U-560E to order product of SSO-12 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawing

12-Lead Surface Mount



Dimensions in inches (millimeters)

Lead coplanarity = 0.004 inches (0.1mm)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used

Regulatory Information

The ACFL-5211U is approved by the following organizations:

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 5kV_{RMS}
CSA	Approved under CSA Component Acceptance Notice #5A
IEC/EN/DIN EN 60747-5-5	Approved under IEC/EN/DIN EN 60747-5-5

Insulation and Safety Related Specifications

Parameter	Symbol	ACFL-5211U	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

IEC / EN / DIN EN 60747-5-5 Insulation Related Characteristic (Option 060E and 560E)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms for rated mains voltage < 1000 V rms		 I-III I-III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2137	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} x 1.6 = V_{PR}, Type and sample test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	10^9	W

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Condition
Storage Temperature		T_S	-55	150	°C	
Operating Temperature		T_A	-40	125	°C	
Junction Temperature		T_J		150	°C	
Lead Soldering Cycle	Temperature			260	°C	
	Time			10	s	
Average Forward Input Current		$I_{F(avg)}$		20	mA	
Peak Forward Input Current (50% duty cycle, 1ms pulse width)		$I_{F(peak)}$		40	mA	
Peak Transient Input Current (≤1μs pulse width, 300ps)		$I_{F(trans)}$		100	mA	
Reversed Input Voltage		V_R		5	V	
Input Power Dissipation		P_{IN}		30	mW	
Output Power Dissipation		P_O		100	mW	
Average Output Current		I_O		8	mA	
Peak Output Current		$I_{O(pk)}$		16	mA	
Supply Voltage		V_{CC1}/V_{CC2}	-0.5	30	V	
Output Voltage		V_{OUT1}/V_{OUT2}	-0.5	20	V	
Solder Reflow Temperature Profile			See Reflow Temperature Profile			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltages	V_{CC1}/V_{CC2}		20.0	V	
Operating Temperature	T_A	-40	125	°C	

Electrical Specifications (DC) for 5-Pin Configuration

Over recommended operating conditions, unless otherwise specified. All typical specifications are at T_A=25°C, V_{CC}= 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	32	65	100	%	T_A=25°C, V_{CC}=4.5V, V_O=0.5V, I_F=10mA	1, 2, 4	1
		24	65			V_{CC}=4.5V, V_O=0.5V, I_F=10mA		
		33	160			V_{CC}=4.5V, V_O=0.5V, I_F=1.5mA		
		25	165			V_{CC}=4.5V, V_O=0.5V, I_F=0.8mA		
Logic Low Output Voltage	V_{OL}		0.1	0.5	V	T_A=25ºC, V_{CC}=4.5V, I_F=10mA, I_O=2.4mA,		
			0.1			V_{CC}=4.5V, I_F=1.5mA, I_O=0.5mA,		
			0.1			V_{CC}=4.5V, I_F=0.8mA, I_O=0.2mA,		
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A=25ºC, V_O=V_{CC}=5.5V,I_F=0mA	13, 14	
			0.01	5		V_O=V_{CC}=20V,I_F=0mA		
Logic Low Supply Current	I_{CCL}		85	200	µA	I_F=10mA, V_O=open, V_{CC}=20V		
			15		µA	I_F=1.5mA, V_O=open, V_{CC}=20V		
Logic High Supply Current	I_{CCH}		0.02	1	µA	T_A=25°C, I_F=0mA, V_O=open, V_{CC}=20V		
				2.5	µA	I_F=0mA, V_O=open, V_{CC}=20V		
Input Forward Voltage	V_F	1.45	1.55	1.75	V	T_A=25ºC, I_F=10mA	3	
		1.25	1.5	1.85	V	I_F=10mA		
Input Reversed Breakdown Voltage	BV_R	5			V	I_R=10µA		
Temperature Coefficient of Forward Voltage	$\Delta V/\Delta T_A$		-1.5		mV/°C	I_F=10mA		
			-1.8			I_F=1.5mA		
Input Capacitance	C_{IN}		90		pF	F=1MHz, V_F=0		

Switching Specifications (AC)

Over recommended operating conditions, unless otherwise specified. All typical specifications are at T_A=25°C, V_{CC}= 5V.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	0.03	0.15	1.0	µs	I_F = 10mA, R_L = 1.9kΩ	Pulse: f=10kHz, Duty cycle = 50%, V_{CC} = 5.0 V, C_L = 15pF, V_{THHL}=1.5V	5 to 12	2
			0.7	5.0		I_F = 1.5mA, R_L = 10kΩ			
			1	10		I_F = 0.8mA, R_L = 27kΩ			
Propagation Delay Time to Logic High at Output	t_{PLH}	0.03	0.5	1.0	µs	I_F = 10mA, R_L = 1.9kΩ	Pulse: f=10kHz, Duty cycle = 50%, V_{CC} = 5.0 V, C_L = 15pF, V_{THLH}=2.0V	5 to 12	2
			0.9	5.0		I_F = 1.5mA, R_L = 10kΩ			
			2	10		I_F = 0.8mA, R_L = 27kΩ			
Pulse Width Distortion	PWD		0.35	0.85	µs	Pulse: f=10kHz, Duty cycle = 50%, I_F = 10mA, R_L = 1.9kΩ,V_{CC} = 5.0 V, C_L = 15pF, V_{THHL}=1.5V, V_{THLH}=2.0V		5 to 12	2,3
Propagation Delay Difference between Any 2 Parts	PDD		0.35	0.9	µs				2,4
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	15	30		kV/ µs	I_F = 0mA	V_{CM} =1500Vp-p, T_A= 25°C V_{CC} = 5.0 V, R_L=1.9kΩ		5
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	15	30		kV/ µs	I_F = 10mA			

Package Characteristics

All Typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			V_{RMS}	RH ≤ 50%, t = 1 min; T_A = 25°C		6, 7
Input-Output Resistance	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 Vdc		6
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz; V_{I-O} = 0 V_{DC}		6

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

Notes:
1. Current Transfer Ratio in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Use of 1µF bypass capacitors connected between pins 1 and 3 and pins 8 and 10.
3. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
4. The difference between t_{PHL} and t_{PLH} between any 2 parts under the same test conditions.
5. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., Vo > 2.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
6. Device considered a two terminal device: pins 1to 6 shorted together, and pins 7 to 12 shorted together.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000V_{RMS} for 1 second.

Typical Performance Plots

Figure 1 DC and Pulsed Transfer Characteristics

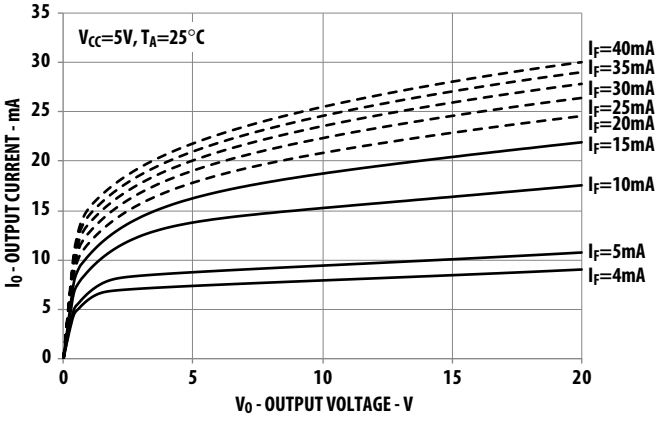


Figure 2 Current Transfer Ratio vs Input Current

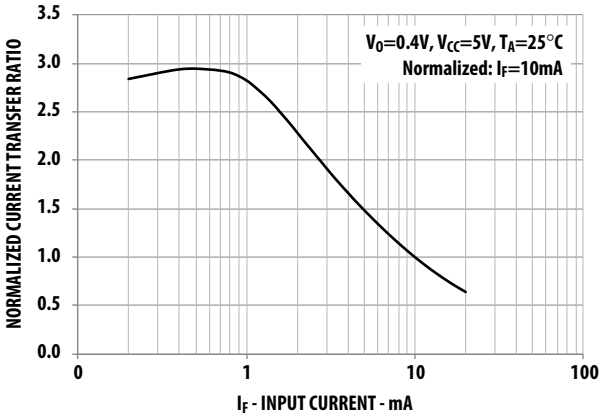


Figure 3 Input Current vs Input Voltage

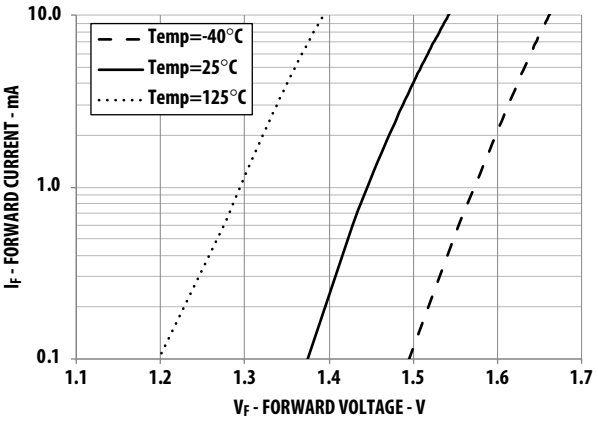


Figure 4 Current Transfer Ratio vs Temperature

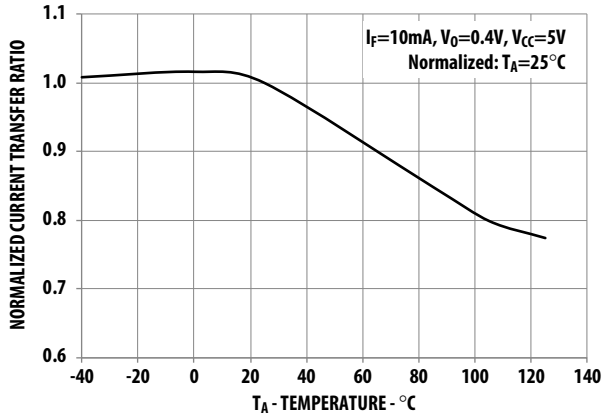


Figure 5 Propagation Delay Time vs Temperature

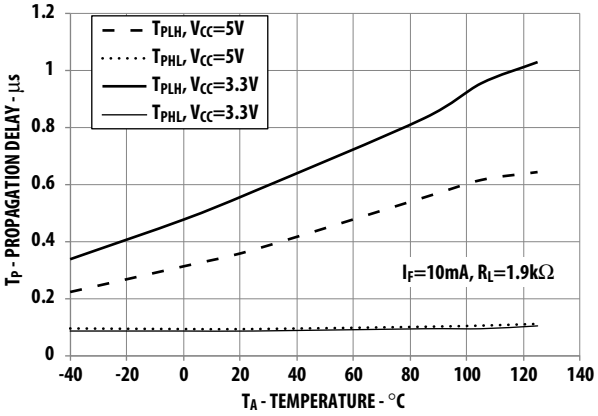


Figure 6 Propagation Delay Time vs Temperature

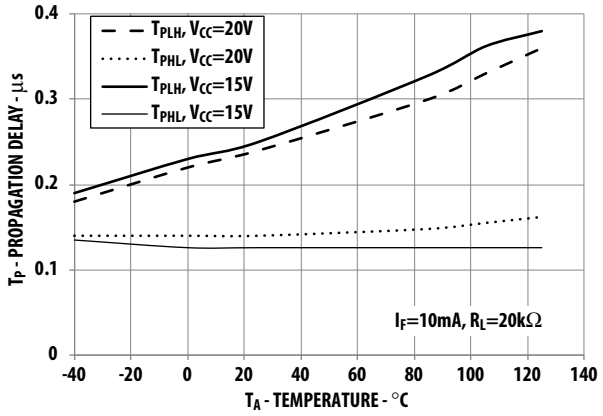


Figure 7 Propagation Delay Time vs Load Resistance

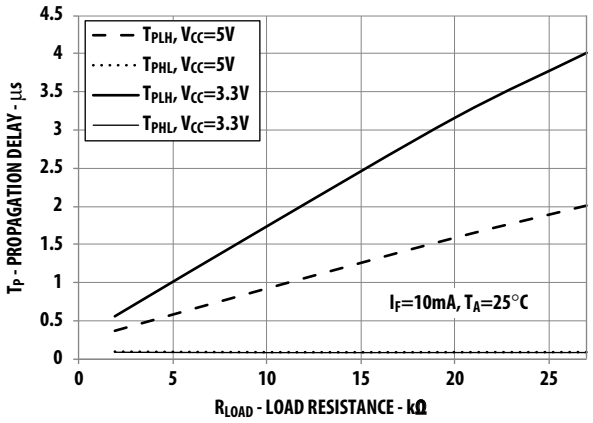


Figure 8 Propagation Delay Time vs Load Resistance

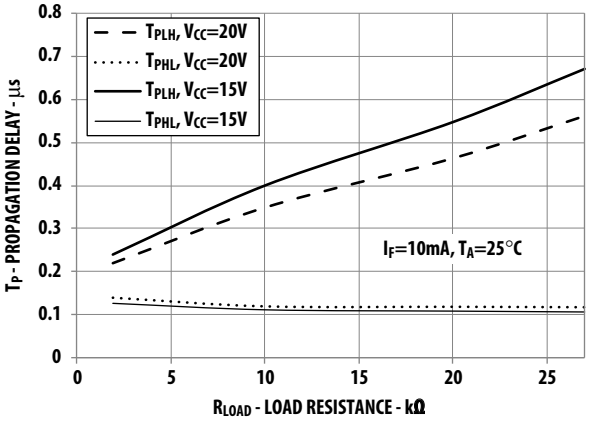


Figure 9 Propagation Delay Time vs Input Current

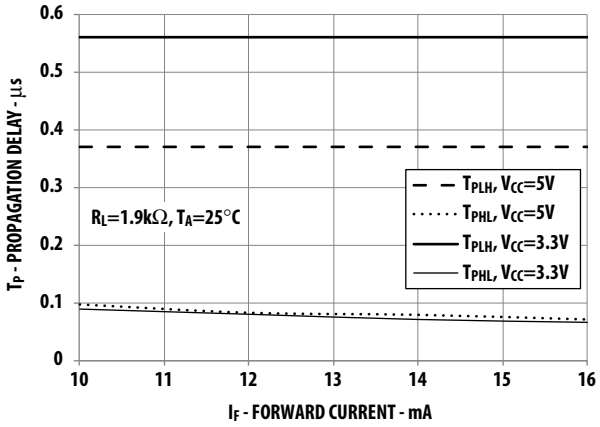


Figure 10 Propagation Delay Time vs Input Current

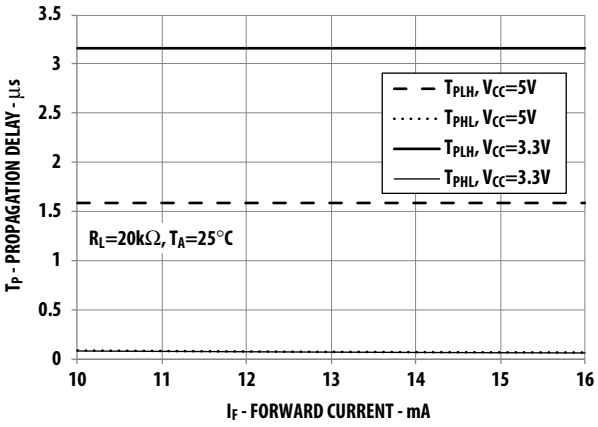


Figure 11 Propagation Delay Time vs Input Current

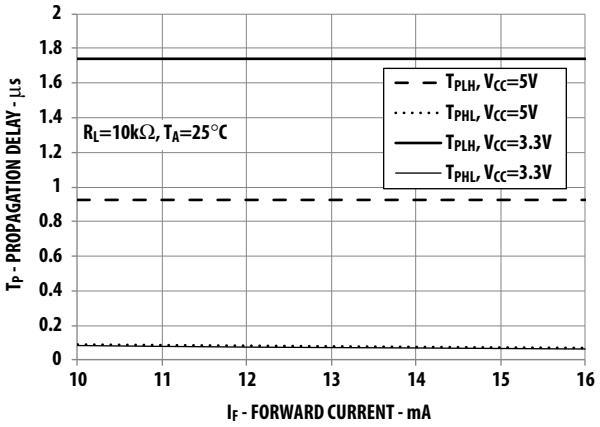


Figure 12 Propagation Delay Time vs Input Current

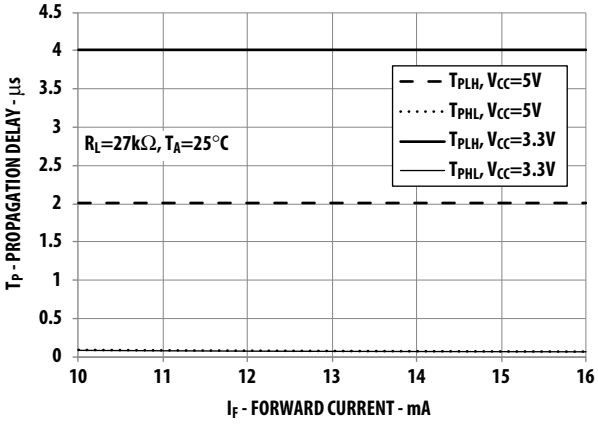


Figure 13 Logic High Output Current vs Supply Voltage

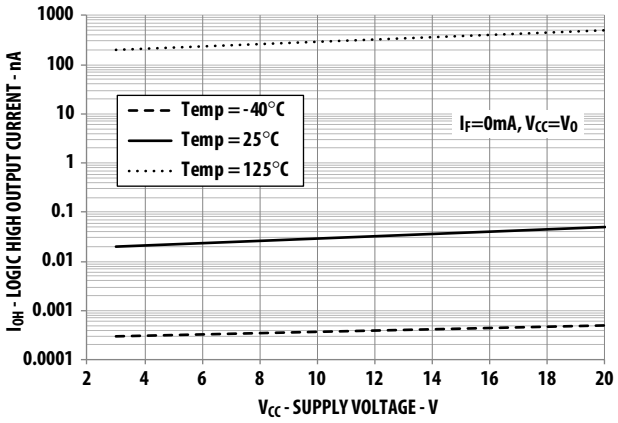
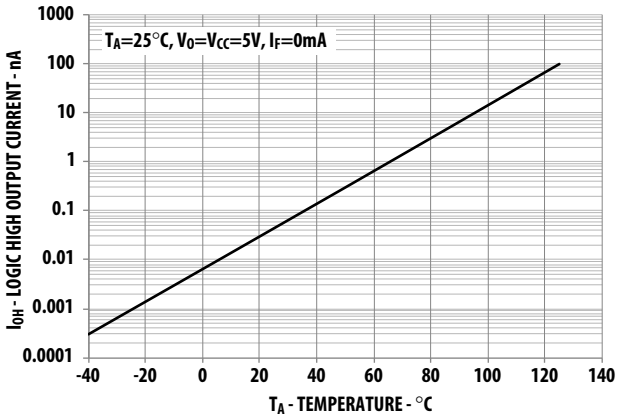


Figure 14 Logic High Output Current vs Temperature



Test Circuits

Figure 15 Switching Test Circuit

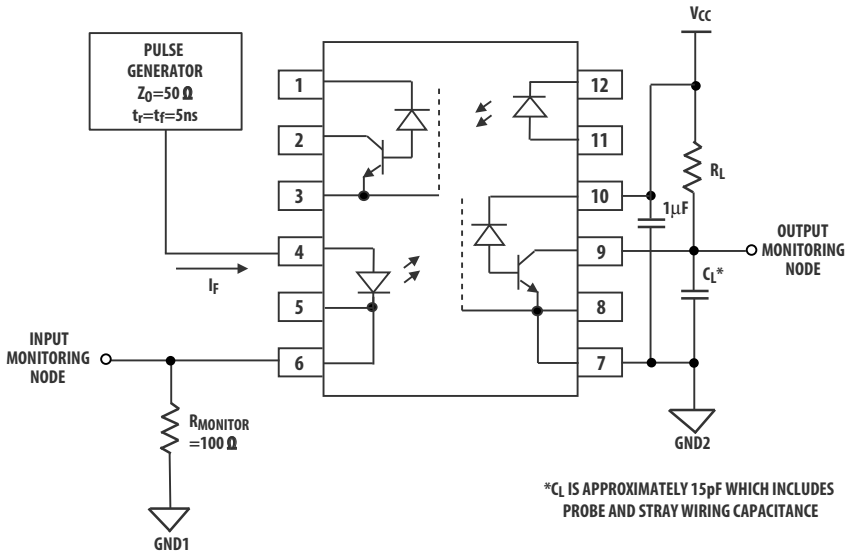
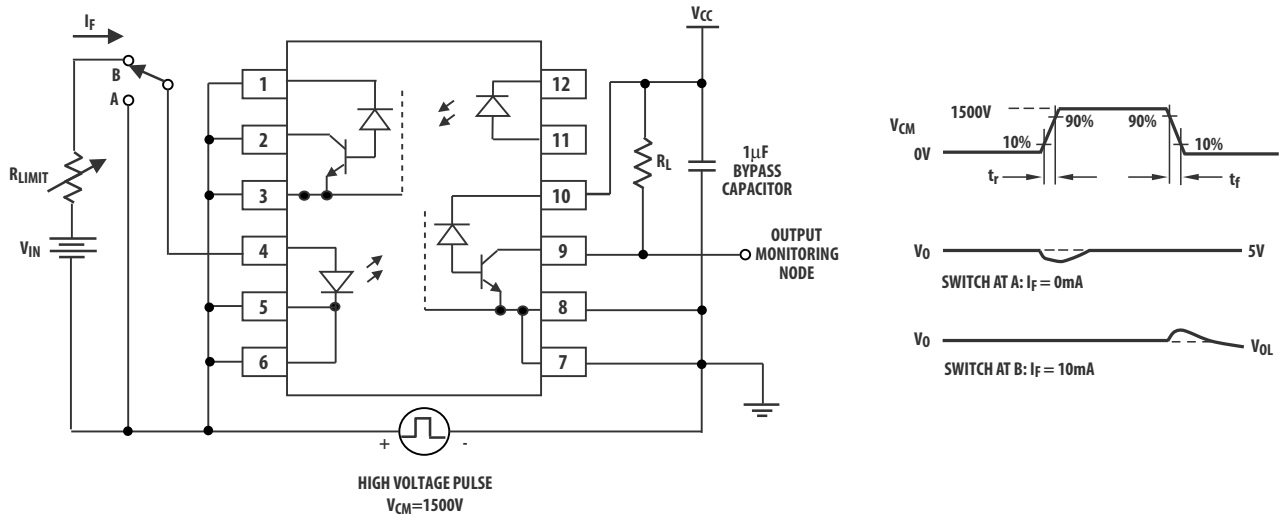


Figure 16 Test Circuit for Transient Immunity and Typical Waveforms

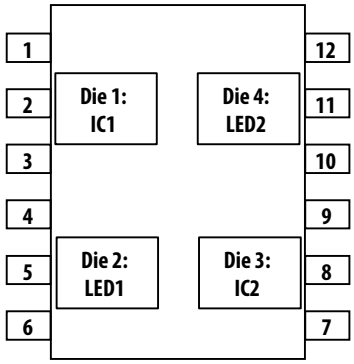


Thermal Resistance Measurement

The diagram of ACFL-5211U for measurement is shown in Figure 17. This is a multi-chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd die is heated and all the dice temperatures are recorded and so on until the 4th die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of two heat sources

$$\begin{vmatrix} R11 & R12 & R13 & R14 \\ R21 & R22 & R23 & R24 \\ R31 & R32 & R33 & R34 \\ R41 & R42 & R43 & R44 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \\ P3 \\ P4 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \\ \Delta T3 \\ \Delta T4 \end{vmatrix}$$

Figure 17 Diagram of ACFL-5211U for measurement



R_{11}: Thermal Resistance of Die1 due to heating of Die1 (˚C/W)

R_{12}: Thermal Resistance of Die1 due to heating of Die2 (˚C/W)

R_{13}: Thermal Resistance of Die1 due to heating of Die3 (˚C/W)

R_{14}: Thermal Resistance of Die1 due to heating of Die4 (˚C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (˚C/W)

R_{22}: Thermal Resistance of Die2 due to heating of Die2 (˚C/W)

R_{23}: Thermal Resistance of Die2 due to heating of Die3 (˚C/W)

R_{24}: Thermal Resistance of Die2 due to heating of Die4 (˚C/W)

R_{31}: Thermal Resistance of Die3 due to heating of Die1 (˚C/W)

R_{32}: Thermal Resistance of Die3 due to heating of Die2 (˚C/W)

R_{33}: Thermal Resistance of Die3 due to heating of Die3 (˚C/W)

R_{34}: Thermal Resistance of Die3 due to heating of Die4 (˚C/W)

R_{41}: Thermal Resistance of Die4 due to heating of Die1 (˚C/W)

R_{42}: Thermal Resistance of Die4 due to heating of Die2 (˚C/W)

R_{43}: Thermal Resistance of Die4 due to heating of Die3 (˚C/W)

R_{44}: Thermal Resistance of Die4 due to heating of Die4 (˚C/W)

P_1: Power dissipation of Die1 (W)

P_2: Power dissipation of Die2 (W)

P_3: Power dissipation of Die3 (W)

P_4: Power dissipation of Die4 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)

T_2: Junction temperature of Die2 due to heat from all dice (°C)

T_3: Junction temperature of Die3 due to heat from all dice (°C)

T_4: Junction temperature of Die4 due to heat from all dice (°C)

Ta: Ambient temperature.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + Ta \text{ -- (1)}$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + Ta \text{ -- (2)}$$

$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + Ta \text{ -- (3)}$$

$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + Ta \text{ -- (4)}$$

ΔT_1: Temperature difference between Die1 junction and ambient (°C)

ΔT_2: Temperature deference between Die2 junction and ambient (°C)

ΔT_3: Temperature difference between Die3 junction and ambient (°C)

ΔT_4: Temperature deference between Die4 junction and ambient (°C)