ACFL-5212T

Automotive R²Coupler™ Wide Operating Temperature 20kBd Digital Optocoupler Configurable as Low Power, Low Leakage Phototransistor

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The ACFL-5212T is an automotive grade dual channel, bi-directional, high CMR, 20kBd digital optocoupler, configurable as a low power, low leakage phototransistor, specifically for use in automotive applications. The stretched SO-12 package outline is designed to be compatible with standard surface mount processes and occupies the same land area as the single channel equivalent, ACPL-K49T, in stretched SO8 package.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

Each channel is also galvanically isolated from each other with no cross-talk.

Avago R2Coupler provides reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

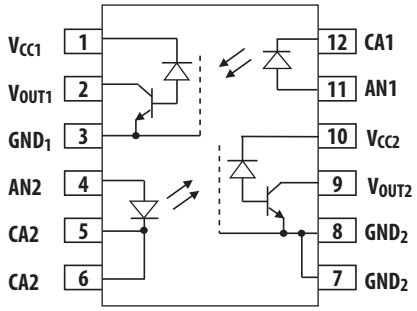
Features

- Qualified to AEC Q100 Grade 1 Guidelines
- Wide Temperature Range: -40°C to +125°C
- Low LED Drive Current: 4mA (typ)
- Low Power, Low Leakage Phototransistor in a "4-pin Configuration" ($I_{(CEO)}$ < 5µA)
- 30 kV/µs High Common-Mode Rejection at V_{CM} = 1500 V (typ)
- Low Propagation Delay: 20µs (max)
- Compact, Auto-Insertable Stretched SO12 Packages
- Worldwide Safety Approval:
  - UL 1577 recognized, 5kV_{RMS}/1 min.
  - CSA Component Acceptance Notice#5A
  - IEC/EN/DIN EN 60747-5-5

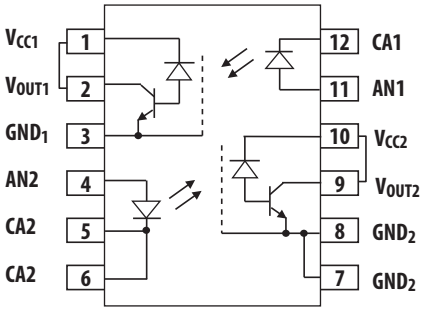
Applications

- Automotive Low Speed Digital Signal Isolation Interface
- Inverter Fault Feedback Signal Isolation
- Switching Power Supplies Feedback Circuit

Functional Diagram



Note: The connection of a 1 µF bypass capacitor between pins 1 and 3 and pins 8 and 10 is recommended.



Note: Pins 1 and 2 and pins 9 and 10 are externally shorted for 4-pin configuration. Do not connect bypass capacitors in this configuration.

Truth Table

LED	VO
ON	LOW
OFF	HIGH

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.*

Pin Description

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	V_{CC1}	Primary Side Power Supply	7	GND2	Secondary Side Ground
2	V_{OUT1}	Output 1	8	GND2	Secondary Side Ground
3	GND1	Primary Side Ground	9	V_{OUT2}	Output 2
4	AN2	Anode 2	10	V_{CC2}	Secondary Side Power Supply
5	CA2	Cathode 2	11	AN1	Anode 1
6	CA2	Cathode 2	12	CA1	Cathode 1

Ordering Information

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACFL-5212T	-000E	Stretched SO-12	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

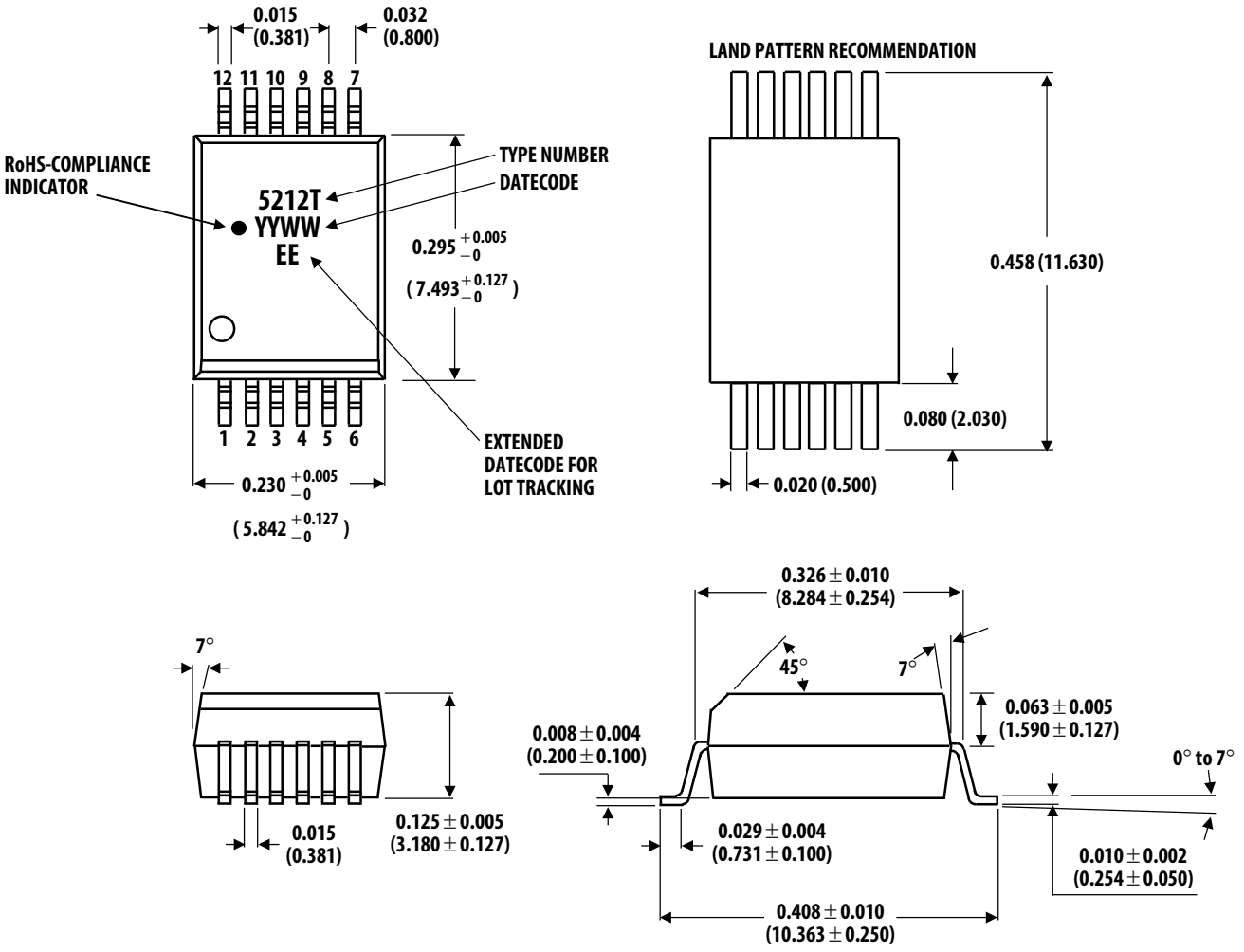
Example 1:

ACFL-5212T-560E to order product of SSO-12 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawing

12-Lead Surface Mount



Dimensions in inches (millimeters)
Lead coplanarity = 0.004 inches (0.1mm)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used

Regulatory Information

The ACFL-5212T is approved by the following organizations:

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 5kV_{RMS}
CSA	Approved under CSA Component Acceptance Notice #5A
IEC/EN/DIN EN 60747-5-5	Approved under IEC/EN/DIN EN 60747-5-5

Insulation and Safety Related Specifications

Parameter	Symbol	ACFL-5212T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

IEC / EN / DIN EN 60747-5-5 Insulation Related Characteristic (Option 060E and 560E)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 600 V rms		I-III	
for rated mains voltage < 1000 V rms		I-III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2137	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} x 1.6 = V_{PR}, Type and sample test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	10^9	Ω

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Condition
Storage Temperature		T_S	-55	150	℃	
Operating Temperature		T_A	-40	125	℃	
Junction Temperature		T_J		150	℃	
Lead Soldering Cycle	Temperature			260	℃	
	Time			10	s	
Average Forward Input Current		$I_{F(avg)}$		20	mA	
Peak Forward Input Current (50% duty cycle, 1ms pulse width)		$I_{F(peak)}$		40	mA	
Peak Transient Input Current (≤1μs pulse width, 300ps)		$I_{F(trans)}$		100	mA	
Reversed Input Voltage		V_R		5	V	
Input Power Dissipation		P_{IN}		30	mW	
Output Power Dissipation		P_O		100	mW	
Average Output Current		I_O		8	mA	
Peak Output Current		$I_{O(pk)}$		16	mA	
Supply Voltage		V_{CC1}/V_{CC2}	-0.5	30	V	
Output Voltage		V_{OUT1}/V_{OUT2}	-0.5	20	V	
Solder Reflow Temperature Profile			See Reflow Temperature Profile			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltages	V_{CC1}/V_{CC2}		20.0	V	
Operating Temperature	T_A	-40	125	℃	

Electrical Specifications (DC) for 5-Pin Configuration

Over recommended operating conditions, unless otherwise specified. All typical specifications are at T_A=25°C, V_{CC}= 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	32	65	100	%	T_A=25°C, V_{CC}=4.5V, V_O=0.5V, I_F=10mA	1,2,3	1
		24	65			V_{CC}=4.5V, V_O=0.5V, I_F=10mA		
		65	110	150		T_A=25°C, V_{CC}=4.5V, V_O=0.5V, I_F=4mA	1,2, 3	1
		50	110			V_{CC}=4.5V, V_O=0.5V, I_F=4mA		
Logic Low Output Voltage	V_{OL}		0.1	0.5	V	T_A=25°C, I_F=10mA, V_{CC}=4.5V, I_O=2.4mA,	3	
			0.1	0.5		I_F=4mA, V_{CC}=4.5V, I_O=2.0mA,		
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A=25°C, V_O=V_{CC}=5.5V, I_F=0mA	7	
			0.01	5		V_O=V_{CC}=20V, I_F=0mA		
Logic Low Supply Current	I_{CCL}		35	100	µA	I_F=4mA, V_O=open, V_{CC}=20V		
Logic High Supply Current	I_{CCH}		0.02	1	µA	T_A=25°C, I_F=0mA, V_O=open, V_{CC}=20V		
				2.5	µA	I_F=0mA, V_O=open, V_{CC}=20V		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F=4mA	6	
Input Reversed Breakdown Voltage	BV_R	5			V	I_R=10µA		
Temperature Coefficient of Forward Voltage	$\Delta V/\Delta T_A$		-1.5		mV/°C	I_F=10mA		
Input Capacitance	C_{IN}		90		pF	F=1MHz, V_F=0		

Switching Specifications (AC) for 5-Pin Configuration

Over recommended operating conditions, unless otherwise specified. All typical specifications are at T_A=25°C, V_{CC}= 5V.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}			20	µs	Pulse: f=10kHz, Duty cycle = 50%, I_F = 4mA, V_{CC} = 5.0 V, R_L = 8.2kΩ, C_L = 15pF V_{THHL}=1.5V			2
Propagation Delay Time to Logic High at Output	t_{PLH}			20	µs	Pulse: f=10kHz, Duty cycle = 50%, I_F = 4mA, V_{CC}=5.0 V, R_L=8.2kΩ, C_L=15pF, V_{THLH}=2.0V			2
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	15	30		kV/ µs	I_F=0mA	V_{CM}=1500Vp-p, T_A=25°C, RL=1.9kΩ		3
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	15	30		kV/ µs	I_F=10mA			
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		15		kV/ µs	I_F=4mA	V_{CM}=1500Vp-p, T_A=25°C, RL=8.2kΩ		

Electrical Specifications (DC) for 4-Pin Configuration

Over recommended operating conditions, unless otherwise specified. All typical specifications are at T_A=25°C, V_{CC}= 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR		120		%	T_A=25°C, V_{CC}=V_O=5V, I_F=5mA	4	5, 8
		70	130	250		T_A=25°C, V_{CC}=V_O=5V, I_F=4mA		
Current Transfer Ratio	$CTR_{(Sat)}$	24	60			I_F=10mA, V_{CC}=V_O=0.5V	5	5, 8
		35	110			I_F=4mA, V_{CC}=V_O=0.5V		
Logic Low Output Voltage	V_{OL}		0.1	0.5	V	I_F=10mA, V_{CC}=4.5V, I_O=2.4mA,	5	8
			0.1	0.4		I_F=4mA, V_{CC}=4.5V, I_O=2.4mA,		
Off-State Current	$I_{(CEO)}$		4x10-4	5	µA	V_O=V_{CC}=20V, I_F=0mA	8	8
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F=4mA	6	
Input Reversed Breakdown Voltage	BV_R	5			V	I_R=10µA		
Temperature Coefficient of Forward Voltage	$\Delta V/\Delta T_A$		-1.5		mV/oC	I_F=10mA		
Input Capacitance	C_{IN}		90		pF	F=1MHz, V_F=0		
Output Capacitance	C_{CE}		35		pF	F=1MHz, V_F=0, V_O=V_{CC} =0V		

Switching Specifications (AC) for 4-Pin Configuration

Over recommended operating conditions, unless otherwise specified. All typical specifications are at T_A=25°C, V_{CC}= 5V.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		2	100	µs	Pulse: f=1kHz, Duty cycle = 50%, I_F = 4mA, V_{CC} = 5.0 V, R_L = 8.2kΩ, C_L = 15pF, V_{THHL}=1.5V			8
Propagation Delay Time to Logic High at Output	t_{PLH}		19	100	µs	Pulse: f=1kHz, Duty cycle = 50%, I_F = 4mA, V_{CC} = 5.0 V, R_L = 8.2kΩ, C_L = 15pF, V_{THLH}=2.0V			8
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	15	30		kV/ µs	I_F=0mA	V_{CM}=1500Vp-p, T_A=25°C R_L=8.2kΩ		8, 9
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	15	30		kV/ µs	I_F=4mA	V_{CM}=1500Vp-p, T_A=25°C R_L=8.2kΩ		

Package Characteristics

All Typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			V_{RMS}	RH ≤ 50%, t = 1 min; T_A = 25°C		6, 7
Input-Output Resistance	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 Vdc		6
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz; V_{I-O} = 0 V_{DC}		6

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

Notes:

1. Current Transfer Ratio in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, IF, times 100.
2. Use of 1µF bypass capacitors connected between pins 1 and 3 and pins 8 and 10 for 5-pin configuration.
3. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the ouput will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
4. Device considered a two terminal device: pins 1 to 6 shorted together, and pins 7 to 12 shorted together.
5. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000V_{RMS} for 1 second.

Typical Performance Plots

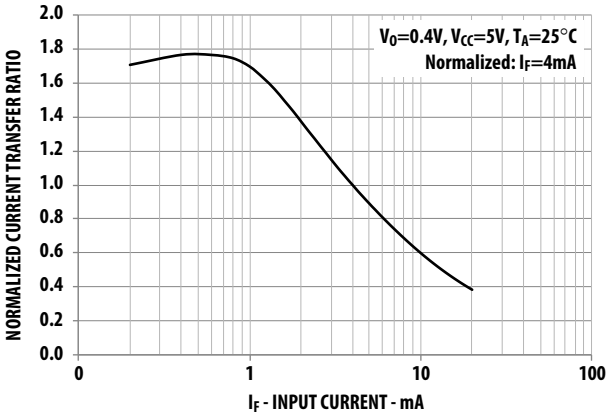


Figure 1. Current Transfer Ratio vs. Input Current

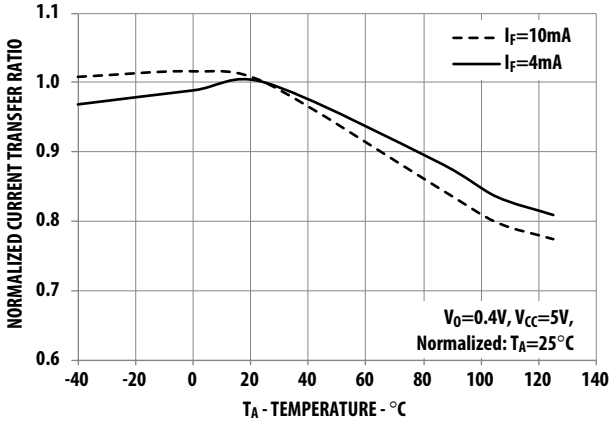


Figure 2. Normalized Current Transfer Ratio vs. Temperature

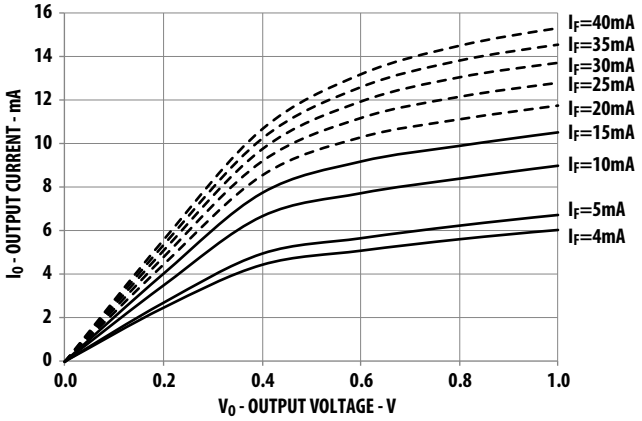


Figure 3. Typical Low Level Output Current vs Output Voltage

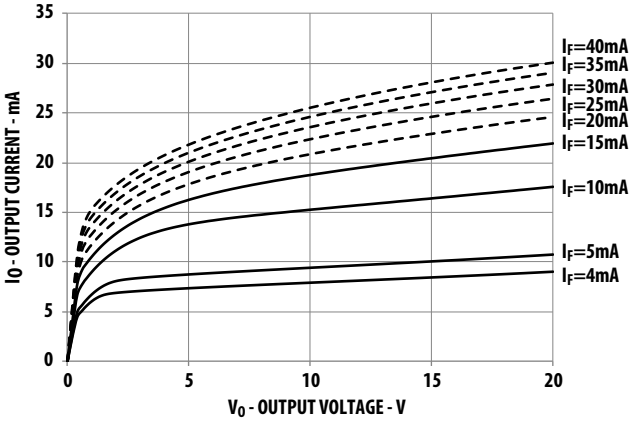


Figure 4. Output Current vs Output Voltage (4-Pin Configuration)

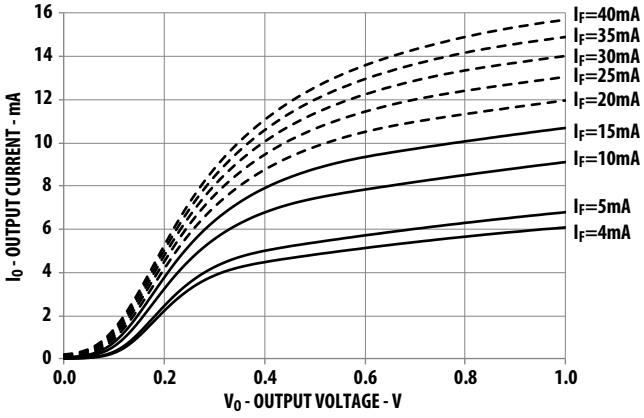


Figure 5. Typical Low Level Output Current vs Output Voltage (4-Pin Configuration)

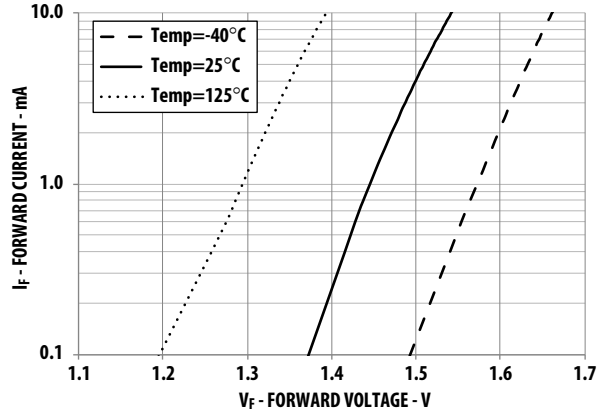


Figure 6. Typical Input Current vs Forward Voltage

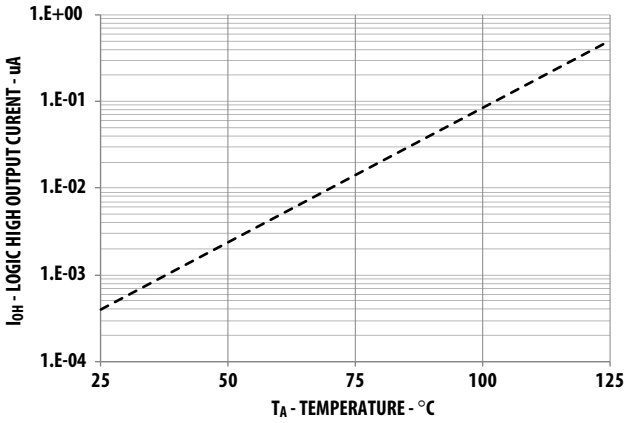


Figure 7. Typical High Level Output Current vs Temperature

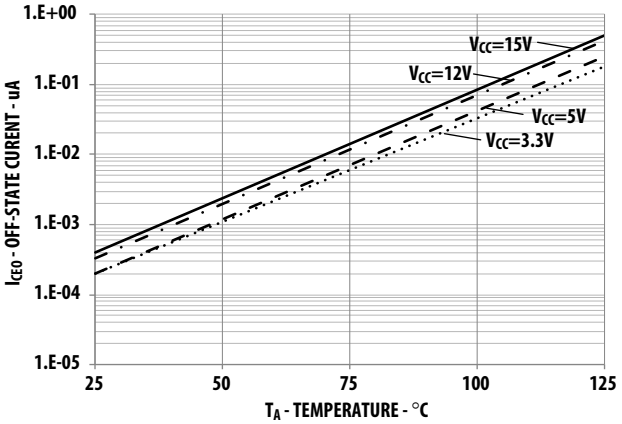


Figure 8. Typical Off-State Current vs Temperature (4-Pin Configuration)

Test Circuits

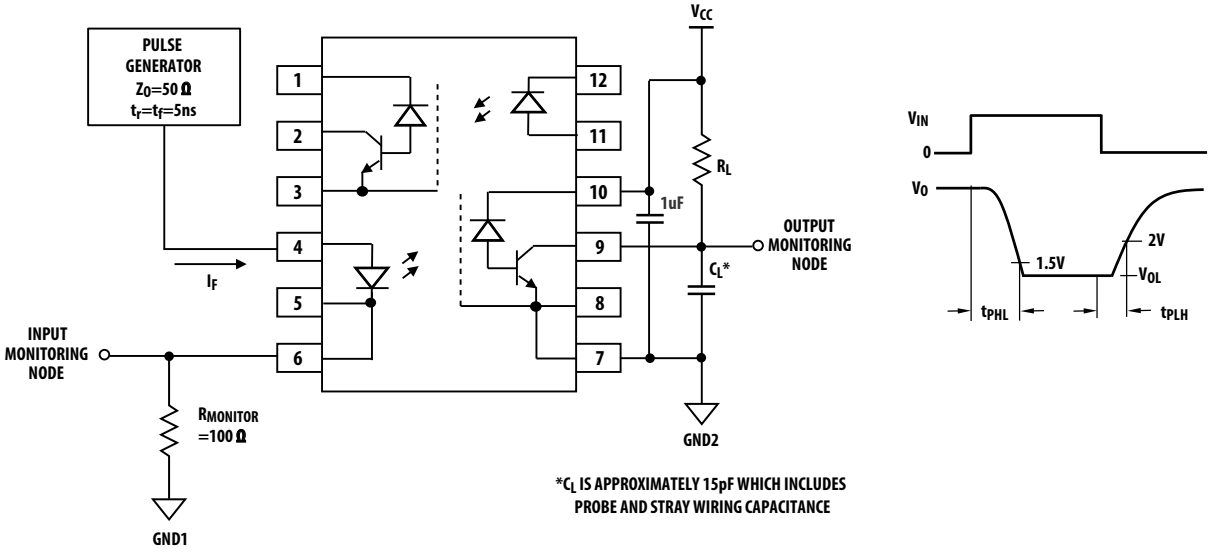


Figure 9. Switching Test Circuit (5-pin Configuration)

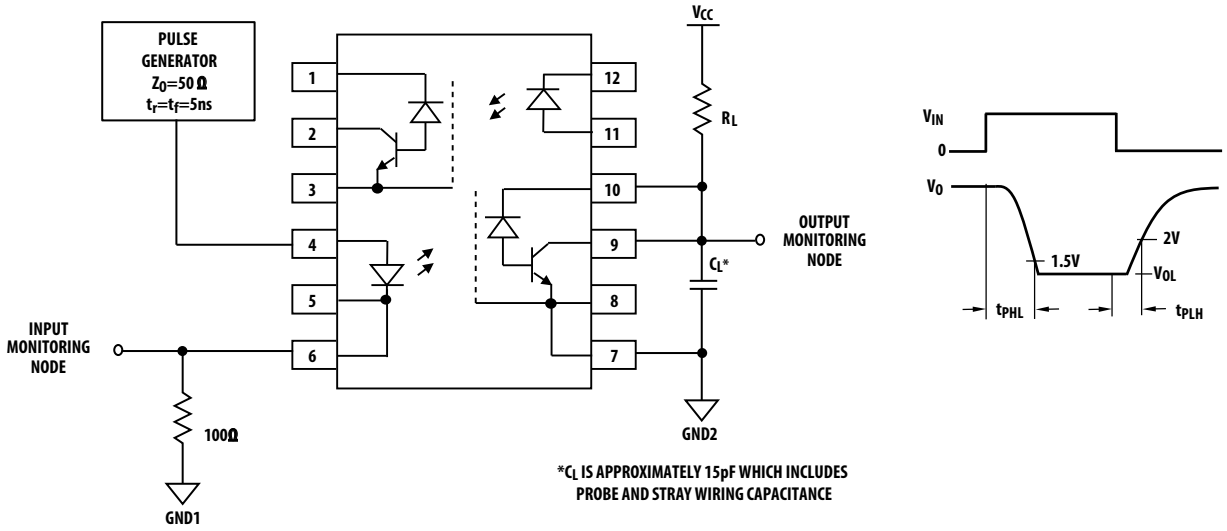


Figure 10. Switching Test Circuit (4-pin Configuration)

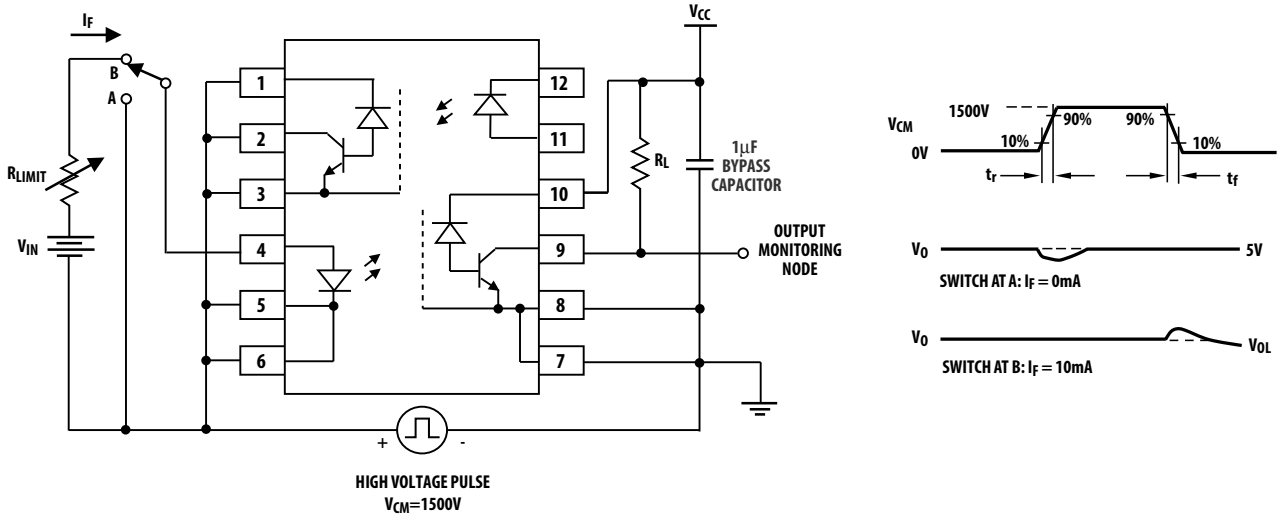


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms (5-Pin Configuration)

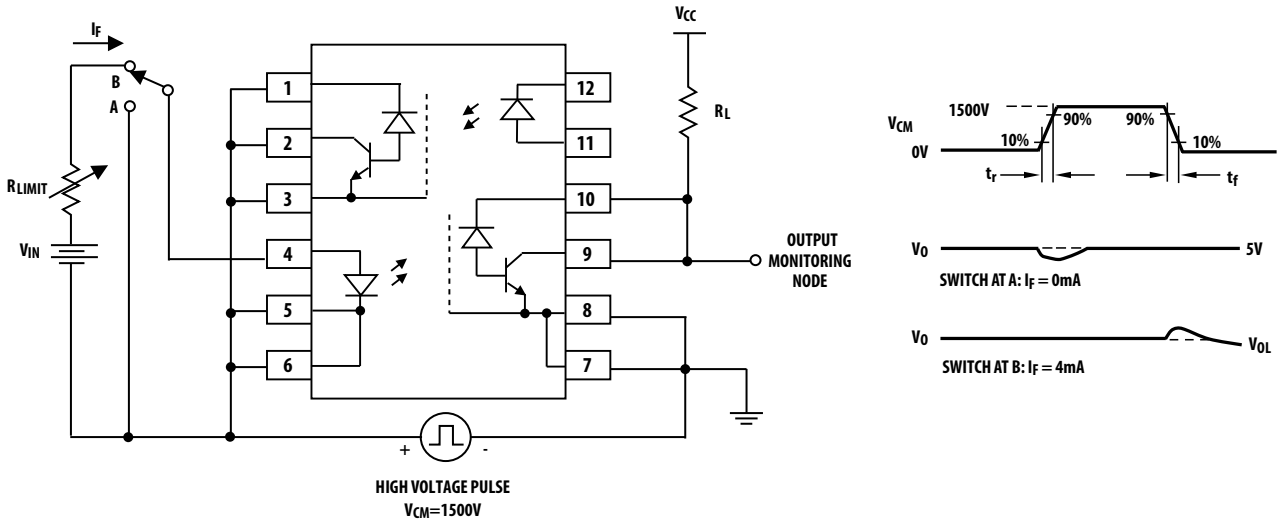


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms (4-Pin Configuration)

Thermal Resistance Measurement

The diagram of ACFL-5212T for measurement is shown in Figure 13. This is a multi-chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd die is heated and all the dice temperatures are recorded and so on until the 4th die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of two heat sources.

$$\begin{vmatrix} R11 & R12 & R13 & R14 \\ R21 & R22 & R23 & R24 \\ R31 & R32 & R33 & R34 \\ R41 & R42 & R43 & R44 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \\ P3 \\ P4 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \\ \Delta T3 \\ \Delta T4 \end{vmatrix}$$

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (˚C/W)
R_{12}: Thermal Resistance of Die1 due to heating of Die2 (˚C/W)
R_{13}: Thermal Resistance of Die1 due to heating of Die3 (˚C/W)
R_{14}: Thermal Resistance of Die1 due to heating of Die4 (˚C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (˚C/W)
R_{22}: Thermal Resistance of Die2 due to heating of Die2 (˚C/W)
R_{23}: Thermal Resistance of Die2 due to heating of Die3 (˚C/W)
R_{24}: Thermal Resistance of Die2 due to heating of Die4 (˚C/W)

R_{31}: Thermal Resistance of Die3 due to heating of Die1 (˚C/W)
R_{32}: Thermal Resistance of Die3 due to heating of Die2 (˚C/W)
R_{33}: Thermal Resistance of Die3 due to heating of Die3 (˚C/W)
R_{34}: Thermal Resistance of Die3 due to heating of Die4 (˚C/W)

R_{41}: Thermal Resistance of Die4 due to heating of Die1 (˚C/W)
R_{42}: Thermal Resistance of Die4 due to heating of Die2 (˚C/W)
R_{43}: Thermal Resistance of Die4 due to heating of Die3 (˚C/W)
R_{44}: Thermal Resistance of Die4 due to heating of Die4 (˚C/W)

P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)
P_3: Power dissipation of Die3 (W)
P_4: Power dissipation of Die4 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)
T_2: Junction temperature of Die2 due to heat from all dice (°C)
T_3: Junction temperature of Die3 due to heat from all dice (°C)
T_4: Junction temperature of Die4 due to heat from all dice (°C)

Ta: Ambient temperature.
ΔT_1: Temperature difference between Die1 junction and ambient (°C)
ΔT_2: Temperature deference between Die2 junction and ambient (°C)
ΔT_3: Temperature difference between Die3 junction and ambient (°C)
ΔT_4: Temperature deference between Die4 junction and ambient (°C)

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + Ta$ -- (1)
$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + Ta$ -- (2)
$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + Ta$ -- (3)
$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + Ta$ -- (4)

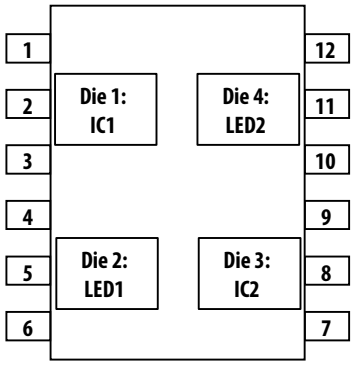


Figure 13. Diagram of ACFL-5212T for measurement

Measurement data on a low K (conductivity) board:

R_{11} = 181 °C/W
R_{21} = 103 °C/W
R_{31} = 82 °C/W
R_{41} = 110 °C/W
R_{12} = 91 °C/W
R_{22} = 232 °C/W
R_{32} = 97 °C/W
R_{42} = 86 °C/W
R_{13} = 85 °C/W
R_{23} = 109 °C/W
R_{33} = 180 °C/W
R_{43} = 101 °C/W
R_{14} = 112 °C/W
R_{24} = 91 °C/W
R_{34} = 91 °C/W
R_{44} = 277 °C/W

Measurement data on a high K (conductivity) board:

R_{11} = 117 °C/W
R_{21} = 37 °C/W
R_{31} = 35 °C/W
R_{41} = 47 °C/W
R_{12} = 42 °C/W
R_{22} = 161 °C/W
R_{32} = 53°C/W
R_{42} = 30 °C/W
R_{13} = 32 °C/W
R_{23} = 39 °C/W
R_{33} = 114 °C/W
R_{43} = 29 °C/W
R_{14} = 60 °C/W
R_{24} = 33 °C/W
R_{34} = 34 °C/W
R_{44} = 189 °C/W