

## Data Sheet

### Description

The ACNV2601 is an optically coupled gate that combines an AlGaAs light-emitting diode and an integrated photo detector housed in a widebody package. The distance-through-insulation (DTI) between the emitting diode and photo-detector is at 2 mm. The output of the detector IC is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 20 kV/ $\mu$ s at  $V_{cm} = 1500V$ .

With creepage and clearance of greater than 13 mm, ACNV2601 is designed to provide high isolation voltage (7500  $V_{rms}$ ). It can withstand a continuous high working voltage of 2262  $V_{peak}$  and a surge voltage of 12,000  $V_{peak}$ , meeting IEC60747-5-5, UL, and CSA standard for reinforced insulation. ACNV2601 provides the high insulation voltage protection at a high data rate of 10 MBd.

**CAUTION** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments

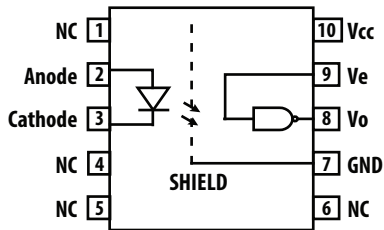
### Features

- High voltage insulation with minimum 13-mm creepage and clearance
- 20 kV/ $\mu$ s minimum common mode rejection (CMR) at  $V_{CM} = 1500V$
- High speed: 10 MBd typical
- TTL compatible
- Open collector output
- Guaranteed AC and DC performance over wide temperature:  $-40^{\circ}C$  to  $+105^{\circ}C$
- Available in 10-pin widebody packages
- Safety approval:
  - Approval at 7500  $V_{rms}$  for 1 minute per UL1577
  - CSA
  - IEC/EN/DIN EN 60747-5-5 with  $V_{iorm} = 2262 V_{peak}$

### Applications

- High voltage insulation
- Instrument input/output isolation
- Line receivers
- Ground loop elimination
- Isolation of high-speed logic systems
- Microprocessor system interfaces

## Functional Diagram



**NOTE** A 0.1- $\mu$ F bypass capacitor must be connected between pins  $V_{CC}$  and GND.

## Truth Table (Positive Logic)

LED	ENABLE	OUTPUT
On	H	L
Off	H	H
On	L	H
Off	L	H
On	NC	L
Off	NC	H

## Ordering Information

ACNV2601 is UL recognized with 7500  $V_{rms}$  for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Gull Wing	Tape & Reel	UL 7500 $V_{rms}$ / 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant							
ACNV2601	-000E	500 mil DIP-10				X	X	35 per tube
	-300E		X	X		X	X	35 per tube
	-500E		X	X	X	X	X	500 per reel

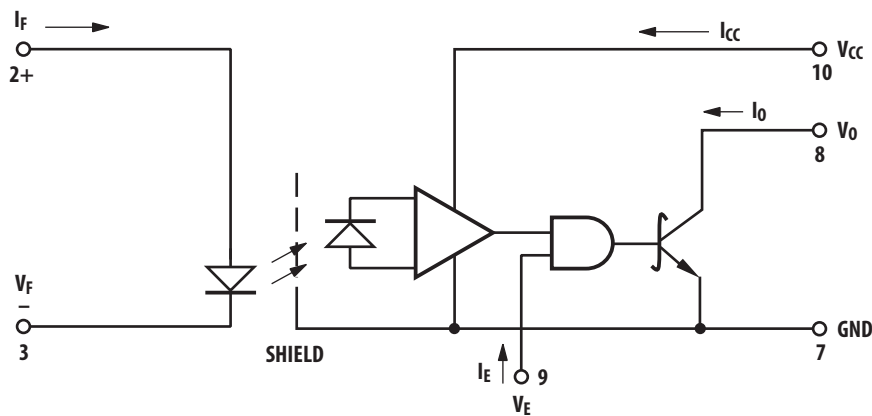
To order, choose a part number from the Part Number column and combine with the desired option from the Option column to form an order entry.

### Example 1:

ACNV2601-500E to order product of 500 mil DIP-10 Widebody with Gull Wing Surface Mount package in Tape and Reel packaging with both UL 7500  $V_{rms}$ /1 min and IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

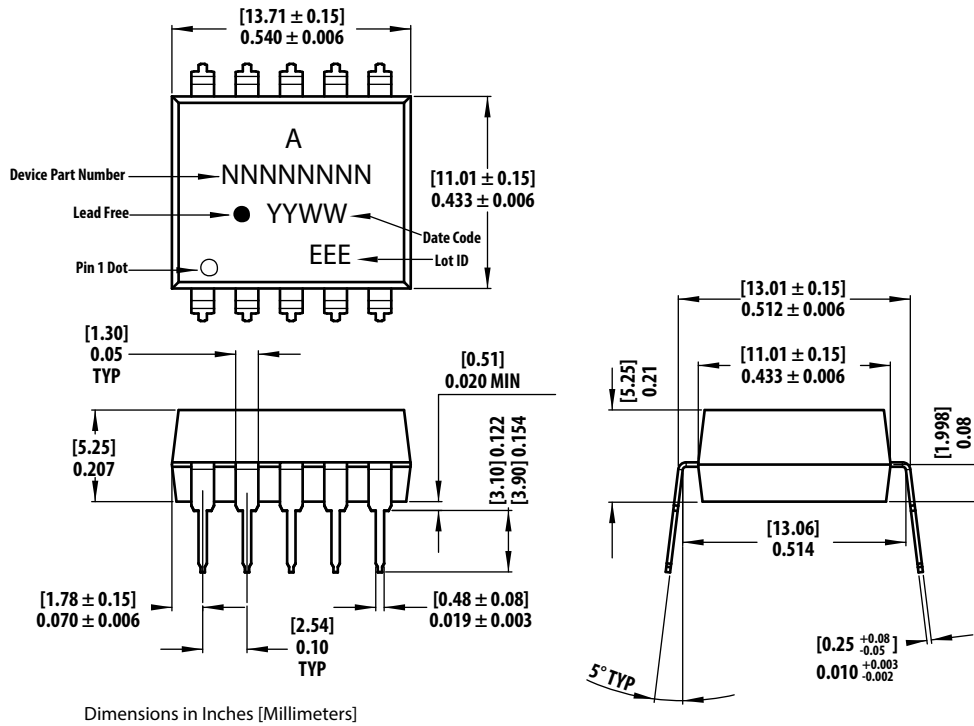
## Schematic



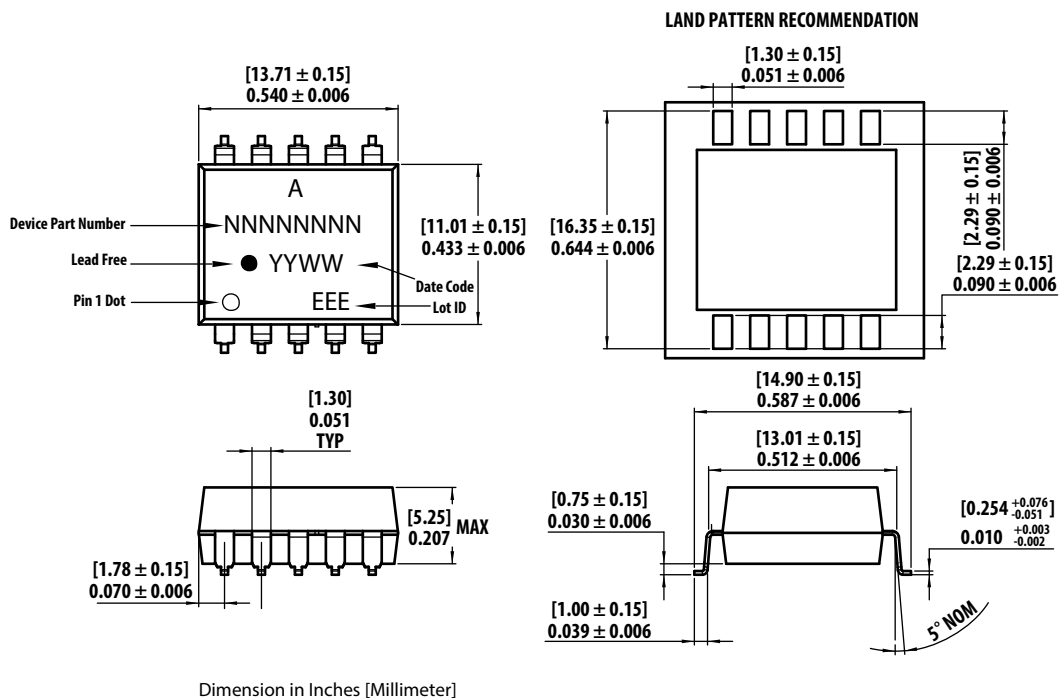
**NOTE** Use of a 0.1- $\mu$ F bypass capacitor connected between pins of 7 and 10 is recommended.

## Package Drawings

### 10-Pin Widebody (500 mils) DIP Package



### 10-Pin Widebody (500 mils) DIP Package with Gull Wing Surface Mount Option 300



## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

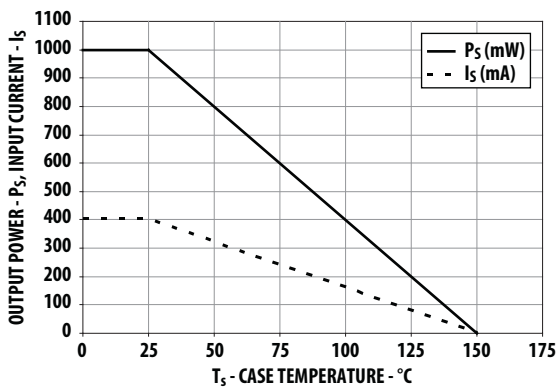
## Insulation and Safety Related Specifications

Parameter	Symbol	ACNV2601	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	13	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	13	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		2.0	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		4.6	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics<sup>a</sup>

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage $\leq 600 V_{rms}$ For Rated Mains Voltage $\leq 1000 V_{rms}$		I – IV I – III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	2262	$V_{peak}$
Input to Output Test Voltage, Method b <sup>a</sup> $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	4241	$V_{peak}$
Input to Output Test Voltage, Method a <sup>a</sup> $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	3619	$V_{peak}$
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	12000	$V_{peak}$
Safety-Limiting Values — Maximum Values Allowed in the Event of a Failure			
Case Temperature	$T_S$	150	$^{\circ}C$
Input Current <sup>b</sup>	$I_{S, INPUT}$	400	mA
Output Power <sup>b</sup>	$P_{S, OUTPUT}$	1	W
Insulation Resistance at $T_S$ , $V_{IO} = 500V$	$R_S$	$>10^9$	$\Omega$

- a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.
- b. Refer to the following figure for dependence of  $P_S$  and  $I_S$  on ambient temperature:



**NOTE** These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	$T_S$	-55	125	°C
Operating Temperature	$T_A$	-40	105	°C
Average Input Current	$I_{F(AVG)}$	—	20	mA
Reverse Input Voltage	$V_R$	—	3	V
Input Power Dissipation	$P_I$	—	40	mW
Supply Voltage (1 Minute Maximum)	$V_{CC}$	—	7	V
Enable Input Voltage (Not to exceed $V_{CC}$ by more than 500 mV)	$V_E$	—	$V_{CC} + 0.5$	V
Enable Input Current	$I_E$	—	5	mA
Output Collector Current	$I_O$	—	50	mA
Output Collector Voltage	$V_O$	—	7	V
Output Collector Power Dissipation	$P_O$	—	85	mW
Lead Solder Temperature	$T_{LS}$	—	245°C for 10 sec, up to seat plane	

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Notes
Input Current, Low Level	$I_{FL}^a$	0	250	μA	
Input Current, High Level	$I_{FH}^b$	9	16	mA	c
Power Supply Voltage	$V_{CC}$	4.5	5.5	V	
Low Level Enable Voltage	$V_{EL}$	0	0.8	V	
High Level Enable Voltage	$V_{EH}$	2.0	$V_{CC}$	V	
Operating Temperature	$T_A$	-40	105	°C	
Fan Out (at $R_L = 1\text{ k}\Omega$ )	N	—	5	TTL Loads	
Output Pull-up Resistor	$R_L$	330	4k	Ω	

- The off condition can also be guaranteed by ensuring that  $V_{FL} 0.8V$ .
- The initial switching threshold is 8 mA or less. It is recommended that 9 mA to 16 mA be used for best performance and to permit at least a 20% LED degradation guardband.
- Peaking circuits may produce transient input currents up to 50-mA, 50-ns maximum pulse width, provided average current does not exceed 20 mA.

## Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified. All typicals at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
High Level Output Current	$I_{OH}$	—	5.5	100	$\mu A$	$V_{CC} = 5.5V$ , $V_E = 2.0V$ $V_O = 5.5V$ , $I_{FL} = 250 \mu A$		a
Input Threshold Current	$I_{TH}$	—	3.5	8	mA	$V_{CC} = 5.5V$ , $V_E = 2.0V$ , $V_O = 0.6V$ , $I_{OL} > 13 \text{ mA}$	1, 2	a
Low Level Output Voltage	$V_{OL}$	—	0.35	0.6	V	$V_{CC} = 5.5V$ , $V_E = 2.0V$ , $I_F = 8 \text{ mA}$ , $I_{OL(Sinking)} = 13 \text{ mA}$	1, 2, 3, 4	a
High Level Supply Current	$I_{CCH}$	—	7.0	12	mA	$V_E = 0.5V$   $V_{CC} = 5.5V$ , $V_E = V_{CC}$   $I_F = 0 \text{ mA}$		
Low Level Supply Current	$I_{CCL}$	—	9.0	13	mA	$V_E = 0.5V$   $V_{CC} = 5.5V$ , $V_E = V_{CC}$   $I_F = 10 \text{ mA}$		
High Level Enable Current	$I_{EH}$	—	-0.7	—	mA	$V_{CC} = 5.5V$ , $V_E = 2.0V$		
Low Level Enable Current	$I_{EL}$	—	-0.9	—	mA	$V_{CC} = 5.5V$ , $V_E = 0.5V$		
High Level Enable Voltage	$V_{EH}$	2.0	—	—	mA	$V_{CC} = 5.5V$ , $V_E = 2.0V$		a
Low Level Enable Voltage	$V_{EL}$	—	—	0.8	mA	$V_{CC} = 5.5V$ , $V_E = 0.5V$		
Input Forward Voltage	$V_F$	1.25	1.64	1.85	V	$T_A = 25^\circ C$   $I_F = 10 \text{ mA}$	5	
		1.2	—	2.05				
Input Reverse Breakdown Voltage	$BV_R$	5	—	—	V	$I_R = 100 \mu A$ , $T_A = 25^\circ C$		
Input Capacitance	$C_{IN}$	—	60	—	pF	$f = 1 \text{ MHz}$ , $V_F = 0V$		
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$	—	-1.9	—	mV/ $^\circ C$	$I_F = 10 \text{ mA}$		

- a. No external pull-up is required for a high logic state on the enable input. If the  $V_E$  pin is not used, tying  $V_E$  to  $V_{CC}$  results in improved  $CM_R$  performance

## Switching Specifications (AC)

Over recommended temperature ( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ),  $V_{CC} = 5\text{V}$ ,  $I_F = 10\text{ mA}$  unless otherwise specified. All typicals are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
Propagation Delay Time to High Output Level	$t_{PLH}$	30	50	80	ns	$T_A = 25^\circ\text{C}$ $R_L = 350\Omega$ , $C_L = 15\text{ pF}$	6, 7, 8	a, b
Propagation Delay Time to Low Output Level	$t_{PHL}$	35	55	80	ns	$T_A = 25^\circ\text{C}$		c, b
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	—	5	40	ns	$R_L = 350\Omega$ , $C_L = 15\text{ pF}$	6, 7, 8, 9	b
Propagation Delay Skew	$t_{psk}$	—		50	ns			d, b
Output Rise Time (10% to 90%)	$T_r$	—	25	—	ns		10	b
Output Fall Time (10% to 90%)	$T_f$	—	10	—	ns		10	b
Propagation Delay Time of Enable from $V_{EH}$ to $V_{EL}$	$t_{ELH}$	—	30	—	ns	$R_L = 350\Omega$ , $C_L = 15\text{ pF}$ , $V_{EL} = 0\text{V}$ , $V_{EH} = 3\text{V}$	11, 12	e
Propagation Delay Time of Enable from $V_{EL}$ to $V_{EH}$	$t_{EHL}$	—	20	—	ns	$R_L = 350\Omega$ , $C_L = 15\text{ pF}$ , $V_{EL} = 0\text{V}$ , $V_{EH} = 3\text{V}$	11, 12	f
Output High Level Common Mode Transient Immunity	$ CM_H $	20	25	—	kV/ $\mu\text{s}$	$V_{CC} = 5\text{V}$ , $I_F = 0\text{ mA}$ , $V_{O(MIN)} = 2\text{V}$ , $R_L = 350\Omega$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 1500\text{V}$	13	g, h, b
Output Low Level Common Mode Transient Immunity	$ CM_L $	20	25	—	kV/ $\mu\text{s}$	$V_{CC} = 5\text{V}$ , $I_F = 10\text{ mA}$ , $V_{O(MAX)} = 0.8\text{V}$ , $R_L = 350\Omega$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 1500\text{V}$		h, i, b

- The  $t_{PLH}$  propagation delay is measured from the 5 mA point on the falling edge of the input pulse to the 1.5V point on the rising edge of the output pulse.
- No external pull-up is required for a high logic state on the enable input. If the  $V_E$  pin is not used, tying  $V_E$  to  $V_{CC}$  results in improved  $CM_R$  performance.
- The  $t_{PHL}$  propagation delay is measured from the 5 mA point on the rising edge of the input pulse to the 1.5V point on the falling edge of the output pulse.
- $t_{psk}$  is equal to the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that is seen between units at any given temperature and specified test conditions.
- The  $t_{ELH}$  enable propagation delay is measured from the 1.5V point on the falling edge of the enable input pulse to the 1.5V point on the rising edge of the output pulse.
- The  $t_{EHL}$  enable propagation delay is measured from the 1.5V point on the rising edge of the enable input pulse to the 1.5V point on the falling edge of the output pulse.
- $CM_H$  is the maximum tolerable rate of rise of the common mode voltage to ensure that the output remains in a high logic state (i.e.,  $V_O > 2.0\text{V}$ ).
- For sinusoidal voltages,  $(|dV_{CM}|/dt)_{\text{max}} = \pi f_{CM} V_{CM(p-p)}$ .
- $CM_L$  is the maximum tolerable rate of fall of the common mode voltage to ensure that the output remains in a low logic state (i.e.,  $V_O < 0.8\text{V}$ ).

## Package Characteristics

All typicals are at  $T_A = 25^\circ\text{C}$ .

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
Input-Output Insulation	$V_{ISO}$	7500	—	—	$V_{rms}$	$RH < 50\%$ for 1 min., $T_A = 25^\circ\text{C}$		a, b
Input-Output Resistance	$R_{I-O}$	$10^{12}$	—	—	$\Omega$	$V_{I-O} = 500\text{V}$		a
Input-Output Capacitance	$C_{I-O}$	—	0.5	0.6	pF	$f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$		a

- Device considered a two-terminal device: pins 1, 2, 3, 4 and 5 shorted together, and pins 6, 7, 8, 9 and 10 shorted together.
- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 9000 V_{rms}$  for one second (leakage detection current limit,  $I_{I-O} \leq 5\text{ }\mu\text{A}$ ). This test is performed before the 100% production test for partial discharge (Method b) shown in the [IEC/EN/DIN EN 60747-5-5 Insulation Characteristics](#)<sup>a</sup> table, if applicable.



Figure 1 Typical Output Voltage vs. Forward Input Voltage Current

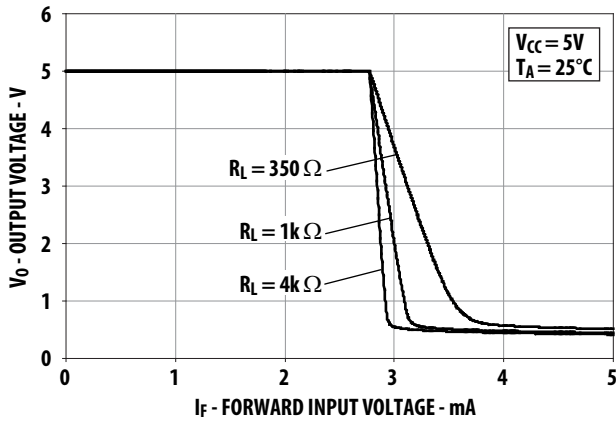


Figure 2 Typical Input Threshold Current vs. Temperature

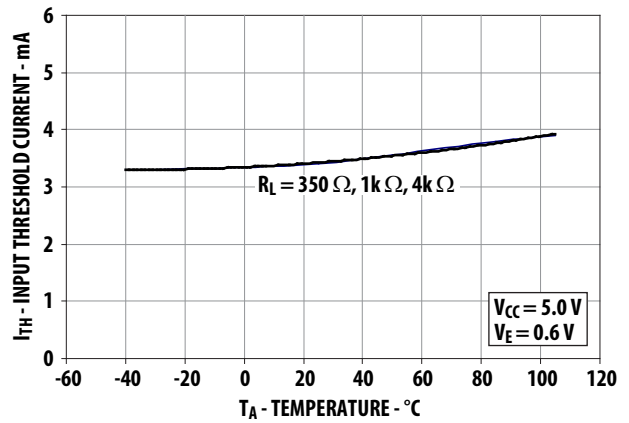


Figure 3 Typical Low Level Output Voltage vs. Temperature

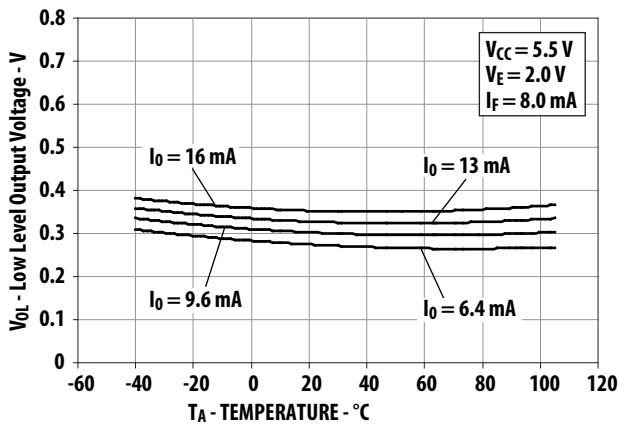


Figure 4 Typical Low Level Output Current vs. Temperature

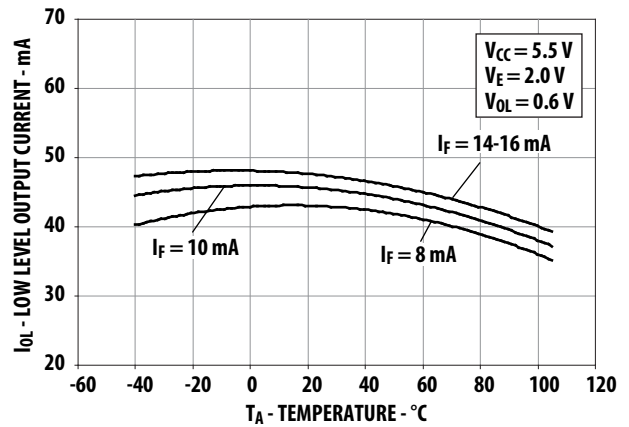


Figure 5 Typical Input Diode Forward Characteristic

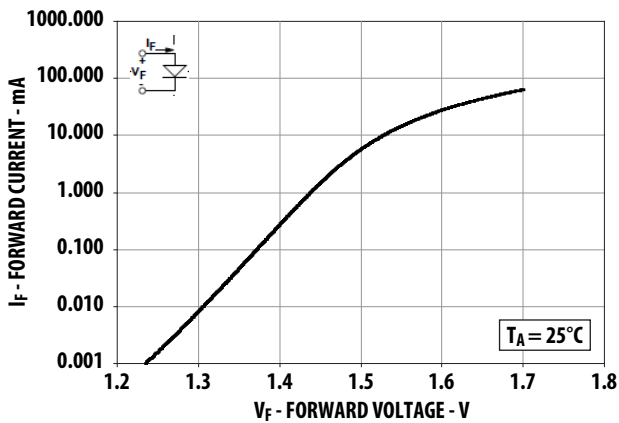


Figure 6 Test Circuit for  $t_{pHL}$  and  $t_{pLH}$

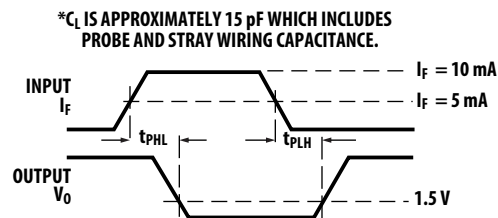
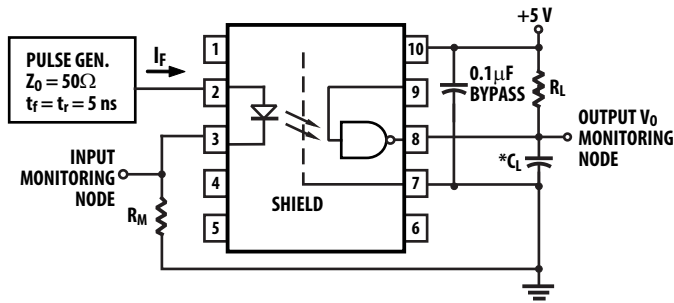


Figure 7 Typical Propagation Delay vs. Temperature

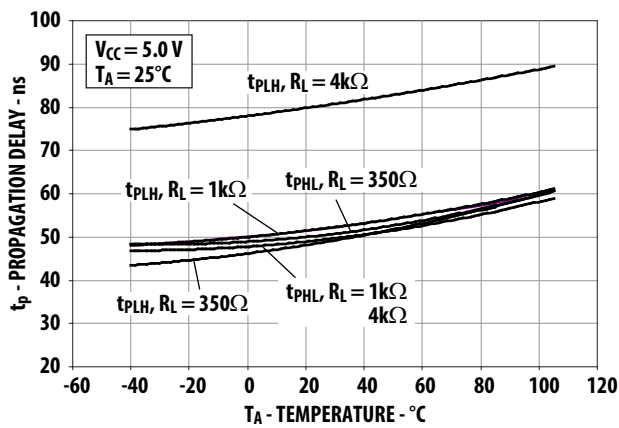


Figure 8 Typical Propagation Delay vs. Pulse Input Current

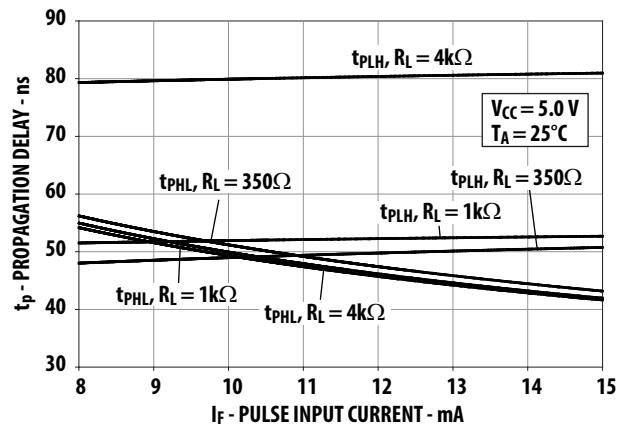


Figure 9 Typical Pulse Width Distortion vs. Temperature

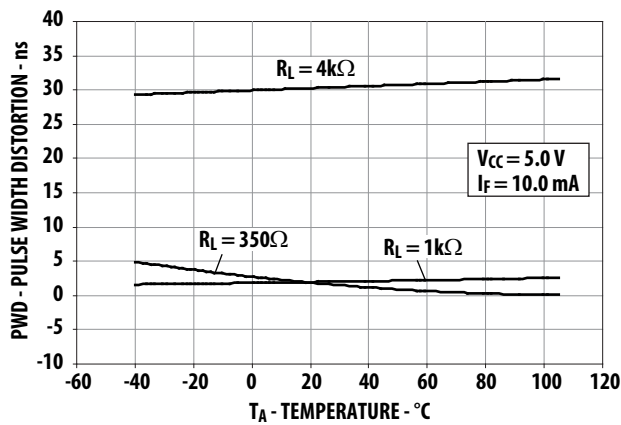


Figure 10 Typical Rise and Fall Time vs. Temperature

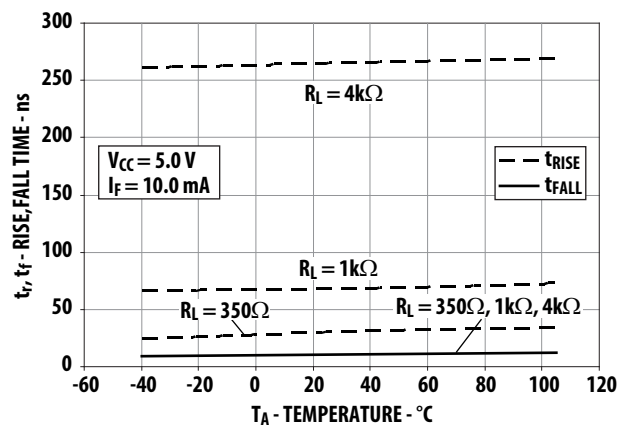
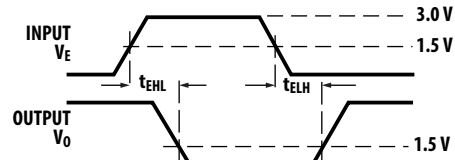
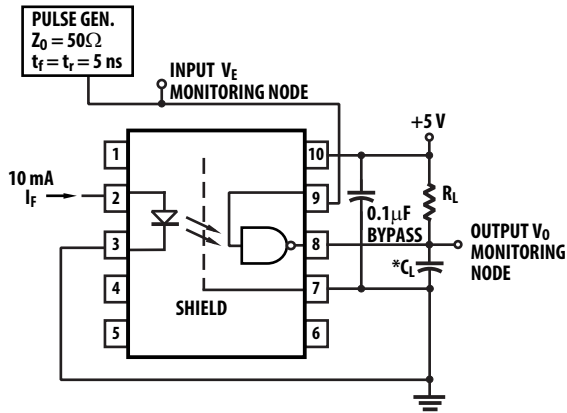
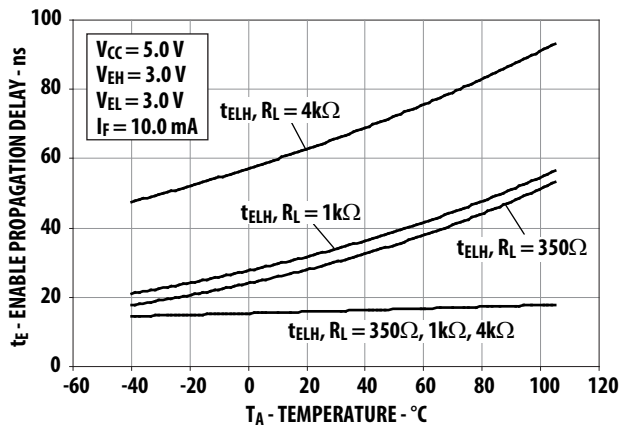


Figure 11 Test Circuit for  $t_{EHL}$  and  $t_{ELH}$

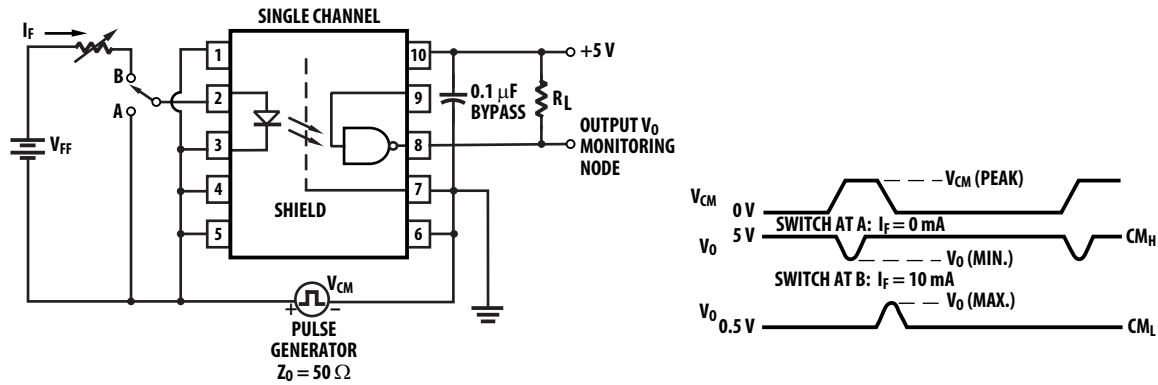


\* $C_L$  IS APPROXIMATELY 15 pF WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 12 Typical Enable Propagation Delay vs. Temperature



**Figure 13 Test Circuit for Common Mode Transient Immunity and Typical Waveforms**



**Figure 14 Recommended Printed Circuit Board Layout**

