

## ACPL-077L

### Low-Power 3.3V/5V High-Speed CMOS Optocoupler Design for System-Level Reliability

#### Description

The Broadcom<sup>®</sup> ACPL-077L optocoupler utilizes the latest CMOS IC technology to achieve outstanding speed and low power performance of minimum 25-MBd data rate and 6-ns maximum pulse width distortion with enhanced reliability relative to system-level IEC 61000-4-X testing (ESD/Burst/Surge).

Available in SO-8 package, the basic building blocks of ACPL-077L are a CMOS LED driver IC, a high-speed LED, and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC, which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

**CAUTION!** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

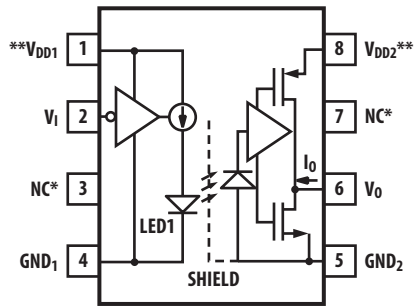
#### Features

- Enhance reliability relative to system-level IEC 61000-4-X testing (ESD/Burst/Surge)
- 3.3V and 5V CMOS compatibility
- CMOS buffer input
- Allow level shifting functionality
- High speed: DC to 25 MBd
- 35-kV/ $\mu$ s minimum common mode rejection (CMR) at  $V_{CM} = 1000V$
- Guaranteed AC and DC performance over wide temperature:  $-40$  to  $+105^{\circ}C$
- Safety and regulatory approvals:
  - UL recognized:
    - 3750  $V_{rms}$  for 1 min. per UL1577
  - CSA component acceptance notice #5
  - IEC/EN/DIN EN 60747-5-5:
    - $V_{IORM} = 567 V_{peak}$  for Option 060E
- Lead-free option available

#### Applications

- Digital fieldbus isolation: CC-Link, DeviceNet, Profibus, SDS
- Multiplexed data transmission
- General instrument and data acquisition
- Computer peripheral interface
- Microprocessor system interface

## Functional Diagram



\* Pin 3 is multiplexed as a test pin that can connect to  $V_{DD}$  or left unconnected. Pin 7 is not connected internally.

\*\* A 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$  bypass capacitor must be connected as close as possible between pins  $V_{DD1}$  and  $GND_1$ , and  $V_{DD2}$  and  $GND_2$ .

## Truth Table

| $V_i$ | LED1 | $V_o$ |
|-------|------|-------|
| HIGH  | OFF  | HIGH  |
| LOW   | ON   | LOW   |

## Ordering Information

ACPL-077L is UL Recognized with 3750  $V_{rms}$  for 1 minute per UL1577.

| Part Number | Option         | Package | Surface Mount | Tape and Reel | IEC/EN/DIN EN 60747-5-5 | Quantity      |
|-------------|----------------|---------|---------------|---------------|-------------------------|---------------|
|             | RoHS Compliant |         |               |               |                         |               |
| ACPL-077L   | -000E          | SO-8    | X             |               |                         | 100 per tube  |
|             | -060E          |         | X             |               | X                       | 100 per tube  |
|             | -500E          |         | X             | X             |                         | 1500 per reel |
|             | -560E          |         | X             | X             | X                       | 1500 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-077L-500E to order product of Mini-flat Surface Mount 8-pin package in Tape and Reel packaging with RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

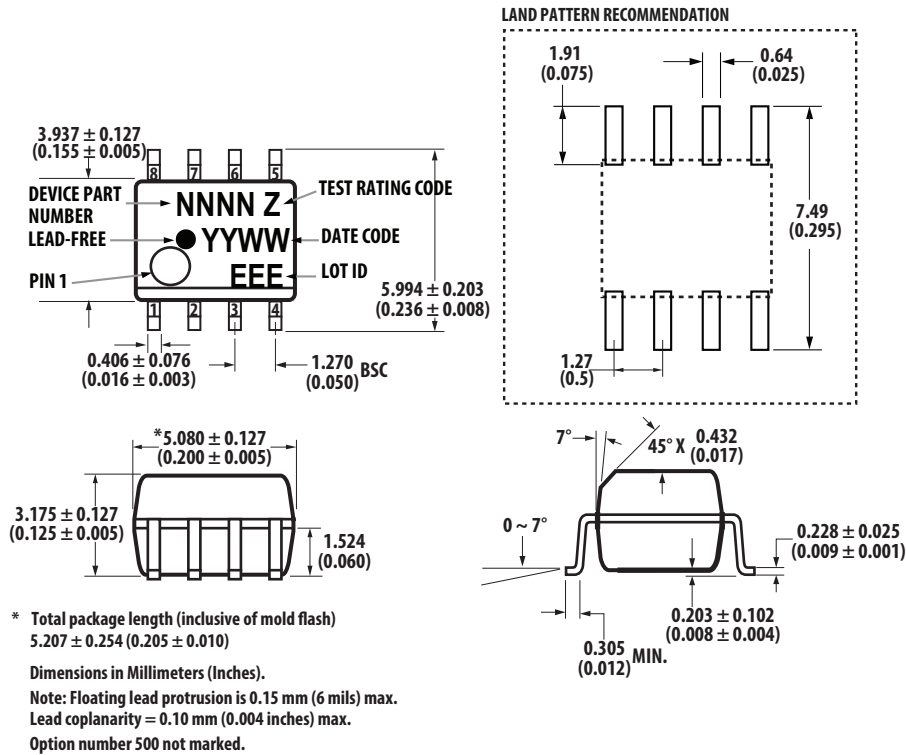
## Regulatory Information

The ACPL-077L will be approved by the following organizations:

- **UL** — Approval under UL 1577, component recognition program up to  $V_{ISO} = 3750 V_{RMS}$ .
- **CSA** — Approval under CSA component acceptance notice #5.
- **IEC/EN/DIN EN 60747-5-5** — (Option 060E only)

# Package Outline Drawings

## ACPL-077L SO-8 Package



## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Insulation and Safety Related Specifications

| Parameter   | Symbol | ACPL-077L | Unit | Conditions   |
|---|--------|-----------|------|--|
| Minimum External Air Gap (Clearance)              | L(I01) | 4.9       | mm   | Measured from input terminals to output terminals, shortest distance through air.  |
| Minimum External Tracking (Creepage)              | L(I02) | 4.8       | mm   | Measured from input terminals to output terminals, shortest distance path along body.  |
| Minimum Internal Plastic Gap (Internal Clearance) |        | 0.08      | mm   | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index)  | CTI    | 175       | V    | DIN IEC 112/VDE 0303 Part 1.   |
| Isolation Group                                   |        | IIIa      |      | Material Group (DIN VDE 0110, 1/89, Table 1).  |

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060E)

| Description   | Symbol        | Characteristic              | Unit        |
|---|---------------|-----------------------------|-------------|
|   |               | ACPL-077L                   |             |
| Installation Classification per DIN VDE 0110/39, Table 1<br>For Rated Mains Voltage $\leq 150V_{rms}$<br>For Rated Mains Voltage $\leq 300V_{rms}$<br>For Rated Mains Voltage $\leq 600V_{rms}$ |               | I – IV<br>I – III<br>I – II |             |
| Climatic Classification   |               | 55/105/21                   |             |
| Pollution Degree (DIN VDE 0110/39)  |               | 2                           |             |
| Maximum Working Insulation Voltage  | $V_{IORM}$    | 567                         | $V_{peak}$  |
| Input to Output Test Voltage, Method b <sup>a</sup><br>$V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1s$ ,<br>Partial Discharge $< 5 pC$                                  | $V_{PR}$      | 1063                        | $V_{peak}$  |
| Input to Output Test Voltage, Method a <sup>a</sup><br>$V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10s$ ,<br>Partial Discharge $< 5 pC$                                       | $V_{PR}$      | 907                         | $V_{peak}$  |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60s$ )  | $V_{IOTM}$    | 6000                        | $V_{peak}$  |
| Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure   |               |                             |             |
| Case Temperature  | $T_S$         | 150                         | $^{\circ}C$ |
| Input Current <sup>b</sup>  | $I_S, INPUT$  | 150                         | mA          |
| Output Power  | $P_S, OUTPUT$ | 600                         | mW          |
| Insulation Resistance at $T_S$ , $V_{IO} = 500V$  | $R_S$         | $\geq 10^9$                 | $\Omega$    |

a. Refer to the optocoupler section of the Isolation and Control Component Designer's Catalog, under Product Safety Regulations section (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

b. Refer to figure 10 for dependence of  $P_S$  and  $I_S$  on ambient temperature.

**NOTE:** These optocouplers are suitable for *safe electrical isolation* only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

## Absolute Maximum Ratings

| Parameter                         | Symbol   | Min.   | Max.            | Unit |
|-----------------------------------|--|--|-----------------|------|
| Storage Temperature               | $T_S$  | -55  | 125             | °C   |
| Operating Temperature             | $T_A$  | -40  | 105             | °C   |
| Supply Voltages                   | $V_{DD1}, V_{DD2}$                                 | 0  | 6.5             | V    |
| Input Voltage                     | $V_I$  | -0.5   | $V_{DD1} + 0.5$ | V    |
| Output Voltage                    | $V_O$  | -0.5   | $V_{DD2} + 0.5$ | V    |
| Average Output Current            | $I_O$  | —  | 10              | mA   |
| Lead Solder Temperature           | $T_{LS}$   | 260° C for 10 sec., 1.6 mm below seating plane |                 |      |
| Solder Reflow Temperature Profile | See <a href="#">Solder Reflow Profile</a> section. |  |                 |      |

## Recommended Operating Conditions

| Parameter                        | Symbol             | Min.                 | Max.                 | Unit |
|----------------------------------|--------------------|----------------------|----------------------|------|
| Operating Temperature            | $T_A$              | -40                  | 105                  | °C   |
| Supply Voltages (3.3V)           | $V_{DD1}, V_{DD2}$ | 3.0                  | 3.6                  | V    |
| Supply Voltages (5V)             | $V_{DD1}, V_{DD2}$ | 4.5                  | 5.5                  | V    |
| Logic High Input Voltage         | $V_{IH}$           | $0.7 \times V_{DD1}$ | $V_{DD1}$            | V    |
| Logic Low Input Voltage          | $V_{IL}$           | 0                    | $0.3 \times V_{DD1}$ | V    |
| Input Signal Rise and Fall Times | $t_{ir}, t_{if}$   | —                    | 1.0                  | ms   |

## Electrical Specifications

Over recommended temperature ( $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ) and supply voltage ( $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ ,  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ ), ( $3\text{V} \leq V_{DD1} \leq 3.6\text{V}$ ,  $3\text{V} \leq V_{DD2} \leq 3.6\text{V}$ ), ( $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ ,  $3\text{V} \leq V_{DD2} \leq 3.6\text{V}$ ) and ( $3\text{V} \leq V_{DD1} \leq 3.6\text{V}$ ,  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ ). All typical specifications are at  $V_{DD1} = V_{DD2} = +3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

| Parameter                                    | Symbol     | Min. | Typ. | Max. | Unit | Test Conditions  |
|--|------------|------|------|------|------|--|
| Logic Low Input Supply Current <sup>a</sup>  | $I_{DD1L}$ | —    | 5.5  | 8    | mA   | $V_I = 0\text{V}$ ; <a href="#">Figure 1</a>                       |
| Logic High Input Supply Current <sup>a</sup> | $I_{DD1H}$ | —    | 0.6  | 2    | mA   | $V_I = V_{DD1}$ ; <a href="#">Figure 2</a>                         |
| Logic Low Output Supply Current              | $I_{DD2L}$ | —    | 1.5  | 2.5  | mA   | $V_I = 0\text{V}$ ; <a href="#">Figure 3</a>                       |
| Logic High Output Supply Current             | $I_{DD2H}$ | —    | 1.5  | 2.5  | mA   | $V_I = V_{DD1}$ ; <a href="#">Figure 4</a>                         |
| Input Current                                | $I_I$      | -10  | —    | 10   | μA   |  |
| Logic High Output Voltage                    | $V_{OH}$   | 2.9  | 3.3  | —    | V    | $I_O = -20 \mu\text{A}$ , $V_I = V_{IH}$ , $V_{DD2} = 3.3\text{V}$ |
|  |            | 1.9  | 2.9  | —    | V    | $I_O = -4 \text{mA}$ , $V_I = V_{IH}$ , $V_{DD2} = 3.3\text{V}$    |
|  |            | 4.0  | 4.7  | —    | V    | $I_O = -4 \text{mA}$ , $V_I = V_{IH}$ , $V_{DD2} = 5.0\text{V}$    |
| Logic Low Output Voltage                     | $V_{OL}$   | —    | 0    | 0.1  | V    | $I_O = 20 \mu\text{A}$ , $V_I = V_{IL}$                            |
|  |            | —    | 0.35 | 1.0  | V    | $I_O = 4 \text{mA}$ , $V_I = V_{IL}$                               |

a. The LED is ON when  $V_I$  is low and OFF when  $V_I$  is high.

## Switching Specifications

Over recommended temperature ( $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ) and supply voltage ( $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ ,  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ ), ( $3\text{V} \leq V_{DD1} \leq 3.6\text{V}$ ,  $3\text{V} \leq V_{DD2} \leq 3.6\text{V}$ ), ( $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ ,  $3\text{V} \leq V_{DD2} \leq 3.6\text{V}$ ) and ( $3\text{V} \leq V_{DD1} \leq 3.6\text{V}$ ,  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ ). All typical specifications are at  $V_{DD1} = V_{DD2} = +3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

| Parameter  | Symbol    | Min. | Typ. | Max. | Unit              | Test Conditions   |
|--|-----------|------|------|------|-------------------|---|
| Propagation Delay Time to Logic Low Output <sup>a</sup>          | $t_{PHL}$ | —    | 24   | 40   | ns                | $C_L = 15\text{ pF}$ , CMOS Signal Levels; <a href="#">Figure 5</a> and <a href="#">Figure 6</a> .  |
| Propagation Delay Time to Logic High Output <sup>a</sup>         | $t_{PLH}$ | —    | 23   | 40   | ns                | $C_L = 15\text{ pF}$ , CMOS Signal Levels; <a href="#">Figure 5</a> and <a href="#">Figure 6</a> .  |
| Pulse Width  | $t_{PW}$  | 40   | —    | —    | ns                | $C_L = 15\text{ pF}$ , CMOS Signal Levels.  |
| Maximum Data Rate  |           | —    | —    | 25   | MBd               | $C_L = 15\text{ pF}$ , CMOS Signal Levels.  |
| Pulse Width Distortion <sup>b</sup> $ t_{PHL} - t_{PLH} $        | $ PWD $   | —    | 1    | 6    | ns                | $C_L = 15\text{ pF}$ , CMOS Signal Levels; <a href="#">Figure 7</a> and <a href="#">Figure 8</a> .  |
| Propagation Delay Skew <sup>c</sup>                              | $t_{PSK}$ | —    | —    | 15   | ns                | $C_L = 15\text{ pF}$ , CMOS Signal Levels.  |
| Output Rise Time (10% to 90%)                                    | $t_R$     | —    | 4    | —    | ns                | $C_L = 15\text{ pF}$ , CMOS Signal Levels, <a href="#">Figure 9</a> .                               |
| Output Fall Time (90% to 10%)                                    | $t_F$     | —    | 3    | —    | ns                |   |
| Common Mode Transient Immunity at Logic High Output <sup>d</sup> | $ CM_H $  | 35   | 50   | —    | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{V}$ , $T_A = 25^\circ\text{C}$ , $V_I = V_{DD1}$ , $V_O > 0.8 \times V_{DD2}$ . |
| Common Mode Transient Immunity at Logic Low Output <sup>d</sup>  | $ CM_L $  | 35   | 50   | —    | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{V}$ , $T_A = 25^\circ\text{C}$ , $V_I = 0\text{V}$ , $V_O < 0.8\text{V}$ .      |

- $t_{PHL}$  propagation delay is measured from the 50% level on the falling edge of the  $V_I$  signal to the 50% level of the falling edge of the  $V_O$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level on the rising edge of the  $V_I$  signal to the 50% level of the rising edge of the  $V_O$  signal.
- PWD is defined as  $|t_{PHL} - t_{PLH}|$ . %PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
- $t_{PSK}$  is equal to the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature within the recommended operating conditions.
- $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8\text{V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

## Package Characteristics

All typical specifications are at  $T_A = 25^\circ\text{C}$ .

| Parameter                                  | Symbol    | Min. | Typ.      | Max. | Unit      | Test Conditions                                    |
|--|-----------|------|-----------|------|-----------|--|
| Input-Output Insulation <sup>a, b, c</sup> | $V_{ISO}$ | 3750 | —         | —    | $V_{RMS}$ | $RH \leq 50\%$ for 1 min, $T_A = 25^\circ\text{C}$ |
| Input-Output Resistance <sup>a</sup>       | $R_{I-O}$ | —    | $10^{12}$ | —    | $\Omega$  | $V_{I-O} = 500\text{V}$                            |
| Input-Output Capacitance                   | $C_{I-O}$ | —    | 0.6       | —    | pF        | $f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$      |
| Input Capacitance <sup>d</sup>             | $C_I$     | —    | 3.0       | —    | pF        |  |

- Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
- In accordance with UL1577, each ACPL-077L is proof tested by applying an insulation test voltage  $\geq 4500 V_{RMS}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5\ \mu\text{A}$ ).
- The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, Optocoupler Input-Output Endurance Voltage.
- $C_I$  is the capacitance measured at pin 2 ( $V_I$ ).

Figure 1: Typical Logic Low Input Supply Current vs. Temperature

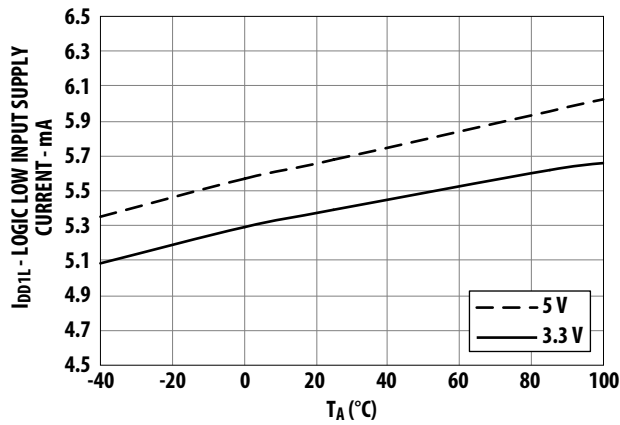


Figure 2: Typical Logic High Input Supply Current vs. Temperature

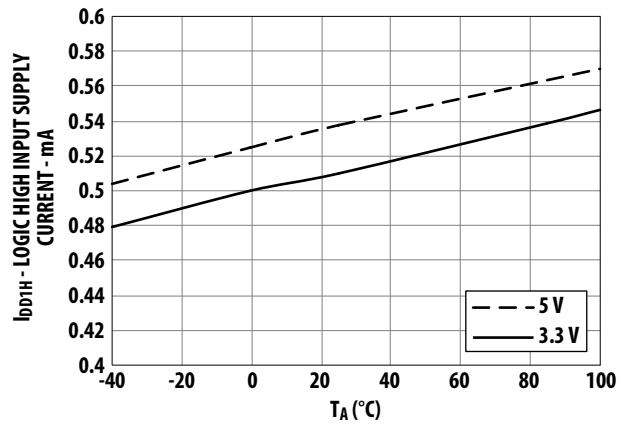


Figure 3: Typical Logic Low Output Supply Current vs. Temperature

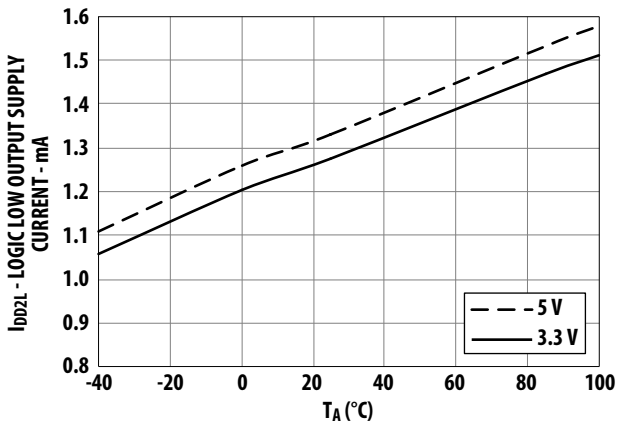


Figure 4: Typical Logic High Output Supply Current vs. Temperature

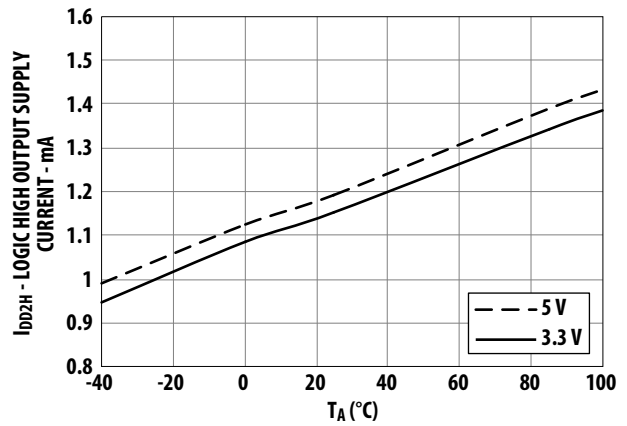


Figure 5: Typical Propagation Delay vs. Temperature at 3.3V Supply Voltage

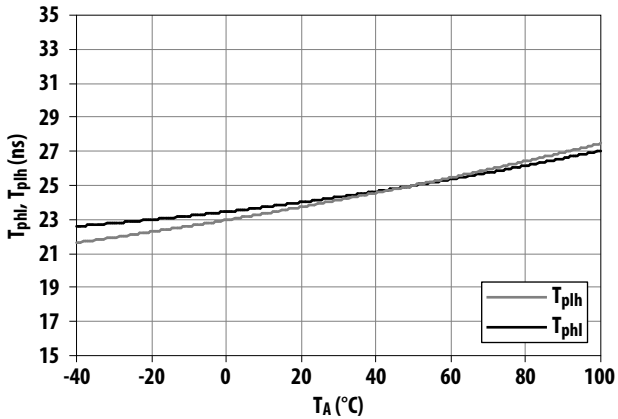
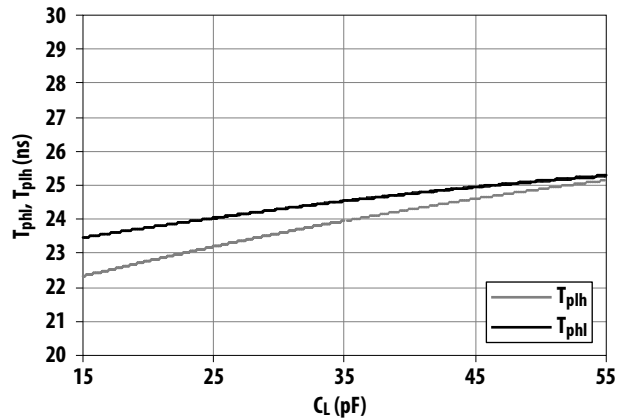
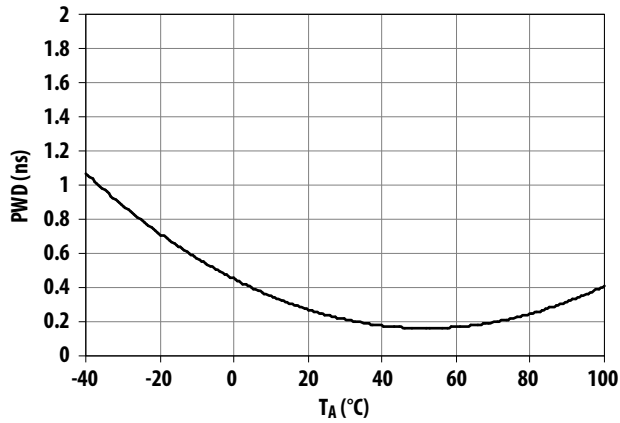


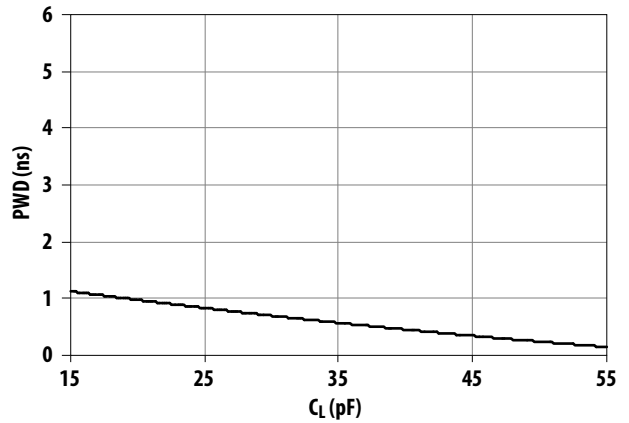
Figure 6: Typical Propagation Delays vs. Load Capacitance at 3.3V Supply Voltage



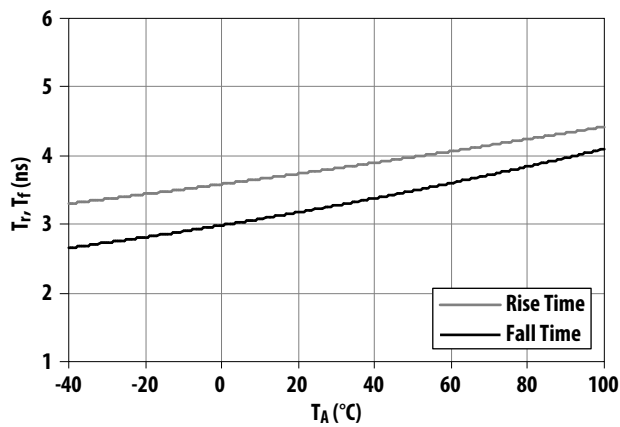
**Figure 7: Typical Pulse Width Distortion vs Temperature at 3.3V Supply Voltage**



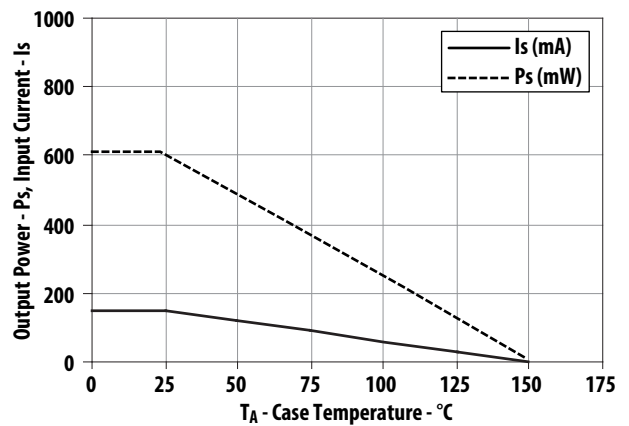
**Figure 8: Typical Pulse Width Distortion vs Load Capacitance at 3.3V Supply Voltage**



**Figure 9: Typical Rise and Fall Time vs Temperature at 3.3V Supply Voltage**



**Figure 10: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5**





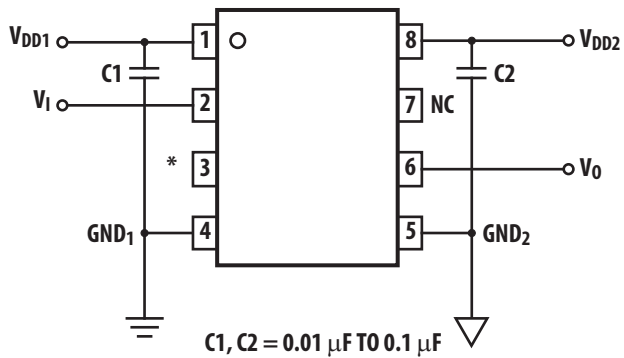
## Application Information

### Bypassing and PC Board Layout

The ACPL-077L optocoupler is extremely easy to use. No external interface circuitry is required because ACPL-077L uses high-speed CMOS IC technology, allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in [Figure 11](#), the only external components required for proper operation are two bypass capacitors. Capacitor values should be between  $0.01\ \mu\text{F}$  and  $0.1\ \mu\text{F}$ . Each capacitor should be placed as close as possible to the input and output power-supply pins of the optocoupler.

**Figure 11: Recommended Circuit Diagram**



\* Pin 3 is multiplexed as a test pin that can connect to VDD or left unconnected. Pin 7 is not connected internally.