

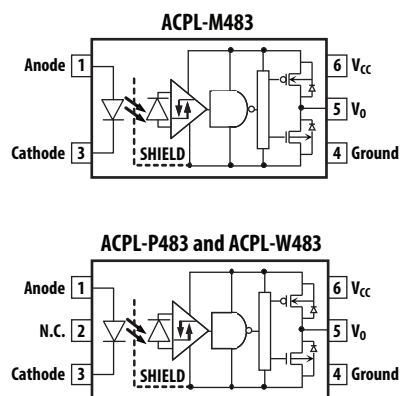
Inverted Logic High CMR Intelligent Power Module and Gate Drive Interface Optocoupler

Data Sheet

Description

The ACPL-M483/P483/W483 fast-speed optocoupler contains a AlGaAs LED and photo detector with built-in Schmitt trigger to provide logic-compatible waveforms, eliminating the need for additional wave shaping. The totem pole output eliminates the need for a pull-up resistor and allows for direct drive Intelligent Power Module or gate drive. Minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time.

Functional Diagram



Note: A 0.1 μF bypass capacitor must be connected between pins 4 and 6. Truth Table Guaranteed: V_{CC} from 4.5V to 30V.

Truth Table (Inverting Logic)

| LED | V_o |
|-----|-------|
| On | LOW |
| OFF | HIGH |

Features

- Inverted output type (totem pole output)
- Truth Table Guaranteed: V_{CC} from 4.5V to 30V
- Performance Specified for Common IPM Applications Over Industrial Temperature Range
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- Hysteresis
- Available in SO-5 (ACPL-M483) and Stretched SO-6 package (ACPL-P483/W483)
- Package Clearance/Creepage at 8 mm (ACPL-W483)
- Safety Approval:
 - UL Recognized with 5000V_{RMS} (ACPL-W483) for 1 minute per UL1577.
 - CSA Approved.
 - IEC/EN/DIN EN 60747-5-5 Approved with $V_{IORM} = 567 V_{peak}$ for ACPL-M483, $V_{IORM} = 891 V_{peak}$ for ACPL-P483, and $V_{IORM} = 1140 V_{peak}$ for ACPL-W483, under option 060.

Specifications

- Wide Operating Temperature Range: -40°C to $+105^{\circ}\text{C}$
- Maximum Propagation Delay $t_{PHL}/t_{PLH} = 120 \text{ ns}/120 \text{ ns}$
- Maximum Pulse Width Distortion (PWD) = 50 ns
- Propagation Delay Difference: Min/Max = $-100 \text{ ns}/+100 \text{ ns}$
- Wide Operating V_{CC} Range: 4.5V to 30V
- 30 kV/ μs Minimum Common Mode Rejection (CMR) at $V_{CM} = 1000\text{V}$

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters
- General Digital Isolation

Ordering Information

ACPL-M483/P483/W483 is UL recognized with 3750/3750/5000V_{RMS}/1 minute rating per UL 1577, respectively.

| Part Number | Option | Package | Surface Mount | Tape and Reel | IEC/EN/DIN EN 60747-5-5 | Quantity |
|------------------------|----------------|-------------------|---------------|---------------|-------------------------|---------------|
| | RoHS Compliant | | | | | |
| ACPL-M483 | -000E | Stretched SO-5 | X | | | 100 per tube |
| | -500E | | X | X | | 1500 per reel |
| | -060E | | X | | X | 100 per tube |
| | -560E | | X | X | X | 1500 per reel |
| ACPL-P483 ACPL-W483 | -000E | Stretched SO-6 | X | | | 100 per tube |
| | -500E | | X | X | | 1000 per reel |
| | -060E | | X | | X | 100 per tube |
| | -560E | | X | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an ordering part number.

- Example 1: ACPL-P483-560E: Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.
- Example 2: ACPL-P483-000E to order product of Stretched SO-6 Surface Mount package in Tube packaging and RoHS compliant.
- Example 3: ACPL-M483-000E to order product of SO-5 Surface Mount package in Tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Recommended Pb-Free IR Profile

The recommended reflow profile is per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

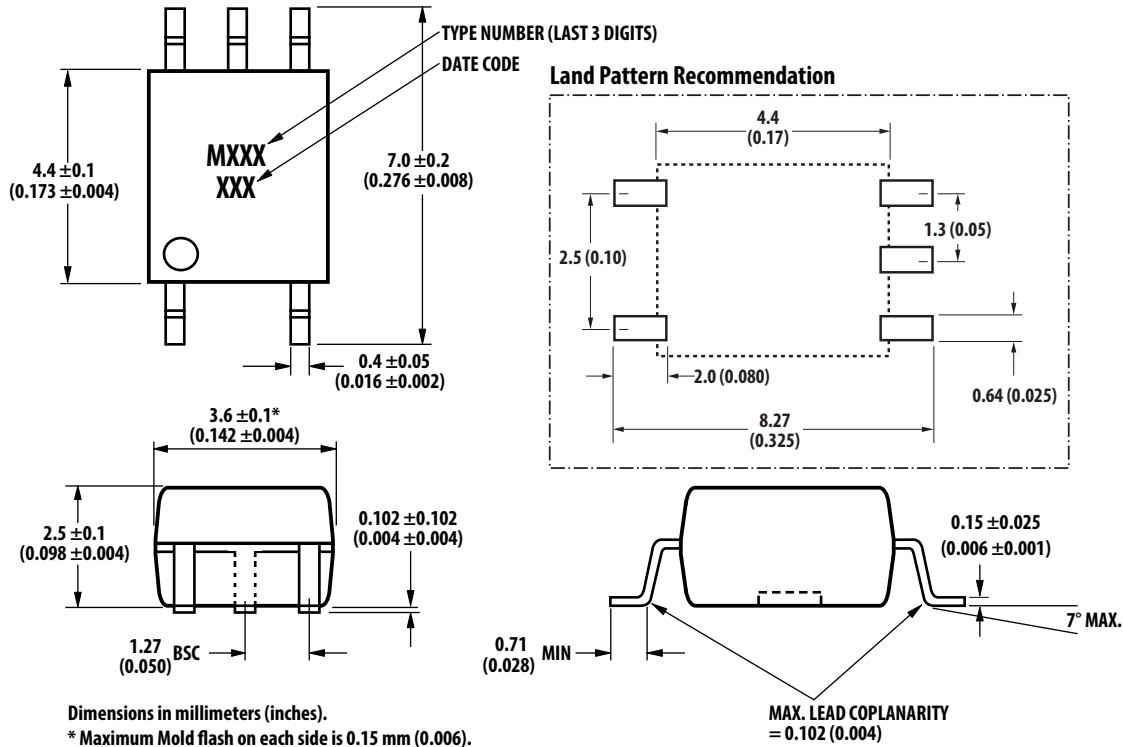
Regulatory Information

The ACPL-M483/P483/W483 is approved by the following organizations:

- IEC/EN/DIN EN 60747-5-5 (Option 060 only): Approved with Maximum Working Insulation Voltage $V_{IORM} = 567V_{peak}$ for ACPL-M483, $V_{IORM} = 891V_{peak}$ for ACPL-P483, and $V_{IORM} = 1140V_{peak}$ for ACPL-W483.
- UL: Approval under UL 1577, component recognition program up to $V_{ISO} = 3750V_{RMS}$ File E55361 for ACPL-M483 and ACPL-P483. Approval under UL 1577, component recognition program up to $V_{ISO} = 5000V_{RMS}$ File E55361 for ACPL-W483;
- CSA: Approval under CSA Component Acceptance Notice #5, File CA 88324.

Package Outline Drawings

ACPL-M483 SO-5 Package (5 mm Creepage and Clearance)

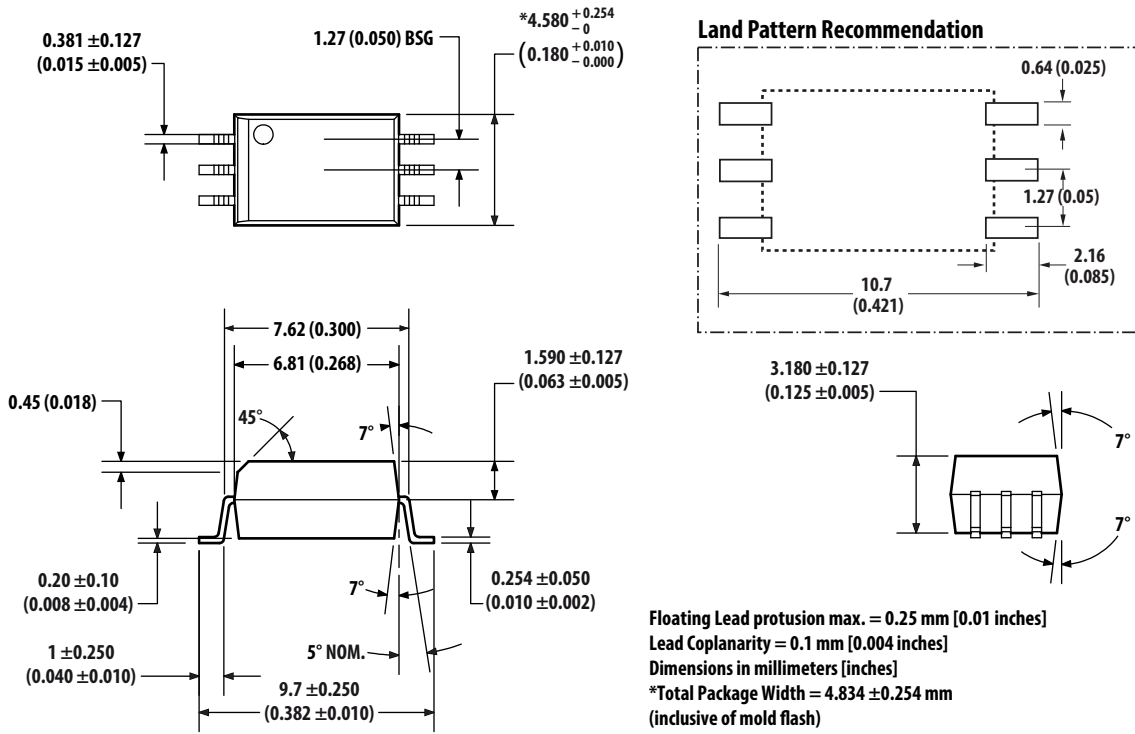


Dimensions in millimeters (inches).

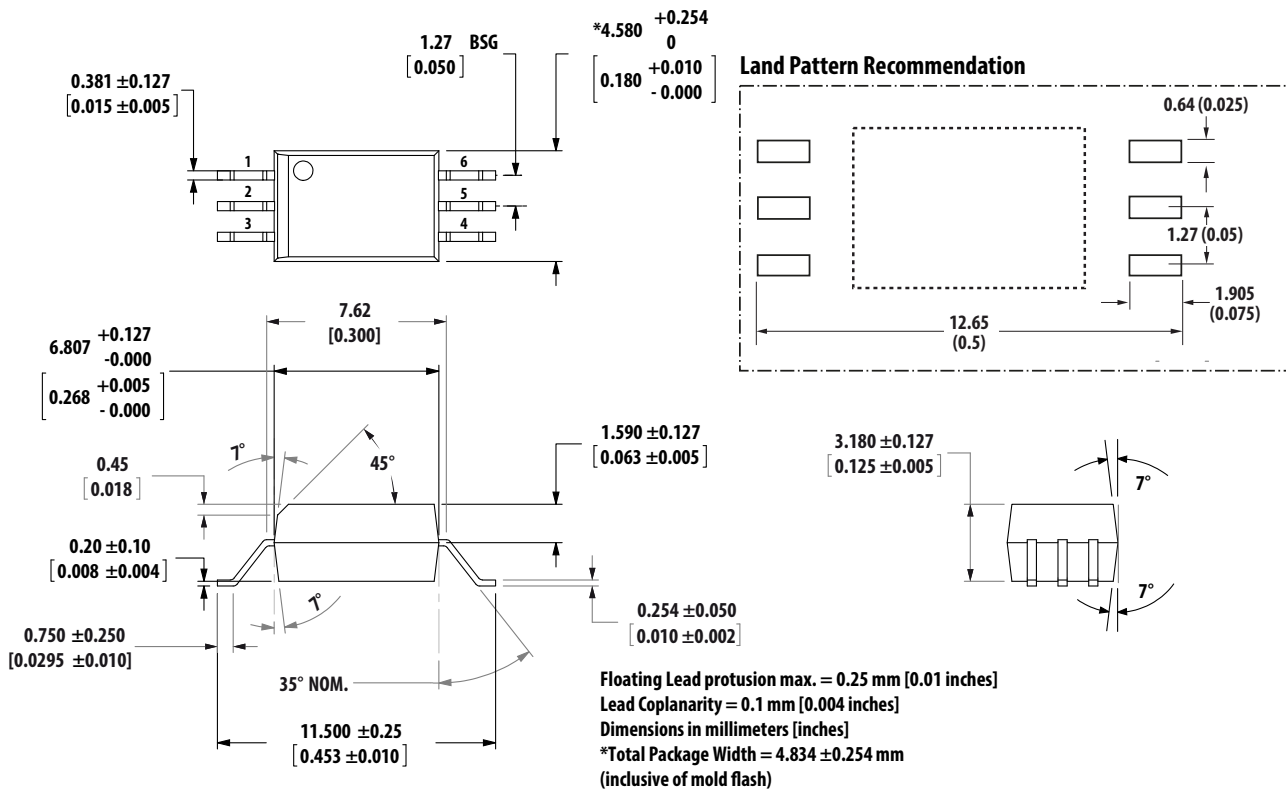
* Maximum Mold flash on each side is 0.15 mm (0.006).

Note: Floating Lead Protrusion is 0.15 mm (6 mils) max.

ACPL-P483 Stretched SO-6 Package (7 mm Clearance) with Land Pattern Recommendation



ACPL-W483 Stretched SO-6 Package (8 mm Clearance) with Land Pattern Recommendation



IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

| Description | Symbol | ACPL-M483 | ACPL-P483 | ACPL-W483 | Unit |
|--|-----------------|--|--|---------------------------------------|------------|
| Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 150V_{RMS}$ for rated mains voltage $\leq 300V_{RMS}$ for rated mains voltage $\leq 450V_{RMS}$ for rated mains voltage $\leq 600V_{RMS}$ for rated mains voltage $\leq 1000V_{RMS}$ | | I – IV I – IV I – III I – III | I – IV I – IV I – III I – III | I – IV I – IV I – IV I – III | |
| Climatic Classification | | 55/105/21 | | | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | | | |
| Maximum Working Insulation Voltage | V_{IORM} | 567 | 891 | 1140 | V_{peak} |
| Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC | V_{PR} | 1063 | 1670 | 2137 | V_{peak} |
| Input to Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10$ sec, Partial Discharge < 5 pC | V_{PR} | 907 | 1426 | 1824 | V_{peak} |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec) | V_{IOTM} | 6000 | 6000 | 8000 | V_{peak} |
| Safety-limiting Values – maximum values allowed in the event of a failure | | | | | |
| Case Temperature | T_S | 175 | | | °C |
| Input Current | $I_{S, INPUT}$ | 230 | | | mA |
| Output Power | $P_{S, OUTPUT}$ | 600 | | | mW |
| Insulation Resistance at $T_S, V_{IO} = 500V$ | R_S | $>10^9$ | | | Ω |

- a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under the Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5), for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

| Parameter | Symbol | ACPL-M483 | ACPL-P483 | ACPL-W483 | Unit | Condition |
|--|--------|-----------|-----------|-----------|------|--|
| Minimum External Air Gap (External Clearance) | L(101) | 5.0 | 7.0 | 8.0 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 5.0 | 8.0 | 8.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | | | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | | | V | DIN IEC 112/VDE 0303 Part 1. |
| Isolation Group | | IIIa | | | | Material Group (DIN VDE 0110, 1/89, Table 1). |

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Note |
|--|----------------------------|------|-----------|---------|------|
| Storage Temperature | T_S | -55 | +125 | °C | |
| Operating Temperature | T_A | -40 | +105 | °C | |
| Average Input Current | $I_{F(AVG)}$ | | 10 | mA | |
| Peak Transient Input Current ($<1 \mu s$ pulse width, 300 pps) ($<200 \mu s$ pulse width, $<1\%$ duty cycle) | $I_{F(TRAN)}$ | | 1.0 40 | A mA | |
| Reverse Input Voltage | V_R | | 5 | V | |
| Average Output Current | I_O | | 50 | mA | |
| Supply Voltage | V_{CC} | 0 | 35 | V | |
| Output Voltage | V_O | -0.5 | 35 | V | |
| Total Package Power Dissipation (ACPL-M483) | P_T | | 145 | mW | 1 |
| Total Package Power Dissipation | P_T | | 210 | mW | 1 |
| Solder Reflow Temperature Profile | See reflow thermal profile | | | | |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Unit | Note |
|-----------------------------------|--------------|------|------|------|------|
| Power Supply Voltage ^a | V_{CC} | 4.5 | 30 | V | 2 |
| Forward Input Current (ON) | $I_{F(ON)}$ | 4 | 7 | mA | |
| Forward Input Voltage (OFF) | $V_{F(OFF)}$ | | 0.8 | V | |
| Operating Temperature | T_A | -40 | +105 | °C | |

a. Truth Table guaranteed: 4.5V to 30V

Electrical Specifications

Over recommended operating conditions $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 4.5\text{V}$ to 30V , $I_{F(ON)} = 4\text{ mA}$ to 7 mA , $V_{F(OFF)} = 0\text{V}$ to 0.8V , unless otherwise specified. All typicals at $T_A = 25^\circ\text{C}$.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---------------------------|-----------|----------------|-----------------|------|------|--|---------|------|
| Logic Low Output Voltage | V_{OL} | | | 0.3 | V | $I_{OL} = 3.5\text{ mA}$ | 1, 3 | |
| | | | | 0.5 | | $I_{OL} = 6.5\text{ mA}$ | | |
| Logic High Output Voltage | V_{OH} | $V_{CC} - 0.3$ | $V_{CC} - 0.04$ | | V | $I_{OH} = -3.5\text{ mA}$ | 2, 3, 7 | |
| | | $V_{CC} - 0.5$ | $V_{CC} - 0.07$ | | | $I_{OH} = -6.5\text{ mA}$ | | |
| Logic Low Supply Current | I_{CCL} | | 1.5 | 3.0 | mA | $V_{CC} = 5.5\text{V}$, $I_F = 7\text{ mA}$, $I_O = 0\text{ mA}$ | | |
| | | | 1.7 | 3.0 | mA | $V_{CC} = 20\text{V}$, $I_F = 7\text{ mA}$, $I_O = 0\text{ mA}$ | | |
| Logic High Supply Current | I_{CCH} | | 1.5 | 3.0 | mA | $V_{CC} = 5.5\text{V}$, $V_F = 0\text{V}$, $I_O = 0\text{ mA}$ | | |
| | | | 1.7 | 3.0 | mA | $V_{CC} = 30\text{V}$, $V_F = 0\text{V}$, $I_O = 0\text{ mA}$ | | |

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---|-------------------------|------|------|------|----------------------|--|------|------|
| Threshold Input Current Low to High | I_{FLH} | | 0.8 | 2.2 | mA | | | |
| Threshold Input Voltage High to Low | V_{FHL} | 0.8 | | | V | | | |
| Logic Low Short Circuit Output Current | I_{OSL} | 125 | 200 | | mA | $V_O = V_{CC} = 5.5V, I_F = 7\text{ mA}, V_O = \text{GND}$ | | 3 |
| | | 125 | 200 | | mA | $V_O = V_{CC} = 20V, I_F = 7\text{ mA}, V_O = \text{GND}$ | | |
| Logic High Short Circuit Output Current | I_{OSH} | | -200 | -125 | mA | $V_{CC} = 5.5V, V_F = 0V$ | | 3 |
| | | | -200 | -125 | mA | $V_{CC} = 20V, V_F = 0V$ | | |
| Input Forward Voltage | V_F | 1.3 | 1.5 | 1.7 | V | $T_A = 25^\circ\text{C}, I_F = 4\text{ mA}$ | 4 | |
| | | | | 1.85 | V | $I_F = 4\text{ mA}$ | | |
| Input Reverse Breakdown Voltage | BV_R | 5 | | | V | $I_R = 10\text{ }\mu\text{A}$ | | |
| Input Diode Temperature Coefficient | $\Delta V_F/\Delta T_A$ | | 1.7 | | mV/ $^\circ\text{C}$ | $I_F = 4\text{ mA}$ | | |
| Input Capacitance | C_{IN} | | 60 | | pF | $f = 1\text{ MHz}, V_F = 0V$ | | 4 |

Switching Specifications

Over recommended operating conditions $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 4.5V$ to $30V$, $I_{F(ON)} = 4\text{ mA}$ to 7 mA , $V_{F(OFF)} = 0V$ to $0.8V$, unless otherwise specified. All typicals at $T_A = 25^\circ\text{C}$.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|--|------------------------------------|------|------|------|-------------------|--|---------|------|
| Propagation Delay Time to Logic Low Output Level | t_{PHL} | | 75 | 120 | ns | $C_L = 100\text{ pF}, I_{F(ON)} = 4\text{ mA} \rightarrow V_F = 0V$ | 5, 6, 8 | 6 |
| | | | | 120 | | Loaded as per Figure 5 | | |
| Propagation Delay Time to Logic High Output Level | t_{PLH} | | 75 | 120 | ns | $C_L = 100\text{ pF}, V_F = 0V \rightarrow I_{F(ON)} = 4\text{ mA}$ | 5, 6, 8 | 6 |
| | | | | 120 | | Loaded as per Figure 5 | | |
| Pulse Width Distortion | $ t_{PHL} - t_{PLH} = \text{PWD}$ | | | 50 | ns | $C_L = 100\text{ pF}$ | | 9 |
| | | | | 50 | | Loaded as per Figure 5 | | |
| Propagation Delay Difference Between Any Two Parts | PDD | -100 | | 100 | ns | $C_L = 100\text{ pF}$ | | 10 |
| | | -100 | | 100 | | Loaded as per Figure 5 | | |
| Output Rise Time (10% to 90%) | t_r | | 6 | | ns | | 5 | |
| Output Fall Time (90% to 10%) | t_f | | 6 | | ns | | 5 | |
| Logic High Common Mode Transient Immunity | $ CM_H $ | 30 | | | kV/ μs | $ V_{CM} = 1000V, I_F = 4.0\text{ mA}, V_{CC} = 5V, T_A = 25^\circ\text{C}$ | 9 | 7 |
| Logic Low Common Mode Transient Immunity | $ CM_L $ | 30 | | | kV/ μs | $ V_{CM} = 1000V, V_F = 0V, V_{CC} = 5V, T_A = 25^\circ\text{C}$ | 9 | 7 |

Package Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Fig. | Note |
|---|-----------|--|-----------|------|-----------|--|------|------|
| Input-Output Momentary Withstand Voltage ^a | V_{ISO} | 3750 (ACPL-M483/P483) 5000 (ACPL-W483) | | | V_{RMS} | RH < 50%, t = 1 min. $T_A = 25^\circ C$ | | 5, 8 |
| Input-Output Resistance | R_{I-O} | | 10^{12} | | Ω | $V_{I-O} = 500V_{DC}$ | | 5 |
| Input-Output Capacitance | C_{I-O} | | 0.6 | | pF | f = 1 MHz, $V_{I-O} = 0V_{DC}$ | | 5 |

- a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

UVLO

Figure 10 and Figure 11 show typical output waveforms during Power-up and Power-down processes.

Notes:

- Derate total package power dissipation, P_T , linearly above $70^\circ C$ free-air temperature at a rate of $4.5 \text{ mW}/^\circ C$ (ACPL-P483/W483) and linearly above $85^\circ C$ free-air temperature at a rate of $0.75 \text{ mW}/^\circ C$ (ACPL-M483).
- Detector requires a V_{CC} of 4.5V or higher for stable operation as output might be unstable if V_{CC} is lower than 4.5V. Be sure to check the power ON/OFF operation other than the supply current.
- Duration of output short circuit time should not exceed $500 \mu s$.
- Input capacitance is measured between pin 1 and pin 3.
- Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
- The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
- CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, $V_O > 2.0V$. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, $V_O < 0.8V$. Note: Equal value split resistors ($R_{in}/2$) must be used at both ends of the LED.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage. $4500V_{RMS}$ for one second (leakage detection current limit, $I_{I-O} \leq 5 \mu A$). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
- Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
- The difference of t_{PLH} and t_{PHL} between any two devices under the same test condition.
- Use of a $0.1 \mu F$ bypass capacitor connected between pins V_{CC} and Ground is recommended.

Figure 1 Typical Logic Low Output Voltage vs. Temperature

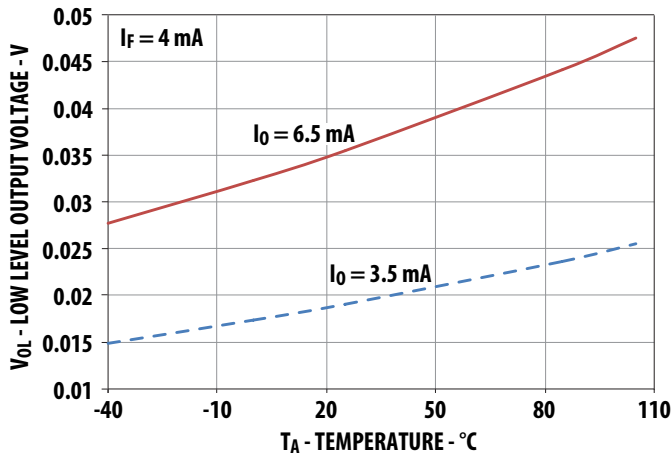


Figure 2 Typical Logic High Output Current vs. Temperature

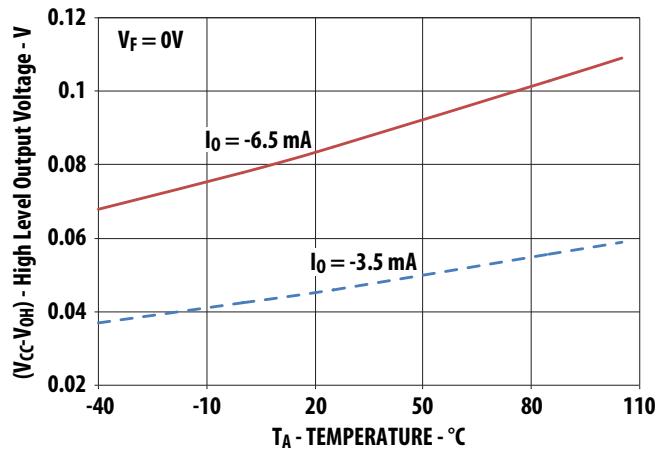


Figure 3 Typical Output Voltage vs. Forward Input Current

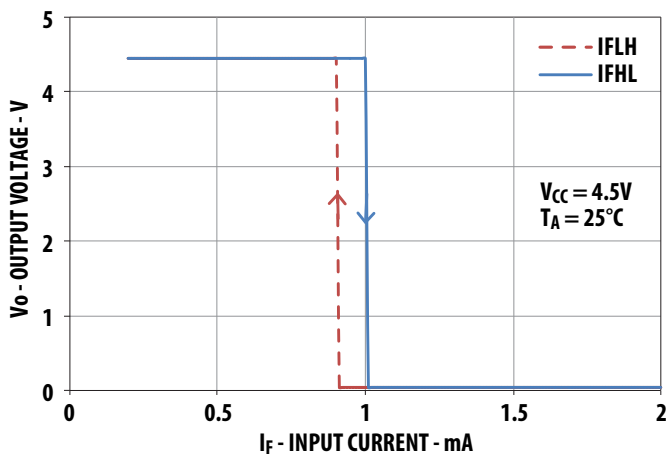


Figure 4 Typical Input Diode Forward Characteristic

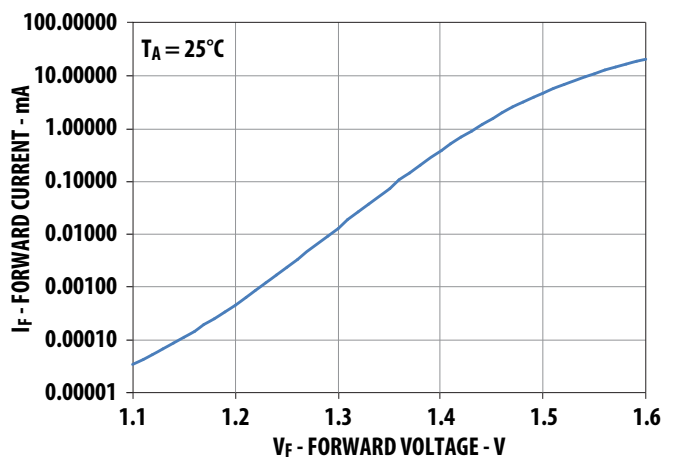


Figure 5 Test Circuit for t_{PLH} , t_{PHL} , t_r and t_f

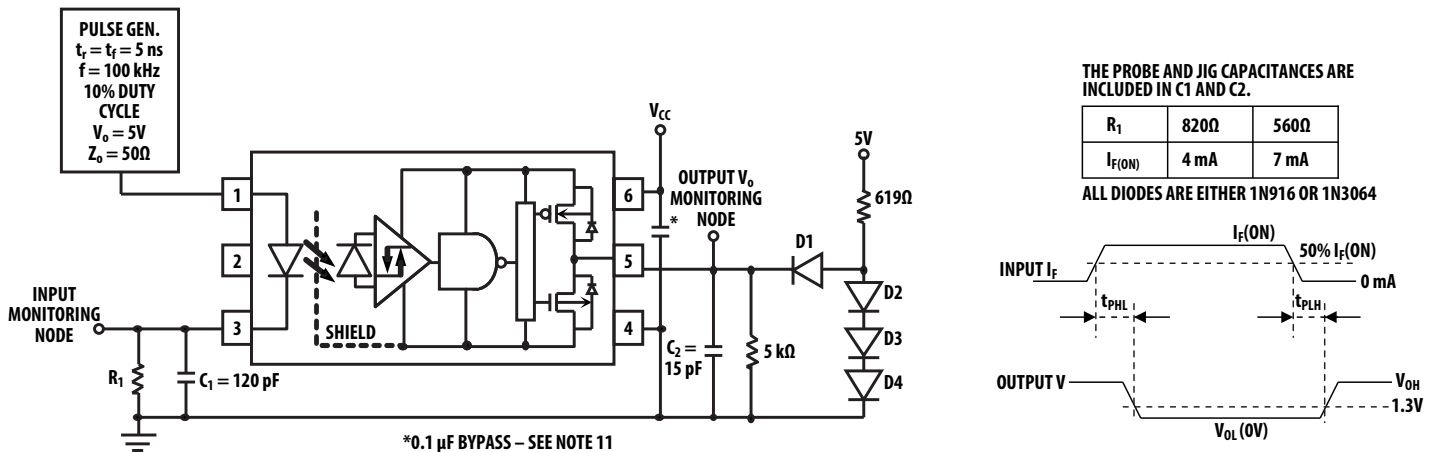


Figure 6 Typical Propagation Delays vs. Temperature

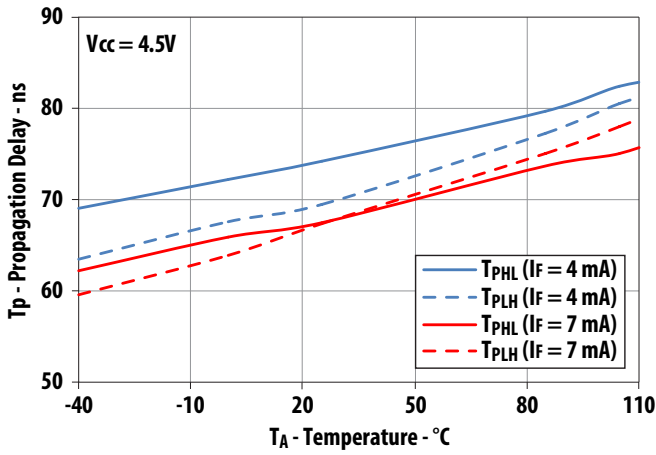


Figure 7 Typical Logic High Output Voltage vs. Supply Voltage

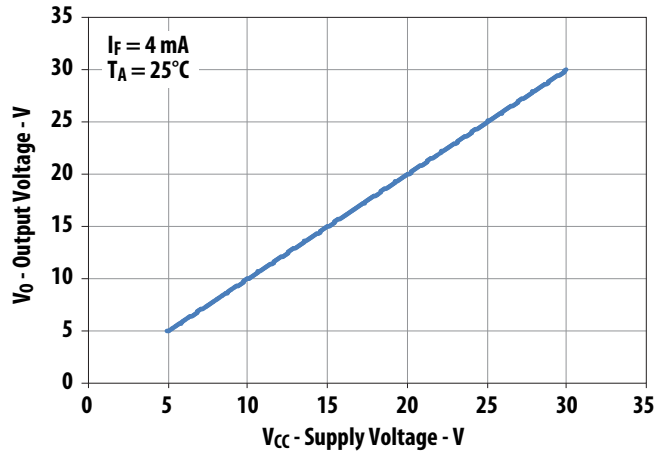


Figure 8 Typical Propagation Delay vs. Supply Voltage

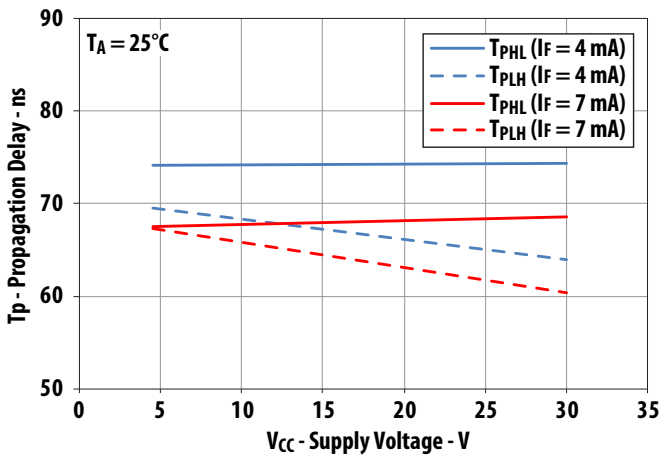


Figure 9 Test Circuit for Common Mode Transient Immunity and Typical Waveforms

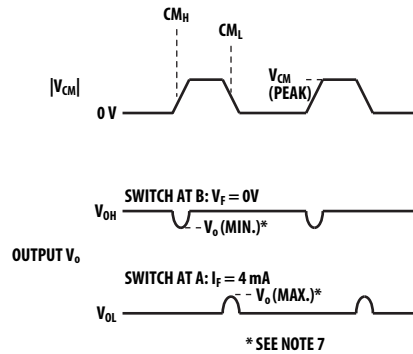
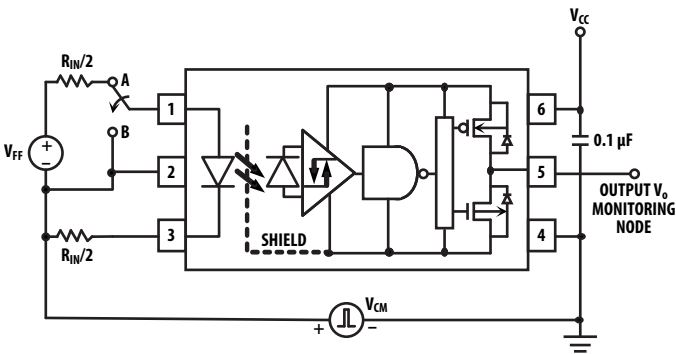


Figure 10 V_{CC} Ramp When LED ON

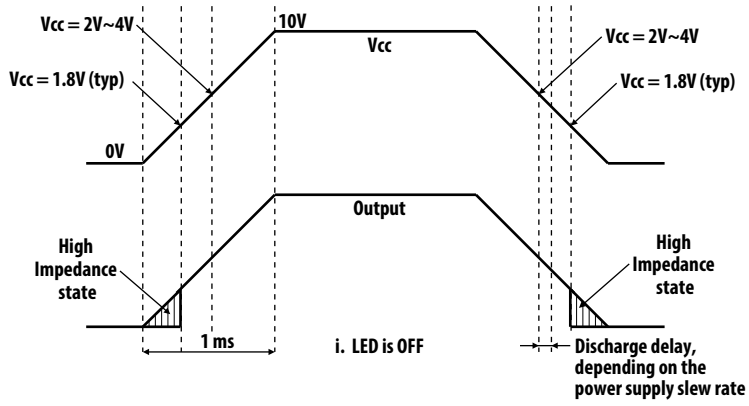
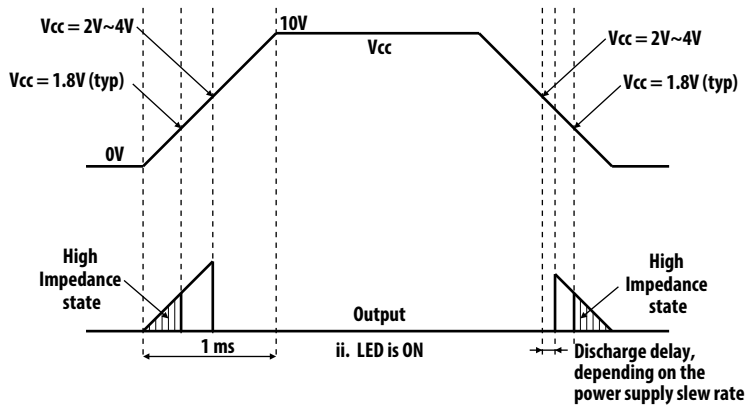


Figure 11 V_{CC} Ramp When LED OFF



Thermal Model for ACPL-M483 SO-5 Package Optocoupler

Definitions

- R_{11} : Junction to Ambient Thermal Resistance of LED due to heating of LED
- R_{12} : Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)
- R_{21} : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.
- R_{22} : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).
- P_1 : Power dissipation of LED (W).
- P_2 : Power dissipation of Detector/Output IC (W).
- T_1 : Junction temperature of LED (°C).
- T_2 : Junction temperature of Detector (°C).
- T_a : Ambient temperature.
- ΔT_1 : Temperature difference between LED junction and ambient (°C).
- ΔT_2 : Temperature difference between Detector junction and ambient.
- Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air

Description

This thermal model assumes that an 5-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a \quad (1)$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a \quad (2)$$

| JEDEC Specifications | R11 | R12, R21 | R22 |
|----------------------|-----|----------|-----|
| Low K board | 191 | 77, 91 | 99 |
| High K board | 126 | 26, 35 | 51 |

Note: Maximum junction temperature for above parts: 125°C.

Thermal Model for ACPL-P483/W483 SO-6 Package Optocoupler

Definitions

- R_{11} : Junction to Ambient Thermal Resistance of LED due to heating of LED
- R_{12} : Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)
- R_{21} : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.
- R_{22} : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).
- P_1 : Power dissipation of LED (W).
- P_2 : Power dissipation of Detector/Output IC (W).
- T_1 : Junction temperature of LED (°C).
- T_2 : Junction temperature of Detector (°C).
- T_a : Ambient temperature.
- ΔT_1 : Temperature difference between LED junction and ambient (°C).
- ΔT_2 : Temperature difference between Detector junction and ambient.
- Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air

Description

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a \quad (1)$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a \quad (2)$$

| JEDEC Specifications | R11 | R12, R21 | R22 |
|----------------------|-----|----------|-----|
| Low K board | 167 | 64, 81 | 89 |
| High K board | 117 | 31, 39 | 54 |

Note: Maximum junction temperature for above parts: 125°C.