

# ACPL-M71T and ACPL-M72T

High Speed, Low Power Digital Optocouplers  
with R<sup>2</sup>Coupler™ Isolation and AEC-Q100 Grade 1 Qualification



## Data Sheet

### Description

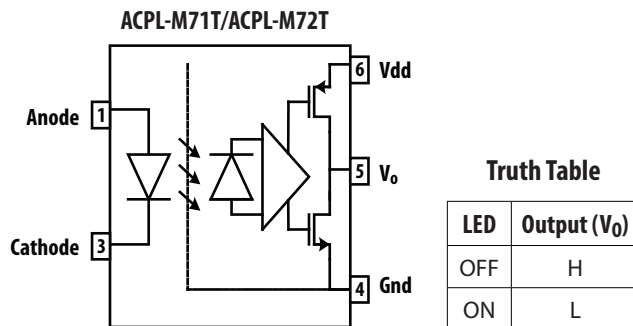
The Avago ACPL-M71T and ACPL-M72T are high temperature, digital CMOS optocouplers in SOIC-5 packages. Suitable for hybrid and electric vehicle applications, the optocouplers use the latest CMOS IC technology to achieve outstanding performance and very low power consumption. All devices are AEC-Q100 compliant and operate over the -40°C to 125 °C temperature range.

The ACPL-M71T uses a high speed LED, and the ACPL-M72T uses a low current LED for lower power dissipation. The high speed ACPL-M71T featuring a 35 ns maximum propagation delay ( $I_F = 10$  mA). The ACPL-M72T optocoupler features very low power. With a low 4 mA LED drive current, ACPL-M72T typical propagation delay is 60 ns.

Each digital optocoupler has a CMOS detector IC, an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Avago R<sup>2</sup>Coupler isolation products provide the reinforced insulation and reliability needed for critical in automotive and high temperature industrial applications

### Functional Block Diagram



Note: A 0.1  $\mu$ F bypass capacitor must be connected between pins 4 and 6.

### Features

- 5 V CMOS compatible
- Common-Mode Rejection 40kV/ $\mu$ s @  $V_{CM} = 1000V$ :
- Wide automotive temperature range: -40°C to 125°C
- Low propagation delay :
  - High Speed ACPL-M71T: 26ns @  $I_F = 10$  mA (Typical)
  - Low Power ACPL-M72T: 60ns @  $I_F = 4$  mA (Typical)
- Worldwide safety approval:
  - UL 1577 recognized, 4000 Vrms / 1 min
  - CSA approved
  - IEC/EN/DIN EN 60747-5-5
- Qualified to AEC-Q100 Grade 1 test guidelines

### Applications

- Automotive CANBus communications interface
- Automotive isolated high speed gate drivers for IGBTs and Power MOSFETs
- High temperature digital signal isolation
- Microcontroller interface
- Digital isolation for A/D and D/A conversion

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Ordering Information

Part Number	Option	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	(RoHS) Compliant					
ACPL-M71T	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-M72T	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

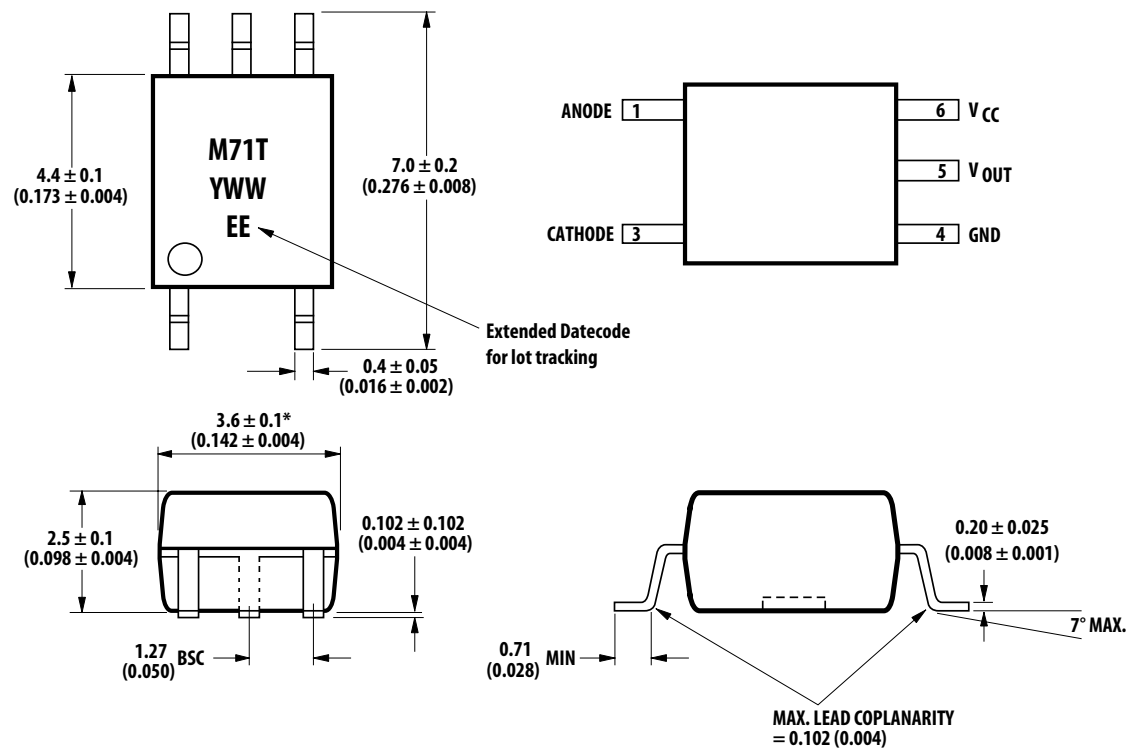
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

For example, the part number ACPL-M71T-500E describes a device with a surface mount SOIC-5 package; delivered in Tape and Reel with 1500 parts per reel; and full RoHS compliance.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Dimensions

### ACPL-M71T / ACPL-M72T (JEDEC MO-155 Package)

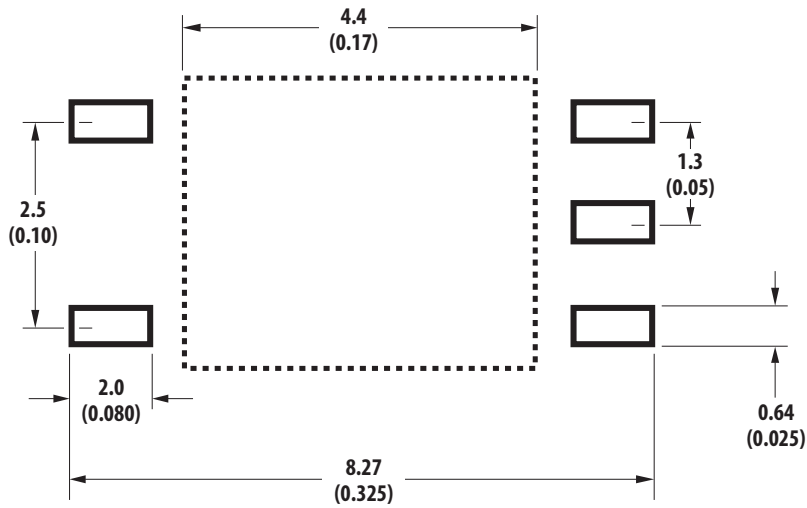


DIMENSIONS IN MILLIMETERS (INCHES)

\* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

## Land Pattern Recommendation



DIMENSION IN MILLIMETERS (INCHES)

## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used.

## Regulatory Information

The ACPL-M71T and ACPL-M72T are approved by the following organizations:

### UL

Approved under UL 1577, component recognition program up to  $V_{ISO} = 4000 V_{RMS}$ .

### CSA

Approved under CSA Component Acceptance Notice #5.

### IEC/EN/DIN EN 60747-5-5

IEC 60747-5-5:

EN 60747-5-5:

DIN EN 60747-5-5:

## Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	>5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	>5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0109)

## IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics

Description	Symbol	ACPL-M71T/ ACPL-M72T	Units
Maximum Working Insulation Voltage	$V_{IORM}$	567	$V_{PEAK}$
Input to Output Test Voltage, Method b <sup>†</sup> $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC	$V_{PR}$	1063	$V_{PEAK}$
Input to Output Test Voltage, Method a <sup>†</sup> $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial Discharge < 5 pC	$V_{PR}$	907	$V_{PEAK}$
Highest Allowable Overvoltage <sup>†</sup> (Transient Overvoltage, $t_{ini} = 60$ sec)	$V_{IOTM}$	6000	$V_{PEAK}$
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Thermal Derating curve, Figure 11.)			
Case Temperature	$T_s$	150	°C
Input Current	$I_{s, INPUT}$	150	mA
Output Power	$P_{s, OUTPUT}$	600	mW
Insulation Resistance at $T_s$ , $V_{IO} = 500$ V	$R_{IO}$	$\geq 10^9$	$\Omega$

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Condition
Storage Temperature	$T_S$	-55	+130	°C	
Ambient Operating Temperature <sup>[1]</sup>	$T_A$	-40	+125	°C	
Supply Voltages	$V_{DD}$	0	6.5	V	
Output Voltage	$V_O$	-0.5	$V_{DD} + 0.5$	V	
Average Forward Input Current	$I_F$	-	20.0	mA	
Peak Transient Input Current ( $I_F$ at 1 $\mu$ s pulse width, <10% duty cycle)	$I_{F(TRAN)}$		1 80	A mA	<1 $\mu$ s Pulse Width, 300 pps <1 $\mu$ s Pulse Width, <10%Duty Cycle
Reverse Input Voltage	$V_R$	-	5	V	
Input Power Dissipation	$P_I$		40	mW	
Output Power Dissipation	$P_O$		30	mW	
Lead Solder Temperature			260 °C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile			See Solder Reflow Temperature Profile Section		

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	$T_A$	-40	+125	°C
Supply Voltages	$V_{DD}$	3.0	5.5	V
Forward Input Current	$I_{F(ON)}$	4.0	15	mA
Forward Off State Voltage	$V_{F(OFF)}$		0.8	V
Input Threshold Current	$I_{TH}$		3.5	mA

## Electrical Specifications

Over recommended temperature ( $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ . All typical specifications are at  $T_A = +25^{\circ}\text{C}$ ,  $V_{DD} = +5\text{V}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig
Input Capacitance	$C_{IN}$		90		pF		
Input Reverse Breakdown Voltage	$BV_R$	5.0			V	$I_R = 10\ \mu\text{A}$	
Logic High Output Voltage	$V_{OH}$	$V_{DD}-0.6$			V	$I_{OH} = -4\text{mA}$	4
Logic Low Output Voltage	$V_{OL}$			0.6	V	$I_{OL} = 4\text{mA}$	3
Logic Low Output Supply Current	$I_{DDL}$		0.9	1.5	mA		
Logic High Output Supply Current	$I_{DDH}$		0.9	1.5	mA		
LED Forward Voltage	$V_f$	1.45	1.5	1.75	V	$I_F = 10\text{mA}$ , $T_A = 25^{\circ}\text{C}$	
		1.25	1.5	1.85	V	$I_F = 10\text{mA}$ , $T_A = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$	
Vf Temperature Coefficient			-1.5		mV/ $^{\circ}\text{C}$		

## ACPL-M71T High Speed Mode Switching Specifications

Over recommended temperature ( $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ . All typical specifications are at  $T_A = +25^{\circ}\text{C}$ ,  $V_{DD} = 5\text{V}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig	Note
Propagation Delay Time to Logic Low Output <sup>[1]</sup>	$t_{PHL}$		26	35	ns	$V_{in} = 4.5\text{V}-5.5\text{V}$ , $R_{in} = 390\Omega \pm 5\%$ , $C_{in} = 100\text{pF}$ , $C_L = 15\text{pF}$	5,6,11	1,2,3
Propagation Delay Time to Logic High Output <sup>[1]</sup>	$t_{PLH}$		26	35	ns			
Pulse Width Distortion <sup>[2]</sup>	PWD		0	12	ns			
Propagation Delay Skew <sup>[3]</sup>	$t_{PSK}$			15	ns			
Output Rise Time (10% – 90%)	$t_R$		10		ns			
Output Fall Time (90% - 10%)	$t_F$		10		ns			
Common Mode Transient Immunity at Logic High Output <sup>[4]</sup>	$ CM_H $	15	25		kV/ $\mu\text{s}$	$V_{in} = 0\text{V}$ $R_{in} = 390\Omega \pm 5\%$ , $C_{in} = 100\text{pF}$ , $V_{cm} = 1000\text{V}$ , $T_A = 25^{\circ}\text{C}$	12	4
Common Mode Transient Immunity at Logic High Output <sup>[5]</sup>	$ CM_L $	15	25		kV/ $\mu\text{s}$	$V_{in} = 4.5\text{V}-5.5\text{V}$ , $R_{in} = 390\Omega \pm 5\%$ , $C_{in} = 100\text{pF}$ , $V_{cm} = 1000\text{V}$ , $T_A = 25^{\circ}\text{C}$	13	5

## ACPL-M72T Low Power Mode Switching Specifications

Over recommended temperature (-40°C to +125°C),  $3.0V \leq V_{DD} \leq 5.5V$ . All typical specifications at +25°C and  $V_{DD} = 5V$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig	Note
Propagation Delay Time to Logic Low Output <sup>[1]</sup>	$t_{PHL}$		60	100	ns	$I_F=4mA, C_L=15pF$	7,8, 9,10, 14	1,2,3
Propagation Delay Time to Logic High Output <sup>[1]</sup>	$t_{PLH}$		35	100	ns			
Pulse Width Distortion <sup>[2]</sup>	PWD		25	50	ns			
Propagation Delay Skew <sup>[3]</sup>	$t_{PSK}$			60	ns			
Output Rise Time (10% – 90%)	$t_R$		10		ns			
Output Fall Time (90% - 10%)	$t_F$		10		ns			
Common Mode Transient Immunity at Logic High Output <sup>[4]</sup>	$ CM_H $	25	40		kV/ $\mu s$	Using Avago LED Driving Circuit, $V_{IN}=0V, R_1=350\Omega \pm 5\%, R_2=350\Omega \pm 5\%, V_{CM}=1000V, T_A=25^\circ C$	15	4
Common Mode Transient Immunity at Logic High Output <sup>[5]</sup>	$ CM_L $	25	40		kV/ $\mu s$	Using Avago LED Driving Circuit, $V_{IN}=4.5-5.5V, R_1=350\Omega \pm 5\%, R_2=350\Omega, V_{CM}=1000V, T_A=25^\circ C$	16	5

## Package Characteristics

All Typical at  $T_A = 25^\circ C$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage	$V_{ISO}$	4000			$V_{rms}$	$RH \leq 50\%, t = 1 \text{ min.}, T_A = 25^\circ C$
Input-Output Resistance	$R_{I-O}$		$10^{14}$		$\Omega$	$V_{I-O} = 500 \text{ V dc}$
Input-Output Capacitance	$C_{I-O}$		0.6		pF	$f = 1 \text{ MHz}, T_A = 25^\circ C$

Notes:

- $t_{PHL}$  propagation delay is measured from the 50% ( $V_{in}$  or  $I_f$ ) on the rising edge of the input pulse to 0.8V on the falling edge of the  $V_O$  signal.  $t_{PLH}$  propagation delay is measured from the 50% ( $V_{in}$  or  $I_f$ ) on the falling edge of the input pulse to the 80% level of the rising edge of the  $V_O$  signal.
- PWD is defined as  $|t_{PHL} - t_{PLH}|$ .
- $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature within the recommended operating conditions.
- $CM_H$  is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- $CM_L$  is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

## Performance Plots

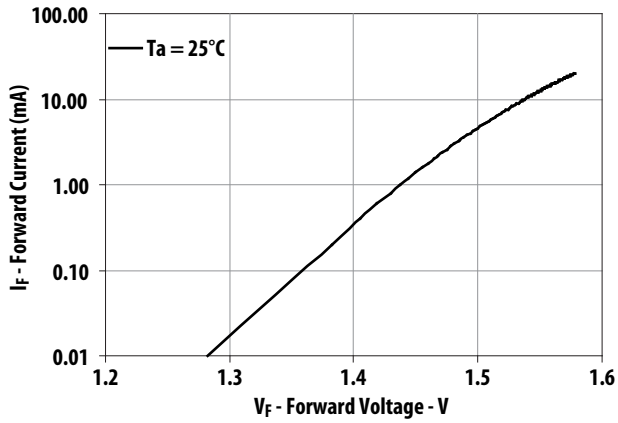


Figure 1. Typical Diode Input Forward Current Characteristic

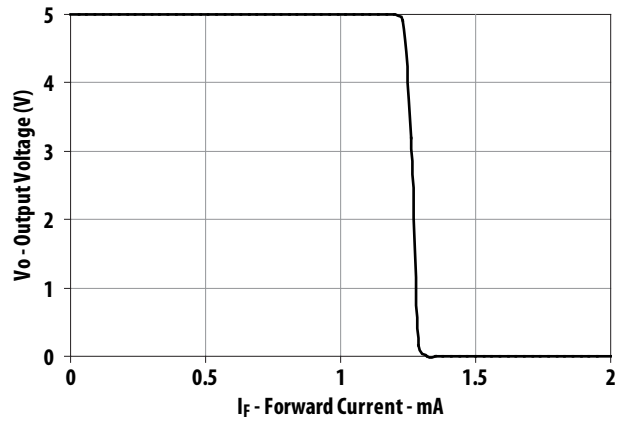


Figure 2. Typical Output Voltage vs Input Forward Current

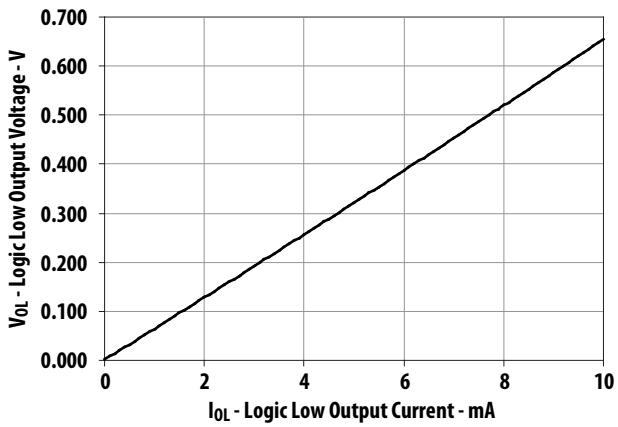


Figure 3. Typical Logic Low Output Voltage vs Logic Low Output Current

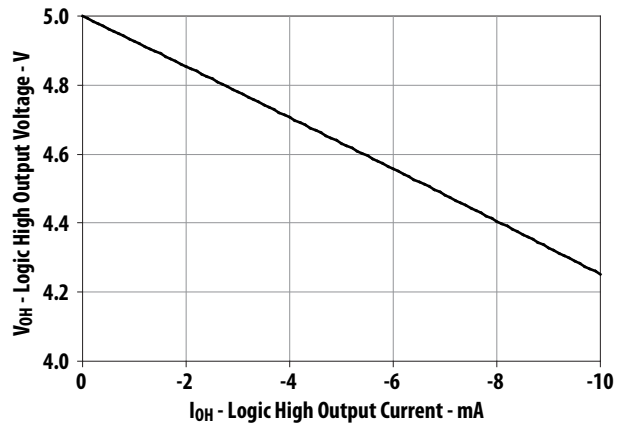


Figure 4. Typical Logic High Output Voltage vs Logic High Output Current

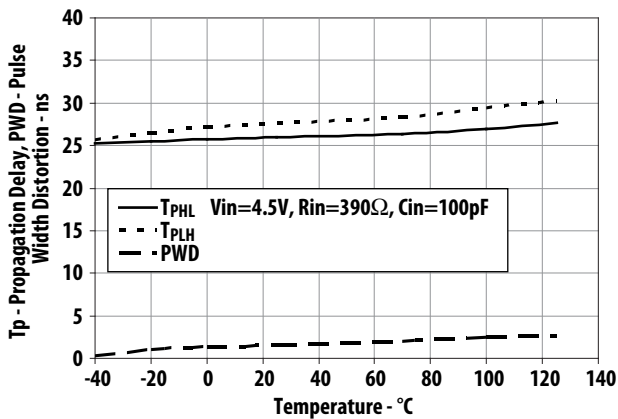


Figure 5. ACPL-M71T (High Speed) Typical Propagation Delay vs Temperature

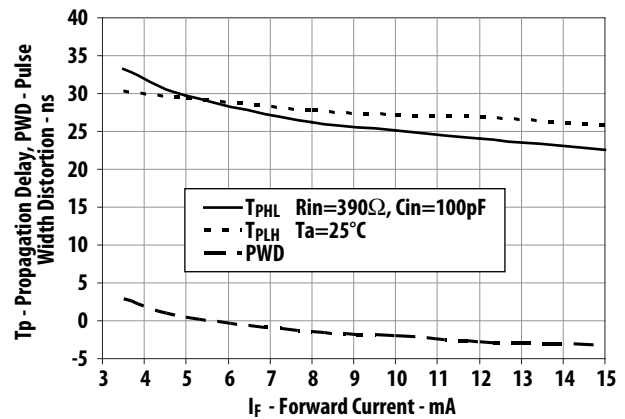


Figure 6. ACPL-M71T (High Speed) Typical Propagation Delay vs Forward Current - I<sub>F</sub>



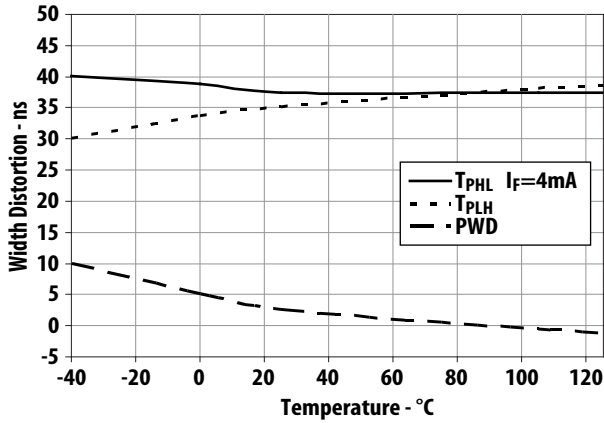


Figure 7. ACPL-M72T (5V) Typical Propagation Delay vs Temperature

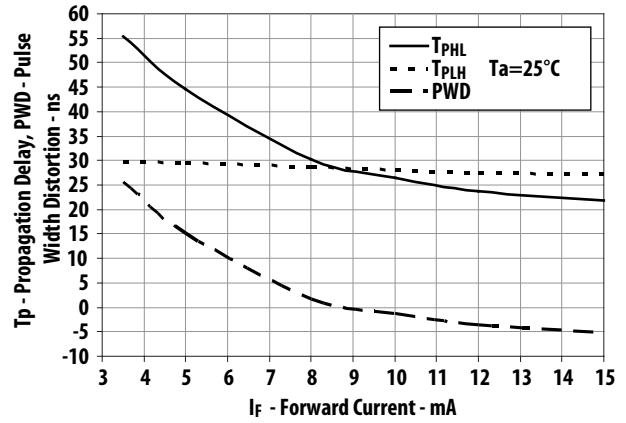


Figure 8. ACPL-M72T (5V) Typical Propagation Delay vs Forward Current -  $I_F$

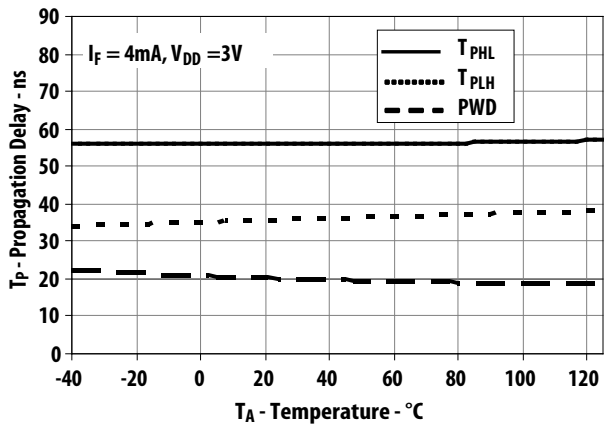


Figure 9. ACPL-M72T (3V) Typical Propagation Delay vs Temperature

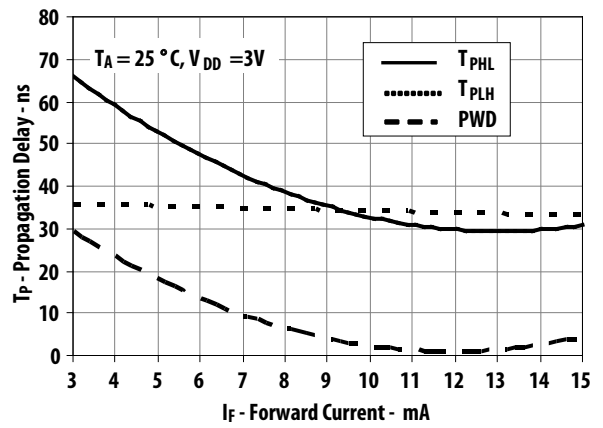


Figure 10. ACPL-M72T (3V) Typical Propagation Delay vs Input Forward Current

## Test Circuit Diagrams

### ACPL-M71T High Speed Mode:

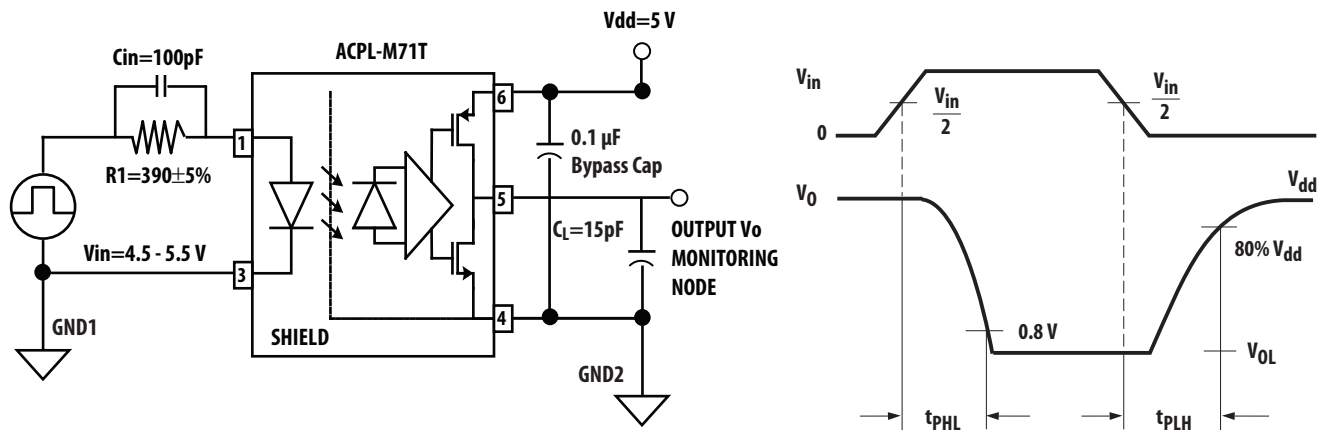


Figure 11. High Speed Mode Test Circuit and Typical Waveform

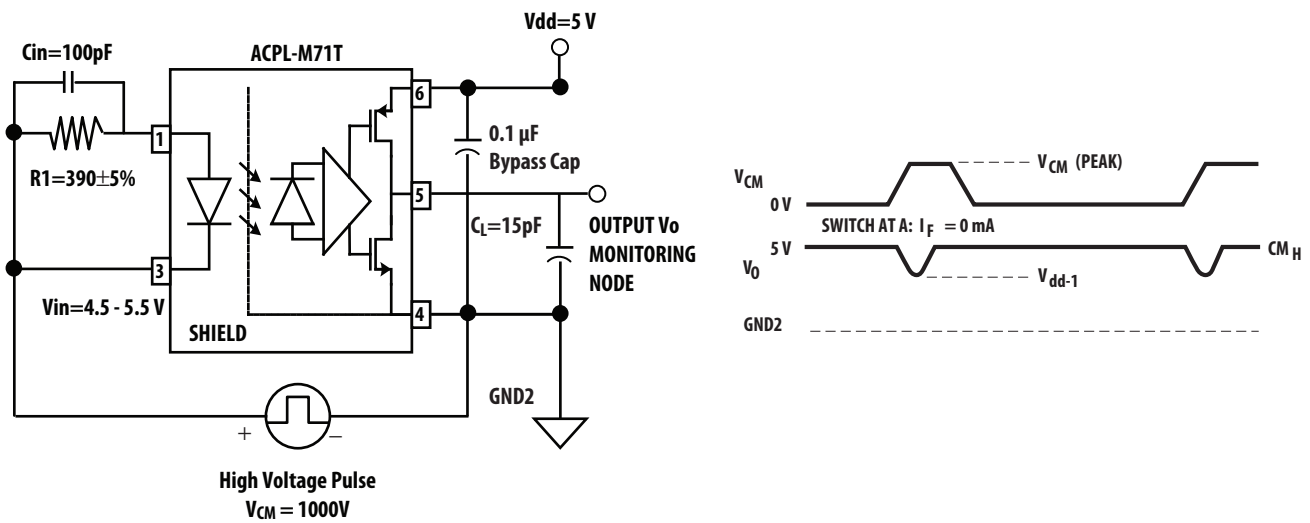


Figure 12. High Speed Mode CMH Test Circuit and Typical Waveform

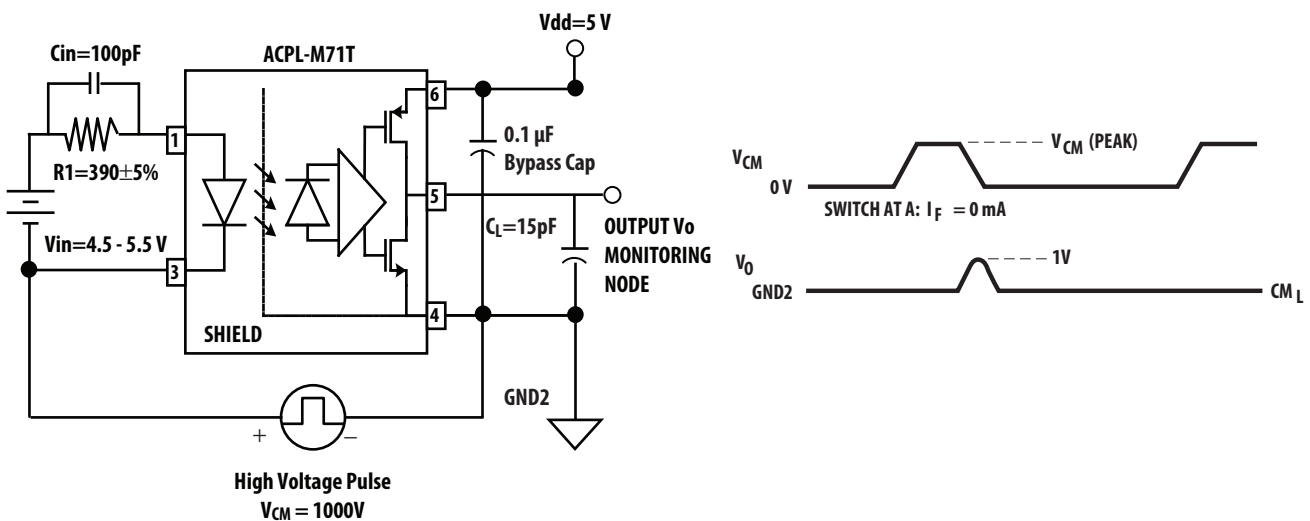


Figure 13. High Speed Mode CML Test Circuit and Typical Waveform

**ACPL-M72T Low Power Mode:**

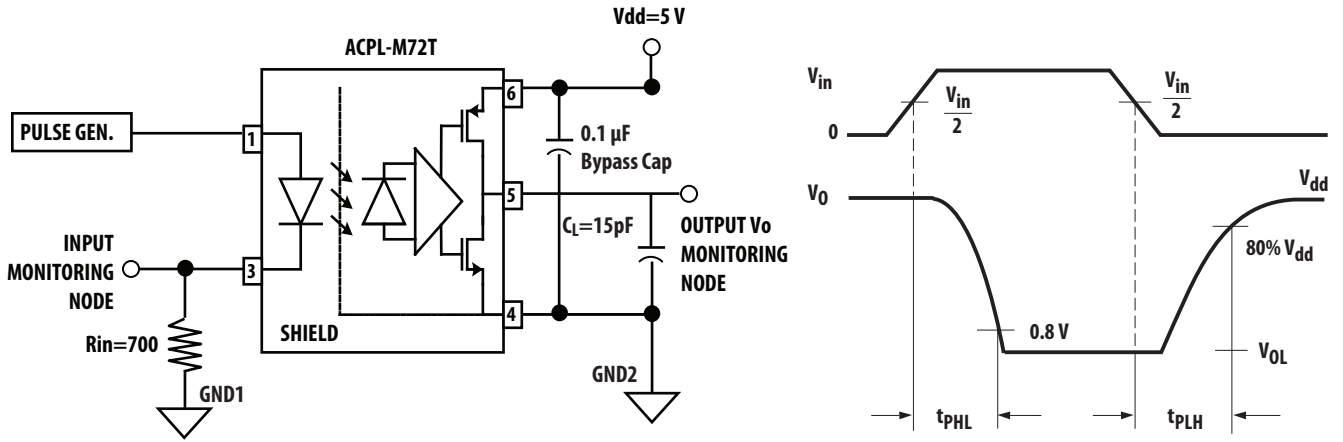


Figure 14. Low Power Mode Switching Test Circuit and Typical Waveform

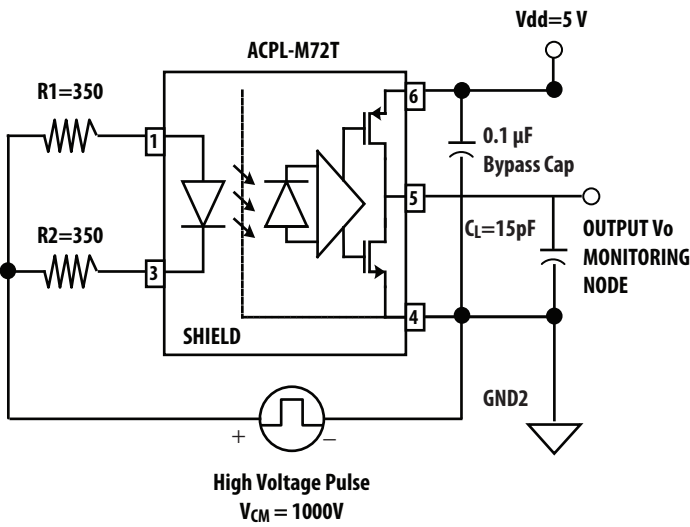


Figure 15. Low Power Mode High CMR, CMH Test Circuit

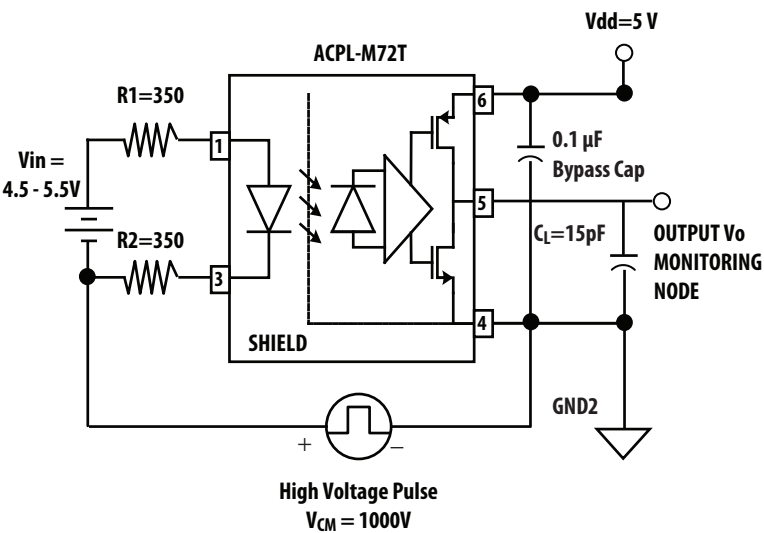


Figure 16. Low Power Mode High CMR, CML Test Circuit