

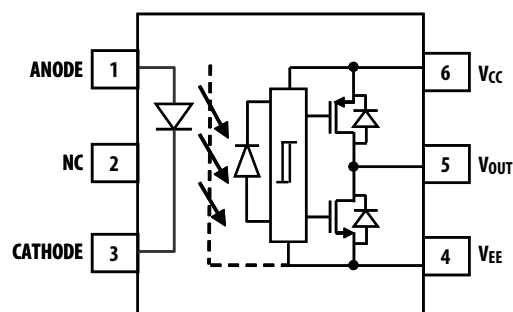
## 3.0 Amp Output Current IGBT Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched S06

### Data Sheet

#### Description

The ACPL-P341/W341 contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving IGBT with ratings up to 1200V/50A. For IGBTs with higher ratings, this optocoupler can be used to drive a discrete power stage which drives the IGBT gate. The ACPL-P341 and ACPL-W341 have the highest insulation voltage of  $V_{IORM} = 891V_{peak}$  and  $V_{IORM} = 1140V_{peak}$  respectively in the IEC/EN/DIN EN 60747-5-5.

#### Functional Diagram



Note: A 1  $\mu$ F bypass capacitor must be connected between pins  $V_{CC}$  and  $V_{EE}$ .

#### Features

- 3.0A maximum peak output current
- 2.5A minimum peak output current
- Rail-to-rail output voltage
- 200 ns maximum propagation delay
- 100 ns maximum propagation delay difference
- LED current input with hysteresis
- 35 kV/ $\mu$ s minimum Common Mode Rejection (CMR) at  $V_{CM} = 1500V$
- $I_{CC} = 3.0$  mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating  $V_{CC}$  Range: 15V to 30V
- Industrial temperature range:  $-40^{\circ}C$  to  $+105^{\circ}C$
- Safety Approval:
  - UL Recognized 3750V/5000V<sub>RMS</sub> for 1 min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5  $V_{IORM} = 891V/1140V_{peak}$

#### Applications

- IGBT/MOSFET gate drive
- AC and Brushless DC motor drives
- Renewable energy inverters
- Industrial inverters
- Switching power supplies

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

## Truth Table

LED	$V_{CC} - V_{EE}$ POSITIVE GOING (TURN-ON)	$V_{CC} - V_{EE}$ NEGATIVE GOING (TURN-OFF)	$V_O$
OFF	0 – 30 V	0 – 30 V	LOW
ON	0 – 12.1 V	0 – 11.1 V	LOW
ON	12.1 – 13.5 V	11.1 – 12.4 V	TRANSITION
ON	13.5 – 30 V	12.4 – 30 V	HIGH

## Ordering Information

ACPL-P341 is UL Recognized with 3750V<sub>RMS</sub> for 1 minute per UL1577. ACPL-W341 is UL Recognized with 5000V<sub>RMS</sub> for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-P341	-000E	Stretched SO6	X			100 per tube
ACPL-W341	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P341-560E to order product of Stretched SO6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACPL-W341-000E to order product of Stretched SO6 Surface Mount package in Tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.



## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

The ACPL-P341/W341 is approved by the following organizations:

<b>UL</b>	Recognized under UL 1577, component recognition program up to $V_{ISO} = 3750V_{RMS}$ (ACPL-P341) and $V_{ISO} = 5000V_{RMS}$ (ACPL-W341).
<b>CSA</b>	CSA Component Acceptance Notice #5, File CA 88324
<b>IEC/EN/DIN EN 60747-5-5 (Option 060 Only)</b>	Maximum Working Insulation Voltage $V_{IORM} = 891V_{peak}$ (ACPL-P341) and $V_{IORM} = 1140V_{peak}$ (ACPL-W341)

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics\* (Option 060)

Description	Symbol	ACPL-P341 Option 060	ACPL-W341 Option 060	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 150V_{RMS}$ for rated mains voltage $\leq 300V_{RMS}$ for rated mains voltage $\leq 450V_{RMS}$ for rated mains voltage $\leq 600V_{RMS}$ for rated mains voltage $\leq 1000V_{RMS}$		I – IV I – IV I – III I – III	I – IV I – IV I – IV I – IV I – III	
Climatic Classification		40/105/21	40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	$V_{IORM}$	891	1,140	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1,671	2,137	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1,426	1,824	$V_{peak}$
Highest Allowable Overvoltage* (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	6,000	8,000	$V_{peak}$
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	$T_S$	175	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at $T_S$ , $V_{IO} = 500V$	$R_S$	$>10^9$	$>10^9$	$\Omega$

\*Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Broadcom Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

Note: These optocouplers are suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

## Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P341	ACPL-W341	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIla	IIla		Material Group (DIN VDE 0110, 1/89, Table 1)

Note: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	$T_S$	-55	+125	°C	
Operating Temperature	$T_A$	-40	+105	°C	
Output IC Junction Temperature	$T_J$		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 $\mu$ s pulse width, 300 pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	$V_R$		5	V	
High Peak Output Current	$I_{OH(PEAK)}$		3.0	A	2
Low Peak Output Current	$I_{OL(PEAK)}$		3.0	A	2
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	35	V	
Input Current (Rise/Fall Time)	$t_{r(IN)}/t_{f(IN)}$		500	ns	
Output Voltage	$V_{O(PEAK)}$	-0.5	$V_{CC}$	V	
Output IC Power Dissipation	$P_O$		700	mW	3
Total Power Dissipation	$P_T$		745	mW	4
Lead Solder Temperature		260°C for 10 sec., 1.6 mm below seating plane			

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature	$T_A$	-40	+105	°C	
Output Supply Voltage	$(V_{CC} - V_{EE})$	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	+0.8	V	

## Electrical Specifications (DC)

All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 30\text{V}$ ,  $V_{EE} = \text{Ground}$ . All minimum and maximum specifications are at recommended operating conditions ( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $I_{F(\text{ON})} = 7\text{ mA}$  to  $+16\text{ mA}$ ,  $V_{F(\text{OFF})} = -3.6\text{V}$  to  $+0.8\text{V}$ ,  $V_{EE} = \text{Ground}$ ,  $V_{CC} = 15\text{V}$  to  $30\text{V}$ ), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
High Level Peak Output Current	$I_{OH}$	-1.0	-2.3		A	$V_O = V_{CC} - 4\text{V}$	14	5
		-2.5			A	$V_{CC} - V_O \leq 15\text{V}$		6
Low Level Peak Output Current	$I_{OL}$	1.0	3.0		A	$V_O = V_{EE} + 2.5\text{V}$	15	5
		2.5			A	$V_O - V_{EE} \leq 15\text{V}$		7
High Output Transistor RDS(ON)	$R_{DS,OH}$		1.7	3.0	$\Omega$	$I_{OH} = -2.5\text{A}$		8
Low Output Transistor RDS(ON)	$R_{DS,OL}$		0.8	1.8	$\Omega$	$I_{OL} = 2.5\text{A}$		8
High Level Output Voltage	$V_{OH}$	$V_{CC} - 0.3$	$V_{CC} - 0.2$		V	$I_O = -100\text{ mA}$	2, 16	9, 10
High Level Output Voltage	$V_{OH}$		$V_{CC}$		V	$I_O = 0\text{ mA}$ , $I_F = 10\text{ mA}$	1	
Low Level Output Voltage	$V_{OL}$		0.1	0.2	V	$I_O = 100\text{ mA}$	5, 17	
High Level Supply Current	$I_{CCH}$		1.9	3.0	mA	$R_g = 10\Omega$ , $C_g = 25\text{ nF}$ , $I_F = 10\text{ mA}$	4, 5	
Low Level Supply Current	$I_{CCL}$		1.9	3.0	mA	$R_g = 10\Omega$ , $C_g = 25\text{ nF}$ , $V_F = 0\text{V}$		
Threshold Input Current Low to High	$I_{FLH}$		1.5	4.0	mA	$R_g = 10\Omega$ , $C_g = 25\text{ nF}$ , $V_O > 5\text{V}$	6, 7, 8	
Threshold Input Voltage High to Low	$V_{FHL}$	0.8			V			
Input Forward Voltage	$V_F$	1.2	1.55	1.95	V	$I_F = 10\text{ mA}$	13	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$		-1.7		mV/ $^\circ\text{C}$	$I_F = 10\text{ mA}$		
Input Reverse Breakdown Voltage	$BV_R$	5			V	$I_R = 100\text{ }\mu\text{A}$		
Input Capacitance	$C_{IN}$		70		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{V}$		
UVLO Threshold	$V_{UVLO+}$	12.1	12.8	13.5	V	$V_O > 5\text{V}$ , $I_F = 10\text{ mA}$	19	
	$V_{UVLO-}$	11.1	11.8	12.4				
UVLO Hysteresis	$UVLO_{HYS}$		1.0		V			

## Switching Specifications (AC)

Unless otherwise noted, all typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 30\text{V}$ ,  $V_{EE} = \text{Ground}$ ; all minimum and maximum specifications are at recommended operating conditions ( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $I_F(\text{ON}) = 7\text{ mA}$  to  $16\text{ mA}$ ,  $V_F(\text{OFF}) = -3.6\text{V}$  to  $+0.8\text{V}$ ,  $V_{EE} = \text{Ground}$ ,  $V_{CC} = 15\text{V}$  to  $30\text{V}$ ).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	$t_{PLH}$	50	98	200	ns	$R_g = 10\Omega$ , $C_g = 25\text{ nF}$ , $f = 20\text{ kHz}$ , Duty Cycle = 50%, $I_F = 7\text{ mA}$ to $16\text{ mA}$ , $V_{CC} = 15\text{V}$ to $30\text{V}$	8, 9, 10, 11, 12, 20	
Propagation Delay Time to Low Output Level	$t_{PHL}$	50	95	200	ns			
Pulse Width Distortion	PWD		22	70	ns			11
Propagation Delay Difference Between Any Two Parts	PDD ( $t_{PHL} - t_{PLH}$ )	-100		+100	ns			27, 28
Rise Time	$t_R$		43		ns	$V_{CC} = 30\text{ V}$	20	
Fall Time	$t_F$		40		ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	35	50		kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $I_F = 10\text{ mA}$ , $V_{CC} = 30\text{V}$ , $V_{CM} = 1500\text{V}$ with split resistors	21	13, 14
Output Low Level Common Mode Transient Immunity	$ CM_L $	35	50		kV/ $\mu\text{s}$			$T_A = 25^\circ\text{C}$ , $V_F = 0\text{V}$ , $V_{CC} = 30\text{V}$ , $V_{CM} = 1500\text{V}$ with split resistors

## Package Characteristics

All typical values are at  $T_A = 25^\circ\text{C}$ . All minimum/maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	$V_{ISO}$	ACPL-P341	3750			$V_{RMS}$	$RH < 50\%$ , $t = 1\text{ min.}$ , $T_A = 25^\circ\text{C}$		16, 18
		ACPL-W341	5000			$V_{RMS}$	$RH < 50\%$ , $t = 1\text{ min.}$ , $T_A = 25^\circ\text{C}$		17, 18
Input-Output Resistance	$R_{I-O}$			$>50^{12}$		$\Omega$	$V_{I-O} = 500\text{V}_{DC}$		18
Input-Output Capacitance	$C_{I-O}$			0.6		pF	$f = 1\text{ MHz}$		
LED-to-Ambient Thermal Resistance	$R_{11}$			135		$^\circ\text{C}/\text{W}$			19
LED-to-Detector Thermal Resistance	$R_{12}$			27					
Detector-to-LED Thermal Resistance	$R_{21}$			39					
Detector-to-Ambient Thermal Resistance	$R_{22}$			47					

\*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

## Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10  $\mu$ s. This value is intended to allow for component tolerances for designs with  $I_O$  peak minimum = 2.5A. See applications section for additional details on limiting  $I_{OH}$  peak.
3. Derate linearly above 85°C free-air temperature at a rate of 16.9 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 15.3 mW/°C. The maximum LED junction temperature should not exceed 125°C.
5. Maximum pulse width = 50  $\mu$ s.
6. Output is sourced at -2.5 A with a maximum pulse width = 10  $\mu$ s.  $V_{CC} - V_O$  is measured to ensure 15V or below.
7. Output is sourced at 2.5 A with a maximum pulse width = 10  $\mu$ s.  $V_O - V_{EE}$  is measured to ensure 15V or below.
8. Output is sourced at -2.5 A/2.5 A with a maximum pulse width = 10  $\mu$ s.
9. In this test  $V_{OH}$  is measured with a dc load current. When driving capacitive loads,  $V_{OH}$  will approach  $V_{CC}$  as  $I_{OH}$  approaches zero amps.
10. Maximum pulse width = 1 ms.
11. Pulse Width Distortion (PWD) is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.
12. The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two ACPL-P341 parts under the same test condition.
13. Pin 2 needs to be connected to LED common.
14. Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state (meaning  $V_O > 15.0V$ ).
15. Common mode transient immunity in a low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (meaning  $V_O < 1.0V$ ).
16. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\leq 4500V_{RMS}$  for 1 second (leakage detection current limit,  $I_{I-O} < 5 \mu A$ ).
17. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\leq 6000V_{RMS}$  for 1 second (leakage detection current limit,  $I_{I-O} < 5 \mu A$ ).
18. Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
19. The device was mounted on a high conductivity test board as per JEDEC 51-7.



# Typical Performance Plots

Figure 1 High Output Rail Voltage vs. Temperature

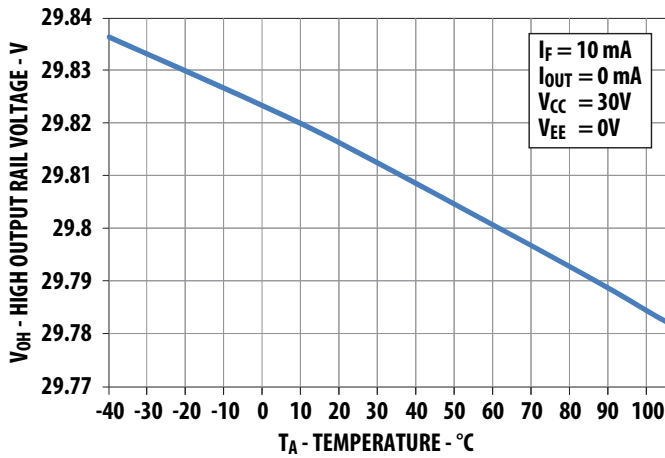


Figure 2 V<sub>OH</sub> vs. Temperature

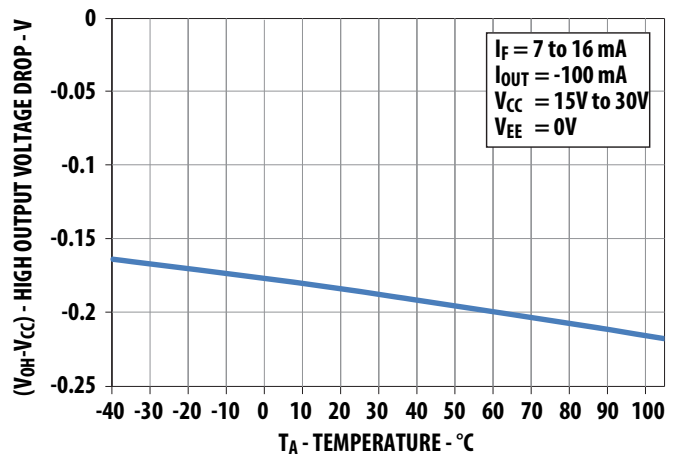


Figure 3 V<sub>OL</sub> vs. Temperature

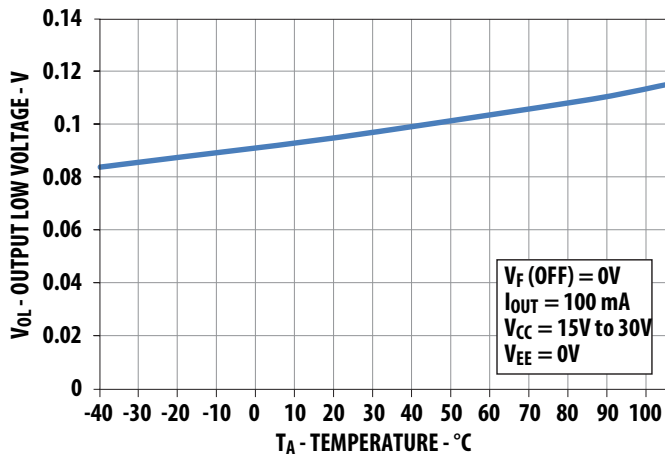


Figure 4 I<sub>CC</sub> vs. Temperature

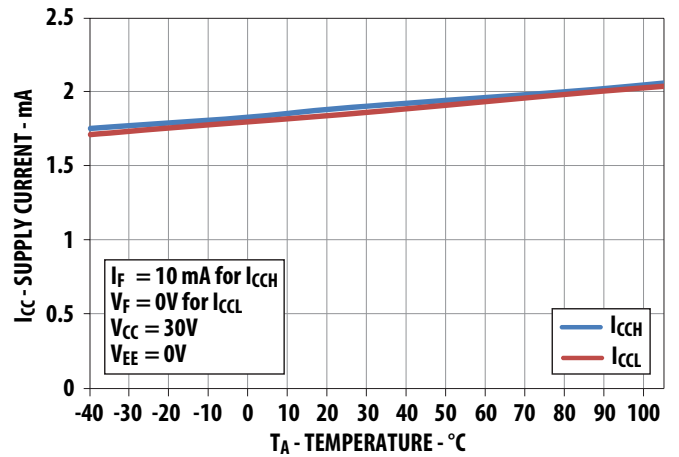


Figure 5 I<sub>CC</sub> vs. V<sub>CC</sub>

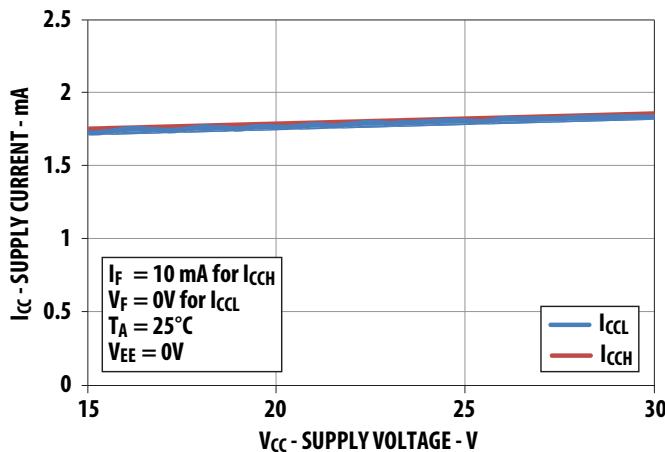


Figure 6 I<sub>FLH</sub> Hysteresis

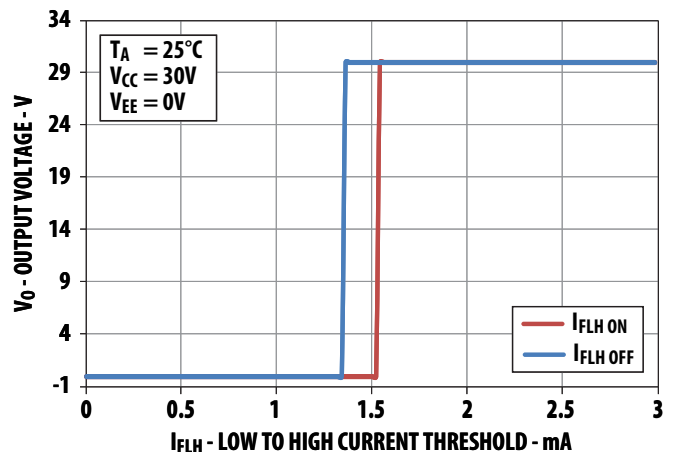


Figure 7  $I_{FH}$  vs. Temperature

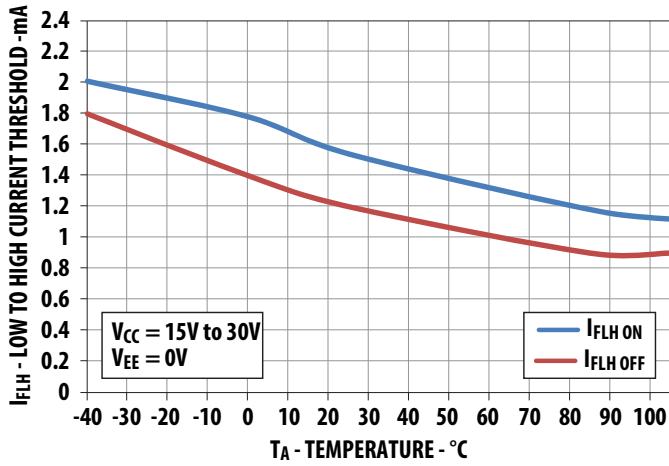


Figure 8 Propagation Delay vs.  $V_{CC}$

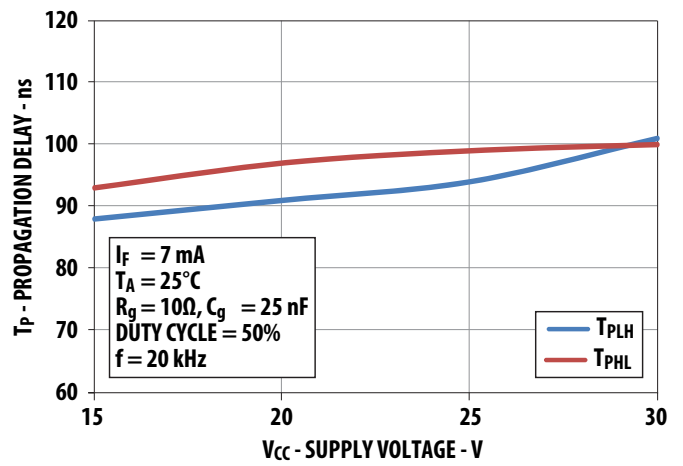


Figure 9 Propagation Delay vs.  $I_F$

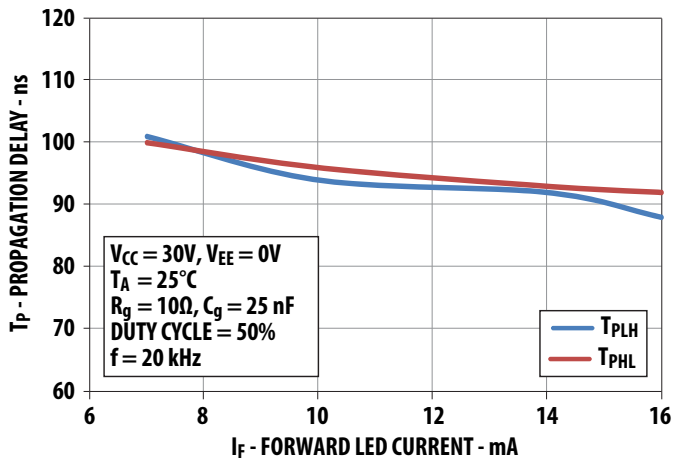


Figure 10 Propagation Delay vs. Temperature

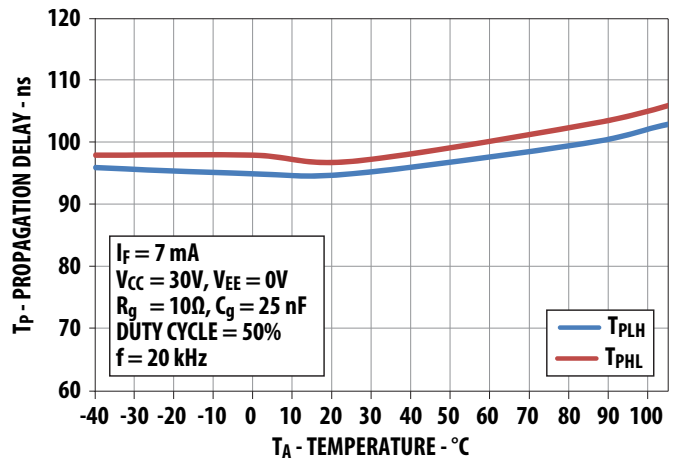


Figure 11 Propagation Delay vs.  $R_g$

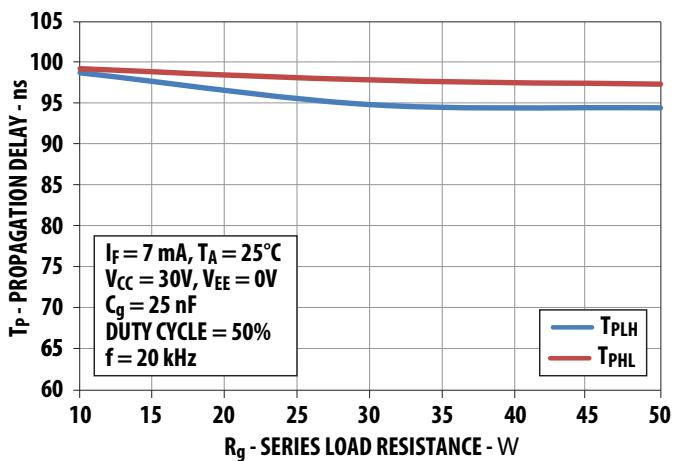


Figure 12 Propagation Delay vs.  $C_g$

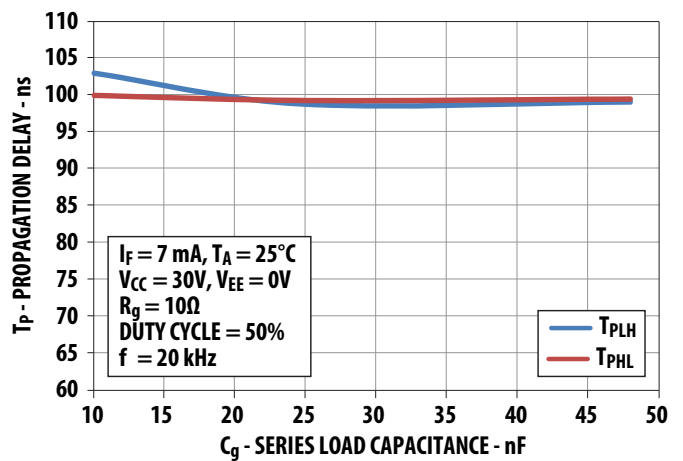


Figure 13 Input Current vs. Forward Voltage

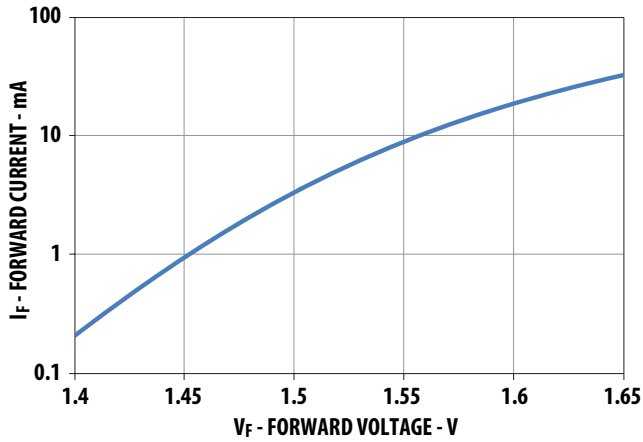


Figure 14  $I_{OH}$  Test Circuit

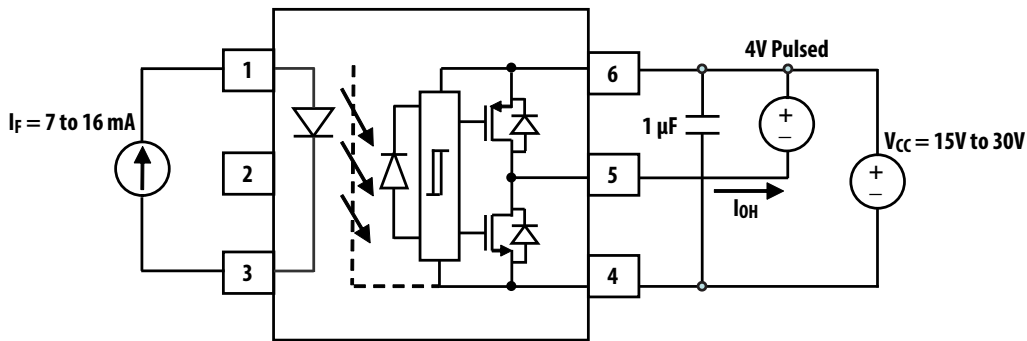


Figure 15  $I_{OL}$  Test Circuit

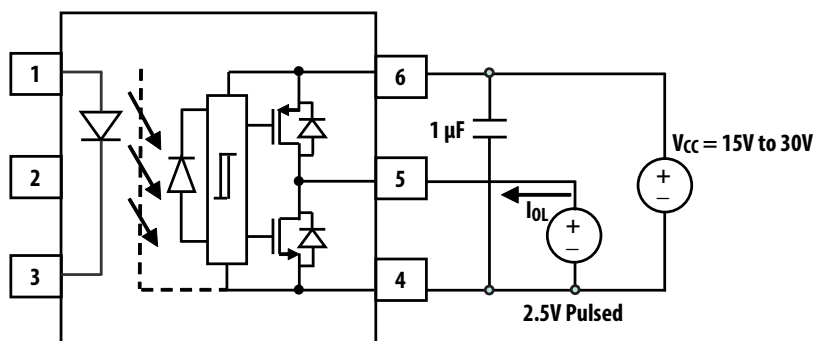


Figure 16  $V_{OH}$  Test Circuit

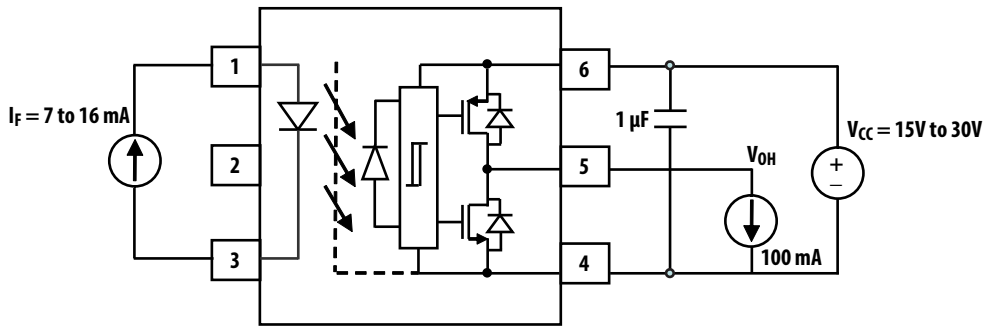


Figure 17  $V_{OL}$  Test Circuit

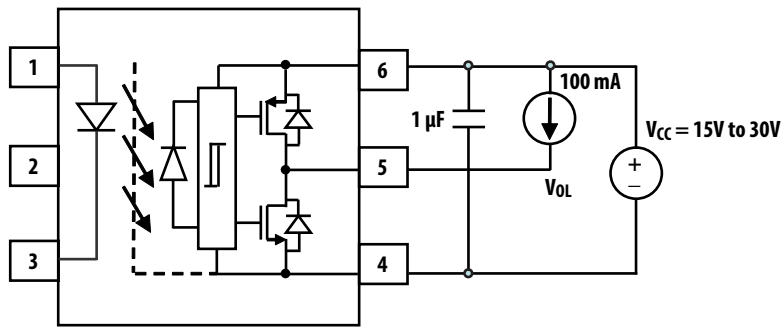


Figure 18  $I_{FLH}$  Test Circuit

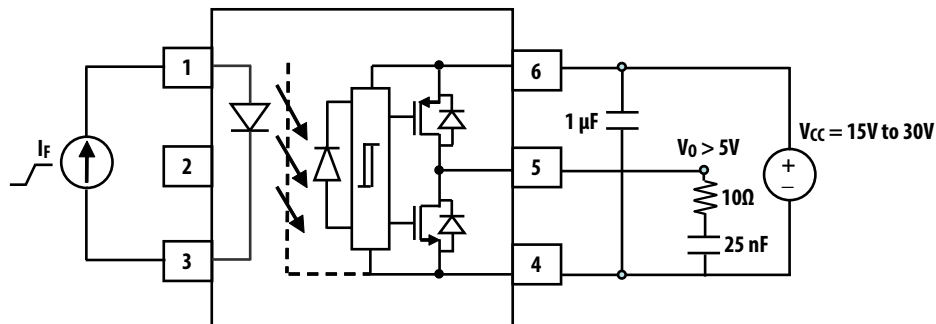


Figure 19 UVLO Test Circuit

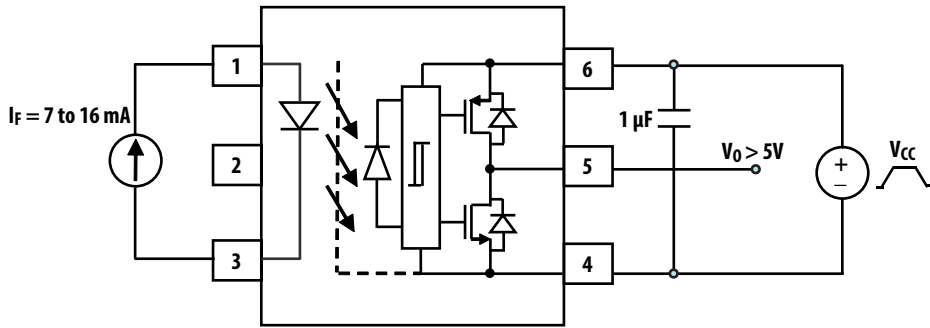


Figure 20  $t_{PHL}$ ,  $t_{PLH}$ ,  $t_r$ , and  $t_f$  Test Circuit and Waveforms

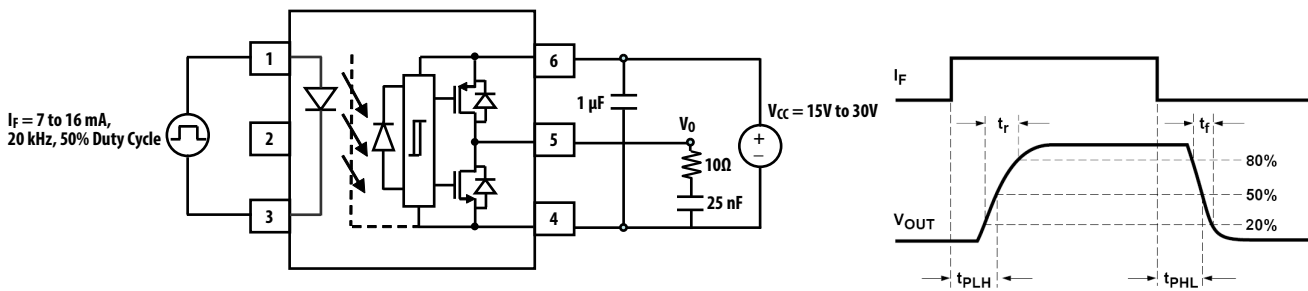
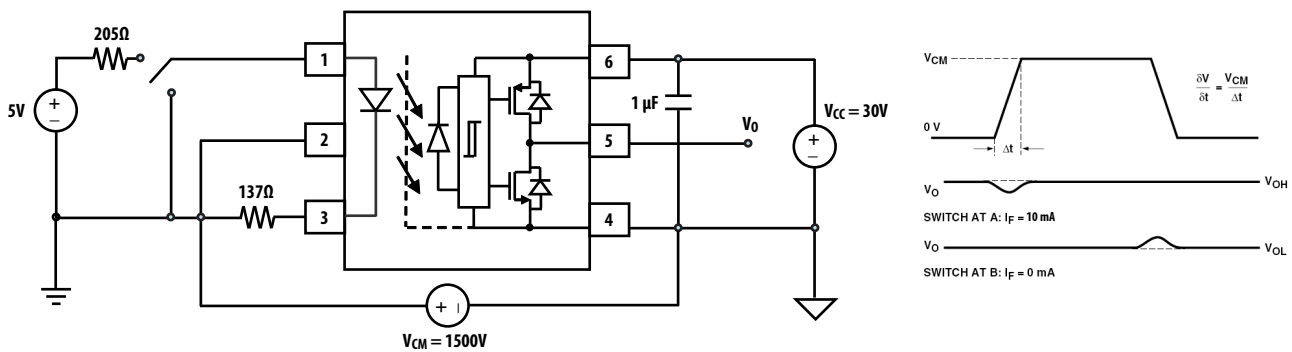


Figure 21 CMR Test Circuit with Split Resistors Network and Waveforms



## Application Information

### Product Overview Description

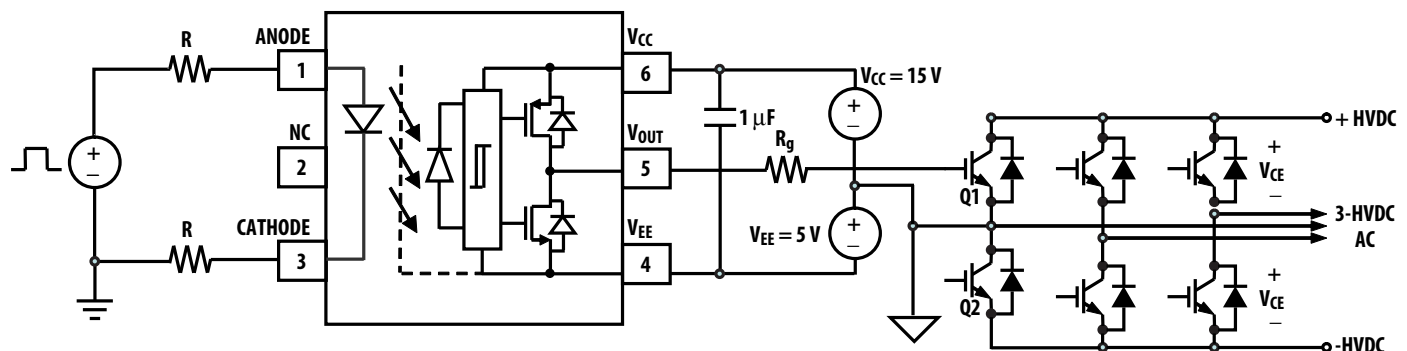
The ACPL-P341/W341 is an optically isolated power output stage capable of driving IGBTs of up to 100A and 1200V. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance, and two times faster speed than the previous generation products.

The high-peak output current and short propagation delay are needed for fast IGBT switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the IGBT's gate voltage is driven to the optimum intended level with no power loss across IGBT. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

It has very high CMR(common mode rejection) rating which allows the microcontroller and the IGBT to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminate the need of additional Schmitt trigger circuit at the input LED.

The stretched SO6 package which is up to 50% smaller than conventional DIP package facilitates smaller more compact design. These stretched packages are compliant to many industrial safety standards such as IEC/EN/DIN EN 60747-5-5, UL 1577 and CSA.

**Figure 22 Recommended Application Circuit with Split Resistors LED**



## Recommended Application Circuit

The recommended application circuit shown in Figure 22 illustrates a typical gate drive implementation using the ACPL-P341. The following describes about driving IGBT. However, it is also applicable to MOSFET. Designers will need to adjust the  $V_{CC}$  supply voltage, depending on the MOSFET or IGBT gate threshold requirements (Recommended  $V_{CC} = 15V$  for IGBT and 12V for MOSFET).

The supply bypass capacitors (1  $\mu F$ ) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (3.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1.5:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

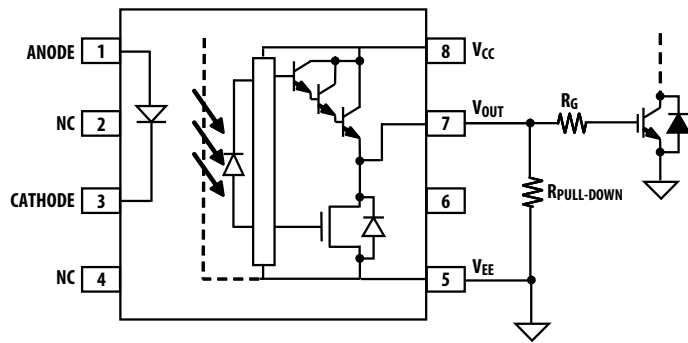
The gate resistor  $R_G$  serves to limit gate charge current and controls the IGBT collector voltage rise and fall times.

In PC board design, care should be taken to avoid routing the IGBT collector or emitter traces close to the ACPL-P341 input as this can result in unwanted coupling of transient signals into ACPL-P341 and degrade performance.

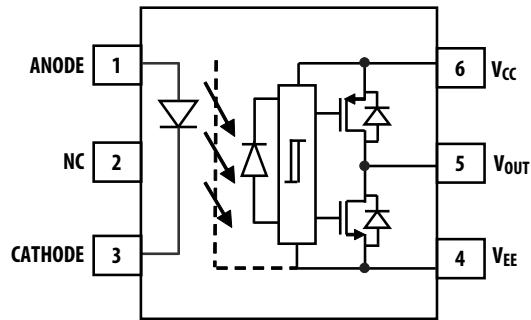
### Rail-to-Rail Output

Figure 23 shows a typical gate driver’s high current output stage with 3 bipolar transistors in darlington configuration. During the output high transition, the output voltage rises rapidly to within 3 diode drops of  $V_{CC}$ . To ensure the  $V_{OUT}$  is at  $V_{CC}$  in order to achieve IGBT rated  $V_{CE(ON)}$  voltage. The level of  $V_{CC}$  will be need to be raised to beyond  $V_{CC}+3(V_{BE})$  to account for the diode drops. And to limit the output voltage to  $V_{CC}$ , a pull-down resistor,  $R_{PULL-DOWN}$  between the output and  $V_{EE}$  is recommended to sink a static current while the output is high.

**Figure 23 Typical Gate Driver with Output Stage in Darlington Configuration**



**Figure 24 PMOS and NMOS Output Stage for Rail-to-Rail Output Voltage**



ACPL-P341 uses a power PMOS to deliver the large current and pull it to  $V_{CC}$  to achieve rail-to-rail output voltage as shown in Figure 24. This ensures that the IGBT’s gate voltage is driven to the optimum intended level with no power loss across IGBT even when an unstable power supply is used.

### Selecting the Gate Resistor ( $R_g$ )

**Step 1:** Calculate  $R_g$  minimum from the  $I_{OL}$  peak specification. The IGBT and  $R_g$  in Figure 22 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-P341/W341.

$$R_g \geq \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{15V + 5V - 2.5V}{3A}$$

$$= 5.8\Omega \approx 6\Omega$$

**Step 1:** Check the ACPL-P341/W341 power dissipation and increase  $R_g$  if necessary. The ACPL-P341/W341 total power dissipation ( $P_T$ ) is equal to the sum of the emitter power ( $P_E$ ) and the output power ( $P_O$ ).

$$P_T = P_E + P_O$$

$$P_E = I_F \times V_F \times \text{Duty Cycle}$$

$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$$

$$= I_{CC} \times (V_{CC} - V_{EE}) + E_{SW}(R_g; C_g) \times f$$

Using  $I_F$ (worst case) = 16 mA,  $R_g = 5\Omega$ , Max Duty Cycle = 80%,  $C_g = 25$  nF,  $f = 25$  kHz and  $T_A$  max = 85°C:

$$P_E = 16 \text{ mA} \times 1.95V \times 0.8 = 25 \text{ mW}$$

$$P_O = 3 \text{ mA} \times 20V + 4.5 \mu\text{J} \cdot 25 \text{ kHz}$$

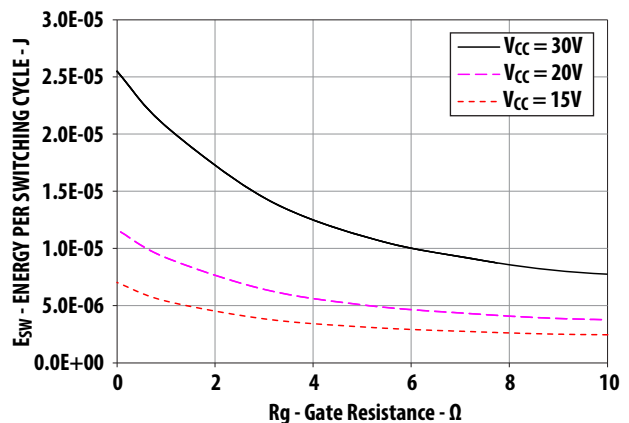
$$= 60 \text{ mW} + 112.5 \text{ mW}$$

$$= 172.5 \text{ mW} < 700 \text{ mW} (P_{O(MAX)} \text{ at } 85^\circ\text{C})$$

The value of 3 mA for  $I_{CC}$  in the previous equation is the maximum  $I_{CC}$  over the entire operating temperature range.

Since  $P_O$  is less than  $P_{O(MAX)}$ ,  $R_g = 6\Omega$  is alright for the power dissipation.

**Figure 25 Energy Dissipated in the ACPL-P341/W341 for each IGBT Switching Cycle**



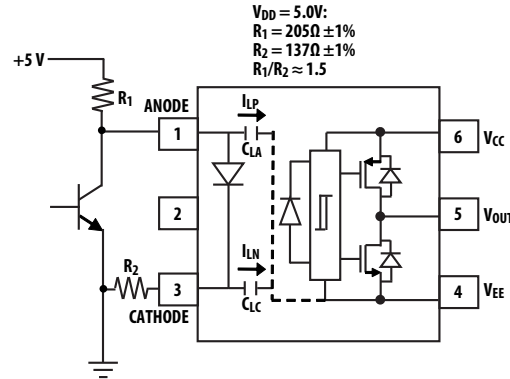
## LED Drive Circuit Considerations for High CMR Performance

Figure 26 shows the recommended drive circuit for the ACPL-P341/W341 that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED’s anode and cathode. Common-mode transients can be capacitive coupled from the LED anode, through  $C_{LA}$  (or cathode through  $C_{LC}$ ) to the output-side ground causing current to be shunted away from the LED (which is not wanted when the LED should be on) or conversely cause current to be injected into the LED (which is not wanted when the LED should be off).

Table 8 shows the directions of  $I_{LP}$  and  $I_{LN}$  depend on the polarity of the common-mode transient. For transients occurring when the LED is on, common-mode rejection ( $CM_H$ , since the output is at “high” state) depends on LED current ( $I_F$ ). For conditions where  $I_F$  is close to the switching threshold ( $I_{FLH}$ ),  $CM_H$  also depends on the extent to which  $I_{LP}$  and  $I_{LN}$  balance each other. In other words, any condition where a common-mode transient causes a momentary decrease in  $I_F$  (meaning when  $dV_{CM}/dt > 0$  and  $|I_{LP}| > |I_{LN}|$ , referring to Table 8) will cause a common-mode failure for transients which are fast enough.

Likewise for a common-mode transient that occurs when the LED is off (meaning  $CM_L$ , since the output is at “low” state), if an imbalance between  $I_{LP}$  and  $I_{LN}$  results in a transient  $I_F$  equal to or greater than the switching threshold of the optocoupler, the transient “signal” may cause the output to spike above 1 V, which constitutes a  $CM_L$  failure. The balanced  $I_{LED}$ -setting resistors help equalize the common mode voltage change at the anode and cathode. The shunt drive input circuit will also help to achieve high  $CM_L$  performance by shunting the LED in the off state.

**Figure 26 Recommended High-CMR Drive Circuit**



## Common Mode Pulse Polarity and LED Current Transients

$dV_{CM}/dt$	$I_{LP}$ Direction	$I_{LN}$ Direction	If $ I_{LP}  <  I_{LN} $ , $I_F$ is momentarily	If $ I_{LP}  >  I_{LN} $ , $I_F$ is momentarily
Positive (>0)	Away from LED anode through $C_{LA}$	Away from LED cathode through $C_{LC}$	Increase	Decrease
Negative(<0)	Toward LED anode through $C_{LA}$	Toward LED cathode through $C_{LC}$	Decrease	Increase

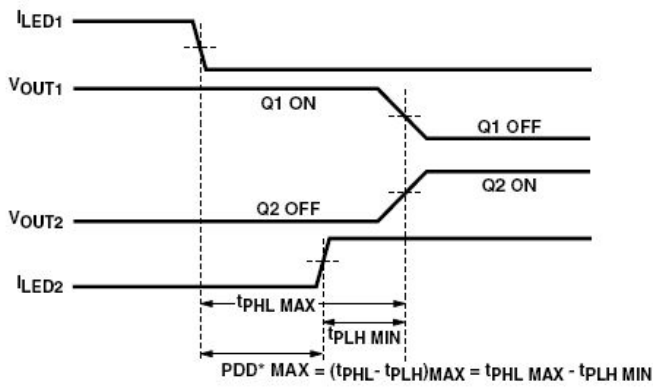


## Dead Time and Propagation Delay Specifications

The ACPL-P341/W341 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 24. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD<sub>MAX</sub>, which is specified to be 100 ns over the operating temperature range of -40°C to 105°C.

Figure 27 Minimum LED Skew for Zero Dead Time

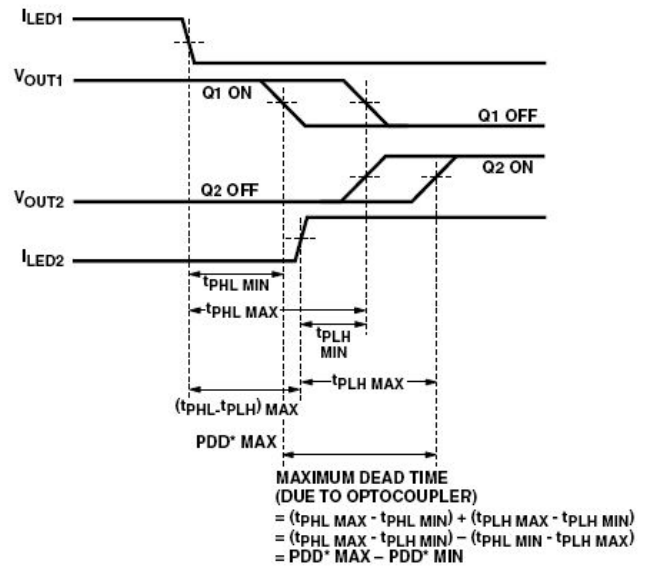


\*PDD = PROPAGATION DELAY DIFFERENCE  
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 25. The maximum dead time for the ACPL-P341/W341 is 100 ns (= 50 ns - (-50 ns)) over an operating temperature range of -40°C to 105°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical MOSFETs.

Figure 28 Waveforms for Dead Time



\*PDD = PROPAGATION DELAY DIFFERENCE  
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

## LED Current Input with Hysteresis

The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 12) provides differential mode noise immunity and minimizes the potential for output signal chatter.

## Under Voltage Lockout

The ACPL-P341/W341 Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the ACPL-P341/W341 output low during power-up. IGBTs typically require gate voltages of 15V to achieve their rated  $V_{CE(ON)}$  voltage. At gate voltages below 13V typically, the  $V_{CE(ON)}$  voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply ( $V_{CC}$ ) is applied. Once  $V_{CC}$  exceeds  $V_{UVLO+}$  (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals.

## Thermal Model for ACPL-P341/W341 Stretched SO6 Package Optocoupler

### Definitions

$R_{11}$ : Junction to Ambient Thermal Resistance of LED due to heating of LED

$R_{12}$ : Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

$R_{21}$ : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

$R_{22}$ : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

$P_1$ : Power dissipation of LED (W).

$P_2$ : Power dissipation of Detector / Output IC (W).

$T_1$ : Junction temperature of LED ( $^{\circ}\text{C}$ ).

$T_2$ : Junction temperature of Detector ( $^{\circ}\text{C}$ ).

$T_a$ : Ambient temperature.

Ambient Temperature: Junction to Ambient Thermal

Resistances were measured approximately 1.25 cm above optocoupler at  $\sim 23^{\circ}\text{C}$  in still air.

Thermal Resistance	$^{\circ}\text{C}/\text{W}$
$R_{11}$	135
$R_{12}$	27
$R_{21}$	39
$R_{22}$	47

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm  $\times$  7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a \quad (1)$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a \quad (2)$$

Using the given thermal resistances and thermal model formula in this datasheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperatures should be within the absolute maximum rating.

For example, given  $P_1 = 17 \text{ mW}$ ,  $P_2 = 124 \text{ mW}$ ,  $T_a = 85^{\circ}\text{C}$ :

LED junction temperature,

$$\begin{aligned} T_1 &= (R_{11} \times P_1 + R_{12} \times P_2) + T_a \\ &= (135 \times 0.025 + 27 \times 0.173) + 85 \\ &= 93^{\circ}\text{C} \end{aligned}$$

Output IC junction temperature,

$$\begin{aligned} T_2 &= (R_{21} \times P_1 + R_{22} \times P_2) + T_a \\ &= (39 \times 0.025 + 47 \times 0.173) + 85 \\ &= 94^{\circ}\text{C} \end{aligned}$$

$T_1$  and  $T_2$  should be limited to  $125^{\circ}\text{C}$  based on the board layout and part placement.

## Related Documents

AV02-0421EN	Application Note 5336	Gate Drive Optocoupler Basic Design for IGBT/MOSFET
AV02-3698EN	Application Note 1043	Common-Mode Noise: Sources and Solutions
AV02-0310EN	Reliability Data	Plastics Optocouplers Product ESD and Moisture Sensitivity