

ACT41000-104-REF01 User's Guide

Description

ACT41000-104-REF01 reference design provides both the drain and gate voltages for many of Qorvo's RF PAs. It automatically searches for and optimizes the optimal RF PA gate voltage to set the required Idq bias current. This reference design demonstrates how Qorvo's ACT41000 simplifies RF PA system level design and cost. The design is specifically configured for the QPA2211, but it can be easily modified for many other RF PAs.

This document describes the characteristics and operation of the Qorvo ACT41000EVK-104-REF01 reference design. It provides setup and operation instructions, schematic, layout, BOM, GUI, and test data. The design demonstrates the ACT41000Q1104-T (22V) power management IC. Other ACT41000Q1xxx options can be evaluated on this EVK by replacing the IC and any other necessary components. The initial design is optimized for the QPA2211.

Functions

The design accepts an input voltage range up to 40V. The minimum input voltage is dependent on the drain voltage being tested. With the QPA2211 22V drain voltage, the design works down to 24V. The ACT41000 converts the input voltage to the high-power RF PA drain voltage of 22V at up to 4A. Typical RF PA drain voltages are the range of 20V to 24V. The design also includes a 2nd on-board power supply to generate the negative RF gate voltage. Input power for the gate voltage supply comes from the ACT41000 auxiliary 5V bias output.

To fully utilize the reference design features, the user must connect the reference design to a PC to use the graphical user interface (GUI) software. The GUI allows the user to program the exact voltage and current for the specific RF PA being tested. The user can use GUI to set the Idq bias current requirement and the design autonomously finds and stores the optimal gate voltage for the Idq bias current. After the optimal gate bias voltage is found, the user can then apply an RF signal to test the RF PA functionality. The GUI gives the user full control over the drain voltage, the drain current limit, and the gate voltage. The overall system design consists of two separate PCBs, the ACT41000-104-REF01 board and an RF PA EVK, that the user must manually wire together.



Figure 1. Reference Design Picture

EVK Contents

The ACT41000EVK-104-REF01 evaluation kit comes with the following items:

- PCB assembly

Required Equipment

- ACT41000EVK-104-REF01
- Power supply - 24~40V @ 5A for full power operation
- Oscilloscope - 100MHz, 4 channels
- Digital Multi-meters (DMM)
- Windows compatible PC with spare USB port
- USB cable shown in Figure 3

Hardware Setup



Figure 2. Reference Setup with QPA2211

Quick Start

Hardware Connections

Refer to Figure 2 for hardware connections.

1. Connect a DC power supply to connector for input voltage (VIN). Please ensure the correct power supply polarity.
2. Connect Digital Multi-Meters to VIN, Vdrain and Vgate to monitor the input voltage, drain and gate voltages.
3. Add a digital Multi-Meter in series with VIN and Vdrain if you want to observe input and output current.
4. Be careful to keep the input voltage within the specifications.
5. Connect the PCB to the PC with a USB cable.
6. If connecting an RF input source to the RF PA, ensure that it disabled.



Figure 3. Board-USB-Laptop Connection

GUI Setup

1. Refer to the end of this document for detailed instructions to install the ACT41000-104-REF01 GUI.

Recommended Operating Conditions

The ACT41000-104-REF01 is designed for a 24V-40V input voltage. The maximum operating voltage is determined by the IC's maximum input voltage rating of 40V. The minimum operating voltage is determined by the IC's output voltage setting. The default ACT41000QI104 output voltage is 22V, so the design should be operated with V_{in} greater than 22V by default. See Figure 5 for details on modifying this drain voltage. The maximum output current is configured by the CMI and external components. The default hardware design is rated at 4A, but the default current limit setting is 4003.84mA. The switching frequency is set to 450kHz to optimize efficiency. The customer can easily reconfigure the EVK for different switching frequencies and output voltages after referring to the datasheet for the required component changes. The output voltage can be changed via I²C either before or after the output voltage is enabled.

Table 1. Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VIN	Input voltage	24	-	40	V
Vdrain	Drain voltage	3	-	22	V
Idrain	Drain current	0	-	4	A
Vgate	Gate voltage	-5	-	0	V
Igate	Gate current	0	-	50	mA
Frequency	Switching frequency		450		KHz

Refence Design Operation

GUI Functions

After setting up the hardware and GUI, the reference design can be powered on. Figure 4 shows the main GUI units.

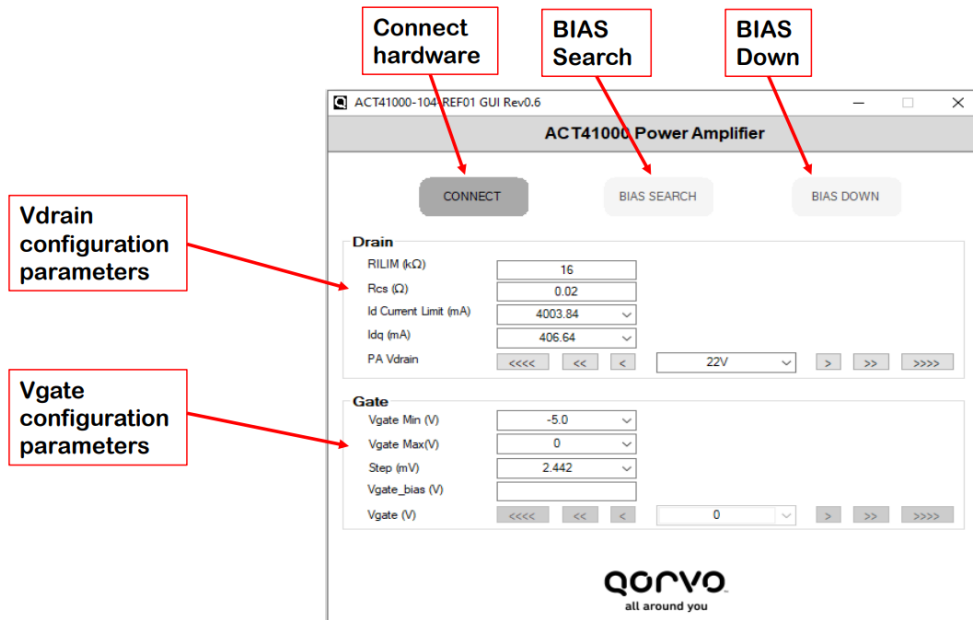


Figure 4. ACT41000 Power Amplifier GUI Functions

GUI Detailed Functional Buttons

CONNECT **Connect**
 Connect button will check the connection from PC with ACT41000 board. The "Hardware error" message will pop up to notify the user that hardware is not ready to use. Otherwise, when connect successfully, the background of the buttons will be change to blue

BIAS SEARCH **BIAS Search**
 BIAS search button will find the optimal gate bias voltage after the user set up necessary parameters of Vdrain and Vgate, the user can then apply an RF signal to the RF PA. A text box will display Vgate value found, if no value found, it will display "not found"

BIAS DOWN **BIAS Down/Stop**
 BIAS down/Stop button will put the system in Bias Down State (Vdrain =0, Vgate=0).

Figure 5. GUI Detailed Functional Buttons

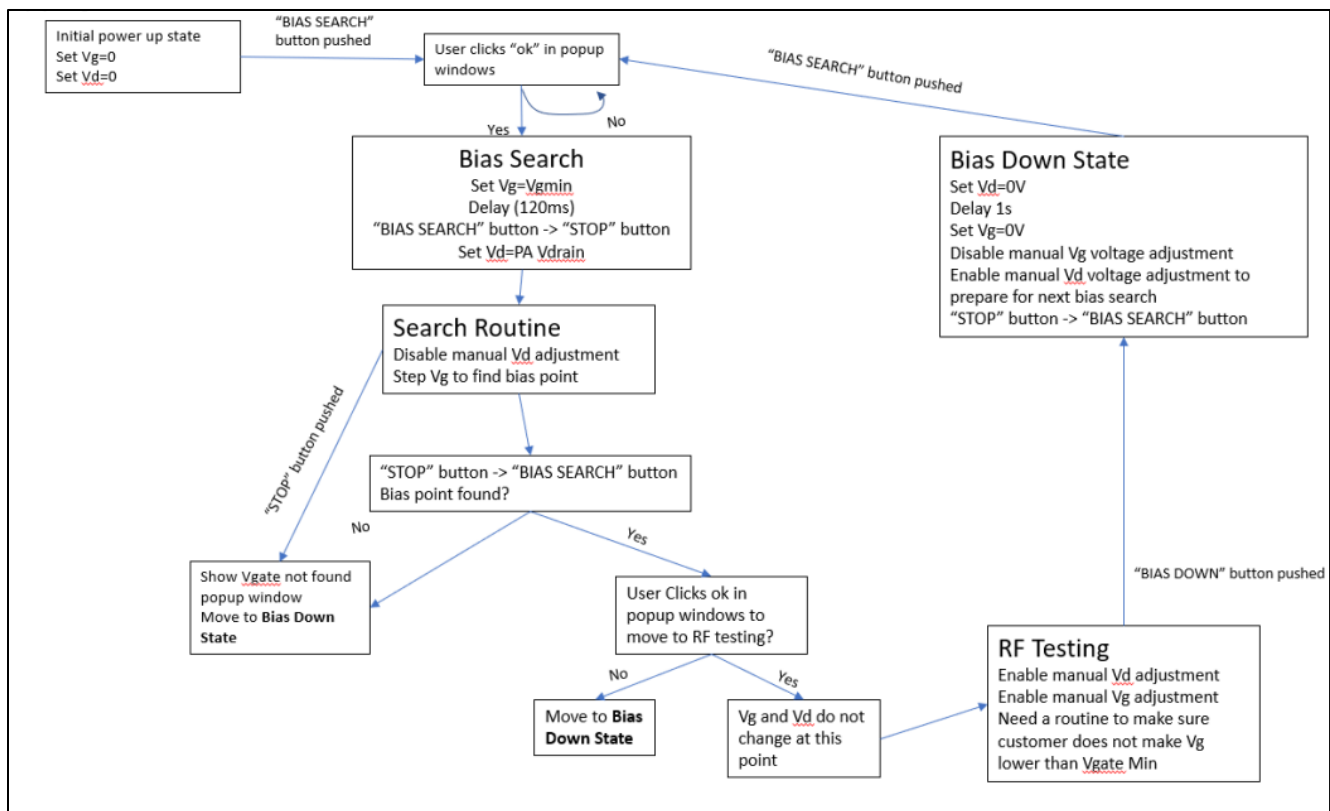


Figure 6. Bias Search Routine Flow Chart

Figure 8 shows the QPA2211 datasheet bias sequence requirements. The default GUI and hardware settings are compatible with the QPA2211 but can easily be modified to support other RF PAs. Complete the following steps to configure the GUI setup for other RF PAs. The following figures show the QPA2211 settings and bias procedure. This reference design automatically performs both the Bias Up and Bias Down Procedure.

The QPA2211 Bias Sequence with ACT41000

Bias Up Procedure

1. @MCU & Gate Driver
Set I_G limit to 40mA
2. @ACT41000
Set current limit at 280 mA ^[1]
3. @MCU & Gate Driver
Apply -5 V to V_G
4. @ACT41000
Turn on V_D ^[2]
5. @MCU & Gate Driver
Start sweeping up V_G
6. @MCU & Gate Driver
Stop sweeping V_G upon an interrupt from the PGBIAS pin of ACT41000
7. @ACT41000
Set current limit at 3500 mA ^[3]
8. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. @ACT41000
Set current limit at 280 mA
3. @MCU & Gate Driver
Reduce V_G to -5 V
4. @ACT41000
Set voltage reference at the minimum ^[4]
5. @ACT41000
Turn off V_D ^[2]
6. @MCU & Gate Driver
Turn off V_G supply

Figure 8. QPA2211 Bias Sequence

Configure the GUI Inputs

1. Ensure that the input power supply is connected to VIN is between 24V and 40V, and that the current limit is set greater than 4A.
2. Turn on the input power supply.
3. Open GUI that was installed on the computer. GUI interface and functional buttons are shown in Figure 5 and 6.
4. Click the CONNECT button. If the GUI and the PCB communicate properly, the CONNECT button turns blue. If the button does not turn blue, disconnect and reconnect the USB cable.
5. Change the default RLIM and Rcs resistor values if these components were physically changed on the PCB. The GUI must have the correct values to properly calculate the current limits.
6. Select Id Current Limit, the drain current maximum limit, for the RF PA being tested.
7. Set Idq, the drain bias current, for the RF PA being tested.
8. Set PA Vdrain, the RF PA drain voltage, for the RF PA being tested.
9. Set Vgate Min, the minimum allowable gate voltage, for the search routine. This is the starting voltage for the Vgate search routine. It must be greater than -5V.
10. Set Vgate Max, the maximum allowable gate voltage, for the Vgate search routine. It must be lower than 0V.
11. Select Step, the gate voltage step resolution. A smaller step results in a more accurate search result, but takes longer to find the required gate voltage.

Bias Search

1. Click the BIAS SEARCH button. Note that the search routine can be stopped at any time by pressing the “STOP” button.
2. The GUI sets the ACT41000 current limit to programmed Idq Current Limit threshold and then simultaneously sweeps the Vgate voltage while measuring the drain current. When the drain current crosses the programmed Idq threshold, the GUI displays the optimized bias gate voltage value. If there is a setup issue and the optimized Vgate voltage is not found, the GUI displays “not found”.
3. Figure 7 shows the bias search routine.
4. After the optimal bias point is found, click to either move to begin test the RF PA functionality or to power down the test. To avoid damaging the RF PA, always click the “BIAS DOWN” button to power down the system.

RF Testing

1. If moving forward with RF testing, the EVK changes the ACT41000 current limit to the Id Current Limit threshold.
2. The GUI now allows the user to manually change the PA Vdrain voltage and the Vgate voltage. For safety, the allowable Vgate range is still bounded by the Vgate Min and Max settings.
3. Apply RF to the RF PA EVK.
4. To avoid damaging the RF PA, always click the “BIAS DOWN” button to power down the system.

Modifications to Test a Different RF PA

The ACT41000-104-REF01 default settings are compatible with the QPA2211. The design can be easily modified to support any other RF PAs with drain voltages up to 24V and drain currents up to 4A. Typically, only four modifications needed to test a different RF PA. These include the following.

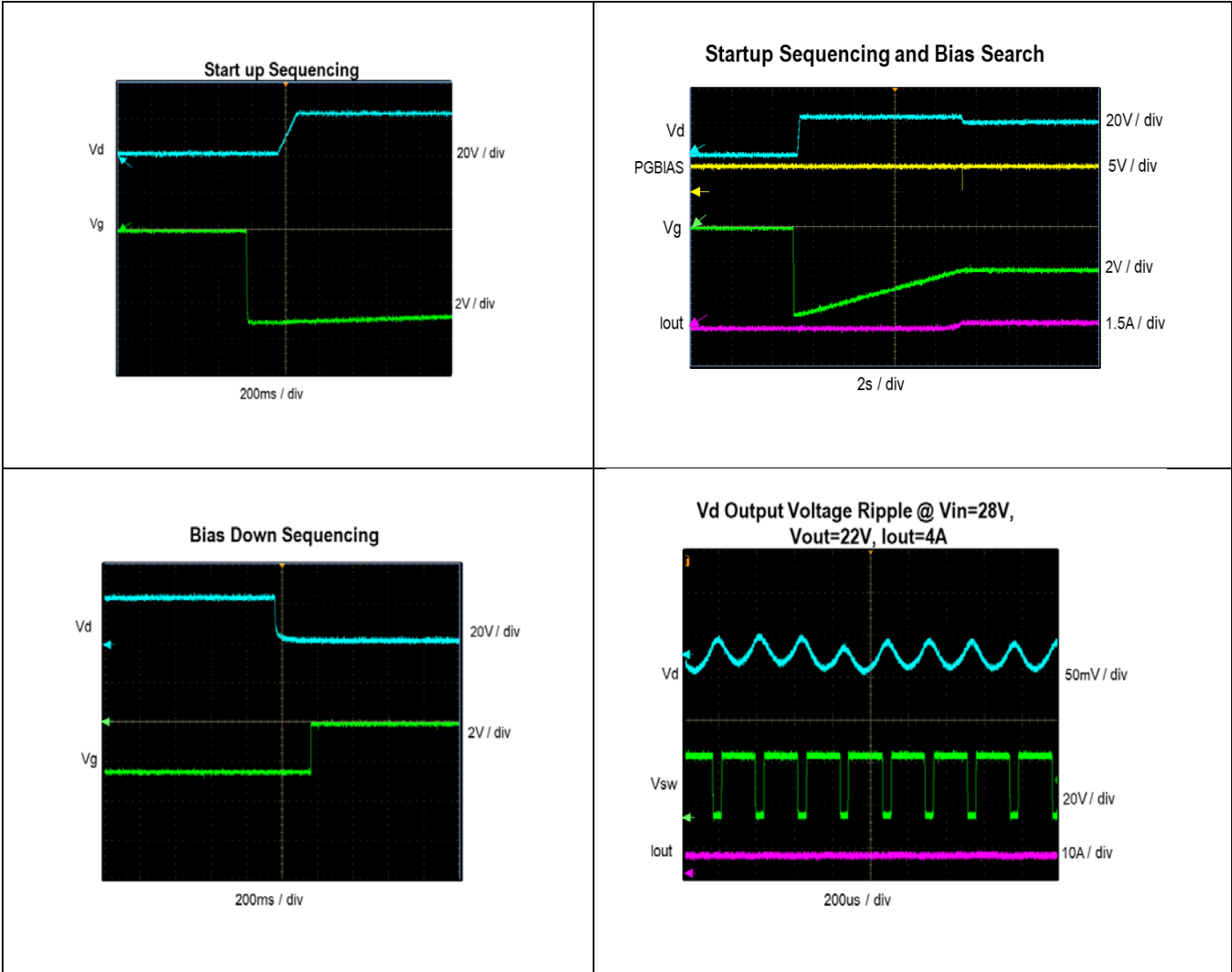
PA Vdrain Voltage - Drain voltage during the search routine and the RF testing. This voltage is generated by the ACT41000. The PA drain voltage defaults to 22V but can be changed to a different voltage via the GUI. It can also be changed by replacing the ACT41000-104 with a different version of the IC with a different default output voltage. Refer to the ACT41000 datasheet for additional details and equations.

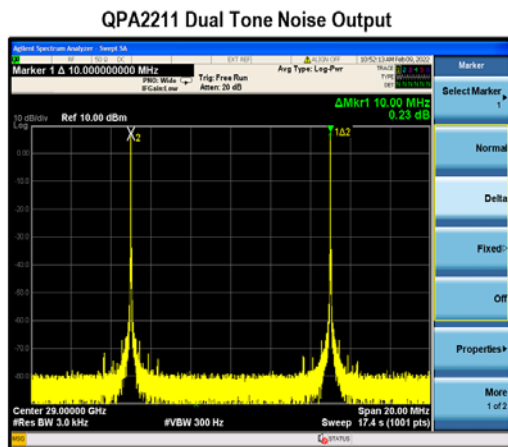
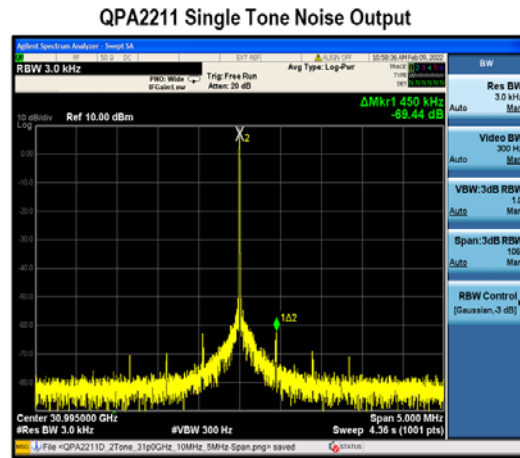
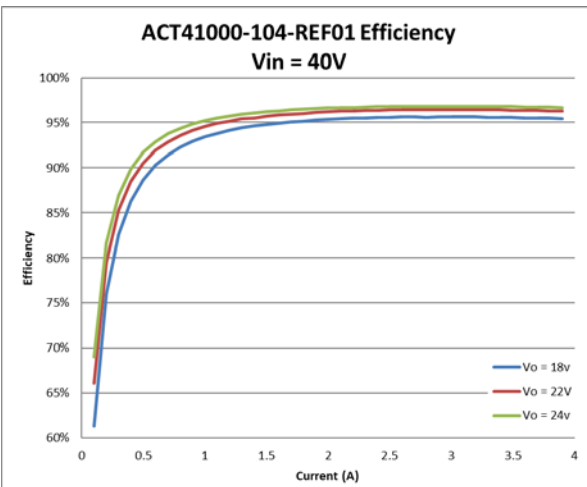
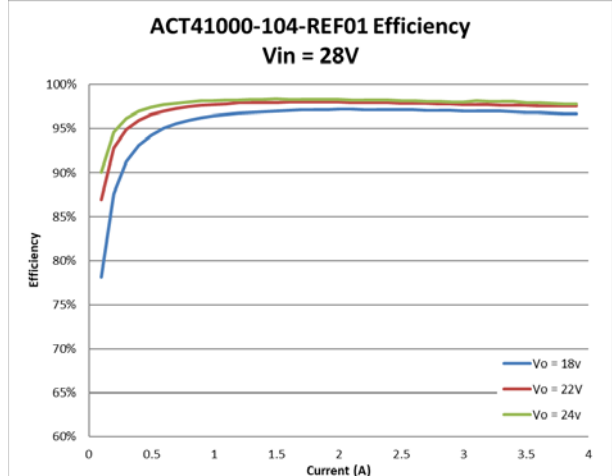
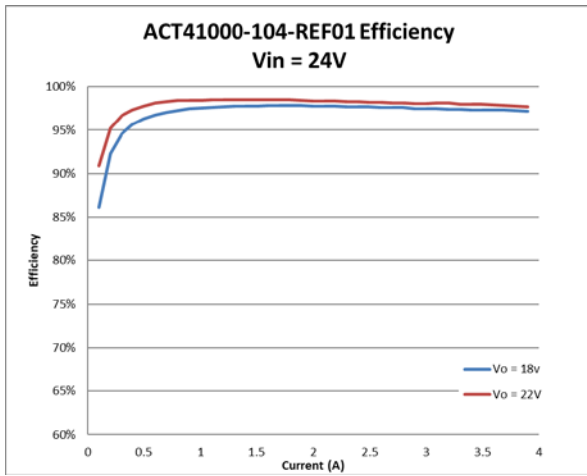
Id Current Limit – Drain current limit threshold during RF testing. This current is the same as the ACT41000EVK-104 output current limit, which is set to 4A. The current limit is a function of the 20mΩ current sense resistor (R5), the 16kΩ ILIM resistor (R9), and the I²C ILIM Output Current Limit bits which are set to 100uA by default. The ACT41000 integrates a digital-to-analog converter (ILIM DAC) for the purpose of generating the reference current used by the Current Limit block. Although any of these three items can be used to change the Id Current Limit, the easiest way to change the output current limit is with the ILIM DAC field in the GUI. Note that the RILIM and Rcs resistance values in the GUI must always match the actual hardware values. The output current limit is easily changed by modifying any of these three parameters. Refer to the ACT41000 datasheet for additional details and equations.

Idq Current – The RF PA Drain current threshold that corresponds to the optimal gate voltage. The Idq current setting is achieved by changing the ACT41000 I²C ILIM current limit bits. The Idq step size is always 1/256 of the maximum Id allowable current. If a smaller Id step size is needed, the user must reduce the maximum allowable Id current by changing resistors on the PCB.

Vgate Min and Vgate Max – The minimum and maximum allowable voltages that can be applied to the gate. These two voltages can only be adjusted using the GUI inputs.

Test Results





Schematic

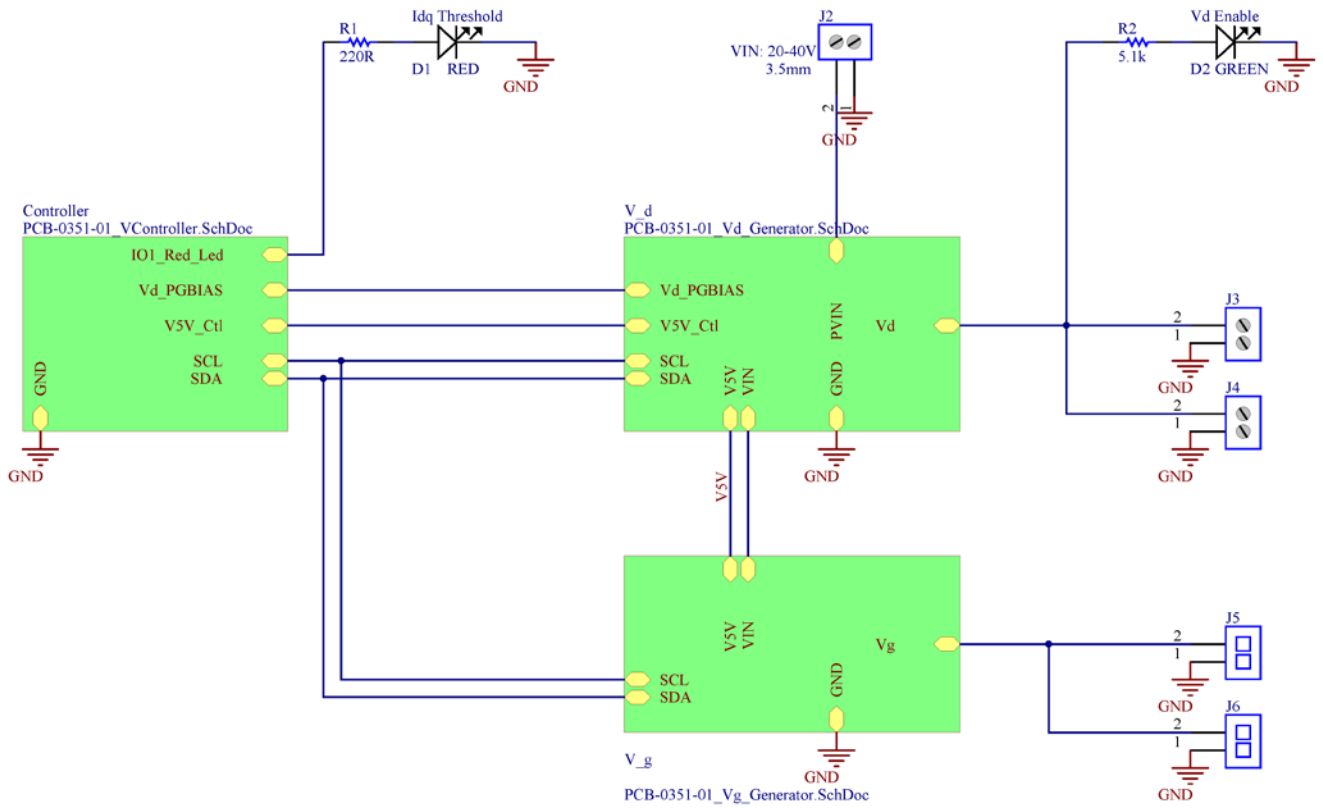


Figure 9. Schematic Top Level

V_d Generator
 Input: PVIN= 24-40V
 Output: V_d=20-24V, V5V

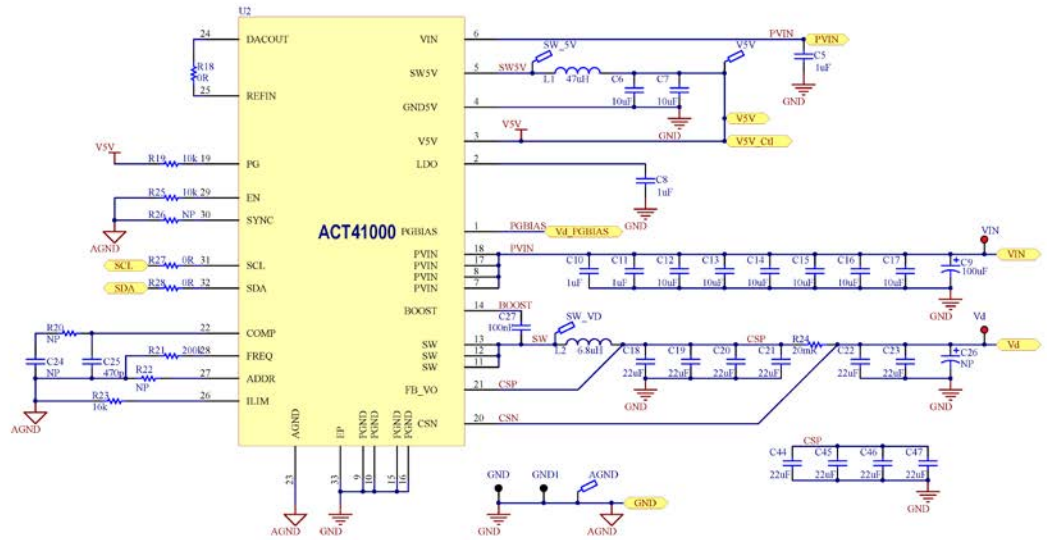


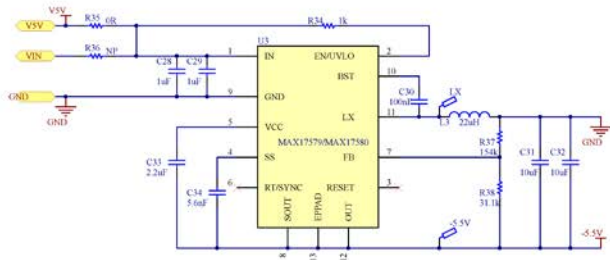
Figure 11. Schematic Vdrain Supply

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V_g Generator

Input: P_{VIN}= 24-40V and V_{5V}

Output: V_g = -5V to 0V



Output: $V_g = - \text{DACOUT} \cdot (R32/R33) = - \text{DACOUT} \cdot 2$

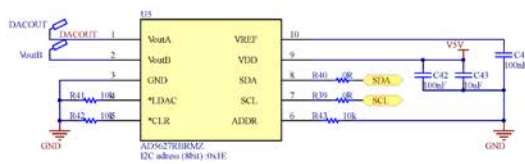
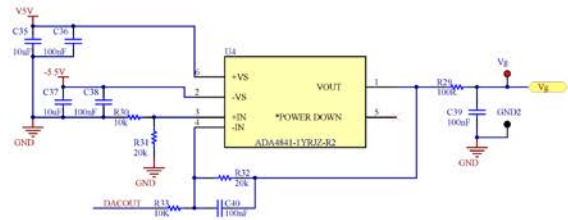


Figure 12. Schematic Vgate Supply

Layout

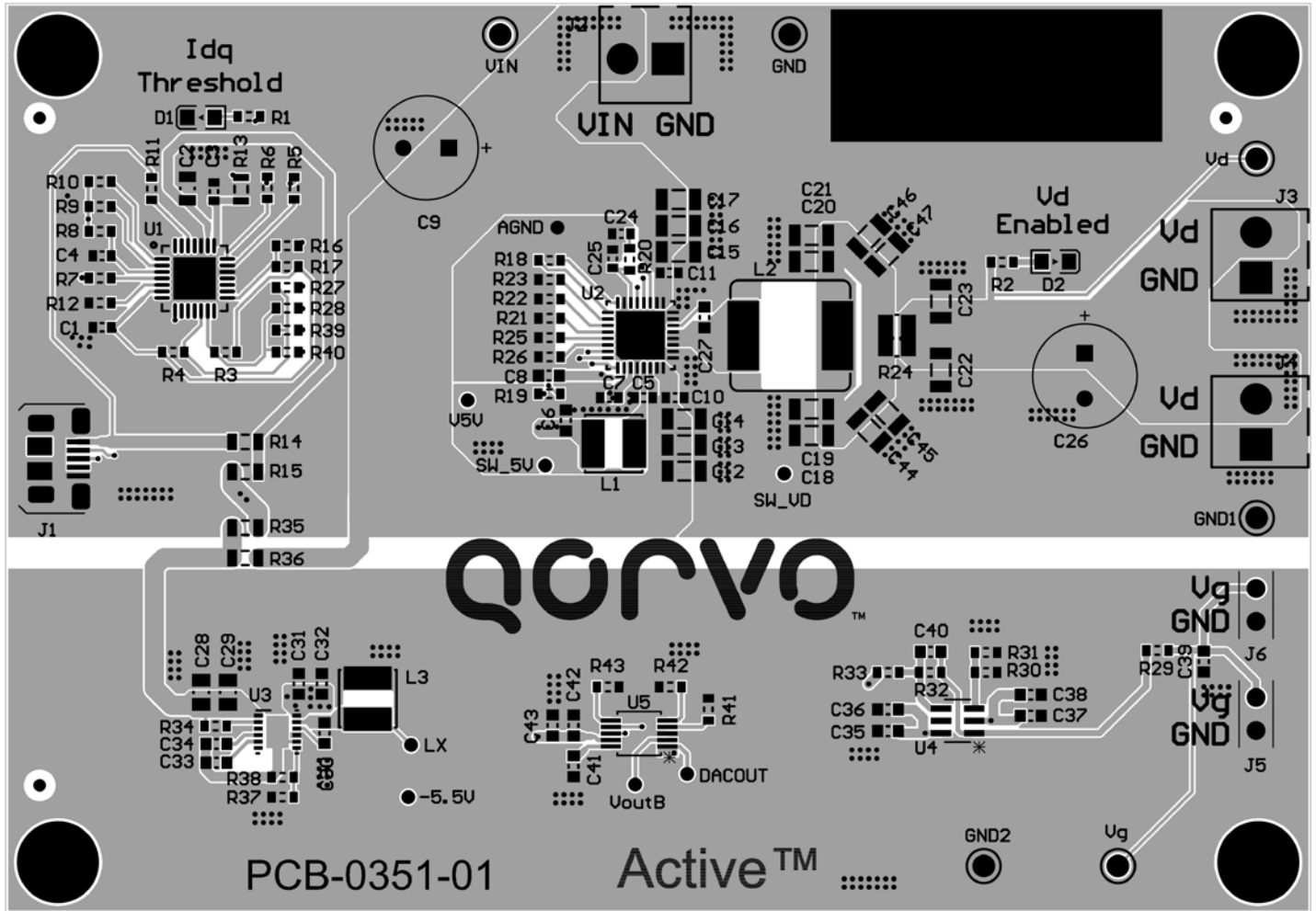


Figure 13. Assembly Layer

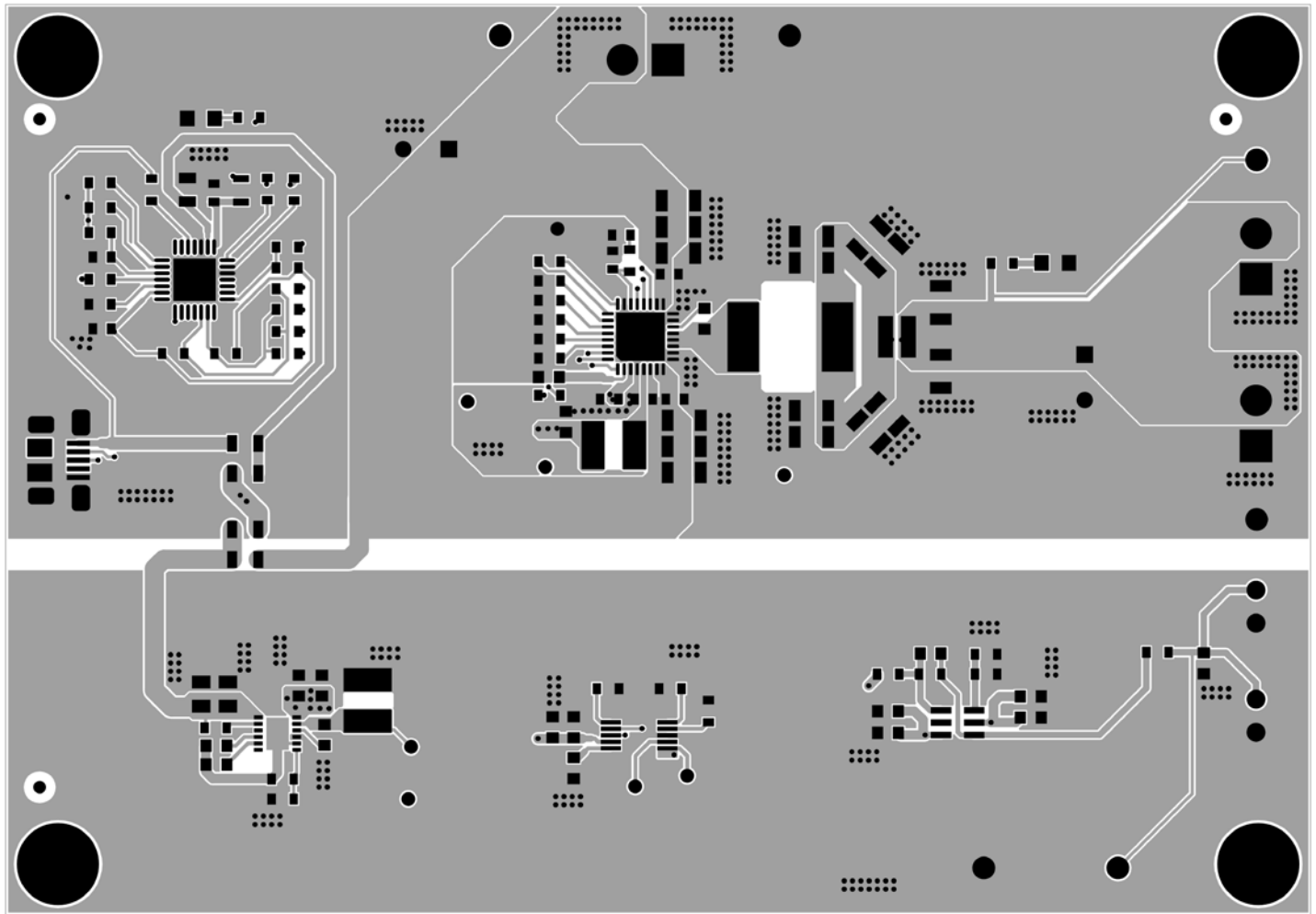


Figure 14. Layout Top Layer

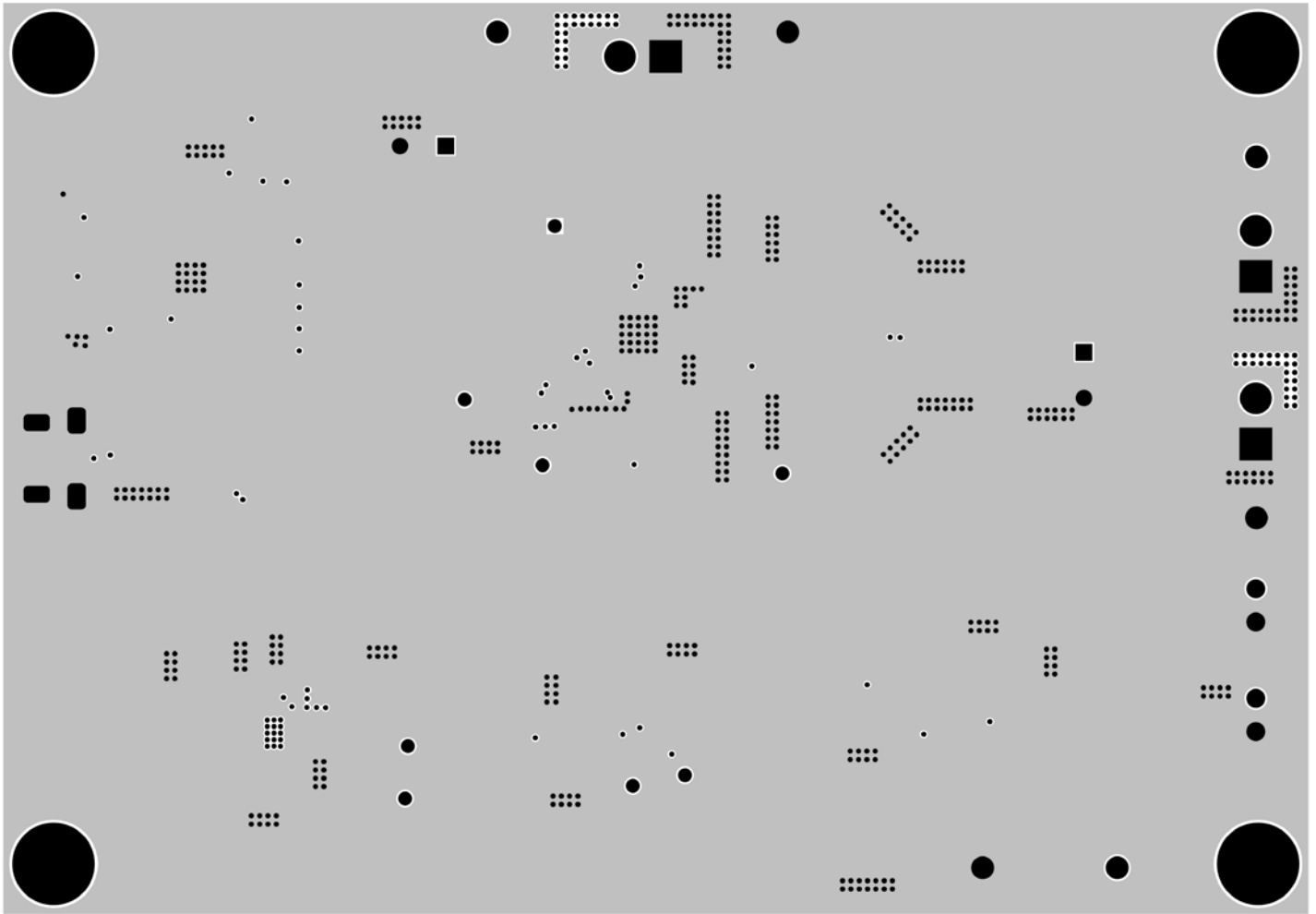


Figure 15. Layout Layer 2 - GND

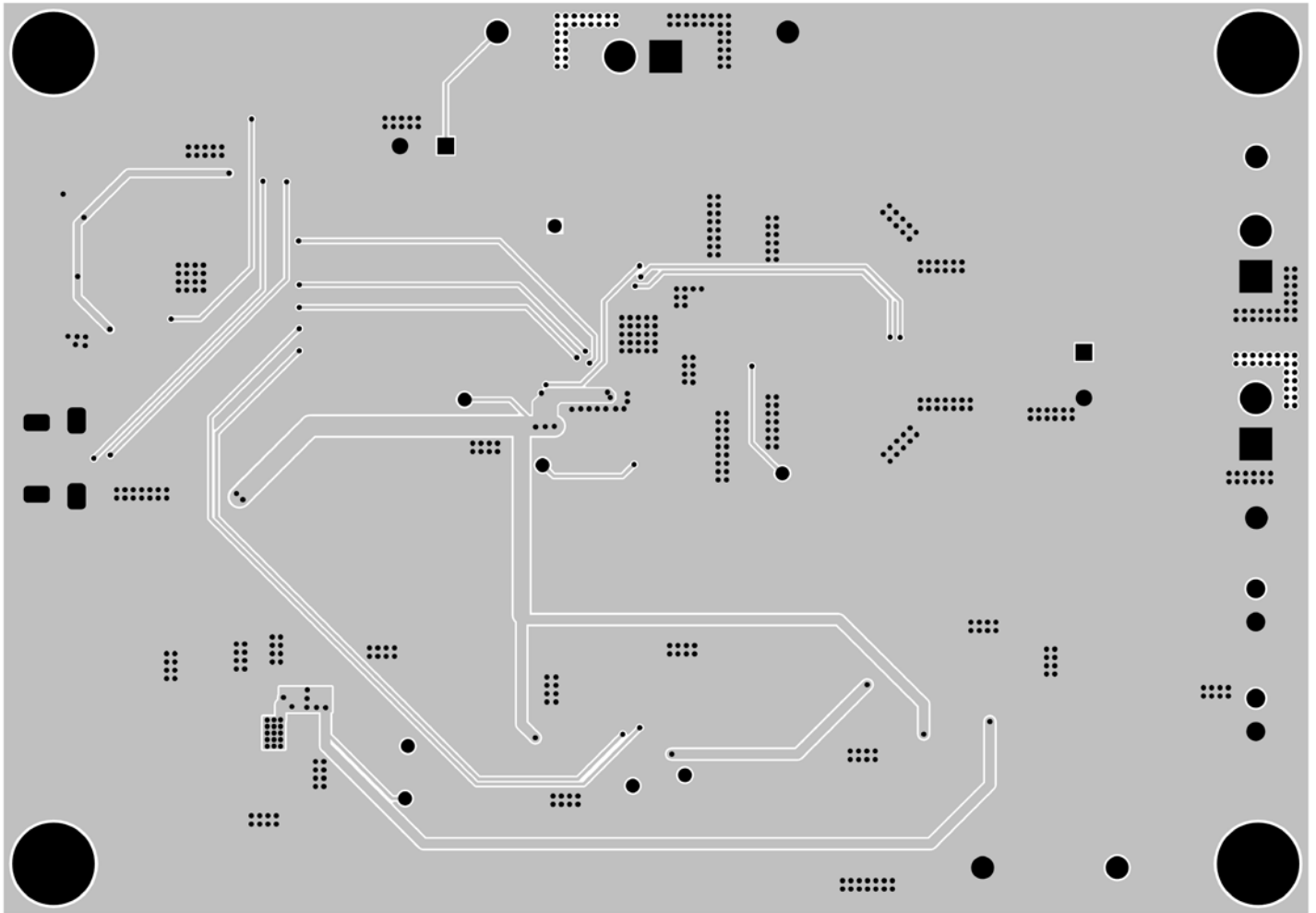


Figure 16. Layout Layer 3

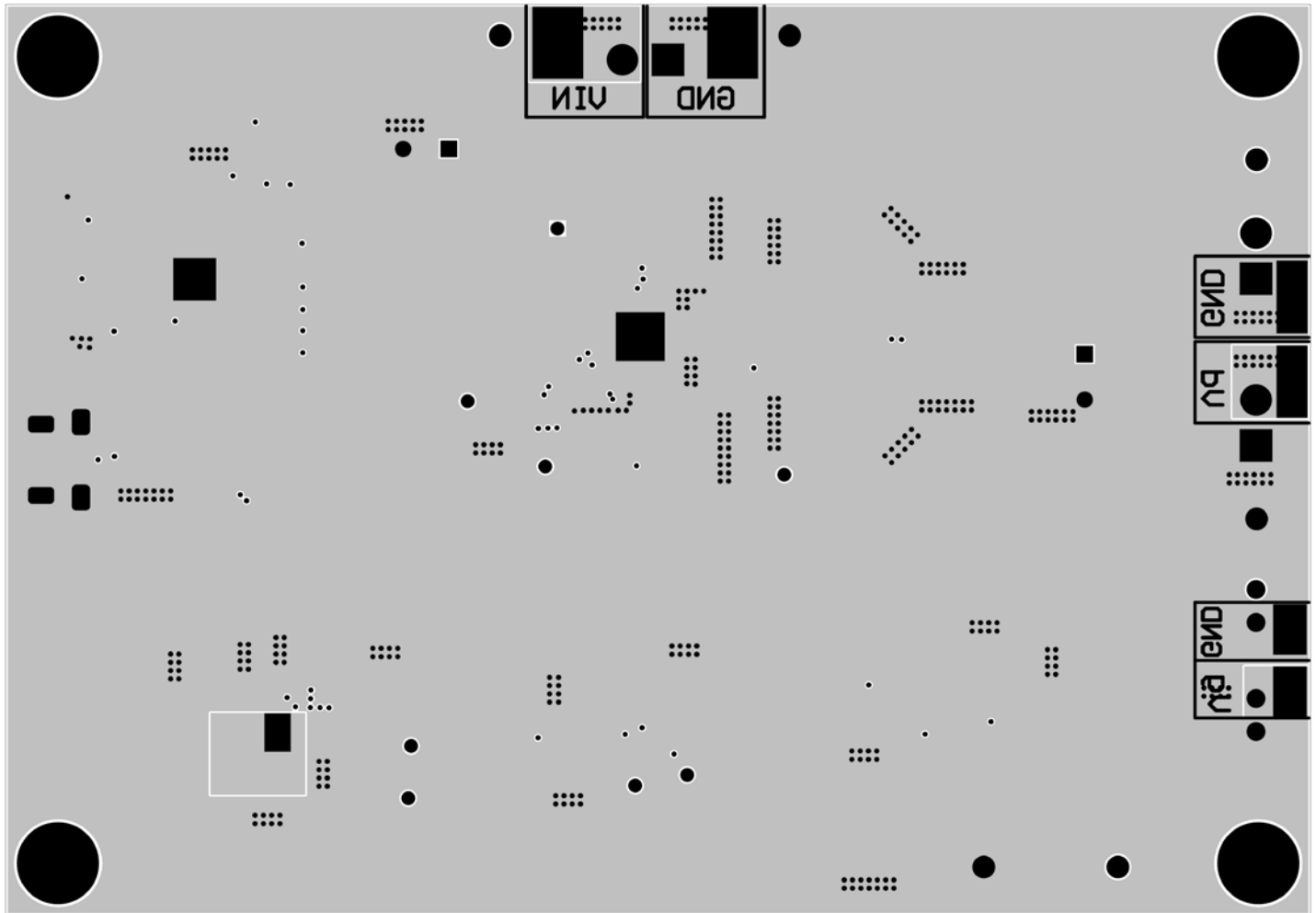


Figure 17. Layout Bottom Layer

Bill of Materials

Item	Ref Des	QTY	Description	Package	MFR	Part number
1	C1, C3, C27, C30, C36, C38, C39, C40	8	Cap, Ceramic, 100nF, 25V, 20%, X5R	0603	Standard	Standard
2	C2	1	Cap, Ceramic, 22uF, 10V, 20%, X5R	0805	Standard	Standard
3	C4	1	Cap, Ceramic, 4.7uF, 10V, 20%, X5R	0603	Standard	Standard
4	C5, C8, C10, C11	4	Cap, Ceramic, 1uF, 50V, 20%, X5R	0603	Standard	Standard
5	C6, C7, C31, C32, C35, C37, C43	7	Cap, Ceramic, 10uF, 16V, 20%, X5R	0603	Murata	GRT188R61C106ME13D
6	C9	1	Cap, Aluminium Electrolytic, 100uF, 50V	8x11.5	Wurth	860010674014
7	C12, C13, C14, C15, C16, C17	6	Cap, Ceramic, 10uF, 50V, 10%, X5R	1206	TDK	CGA5L3X5R1H106K160AB
8	C18, C19, C20, C21, C22, C23, C44, C45, C46, C47	10	Cap, Ceramic, 22uF, 35V, 20%, X5R	1206	TDK	C3216X5R1V226M160AC
9	C24	0	NP	0603	Standard	Standard
10	C25	1	Cap, Ceramic, 470pF, 16V, 20%, X5R	0603	Standard	Standard
11	C26	0	NP	8x11.5	Wurth	860010674014
12	C28, C29	2	Cap, Ceramic, 1uF, 50V, 10%, X7R	0805	Murata	GCJ21BR71H105KA01L
13	C33	1	Cap, Ceramic, 2.2uF, 10V, 10%, X7R	0603	Murata	GRM188R71A225KE15
14	C34	1	Cap, Ceramic, 5.6nF, 10V, 20%, X5R	0603	Standard	Standard
15	C41, C42	2	Cap, Ceramic, 100nF, 16V, 20%, X5R	0603	Standard	Standard
16	D1	1	Diode, RED	0805	Std	Std
17	D2	1	Diode, GREEN	0805	Std	Std
18	J1	1	Connector, RCPT 5POS MICRO USB R/A	/	Amphenol FCI	10103594-0001LF
19	J2, J3, J4	3	Connector, Screw Terminal, 3.50, 2P	/	Wurth	691214110002S
20	J5, J6	2	Header, Unshrouded , 2.54, Male, 2P	/	Wurth	61300211121
21	L1	1	Inductor, 47uH, 0.71A , SMD	4025	Wurth	74404043470A
22	L2	1	Inductor, 6.8uH, 6.4A , SMD	8040	Wurth	74437358068
23	L3	1	Inductor, 22uH, 1.11A , SMD	4025	Wurth	74404043220A
24	R1	1	Res, 220Ω	0603	Standard	Standard
25	R2, R11	2	Res, 5.1kΩ	0603	Standard	Standard
26	R3, R4, R34	3	Res, 1kΩ	0603	Standard	Standard
27	R5, R6	2	Res, 33Ω	0603	Standard	Standard
28	R7, R8, R9, R10, R12, R17, R19, R25, R41, R42, R43	11	Res, 10kΩ	0603	Standard	Standard
29	R13, R15, R35	3	Res, 0Ω	0805	Standard	Standard
30	R14, R36	0	NP	0805	Standard	Standard
31	R16, R18, R27, R28, R39, R40	6	Res, 0Ω	0603	Standard	Standard

32	R20, R22, R26	0	NP	0603	Standard	Standard
33	R21	1	Res, 200kΩ, 1%	0603	Standard	Standard
34	R23	1	Res, 16kΩ, 1%	0603	ROHM Semiconductor	KTR03EZPF1602
35	R24	1	Res, 20mΩ, 1%, 1W	0612	ROHM Semiconductor	LTR18EZPF SR020
36	R29	1	Res, 100Ω	0603	Standard	Standard
37	R30, R33	2	Res, 10kΩ, 1%	0603	ROHM Semiconductor	SFR03EZPF1002
38	R31, R32	2	Res, 20kΩ, 1%	0603	ROHM Semiconductor	SFR03EZPF2002
39	R37	1	Res, 154kΩ, 1%	0603	Standard	Standard
40	R38	1	Res, 30.1kΩ, 1%	0603	Standard	Standard
41	U1	1	IC, FT260	VQFN	FTDI	FT260
42	U2	1	IC, ACT41000	QFN 5x5-32L	Qorvo/Active-semi	ACT41000
43	U3	1	IC, MAX17580	/	Maxim	MAX17580
44	U4	1	IC, ADA4841-1YRJZ-R2	/	Analog Devices Inc	ADA4841-1YRJZ-R2
45	U5	1	IC, AD5627RBRMZ-1REEL7	/	Analog Devices Inc	AD5627RBRMZ-1REEL7
46	Vd, Vg, VIN	3	Test Point, Red	/	KeyStone	TESTPOINT 5000
47	GND, GND1, GND2	3	Test Point, Black	/	KeyStone	TESTPOINT 5001
48	PCB	1	PCB, ACT41000-104-REF01	/	/	PCB-0351-01

GUI Installation

1. Get GUI files from the Qorvo website
2. Plug the USB-TO-I2C cable into a free USB port.
3. Follow the instructions in the "How to install driver for dongle" folder.
4. Double click on the ACT41000 Power Amplifier Rev0.6.exe to start the ACT41000EVK 104 REF01.

GUI Guidelines

Refer to the separate GUI User's Guide in the downloaded GUI zip file for more information.