ACT8846

Advanced PMU for Multi-core Application Processors

FEATURES

INTEGRATED POWER SUPPLIES

- Four DC/DC Step-Down (Buck) Regulators
  - 2 x 2.8A, 2 x 1.5A
- Five Low-Noise LDOs
  - 2 x 150mA, 3 x 350mA
- Three Low-Input Voltage LDOs
  - 1 x 150mA, 2 x 350mA
- One Low IQ Keep-Alive LDO
- Backup Battery Charger

SYSTEM CONTROL AND INTERFACE

- Four General Purpose I/O with PWM Drivers
- I^2C Serial Interface
- Interrupt Controller

SYSTEM MANAGEMENT

- Reset Interface and Sequencing Controller
  - Power on Reset
  - Soft / Hard Reset
  - Watchdog Supervision
  - Multiple Sleep Modes
- Thermal Management Subsystem

APPLICATIONS

- Tablet PC
- Mobile Internet Devices (MID)
- E-books
- Personal Navigation Devices
- Smart Phones

GENERAL DESCRIPTION

The ACT8846 is a complete, cost effective, and highly-efficient ActivePMU™ power management solution optimized for the power, voltage sequencing and control requirements of Rockchip RK31x8 application processor family.

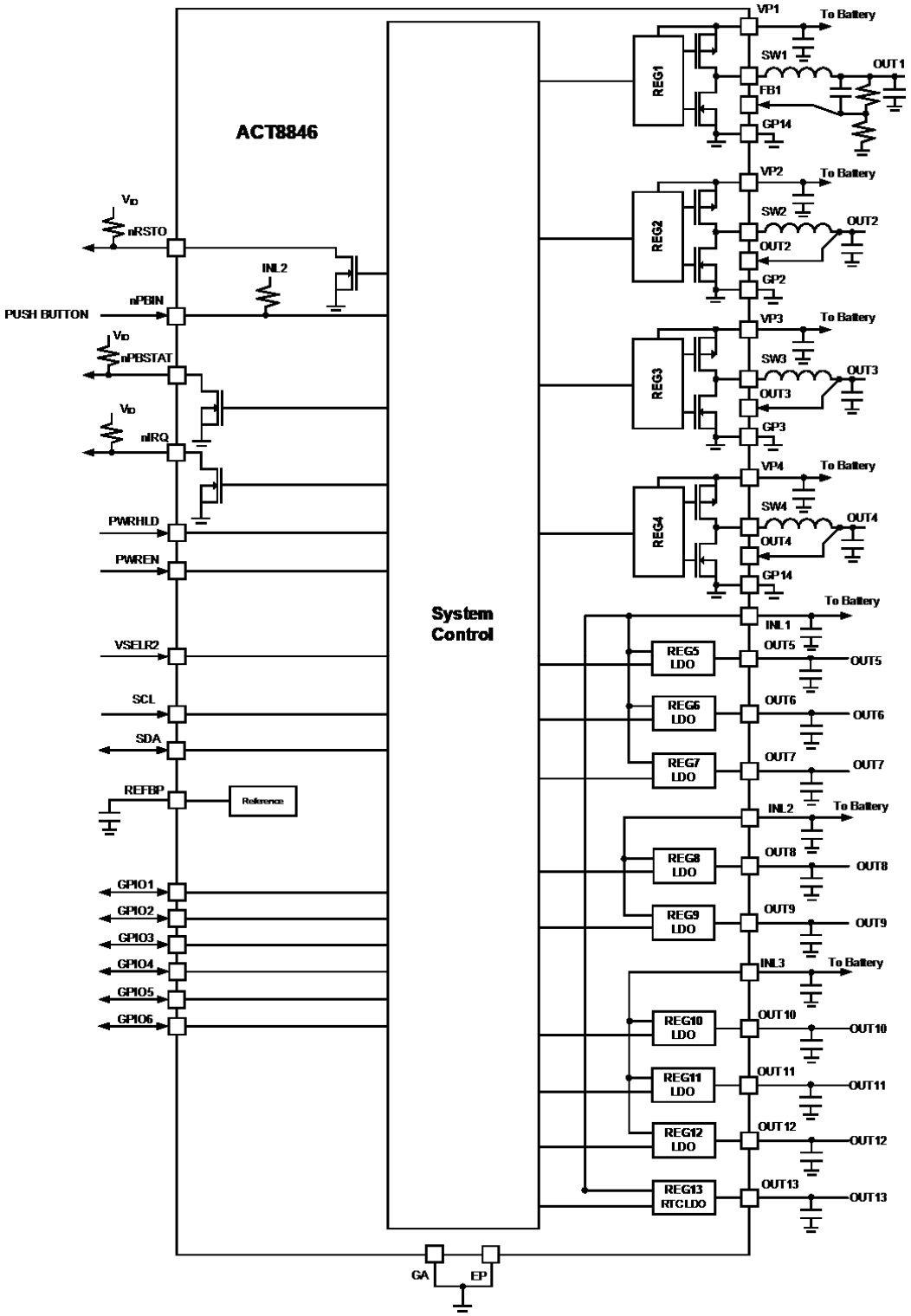
The ACT8846 features four fixed-frequency, current-mode, synchronous PWM step-down converters that achieve peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. These buck regulators supply up to 2.8A of output current and can fully satisfy the power and control requirements of the multi-core application processor. Dynamic Voltage Scaling (DVS) is supported either by dedicated control pins, or through I2C interface to optimize the energy-per-task performance for the processor. This device also include eight low-noise LDOs (up to 350mA per LDO), one always-on LDO and an integrated backup battery charger to provide a complete power system for the processor.

The power sequence and reset controller provides power-on reset, SW-initiated reset, and power cycle reset for the processor. It also features the watchdog supervisory function. Multiple sleep modes with autonomous sleep and wake-up sequence control are supported.

The thermal management and protection subsystem allows the host processor to manage the power dissipation of the PMU and the overall system dynamically. The PMU provides a thermal warning to the host processor when the temperature reaches a certain threshold such that the system can turn off some of the non-essential functions, reduce the clock frequency and etc to manage the system temperature.

The ACT8846 is available in a compact, Pb-Free and RoHS-compliant TQFN66-48 package.

FUNCTIONAL BLOCK DIAGRAM



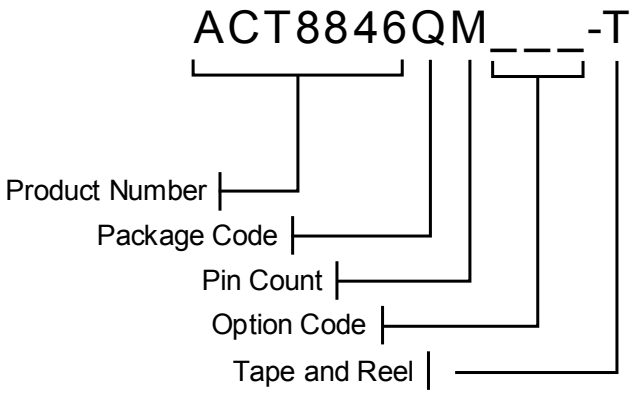
ORDERING INFORMATION①

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	V_{OUT8}	V_{OUT9}	V_{OUT10}	V_{OUT11}	V_{OUT12}	V_{OUT13}
ACT8846QM460-T	Adjustable	1.0V	1.0V	3.0V	1.0V	1.2V	1.8V	3.3V	3.3V	3.3V	1.8V	2.8V	1.8V
ACT8846QM468-T②	Adjustable	1.0V	1.0V	3.0V	1.0V	1.2V	1.8V	3.3V	3.3V	3.3V	1.8V	2.8V	1.8V
ACT8846QM490-T②	Adjustable	3.3V	1.1V	2.0V	3.3V	1.0V	3.3V	3.3V	3.3V	1.0V	1.8V	1.8V	1.8V
ACT8846QM468-T15②	Adjustable	1.0V	1.0V	3.0V	1.0V	1.2V	1.8V	3.3V	3.3V	3.3V	1.8V	2.8V	1.8V
ACT8846QM106-T	1.2V	0.95V	3.3V	1.8V	1.8V	1.8V	3.3V	1.2V	2.8V	1.5V	2.8V	1.8V	OFF
ACT8846QM108-T	1.8V	0.8V	1.125V	3.0V	1.8V	1.8V	1.8V	3.3V	3.3V	3.3V	2.5V	3.3V	1.8V
ACT8846QM109-T	1.45V	1.8V	1.1V	2.8V	2.5V	3.0V	2.5V	1.8V	3.3V	0.95V	2.8V	1.8V	1.8V
ACT8846QM111-T	1.8V	2.4V	1.2V	3.0V	3.0V	3.3V	1.8V	3.3V	3.3V	3.3V	2.5V	1.8V	1.8V
ACT8846QM112-T	1.8V	0.9V	1.2V	3.0V	3.3V	1.8V	1.8V	3.3V	3.3V	3.3V	2.5V	3.3V	1.8V
ACT8846QM113-T	1.5V	3.3V	0.85V	1.8V	0.9V	1.2V	3.3V	2.8V	1.5V	3.3V	3.3V	3.3V	1.8V
ACT8846QM114-T	1.35V	1.0V	3.3V	1.8V	3.3V	3.3V	3.3V	1.8V	1.8V	1.8V	2.5V	2.5V	1.8V

PACKAGE	PINS	TEMPERATURE RANGE
TQFN66-48	48	-40°C to +85°C

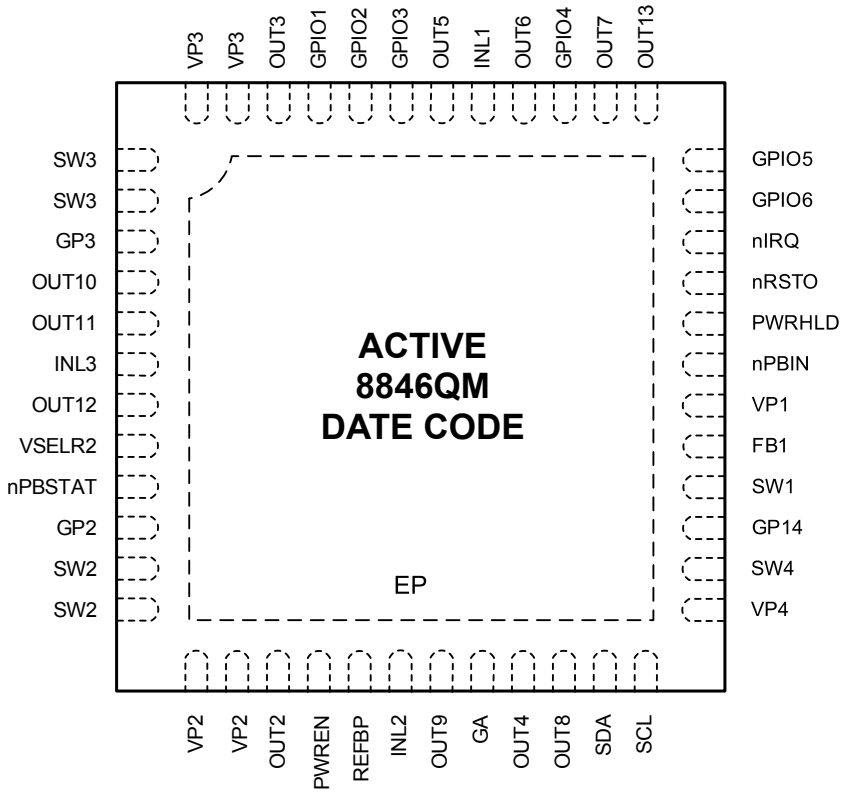
①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

②: Push button 10s shut down function is supported in ACT8846QM468-T and ACT8846QM490-T and ACT8846QM468-T15.



PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN66-48)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 2	SW3	Switch Node for REG3.
3	GP3	Power Ground for REG3. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
4	OUT10	REG10 output. Bypass it to ground with a 2.2μF capacitor.
5	OUT11	REG11 output. Bypass it to ground with a 2.2μF capacitor.
6	INL3	Power input for REG10, REG11 and REG12.
7	OUT12	REG12 output. Bypass it to ground with a 2.2μF capacitor.
8	VSELR2	Output Voltage Selection for REG2. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
9	nPBSTAT	Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise.
10	GP2	Power ground for REG2. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
11, 12	SW2	Switch Node for REG2.
13, 14	VP2	Power input for REG2. Bypass to GP2 with a high quality ceramic capacitor placed as close to the IC as possible.
15	OUT2	Output Voltage Sense for REG2.
16	PWREN	Power Enable Input for REG3. PWREN is functional only when PWRHLD is driven high. Drive PWREN to a logic high to turn on the REG3. Drive PWREN to a logic low to turn off the REG3.
17	REFBP	Reference Bypass. Connect a 0.047μF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
18	INL2	Power Input for REG8, REG9.
19	OUT9	REG9 output. Bypass it to ground with a 2.2μF capacitor.
20	GA	Analog Ground.
21	OUT4	Output voltage sense for REG4.
22	OUT8	REG8 output. Bypass it to ground with a 2.2μF capacitor.
23	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.
24	SCL	Clock Input for I^2C Serial Interface.
25	VP4	Power input for REG4. Bypass to GP14 with a high quality ceramic capacitor placed as close to the IC as possible.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
26	SW4	Switch Node for REG4.
27	GP14	Power Ground for REG1 and REG4. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
28	SW1	Switch Node for REG1.
29	FB1	Output Feedback Sense for REG1. For the adjustable output voltage options, connect this pin to the center of the output feedback resistor divider for voltage setting, connect this pin to the output directly to regulate the output voltage at 1.2V.
30	VP1	Power Input for REG1. Bypass to GP14 with a high quality ceramic capacitor placed as close to the IC as possible.
31	nPBIN	Master Enable Input. Drive nPBIN to GA through a 50kΩ resistor for 32ms to enable the IC. Drive nPBIN to GA through a 50kΩ resistor for 10 seconds to disable the IC.① Drive nPBIN directly to GA to assert a Manual-Reset condition.
32	PWRHLD	Power Hold Input, enable input for REG1, REG2, REG4, REG5, REG6, REG8 and REG10. PWRHLD is internally pulled down to GA through a 900kΩ resistor.
33	nRSTO	Open-Drain Reset Output.
34	nIRQ	Open-Drain Interrupt Output.
35	GPIO6	General Purpose I/O #6. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Drive section for more information.
36	GPIO5	General Purpose I/O #5. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Driver section for more information.
37	OUT13	REG13 output. Bypass it to ground with a 0.47μF capacitor.
38	OUT7	REG7 output. Bypass it to ground with a 2.2μF capacitor.
39	GPIO4	General Purpose I/O #4. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Driver section for more information.
40	OUT6	REG6 output. Bypass it to ground with a 2.2μF capacitor.
41	INL1	Power Input for REG5, REG6, REG7.
42	OUT5	REG5 output. Bypass it to ground with a 2.2μF capacitor.
43	GPIO3	General Purpose I/O #3. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the PWM LED Drier section for more information.
44	GPIO2	General Purpose I/O #2. Configured as VSELR4 for Voltage Selection of REG4. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
45	GPIO1	General Purpose I/O #1. Configured as VSELR3 for Voltage Selection of REG3. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
46	OUT3	Output Voltage Sense for REG3.
47,48	VP3	Power input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

①: Only for ACT8846QM468

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
INL1, INL2, INL3 to GA; VP1, SW1, FB1 to GP14; VP2, SW2, OUT2 to GP2; VP3, SW3, OUT3 to GP3; VP4, SW4, OUT4 to GP14	-0.3 to 6	V
GP14, GP2, GP3 to GA	-0.3 to + 0.3	V
OUT5, OUT6, OUT7, OUT13 TO GA	-0.3 to INL1 + 0.3	V
OUT8, OUT9, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, VSELR2, nPBIN, nRSTO, nIRQ, nPBSTAT, PWREN, PWRHLD, REFBP, SCL, SDA to GA	-0.3 to INL2 + 0.3	V
OUT10, OUT11, OUT12 to GA	-0.3 to INL3 + 0.3	V
Junction to Ambient Thermal Resistance	21	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

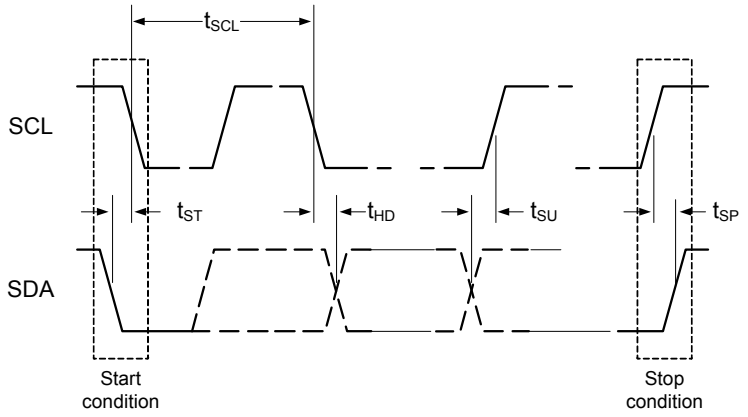
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{INL2} = 3.1V to 5.5V, T_A = -40°C to 85°C			0.35	V
SCL, SDA Input High	V_{INL2} = 3.1V to 5.5V, T_A = -40°C to 85°C	1.55			V
SDA Leakage Current				1	µA
SCL Leakage Current				1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1: I²C Compatible Serial Bus Timing



GLOBAL REGISTER MAP

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	nBAT-LEVMSK	nBATSTAT	VBATDAT	Reserved	BATLEV[3]	BATLEV[2]	BATLEV[1]	BATLEV[0]
		DEFAULT①	0	R	R	R	0	1	0	0
SYS	0x01	NAME	nTMSK	TSTAT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		DEFAULT①	0	R	0	0	0	0	0	0
REG1	0x12	NAME	ON	Reserved	Reserved	Reserved	Reserved	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	1	0	0	R
REG2	0x20	NAME	Reserved	Reserved	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	0	0	0	0
REG2	0x21	NAME	Reserved	Reserved	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	0	0	0	0
REG2	0x22	NAME	ON	Reserved	Reserved	Reserved	Reserved	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	1	0	0	R
REG3	0x30	NAME	Reserved	Reserved	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	0	0	0	0
REG3	0x31	NAME	Reserved	Reserved	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	0	0	0	0
REG3	0x32	NAME	ON	Reserved	Reserved	Reserved	Reserved	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	1	1	1	0	R
REG4	0x40	NAME	Reserved	Reserved	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	1	1	0	1	1	0
REG4	0x41	NAME	Reserved	Reserved	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	1	1	0	1	1	0
REG4	0x42	NAME	ON	Reserved	Reserved	Reserved	Reserved	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	1	1	0	R
REG5	0x50	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	0	1	0	0	0	0

①: Default values of ACT8846QM468-T.

GLOBAL REGISTER MAP CONT'D

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
REG5	0x51	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	1	1	0	R
REG6	0x58	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	0	1	1	0	0	0
REG6	0x59	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	0	1	0	0	1	1	0	R
REG7	0x60	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	0	0	1	0	0
REG7	0x61	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	0	1	0	0	1	1	0	R
REG8	0x68	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	1	0	0	1
REG8	0x69	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	0	1	0	0	1	1	0	R
REG9	0x70	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	1	0	0	1
REG9	0x71	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	0	1	0	0	1	1	0	R
REG10	0x80	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	1	0	0	1
REG10	0x81	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	0	1	0	0	1	1	0	R
REG11	0x90	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	0	0	1	0	0
REG11	0x91	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	1	1	0	R

①: Default values of ACT8846QM468-T.

GLOBAL REGISTER MAP CONT'D

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
REG12	0xA0	NAME	Reserved	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	0	1	0	0
REG12	0xA1	NAME	ON	Reserved	Reserved	Reserved	Reserved	DIS	nFLTMSK	OK
		DEFAULT①	0	1	0	0	1	1	0	R
REG13	0xB1	NAME	ON	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		DEFAULT①	1	0	0	0	0	0	0	0
PB	0xC0	NAME	PBAMSK	PBDMSK	Reserved	Reserved	Reserved	Reserved	WDSREN	WDPCEN
		DEFAULT①	0	0	0	0	0	0	0	0
PB	0xC1	NAME	INTADR [7]	INTADR [6]	INTADR [5]	INTADR [4]	INTADR [3]	INTADR [2]	INTADR [1]	INTADR [0]
		DEFAULT①	R	R	R	R	R	R	R	R
PB	0xC2	NAME	PBASTAT	PBDSTAT	PBDAT	Reserved	Reserved	Reserved	Reserved	Reserved
		DEFAULT①	R	R	R	R	R	R	R	R
PB	0xC3	NAME	Reserved	Reserved	Reserved	OFFSYS	OFFSYSCLR	Reserved	Reserved	SIPC
		DEFAULT①	0	0	0	0	0	0	0	0
PB	0xC5	NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PCSTAT	SRSTAT
		DEFAULT①	0	0	0	0	0	0	R	R
GPIO6	0xE3	NAME	PWM6EN	FRE6[2]	FRE6[1]	FRE6[0]	DUTY6[3]	DUTY6[2]	DUTY6[1]	DUTY6[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO5	0xE4	NAME	PWM5EN	FRE5[2]	FRE5[1]	FRE5[0]	DUTY5[3]	DUTY5[2]	DUTY5[1]	DUTY5[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO3	0xF4	NAME	PWM3EN	FRE3[2]	FRE3[1]	FRE3[0]	DUTY3[3]	DUTY3[2]	DUTY3[1]	DUTY3[0]
		DEFAULT①	1	1	0	1	0	1	1	1
GPIO4	0xF5	NAME	PWM4EN	FRE4[2]	FRE4[1]	FRE4[0]	DUTY4[3]	DUTY4[2]	DUTY4[1]	DUTY4[0]
		DEFAULT①	0	0	0	0	0	0	0	0

①: Default values of ACT8846QM468-T.

REGISTER AND BIT DESCRIPTIONS

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	nBATLEVMSK	R/W	Battery Voltage Level Interrupt Mask. Set this bit to 1 to unmask the interrupt. See the Programmable Battery Voltage Monitor section for more information
SYS	0x00	[6]	nBATSTAT	R	Battery Voltage Status. Value is 1 when BATLEV interrupt is generated, value is 0 otherwise.
SYS	0x00	[5]	VBATDAT	R	Battery Voltage Monitor real time status. Value is 1 when VBAT < BATLEV, value is 0 otherwise.
SYS	0x00	[4]	-	R/W	Reserved.
SYS	0x00	[3:0]	BATLEV	R/W	Battery Voltage Detect Threshold. Defines the BATLEV voltage threshold. See the Programmable Battary Voltage Monitor section for more information.
SYS	0x01	[7]	nTMSK	R/W	Thermal Interrupt Mask. Set this bit to 1 to unmask the interrupt.
SYS	0x01	[6]	TSTAT	R	Thermal Interrupt Status. Value is 1 when a thermal interrupt is generated, value is 0 otherwise.
SYS	0x01	[5:0]	-	R/W	Reserved.
REG1	0x12	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x12	[6:3]	-	R	Reserved.
REG1	0x12	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x12	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x12	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x20	[7:6]	-	R	Reserved.
REG2	0x20	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the Output Voltage Programming section for more information
REG2	0x21	[7:6]	-	R	Reserved.
REG2	0x21	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the Output Voltage Programming section for more information.
REG2	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x22	[6:3]	-	R	Reserved.
REG2	0x22	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG2	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG2	0x22	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG3	0x30	[7:6]	-	R	Reserved.
REG3	0x30	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the Output Voltage Programming section for more information
REG3	0x31	[7:6]	-	R	Reserved.
REG3	0x31	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the Output Voltage Programming section for more information.
REG3	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x32	[6:3]	-	R	Reserved.
REG3	0x32	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG3	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x32	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x40	[7:6]	-	R	Reserved.
REG4	0x40	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the Output Voltage Programming section for more information
REG4	0x41	[7:6]	-	R	Reserved.
REG4	0x41	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the Output Voltage Programming section for more information.
REG4	0x42	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG4	0x42	[6:3]	-	R	Reserved.
REG4	0x42	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG4	0x42	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG4	0x42	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG5	0x50	[7:6]	-	R	Reserved.
REG5	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG5	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x51	[6:3]	-	R	Reserved.
REG5	0x51	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x51	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x58	[7:6]	-	R	Reserved.
REG6	0x58	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG6	0x59	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG6	0x59	[6:3]	-	R	Reserved.
REG6	0x59	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x59	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x59	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG7	0x60	[7:6]	-	R	Reserved.
REG7	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG7	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x61	[6:3]	-	R	Reserved.
REG7	0x61	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x61	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG8	0x68	[7:6]	-	R	Reserved.
REG8	0x68	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG8	0x69	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG8	0x69	[6:3]	-	R	Reserved.
REG8	0x69	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG8	0x69	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG8	0x69	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG9	0x70	[7:6]	-	R	Reserved.
REG9	0x70	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG9	0x71	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG9	0x71	[6:3]	-	R	Reserved.
REG9	0x71	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG9	0x71	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG9	0x71	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG10	0x80	[7:6]	-	R	Reserved.
REG10	0x80	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG10	0x81	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG10	0x81	[6:3]	-	R	Reserved.
REG10	0x81	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG10	0x81	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG10	0x81	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG11	0x90	[7:6]	-	R	Reserved.
REG11	0x90	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG11	0x91	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG11	0x91	[6:3]	-	R	Reserved.
REG11	0x91	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG11	0x91	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG11	0x91	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG12	0xA0	[7:6]	-	R	Reserved.
REG12	0xA0	[5:0]	VSET	R/W	Output Voltage Selection. See the Output Voltage Programming section for more information.
REG12	0xA1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG12	0xA1	[6:3]	-	R	Reserved.
REG12	0xA1	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG12	0xA1	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG12	0xA1	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG13	0xB1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG13	0xB1	[6:0]	-	R	Reserved.
PB	0xC0	7	nPBAMSK	R/W	nPBIN Assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is asserted.
PB	0xC0	6	nPBDMSK	R/W	nPBIN De-assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is de-asserted.
PB	0xC0	[5:2]	-	R	Reserved.
PB	0xC0	1	WDSREN	R/W	Watchdog Soft-Reset Enable. Set this bit to 1 to enable watchdog function. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
PB	0xC0	[5:2]	-	R	Reserved.
PB	0xC0	1	WDSREN	R/W	Watchdog Soft-Reset Enable. Set this bit to 1 to enable watchdog function. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC0	0	WDPCEN	R/W	Watchdog Power-Cycle Enable. Set this bit to 1 to enable watchdog function. When watchdog timer expires, the PMU commence a power cycle. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC1	[7:0]	INTADR	R	Interrupt Address. It holds the address of the block that triggers the interrupt. This byte defaults to 0xFF and is automatically set to 0xFF after being read. Bit 7 is the MSB while Bit 0 is the LSB.
PB	0xC2	7	PBASTAT	R	nPBIN Assertion Interrupt Status. The value of this bit is 1 if the nPBIN Assertion Interrupt is triggered.
PB	0xC2	6	PBDSTAT	R	nPBIN De-assertion Interrupt Status. The value of this bit is 1 if the nPBIN De-assertion Interrupt is triggered.
PB	0xC2	5	PBASTAT	R	nPBIN Status bit. This bit contains the real-time status of the nPBIN pin. The value of this bit is 1 if nPBIN is asserted, and is 0 if nPBIN is de-asserted.
PB	0xC2	[4:0]	-	R	Reserved.
PB	0xC3	[7:5]	-	R	Reserved.
PB	0xC3	[4]	OFFSYS	R/W	Global Off Control. Set OFFSYSCLR[ ] to 1 first, then set this bit to 1 to turn off all outputs.
PB	0xC3	[3]	OFFSYSCLR	R/W	Global Off Control State Clear bit. Set bit to 1, then set OFFSYS[ ] to 1 to turn off all outputs.
PB	0xC3	[2:1]	-	R	Reserved.
PB	0xC3	0	SIPC	R/W	Software Initiated Power Cycle. When this bit is set, the PMU commences a power cycle after 8ms delay.
PB	0xC5	[7:2]	-	R	Reserved.
PB	0xC5	1	PCSTAT	R/W	Power-cycle Flag. The value of this bit is 1 after a power cycle. This bit is automatically cleared to 0 after read.
PB	0xC5	0	SRSTAT	R/W	Soft-reset Flag. The value of this bit is 1 after a soft-reset. This bit is automatically cleared to 0 after read.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
GPIO6	0xE3	[7]	PWM6EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO6.
GPIO6	0xE3	[6:4]	FRE6	R/W	PWM Frequency Selection Bits for GPIO6. See the Table 6 for code to frequency cross.
GPIO6	0xE3	[3:0]	DUTY6	R/W	Duty Cycle Selection Bits for GPIO6. See the Table 7 for code to duty cross.
GPIO5	0xE4	[7]	PWM5EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO5.
GPIO5	0xE4	[6:4]	FRE5	R/W	PWM Frequency Selection Bits for GPIO5. See the Table 6 for code to frequency cross.
GPIO5	0xE4	[3:0]	DUTY5	R/W	Duty Cycle Selection Bits for GPIO5. See the Table 7 for code to duty cross.
GPIO3	0xF4	[7]	PWM3EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO3.
GPIO3	0xF4	[6:4]	FRE3	R/W	PWM Frequency Selection Bits for GPIO3. See the Table 6 for code to frequency cross.
GPIO3	0xF4	[3:0]	DUTY3	R/W	Duty Cycle Selection Bits for GPIO3. See the Table 7 for code to duty cross.
GPIO4	0xF5	[7]	PWM4EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO4.
GPIO4	0xF5	[6:4]	FRE4	R/W	PWM Frequency Selection Bits for GPIO4. See the Table 6 for code to frequency cross.
GPIO4	0xF5	[3:0]	DUTY4	R/W	Duty Cycle Selection Bits for GPIO4. See the Table 7 for code to duty cross.

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		3.0		5.5	V
UVLO Threshold Voltage	V_{INL2} Rising, BATLEV[3:0]=0001	2.6	2.8	3.0	V
UVLO Hysteresis	V_{INL2} Hysteresis		200		mV
Operating Supply Current	All Regulators Enabled but no load		0.6	1.2	mA
Shutdown Supply Current	All Regulators Disabled except REG13		10	20	μA
Oscillator Frequency		2.0	2.25	2.5	MHz
Logic High Input Voltage①		1.4			V
Logic Low Input Voltage				0.4	V
Leakage Current	V[nIRQ] = V[nRSTO] = 4.2V			1	μA
Low Level Output Voltage	nIRQ, nRSTO, ISINK = 5mA			0.3	V
nRSTO Delay			100②		ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

①: PWRHLD, PWREN, VSELR2, GPIO1, GPIO2 are logic inputs.

②: Typical value shown. Actual value may vary from (T-1ms) x 85% to T x 115%, where T = 100ms.

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = V_{VP4} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO Hysteresis	Input Voltage Falling		100		mV
Standby Supply Current	V_{OUT} = 103%, Regulator Enabled		72	100	μA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	2	μA
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1%	V_{NOM}①	1%	V
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{VP} = Max (V_{NOM}① +1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation REG1/4	I_{OUT} = 10mA to IMAX②		1.70		%/A
Load Regulation REG2/3	I_{OUT} = 10mA to IMAX②		1.00		%/A
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2		%V_{NOM}
Switching Frequency	V_{OUT} ≥ 20% of V_{NOM}	2	2.25	2.5	MHz
	V_{OUT} = 0V		550		kHz
Soft-Start Period			400		μs
Minimum On-Time			75		ns
REG1 AND REG4					
Maximum Output Current		1.5			A
Current Limit		1.8	2.2	2.7	A
PMOS On-Resistance	I_{SW} = -100mA		0.11		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	μA
Input Capacitor			4.7		μF
Output Capacitor			33		μF
Power Inductor		1.0	2.2	3.3	μH
REG2 AND REG3					
Maximum Output Current		2.8			A
Current Limit		3.5	4.2		A
PMOS On-Resistance	I_{SW} = -100mA		0.07		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	μA
Input Capacitor			10		μF
Output Capacitor			44		μF
Power Inductor		0.5	1	22	μH

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the Ordering Information section.

②: IMAX Maximum Output Current.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = V_{INL2} = 3.6V, C_{OUT5} = C_{OUT6} = C_{OUT7} = C_{OUT8} = C_{OUT9} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.5		5.5	V
Operating Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM}①	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		75		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		65		
Supply Current per Output	Regulator Enabled		25		μA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		140		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} FALLING		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		μV_{RMS}
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 150mA (REG5 & REG6)					
Dropout Voltage③	I_{OUT} = 80mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		150			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	180			mA
Recommend Output Capacitor			2.2		μF
LDO rated at 350mA (REG7, REG8 & REG9)					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		350			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		μF

①: VNOM refers to the nominal output voltage level for VOUT as defined by the Ordering Information section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ.)

LOW-INPUT VOLTAGE LDO ELECTRICAL CHARACTERISTICS

(V_{INL3} = 3.6V, C_{OUT10} = C_{OUT11} = C_{OUT12} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.7		5.5	V
Operating Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM}①	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		50		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		40		
Supply Current per Output	Regulator Enabled		22		μA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		100		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} FALLING		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		μV_{RMS}
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 150mA (REG10)					
Dropout Voltage③	I_{OUT} = 80mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		150			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	180			mA
Recommend Output Capacitor			2.2		μF
LDO rated at 350mA (REG11, REG12)					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		350			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ)

LOW-POWER(ALWAYS-ON) LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = 3.6V, C_{OUT13} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
REG13 — V_{NOM} = 1.8V					
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy		-3	V_{NOM}①	3	%
Line Regulation	V_{INL1} = Max (V_{OUT} + 0.2V, 2.5V) to 5.5V		13		mV
Supply Current from V_{INL1}			5		μA
Maximum Output current		50			mA
Recommend Output Capacitor		0.47			μF

PWM LED DRIVER ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

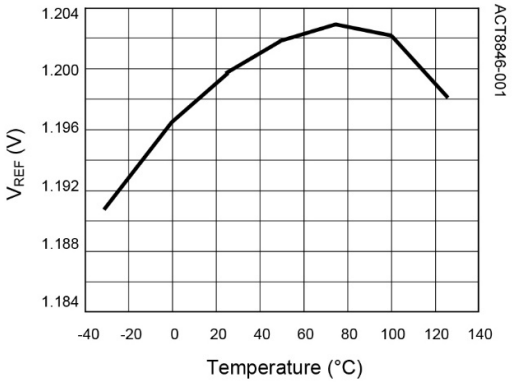
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Current	100% Duty Cycle	6	10	16	mA
Output Low Voltage	Feed in with 6mA			0.35	V
Leakage Current	Sinking from 5.5V source			1	μA
PWM Frequency	FRE[2:0] = 000		0.25		Hz
PWM Duty Adjustment	DUTY[3:0] = 0000 to 1111	6.26		100	%

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the Ordering Information section.

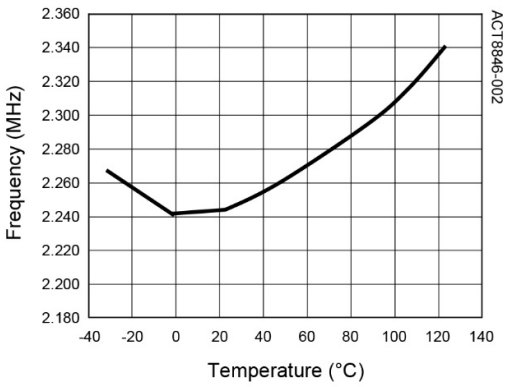
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise specified.)

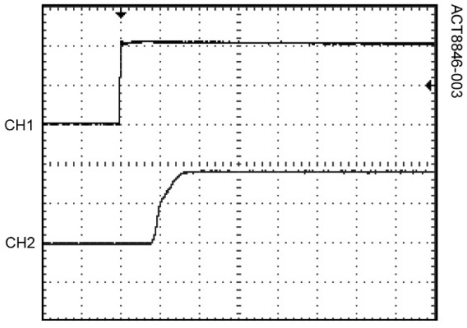
V_{REF} vs. Temperature



Frequency vs. Temperature

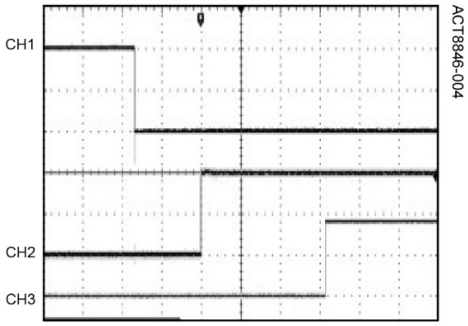


Startup of VIN/OUT13



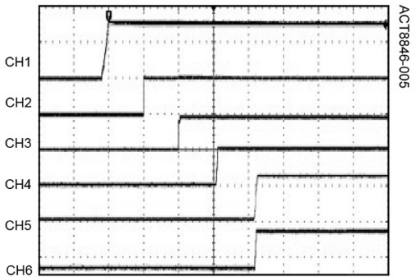
CH1: V_{VIN}, 2V/div
CH2: V_{OUT13}, 1V/div
TIME: 500μs/div

Startup of nPBIN/OUT5/nRSTO



CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT5}, 500mV/div
CH3: V_{nRSTO}, 1V/div
TIME: 20ms/div

Startup of OUT4/OUT5/OUT11/OUT3/ OUT1/OUT2

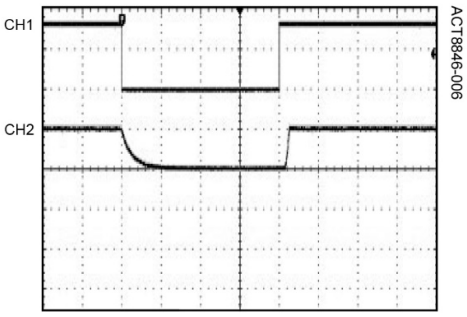


CH1: V_{OUT4}, 2V/div
CH2: V_{OUT5}, 1V/div
CH3: V_{OUT11}, 2V/div
CH4: V_{OUT3}, 1V/div
CH5: V_{OUT1}, 1V/div
CH6: V_{OUT2}, 1V/div
TIME: 2ms/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

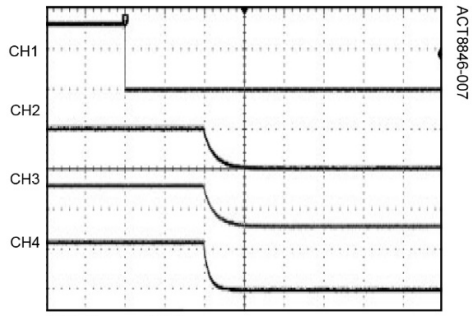
(T_A = 25°C, unless otherwise specified.)

Sleep of PWREN/OUT3



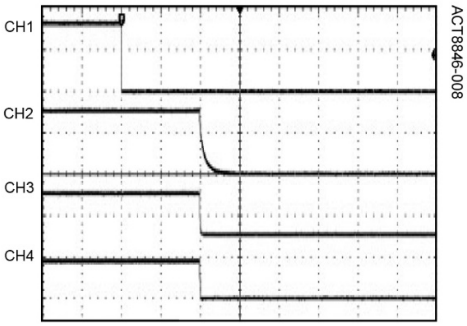
CH1: V_{PWREN}, 2V/div
CH2: V_{OUT3}, 1VV/div
TIME: 1ms/div

Shutdown of PWRHLD/OUT3/OUT2/OUT1



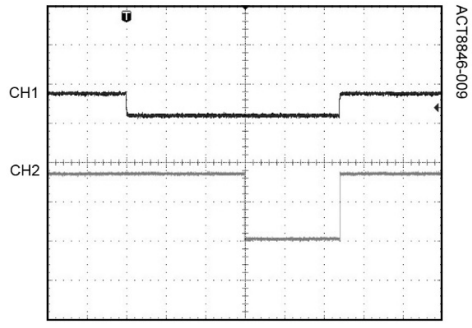
CH1: V_{PWRHLD}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT2}, 1V/div
CH4: V_{OUT1}, 1V/div
TIME: 1ms/div

Shutdown of PWRHLD/OUT4/OUT5/OUT11



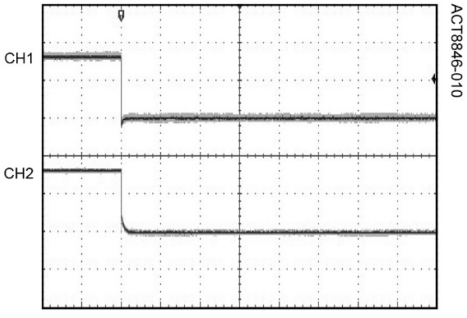
CH1: V_{PWRHLD}, 2V/div
CH2: V_{OUT4}, 2V/div
CH3: V_{OUT5}, 1V/div
CH4: V_{OUT11}, 2V/div
TIME: 1ms/div

nPBIN and nPBSTAT



CH1: V_{nPBIN}, 2V/div
CH2: $V_{nPBSTAT}$, 2V/div
TIME: 10ms/div

Shutdown of PWRHOLD and nRSTO

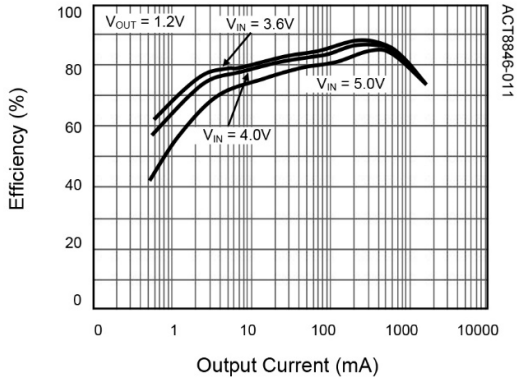


CH1: $V_{PWRHOLD}$, 2V/div
CH2: V_{nRSTO}, 2V/div
TIME: 2ms/div

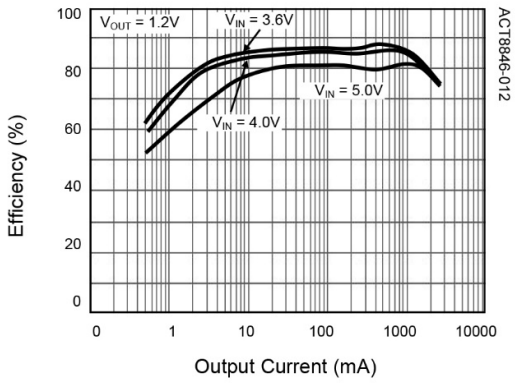
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

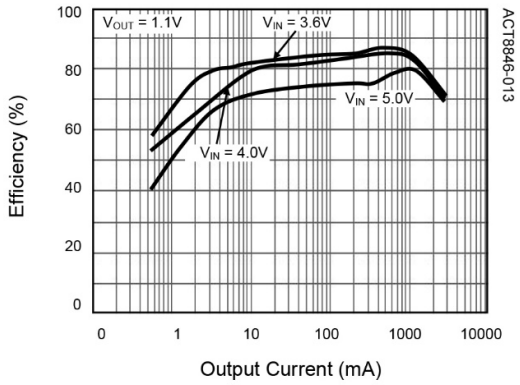
REG1 Efficiency vs. Output Current



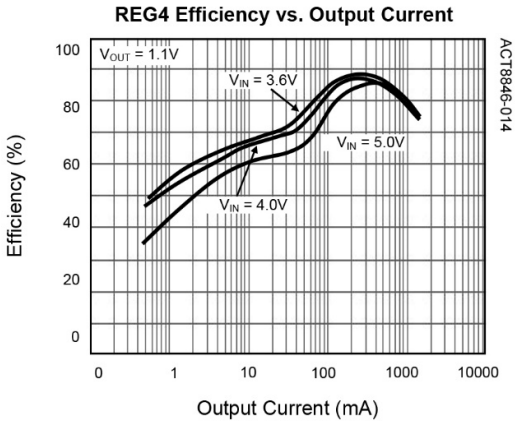
REG2 Efficiency vs. Output Current



REG3 Efficiency vs. Output Current



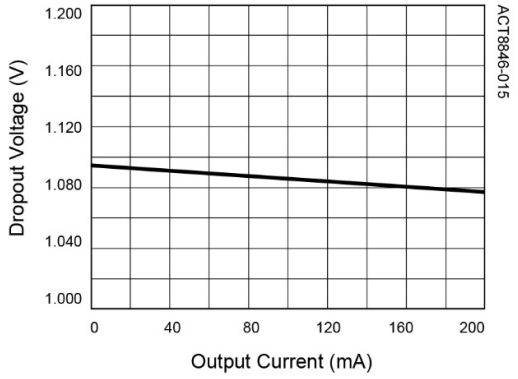
REG4 Efficiency vs. Output Current



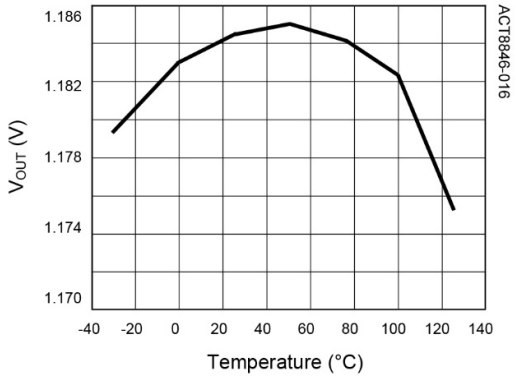
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

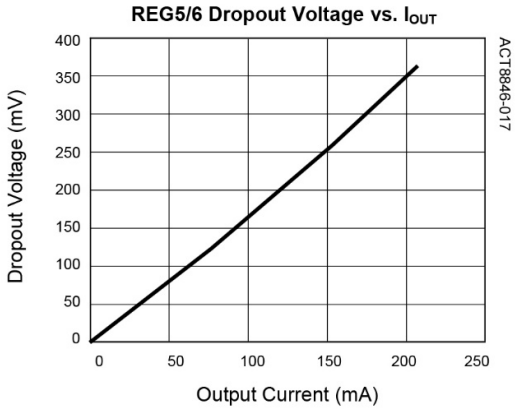
REG5 V_{OUT} vs. I_{OUT}



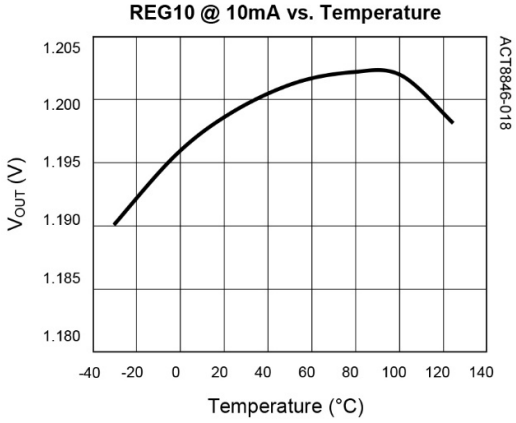
V_{OUT10} @ 150mA vs. Temperature



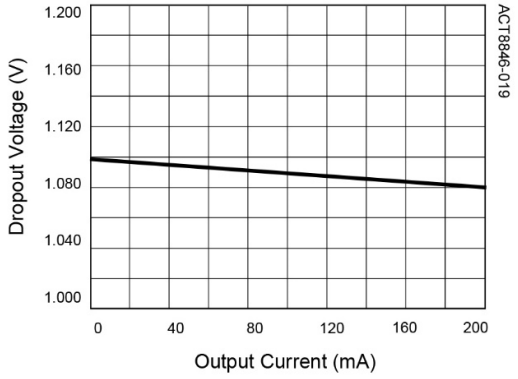
REG5/6 Dropout Voltage vs. I_{OUT}



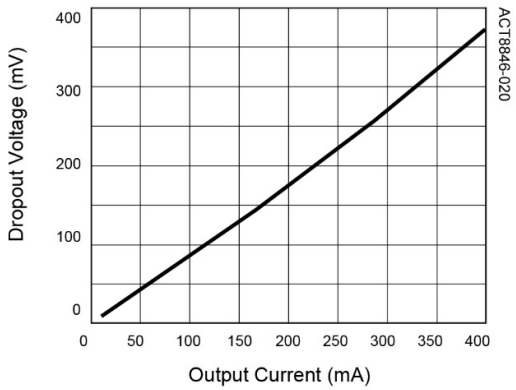
REG10 @ 10mA vs. Temperature



REG6 V_{OUT} vs. I_{OUT}



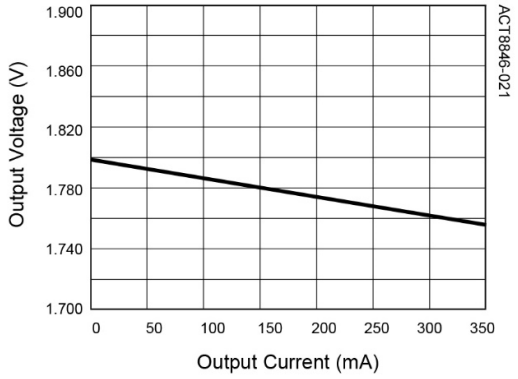
REG7/8/9 Dropout Voltage vs. I_{OUT}



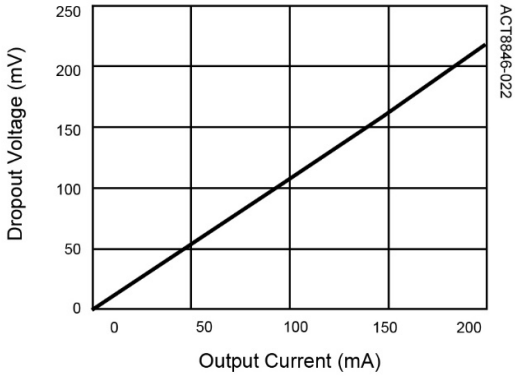
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

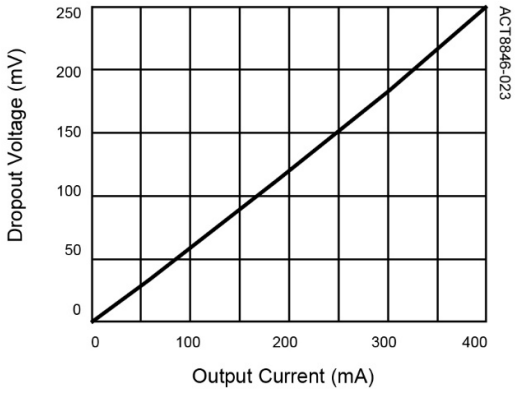
REG8 V_{OUT} vs. I_{OUT}



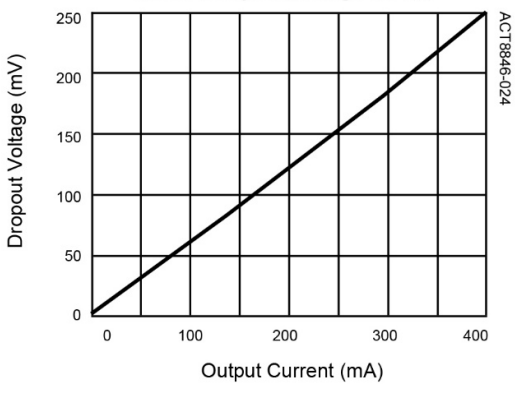
REG10 Dropout Voltage vs. I_{OUT}



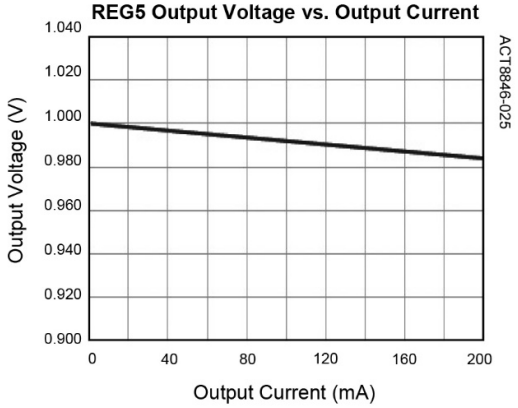
REG11 Dropout Voltage vs. I_{OUT}



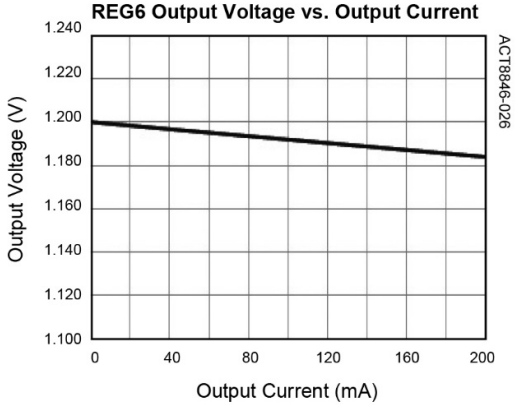
REG12 Dropout Voltage vs. I_{OUT}



REG5 Output Voltage vs. Output Current



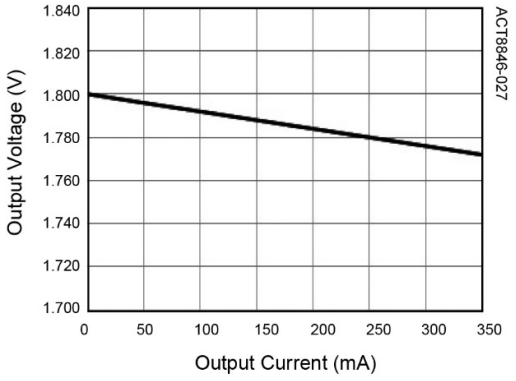
REG6 Output Voltage vs. Output Current



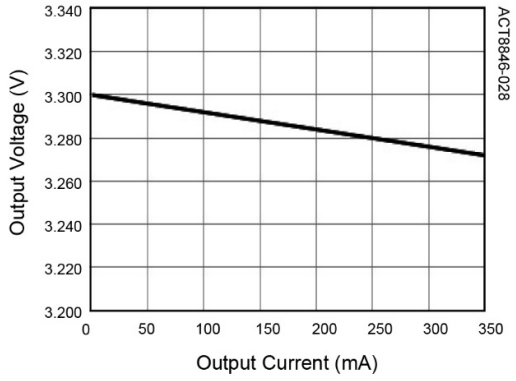
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

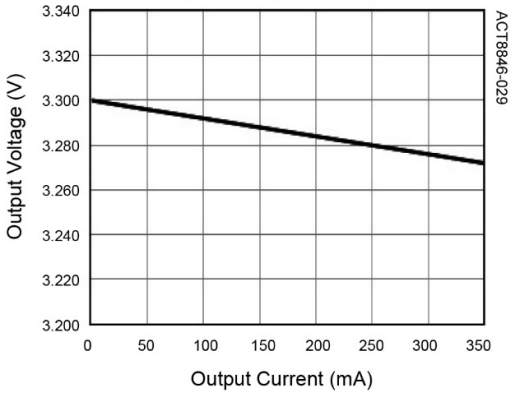
REG7 Output Voltage vs. Output Current



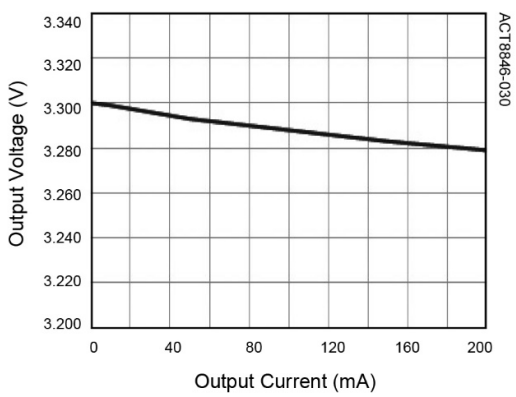
REG8 Output Voltage vs. Output Current



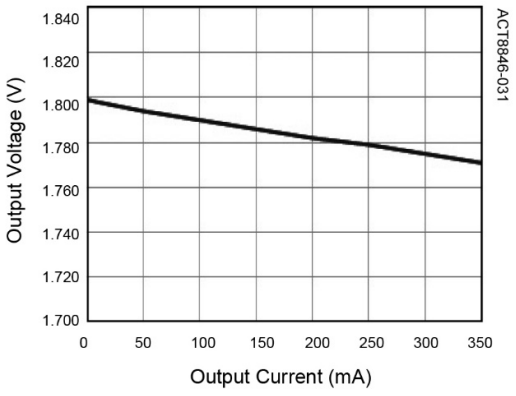
REG9 Output Voltage vs. Output Current



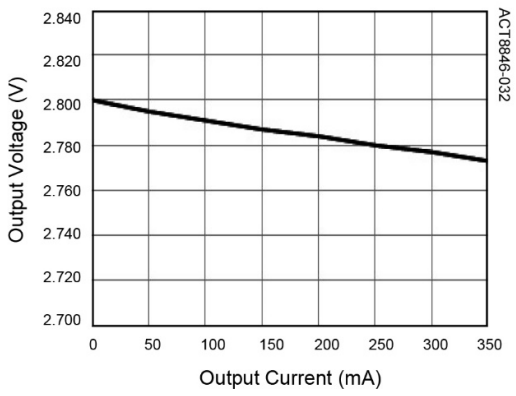
REG10 Output Voltage vs. Output Current



REG11 Output Voltage vs. Output Current



REG12 Output Voltage vs. Output Current



SYSTEM CONTROL INFORMATION

Interfacing with the Rockchip RK31x8 processors

The ACT8846 is optimized for the Rockchip RK31x8 processors, supporting both the power domains as well as the signal interface. The following paragraphs describe how to design ACT8846 with the RK31x8 processors.

While the ACT8846 supports many possible configurations for powering these processors, one of the most common configurations is detailed in this datasheet. In general, this document refers to the ACT8846 pin names and functions. However, in cases where the description of interconnections between these devices benefits by doing so, both the ACT8846 pin names and the RK31x8 processors pin names are provided. When this is done, the RK31x8 pin names are located after the ACT8846 pin names, and are italicized and located inside parentheses. For example, PWREN (GPIOX) refers to the logic signal applied to the ACT8846's PWREN input, identifying that it is driven from the RK31x8's GPIOX output.

Table 1:
ACT8846 and Rockchip RK31x8 Power Domains

ACT8846 Regulator	Power Domain	DEFAULT VOLTAGE	MAX CURRENT	POWER UP ORDER	ON/OFF @ SLEEP	TYPE
REG1	VCC_DDR	Adjustable	1.5A	5	ON	DC/DC Step Down
REG2	VDD_LOG	1.0V	2.8A	5	ON	DC/DC Step Down
REG3	VDD_ARM	1.0V	2.8A	4	OFF	DC/DC Step Down
REG4	VCC_IO	3.0V	1.5A	1	ON	DC/DC Step Down
REG5	VDD_10	1.0V	150mA	2	ON	Low-Noise LDO
REG6	VDD_JETTA1V2	1.2V	150mA	/	OFF	Low-Noise LDO
REG7	VCC18_CIF	1.8V	350mA	/	OFF	Low-Noise LDO
REG8	VCCA_33	3.3V	350mA	/	OFF	Low-Noise LDO
REG9	VCC_TP	3.3V	350mA	/	OFF	Low-Noise LDO
REG10	VCC_JETTA3V3	3.3V	150mA	/	OFF	Low Input-Voltage LDO
REG11	VCC18_IO	1.8V	350mA	3	ON	Low Input-Voltage LDO
REG12	VCC28_CIF	2.8V	350mA	/	OFF	Low Input-Voltage LDO
REG13	VDD_RTC	1.8V	50mA	0	ON	Always-ON LDO

Table 2:
ACT8846 and Rockchip RK31x8 Power Mode

Power Mode	Control State	Power Domain State	Quiescent Current
ALL ON	PWRHLD is asserted, PWREN is asserted	All Regulators ON	0.6mA
SHUTDOWN	PWRHLD is de-asserted, PWREN is de-asserted, VINL2 > 2.6V	REG13 is ON, all other regulators are off.	10µA
ALL OFF	PWRHLD is de-asserted, PWREN is de-asserted, VINL2 < 2.2V	All regulators off.	5 µA

Table 3:
ACT8846 and RK31x8 Signal Interface①

ACT8846	DIRECTION	ROCKCHIP RK31x8
PWREN	←	GPIO6_B1
SCL	←	I2C1_SCL
SDA	↔	I2C1_SDA
VSELR2	←	GPIO0_D7
GPIO1/VSELR3	←	GPIO0_D6
nRSTO	→	NPOR
nIRQ	→	GPIO6_A4
nPBSTAT	→	GPIO6_A2
PWRHLD	←	GPIO6_B0

Note: Typical connections shown, actual connections may vary.

Control Signals

Enable inputs

The ACT8846 features a variety of control inputs, which are used to enable and disable outputs depending upon the desired mode of operation. PWRHLD is a logic inputs, while nPBIN is a unique, multi-function input.

nPBIN Multi-Function Input

The ACT8846 features the nPBIN multi-function pin, which combines system enable/disable control with a hardware reset function. Select either of the two pin functions by asserting this pin, either through a direct connection to GA as Manual Reset input, or through a 50kΩ resistor to GA for 32ms to enable the IC, or through a 50kΩ resistor to GA for 10s to disable the IC①, as shown in Figure 2.

Manual Reset Function

The second major function of the nPBIN input is to provide a manual-reset input for the processor. To manually-reset the processor, drive nPBIN directly to GA through a low impedance (less than 2.5kΩ). An internal timer detects the duration of the MR event:

Short Press / Soft-Reset:②

If the Manual Reset button is asserted for less than 4s③/10s①, ACT8846 commences a soft-reset operation where nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires. A status bit, SRSTAT[ ], is set after a soft-reset event. The SRSTAT[ ] bit is automatically cleared to 0 after read. After Short Press, set WDSREN[ ] to 1 about 1s after nRSTO de-assert then clear WDSREN[ ] for properly shutdown sequence.

Long Press / Power-cycle:

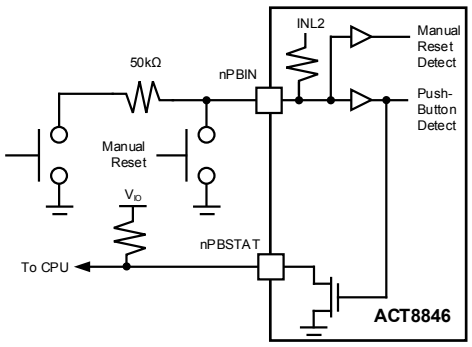
If the Manual Reset button is asserted for more than 4s③/10s①, ACT8846 commences a power cycle routine in which case all regulators are turned off and then turned back on. A status bit, PCSTAT[ ], is set after the power cycle. The PCSTAT[ ] bit is automatically cleared to 0 after read.

nPBSTAT Output

nPBSTAT is an open-drain output that reflects the state of the nPBIN input; nPBSTAT is asserted low whenever nPBIN is asserted, and is high-Z otherwise. This output is typically used as an interrupt signal to the processor, to initiate a software-programmable routine such as operating mode selection or to open a menu. Connect nPBSTAT to an appropriate supply voltage through a 10kΩ or greater resistor.

Figure 2:

nPBIN Input



①: Only for ACT8846QM468 and ACT8846QM490-T.

②: Soft-Reset function is disabled in ACT8846QM460, ACT8846QM468 and ACT8846QM490.

③: Only for ACT8846QM460.

nRSTO Output

nRSTO is an open-drain output which asserts low upon startup or when manual reset is asserted via the nPBIN input. When asserted on startup, nRSTO remains low until reset time-out period expires. When asserted due to manual-reset, nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires.

Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply.

nIRQ Output

nIRQ is an open-drain output that asserts low any time an interrupt is generated. Connect a 10kΩ or greater pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor.

Many of the ACT8846's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I²C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Push-Button Control

The ACT8846 is designed to initiate a system enable sequence when the nPBIN multi-function input is asserted for 32ms. Once this occurs, a power-on sequence commences, as described below. The power-on sequence must complete and the microprocessor must take control (by asserting PWRHLD) before nPBIN is de-asserted. If the microprocessor is unable to complete its power-up routine successfully before the user releases the push-button, the ACT8846 automatically shuts the system down. This provides protection against accidental or momentary assertions of the push-button. If desired, longer “push-and-hold” times can be implemented by simply adding an additional time delay before asserting PWRHLD.

Control Sequences

The ACT8846 features a variety of control sequences that are optimized for supporting system enable and disable, as well as SLEEP mode of the Rockchip RK31x8 processors.

Enabling/Disabling Sequence

A typical enable sequence is initiated whenever the nPBIN is asserted low for 32ms via 50KΩ resistance. The power control diagram is shown in Figure 3. During the boot sequence, the microprocessor must assert PWRHLD (GPIO6_B0) to ensure that the system remains powered after nPBIN is released. Once the power-up routine is completed, the system remains enabled after the push-button is released as long as PWRHLD is asserted high. If the processor does not assert PWRHLD before the user releases the push-button, the boot-up sequence is terminated and all regulators are disabled. This provides protection against "false-enable", when the push-button is accidentally depressed, and also ensures that the system remains enabled only if the processor successfully completes the boot-up sequence.

As with the enable sequence, a typical disable sequence is initiated when the user presses the push-button, which interrupts the processor via the nPBSTAT output. After system is turned on, the processor may shut down the system by setting OFFSYSCLR[ ] to 1 then setting OFFSYS[ ] to 1, or by pulling PWRHLD to logic low. The user could force shut down ACT8846 anytime by pressing the power on push-button for 10 seconds even when software crashes.①

SLEEP Mode Sequence

The ACT8846 supports RK31x8 processor’s SLEEP mode operation. Once a successful power-up routine has been completed, SLEEP mode may be initiated through a variety of software-controlled mechanisms.

SLEEP mode is typically initiated when the user presses the push-button during normal operation. Pressing the push-button asserts the nPBIN input, which asserts the nPBSTAT output, which interrupts the processor. In response to this interrupt the processor should disable REG6, REG7, REG8, REG9, REG10 and REG12 via I²C, then de-assert PWREN(GPIO6_B1), disabling REG3. PWRHLD should remain asserted during SLEEP mode so that REG1, REG2, REG4, REG5, and REG11 remain enabled.

The ACT8846 wakes up from SLEEP mode when either the push-button and/or PWREN (GPIO6_B1) is asserted. In either case, REG3 is enable which allow the system to resume normal operation.

①: Only for ACT8846QM468

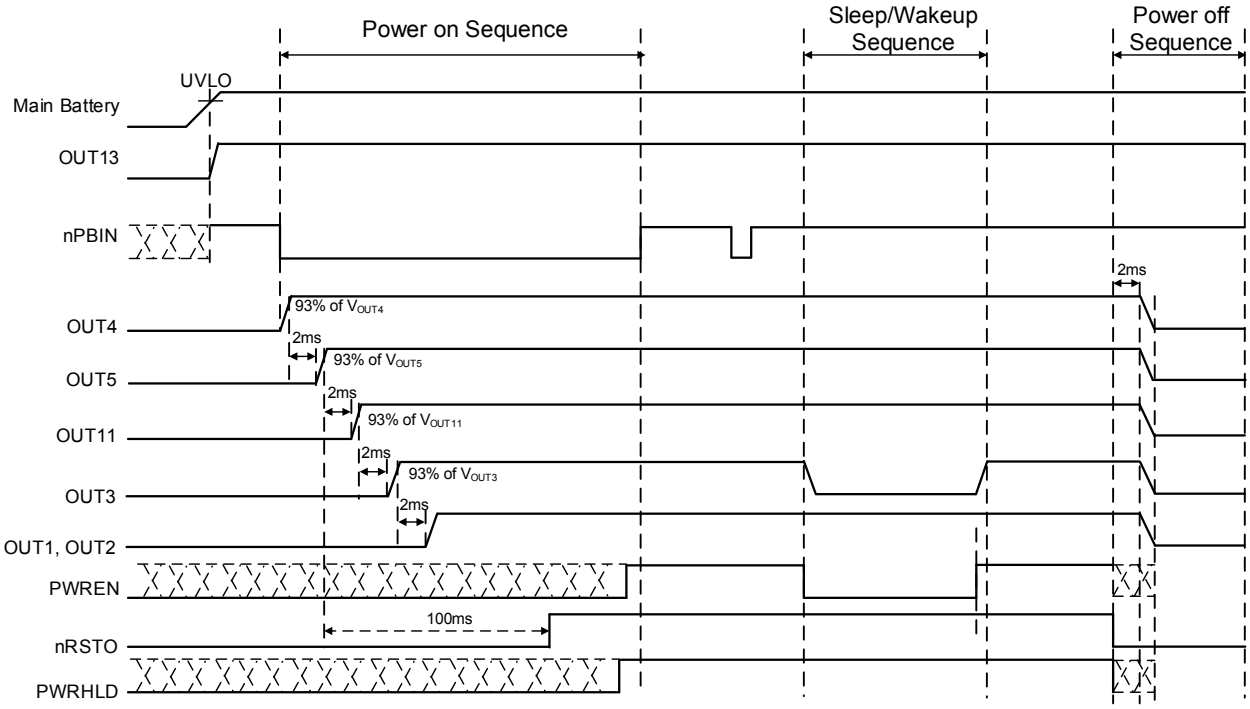
Watch-Dog Supervision①

The ACT8846 features a watchdog supervisory function. An internal watchdog timer of 4s is unmasked by setting either WDSREN[ ] or WDPCEN [ ] bit to one. Once enabled, the watchdog timer is reset whenever there is I²C activity for the PMU. In the case where the system software stops responding and that there is no I²C transactions for 4s, the watchdog timer expires. As a result, the PMU either perform a soft-reset or power cycle, depending on whether WDSREN [ ] or WDPCEN [ ] is set.

Software-Initiated Power Cycle

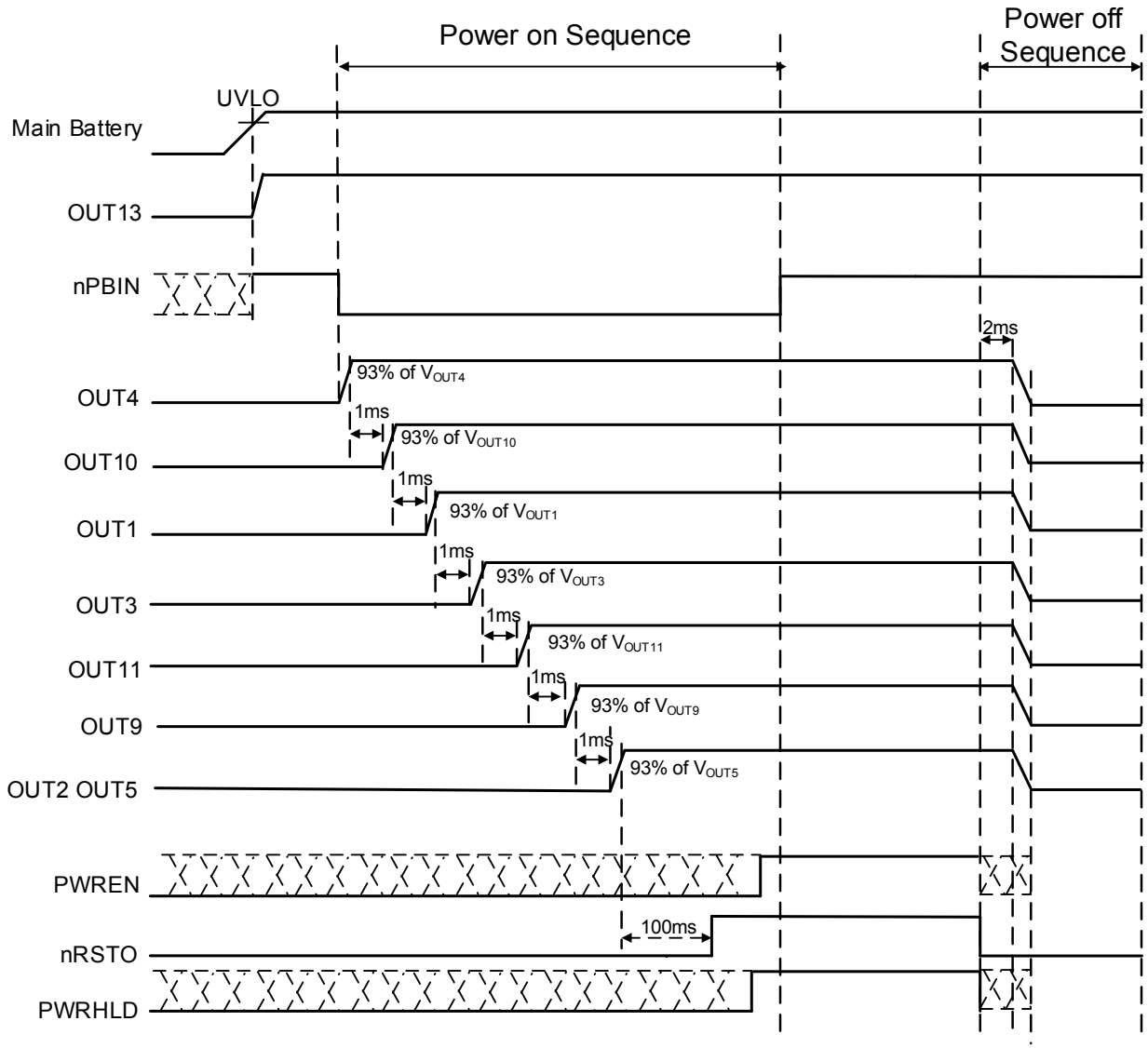
ACT8846 supports software-initiated power cycle. Once the SIPC[ ] bit is set, the PMU waits for 8ms and then initiate a power cycle to restart the entire system.

Figure 3:
ACT8846QM460 and ACT8846QM468 Power Control Sequence



①: Watch-Dog is not supported in ACT8846QM468 and ACT8846QM490-T.

Figure 3A:
ACT8846QM490 Power Control Sequence for RK3288



FUNCTIONAL DESCRIPTION

I²C Interface

The ACT8846 features an I²C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode" operation) and uses standard I²C commands. I²C write-byte commands are used to program the ACT8846, and I²C read-byte commands are used to read the ACT8846's internal registers. The ACT8846 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011010x].

SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com.

Housekeeping Functions

Programmable battery Voltage Monitor

The ACT8846 features a programmable battery-voltage monitor, which monitors the voltage at INL2 (which should be connected directly to the battery) and compares it to a programmable threshold voltage. The VBATMON comparator is designed to be immune to noise resulting from switching, load transients, etc. The BATMON comparator is disable by default; to enable it, set the BATLEV[3:0] register to one of the value in Table 4. Note that there is a 200mV hysteresis between the rising and falling threshold for the comparator. The VBATDAT [ ] bit reflects the output of the BATMON comparator. The value of VBATDAT[ ] is 1 when V_{INL2} < BATLEV; value is 0 otherwise.

The VBATMON comparator can generate an interrupt when V_{INL2} is lower than BATLEV[ ] voltage. The interrupt is masked by default by can be unmasked by setting VBATMSK[ ] = 1.

Table 4:

BATLEV Falling Threshold

BATLEV[3:0]	BATLEV Falling Threshold
0000	2.5
0001	2.6
0010	2.7
0011	2.8
0100	2.9
0101	3.0
0110	3.1
0111	3.2
1000	3.3
1001	3.4
1010	3.5
1011	3.6
1100	3.7
1101	3.8
1110	3.9
1111	4.0

Thermal Protection

The ACT8846 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions.

Thermal Interrupt

If the thermal interrupt is unmasked (by setting nTMSK[ ] to 1), ACT8846 can generate an interrupt when the die temperature reaches 120°C (typ).

Thermal Protection

If the ACT8846 die temperature exceeds 160°C, the thermal protection circuitry disables all regulators and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

STEP-DOWN DC/DC REGULATORS

General Description

REG1, REG2, REG3, and REG4 are fixed-frequency, current-mode, synchronous PWM step-down converters that achieves peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. Additionally, REG1, REG2, REG3, and REG4 are available with a variety of standard and custom output voltages, and may be software-controlled via the I2C interface for systems that require advanced power management functions.

100% Duty Cycle Operation

REG1, REG2, REG3, and REG4 are capable of operating at up to 100% duty cycle. During 100% duty cycle operation, the high-side power MOSFETs are held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Operating Mode

By default, REG1, REG2, REG3, and REG4 operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power.

Synchronous Rectification

REG1, REG2, REG3, and REG4 each feature integrated synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

REG1, REG2, REG3, and REG4 include internal 400 us soft-start ramps which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short-circuit or other fault condition.

Compensation

REG1, REG2, REG3, and REG4 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 10µF ceramic capacitor is recommended for each regulator in most applications.

Output Capacitor Selection

REG1, REG2, REG3, and REG4 were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. REG1, REG2, REG3 and REG4 are designed to operate with 33uF or 44uF output capacitor over most of their output voltage ranges, although more capacitance may be desired depending on the duty cycle and load step requirements.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications, as their characteristics are more stable over their operating ranges, and are highly recommended.

Inductor Selection

REG1, REG2, REG3, and REG4 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 2.2µH or 1µH inductors. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

Configuration Options

Output Voltage Programming

Figure 4:

OUT1 Output Voltage Programming

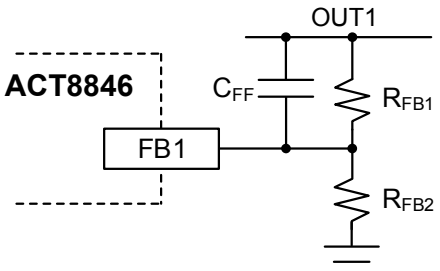


Figure 4 shows the feedback network necessary to set the output voltage for REG1 when using the adjustable output voltage option. Connect the FB1 pin to the output directly to regulate the output voltage at 1.2V. Select components as follows: Set RFB2 = 51kΩ, then calculate RFB1 using the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT1}}{V_{FB1}} - 1\right) \quad (1)$$

where V_{FB1} is 1.2V. Finally choose C_{FF} using the following equation:

$$C_{FF} = \frac{1 \times 10^{-6}}{R_{FB1}} \quad (2)$$

By default, REG2, REG3 and REG4 power up and regulate to their default output voltages. For REG2, REG3 and REG4, the output voltage is selectable by setting corresponding VSELR# pin that when VSELR# is low, output voltage is programmed by VSET0[ ] bits, and when VSELR# is high, output voltage is programmed by VSET1[ ] bits. Also, once the system is enabled, each regulator's output voltage may be independently programmed to a different value. Program the output voltages via the I²C serial interface by writing to the regulator's VSET0[ ] register if VSELR# is low or VSET1[ ] register if VSELR# is high as shown in Table 5.

Enable / Disable Control

During normal operation, each buck may be enabled or disabled via the I²C interface by writing to that regulator's ON[ ] bit.

OK[ ] and Output Fault Interrupt

Each DC/DC features a power-OK status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, that regulator's OK[ ] bit will be 0.

If a DC/DC's nFLTMSK[-] bit is set to 1, the ACT8846 will interrupt the processor if that DC/DC's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I²C.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Step-down DC/DCs exhibit discontinuous input current, so the buck input capacitors must be placed as close as possible to the IC. Connect the capacitors directly to the corresponding VPx input pin and Gx power ground pin. Avoid the use of vias. Best performance is achieved by direct input capacitor connection to the IC and by routing the SWx trace on the top layer, directly under the input capacitor. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

Table 5:

REGx/VSET[ ] Output Voltage Setting

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

LOW-NOISE, LOW-DROPOUT LINEAR REGULATORS

General Description

ACT8846 features eight low-noise, low-dropout linear regulators (LDOs) that supply up to 350mA. Three of these LDOs (REG10, REG11, and REG12) supports extended input voltage range down to 1.7V. Each LDO has been optimized to achieve low noise and high-PSRR.

Output Current Limit

Each LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal and moderate overload conditions, the regulators can support more than their rated output currents. During extreme overload conditions, however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC.

Compensation

The LDOs are internally compensated and require very little design effort, simply select input and output capacitors according to the guidelines below.

Input Capacitor Selection

Each LDO requires a small ceramic input capacitor to supply current to support fast transients at the input of the LDO. Bypassing each INL pin to GA with 1µF. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Output Capacitor Selection

Each LDO requires a small 2.2µF ceramic output capacitor for stability. For best performance, each output capacitor should be connected directly between the output and GA pins, as close to the output as possible, and with a short, direct connection. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Configuration Options

Output Voltage Programming

By default, each LDO powers up and regulates to its default output voltage. Once the system is enabled, each output voltage may be independently programmed to a different value by writing to the regulator's VSET[ ] register via the I²C serial interface as shown in Table 5.

Enable / Disable Control

During normal operation, each LDO may be enabled or disabled via the I²C interface by writing to that LDO's ON[ ] bit.

Output Discharge

Each of the LDOs features an optional output discharge function, which discharges the output to ground through a 1.5kΩ resistance when the LDO is disabled. This feature may be enabled or disabled by setting DIS[ ]; set DIS[ ] to 1 to enable this function, clear DIS[ ] to 0 to disable it.

OK[ ] and Output Fault Interrupt

Each LDO features a power-OK status bit that can be read by the system microprocessor via the interface. If an output voltage is lower than the power-OK threshold, typically 11% below the programmed regulation voltage, the value of that regulator's OK[ ] bit will be 0.

If a LDO's nFLTMSK[ ] bit is set to 1, the ACT8846 will interrupt the processor if that LDO's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I²C.

PCB Layout Considerations

The ACT8846's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

REFBP is a noise-filtered reference, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of via whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

ALWAYS-ON LDO (REG13)

General Description

REG13 is an always-on, low-dropout linear regulator (LDO) that is optimized for RTC and backup-battery applications. REG13 features low-quiescent supply current, current-limit protection, and reverse-current protection, and is ideally suited for always-on power supply applications, such as for a real-time clock, or as a backup-battery or super-cap charger.

Reverse-Current protection

REG13 features internal circuitry that limits the reverse supply current to less than 1μA when the input voltage falls below the output voltage, as can be encountered in backup-battery charging applications. REG13's internal circuitry monitors the input and the output, and disconnects internal circuitry and parasitic diodes when the input voltage falls below the output voltage, greatly minimizing backup battery discharge.

Typical Application

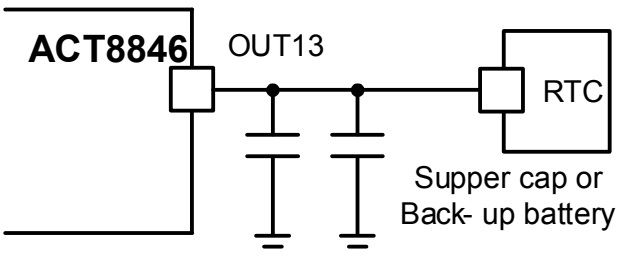
Voltage Regulators

REG13 is ideally suited for always-on voltage-regulation applications, such as for real-time clock and memory keep-alive applications. This regulator requires only a small ceramic capacitor with a minimum capacitance of 0.47μF for stability. For best performance, the output capacitor should be connected directly between the output and GA, with a short and direct connection.

Figure 5:

Typical Application of RTC LDO

Backup Battery Charging



REG13 features a constant current-limit, which protects the IC under output short-circuit conditions as well as provides a constant charge current, when operating as a backup battery charger.

PWM LED DRIVERS

The GPIO3, the GPIO4, the GPIO5, and the GPIO6 are configured as PWM LED drivers, which could support up to 6mA current with programmable frequency and duty cycle. Set PWM#EN[ ] bit to "1" to enable PWM function of GPIO#.

PWM Frequence Selection

Each LED driver may be independently programmed to a different frequency by writing to the GPIO's FRE[2:0] register via the I²C serial interface as shown in Table 6.

Table 6:

FRE#[ ] PWM Frequency Setting

FRE#[2:0]	PWM Frequency [Hz]
000	0.25
001	0.5
010	1
011	2
100	128
101	256

PWM Duty Cycle Selection

Each LED driver may be independently programmed to a different duty cycle by writing to the GPIO's DUTY[3:0] register via the I²C serial interface as shown in Table 7.

Table 7:

DUTY#[ ] PWM Frequency Setting

DUTY#[3:0]	PWM Duty Cycle [%]
0000	6.25
0001	12.5
0010	18.75
0011	25
0100	31.25
0101	37.5
0110	43.75
0111	50
1000	56.25
1001	62.5
1010	68.75
1011	75
1100	81.25
1101	87.5
1110	93.75
1111	100

CMI OPTIONS

CMI 106: ACT8846QM106

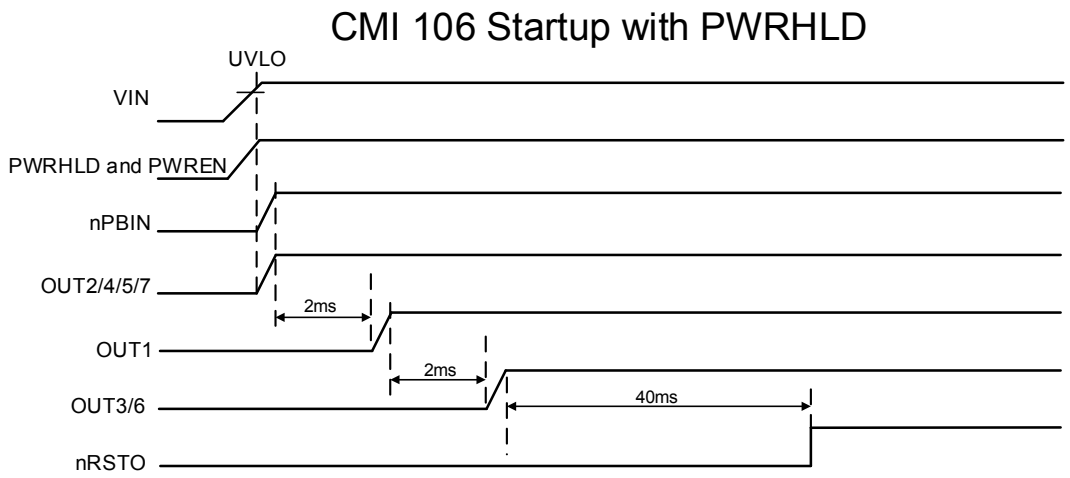
Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
OUT1	1.2	1.2	OUT2	2000	400
OUT2	0.95	0.95	Vin UVLO	0	400
OUT3	3.3	3.3	OUT1	2000	400
OUT4	1.8	1.8	Vin UVLO	0	400
OUT5	1.8	n/a	Vin UVLO	0	140
OUT6	1.8	n/a	OUT1	2000	140
OUT7	3.3	n/a	Vin UVLO	0	140
OUT8	1.2	n/a	I²C	0	140
OUT9	2.8	n/a	I²C	0	140
OUT10	1.5	n/a	I²C	0	100
OUT11	2.8	n/a	I²C	0	100
OUT12	1.8	n/a	I²C	0	100
OUT13	1.8	n/a	I²C	0	100

Hardware Configuration

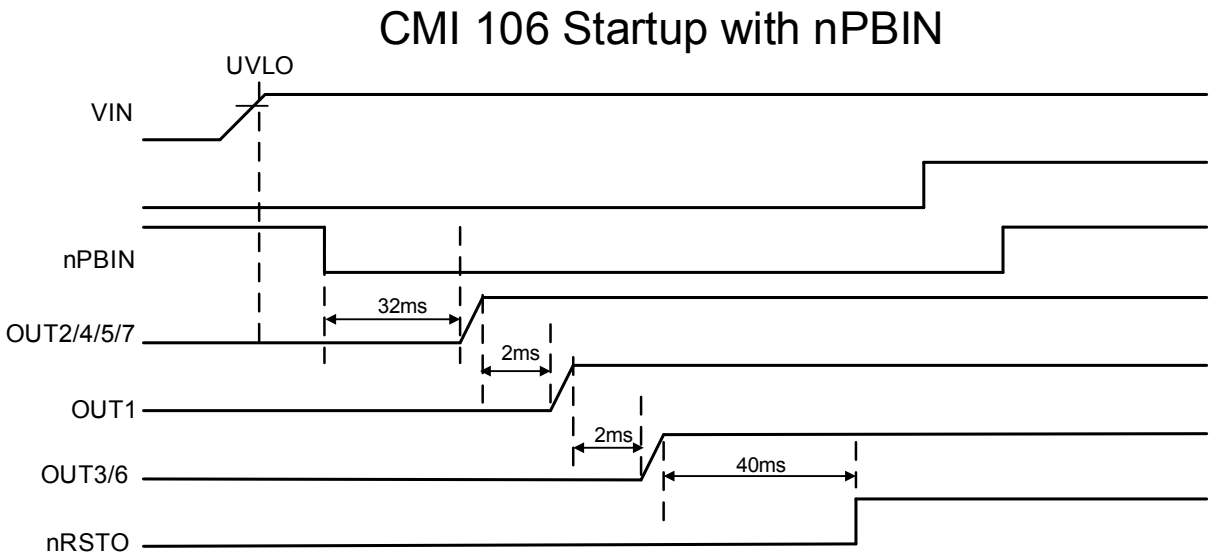
PWRHLD and PWREN must be connected together in CMI 106.

Startup

The ACT8846QM106-T has two startup sequences. The first is pushbutton startup. Asserting nPBIN low starts the startup sequence. nPBIN must stay low until after PWRHLD and PWREN are asserted high by an external source, usually a uP. If nPBIN goes high before PWRHLD goes high, the IC shuts down all outputs. The second startup sequence is with the PWREN and PWRHLD pins. After input power is applied, asserting PWREN high starts the startup sequence. Note that nPBIN should stay high in this application. In both startup conditions, OUT8/9/10/11/12/13 are off by default, but can be enabled via I²C.



CMI 106: ACT8846QM106 continued.



Shutdown

The IC can be turned off by pulling nPBIN low through a 50kohm resistor to GA or by deasserting PWREN and PWRHLD pins low. The IC can also be turned off via I²C.

PWREN

Asserting PWREN high enables the IC. In pushbutton applications, if PWREN is not asserted high before the nPBIN pin goes high, the IC shuts down. Note that PWREN and PWRHLD must be connected together.

nPBIN

nPBIN retains the short and long press functionality described earlier in the datasheet.

NRSTO

nRSTO is gated by OUT6 and OUT7 and has a 40ms delay.

DVS

DVS functionality is only available via I²C.

VSELR/GPIO1/GPIO2

The VSELR/GPIO1/GPIO2 pins are not functional and should be permanently pulled high or low.

GPIO1/2/3/4/5/6

These outputs are off by default but can be enabled via I²C. GPIO3 frequency and duty cycle are 256Hz and 50%. GPIO4/5/6 frequency and duty cycle are 0.25Hz and 6.25%.

Watchdog

All watchdog functionality is disabled by default.

CMI 108: ACT8846QM108

CMI108 is optimized for a custom processor.

Sequencing

Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)	Forced PWM
OUT1	1.8	1.8	OUT7	0	400	Off
OUT2	0.8	0.8	GPIO1	1000	400	On
OUT3	1.125	1.2	OUT1	1000	400	On
OUT4	3.0	3.0	I^2C	0	400	Off
OUT5	1.8	n/a	I^2C	0	140	n/a
OUT6	1.8	n/a	I^2C	0	140	n/a
OUT7	1.8	n/a	GPIO1	2000	140	n/a
OUT8	3.3	n/a	OUT3	500	140	n/a
OUT9	3.3	n/a	OUT3	2000	140	n/a
OUT10	3.3	n/a	OUT3	1000	100	n/a
OUT11	2.5	n/a	OUT1	500	100	n/a
OUT12	3.3	n/a	I^2C	0	100	n/a
OUT13	1.8	n/a	Always On	0	100	n/a

Hardware Configuration

PWRHLD should be connected directly to VIN.

GPIO1 should be connected directly to OUT13.

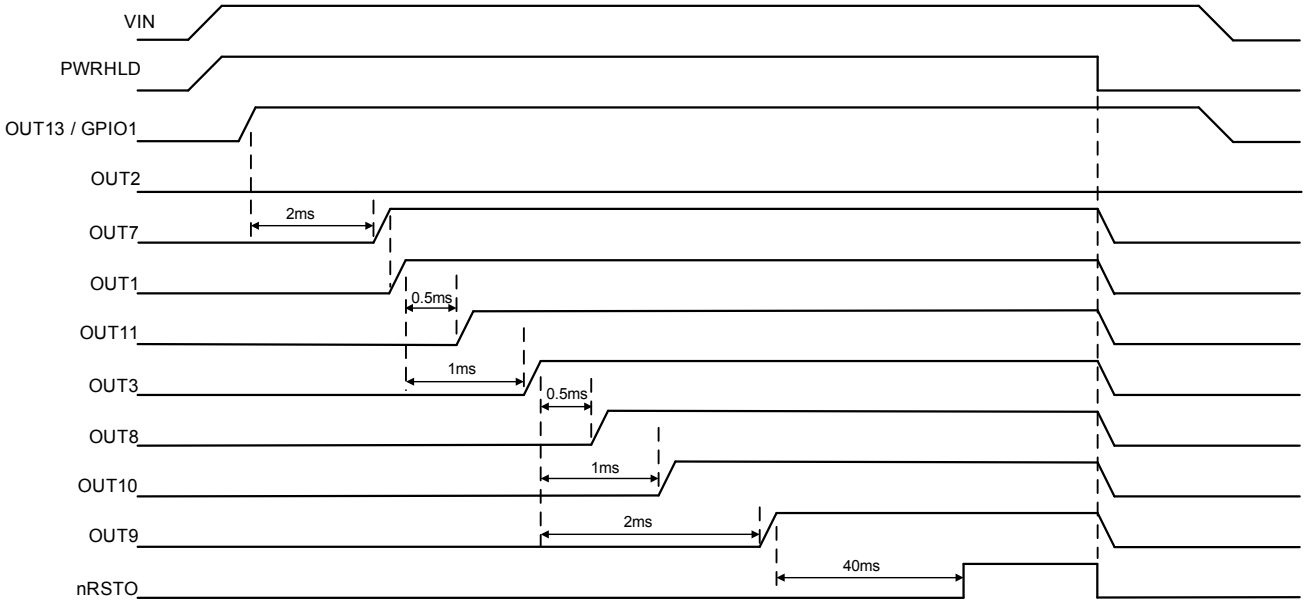
GPIO2 should be connected directly to PWREN.

Startup

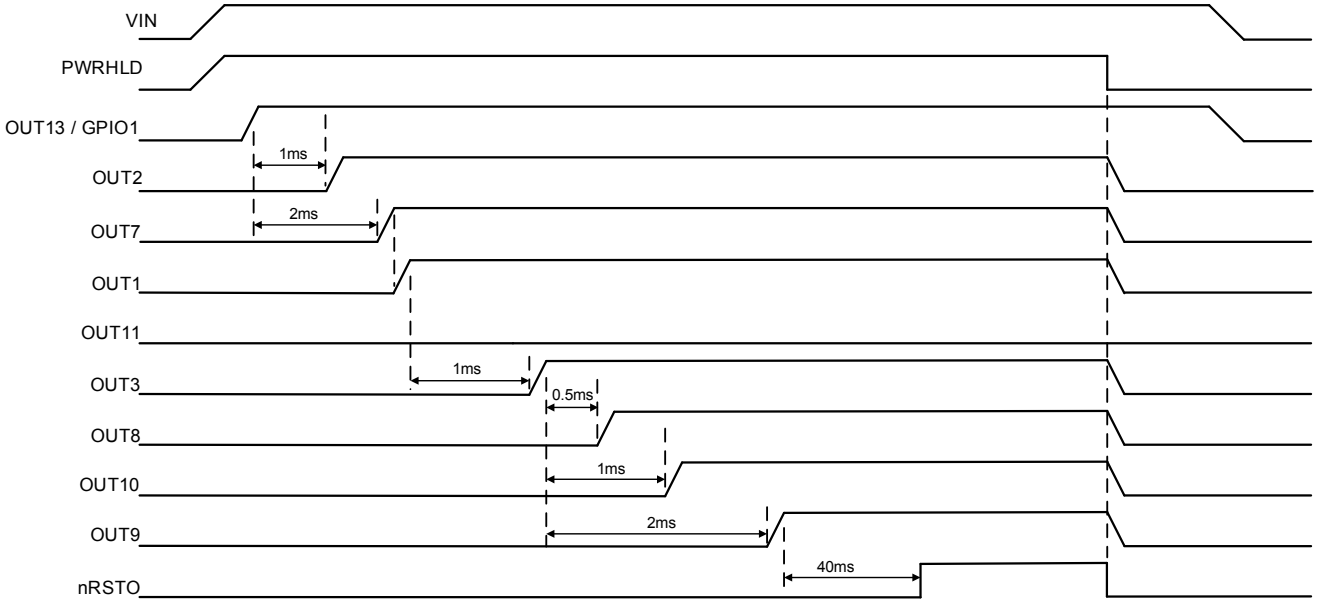
The ACT8846QM108-T automatically turns on with the programmed startup sequencing when power is applied. Note that the PWREN input setting affects the OUT2, OUT3, and OUT11 at turnon.

CMI 108: ACT8846QM108 continued

CMI 108 Startup
PWREN = 0



CMI 108 Startup
PWREN = 1



CMI 108: ACT8846QM108 continued

Shutdown

The processor can turn the IC off with standard I²C commands. Other options for turning off the IC are to pull PWRHLD low or assert nPBIN low for > 10s.

PWREN

PWREN is intended to be pulled high or low at turnon to configure the IC for different processor configurations.

PWREN should be connected high or low before startup.

When PWREN is logic L, OUT2 is configured off, OUT11 is configured on, and OUT3 is configured for 1.2V.

When PWREN is logic H, OUT2 is configured on, OUT11 is configured off, and OUT3 is configured for 1.125V.

nPBIN

nPBIN must be left floating. It can be used to turn off the processor by asserting nPBIN low for > 10s

NRSTO

nRSTO is gated by OUT9 and has a 40ms delay.

DVS

DVS functionality is only available via I²C.

VSELR2

VSELR2 should be tied to ground. VSELR2 does not have functionality with this CMI option.

GPIO1/2

GPIO1 should be connected directly to OUT13.

GPIO2 should be connected directly to PWREN.

GPIO3/4/5/6

These outputs are off by default but can be enabled via I²C. GPIO3 frequency and duty cycle are 256Hz and 50%. GPIO4/5/6 frequency and duty cycle are 0.25Hz and 6.25%.

Watchdog

All watchdog functionality is disabled by default.

CMI 109: ACT8846QM109

CMI109 is optimized to power the Simplight SL3600 processor.

Sequencing

Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
OUT1	1.45	1.45	PWREN	0	400
OUT2	1.8	1.8	PWREN	0	400
OUT3	1.1	1.1	PWREN	0	400
OUT4	2.8	2.8	PWREN	0	400
OUT5	2.5	n/a	PWREN	0	140
OUT6	3.0	n/a	I²C	0	140
OUT7	2.5	n/a	I²C	0	140
OUT8	1.8	n/a	I²C	0	140
OUT9	3.3	n/a	I²C	0	140
OUT10	0.95	n/a	I²C	0	100
OUT11	2.8	n/a	I²C	0	100
OUT12	1.8	n/a	PWRHLD	0	100
OUT13	1.8	n/a	Always On	0	100

Hardware Configuration

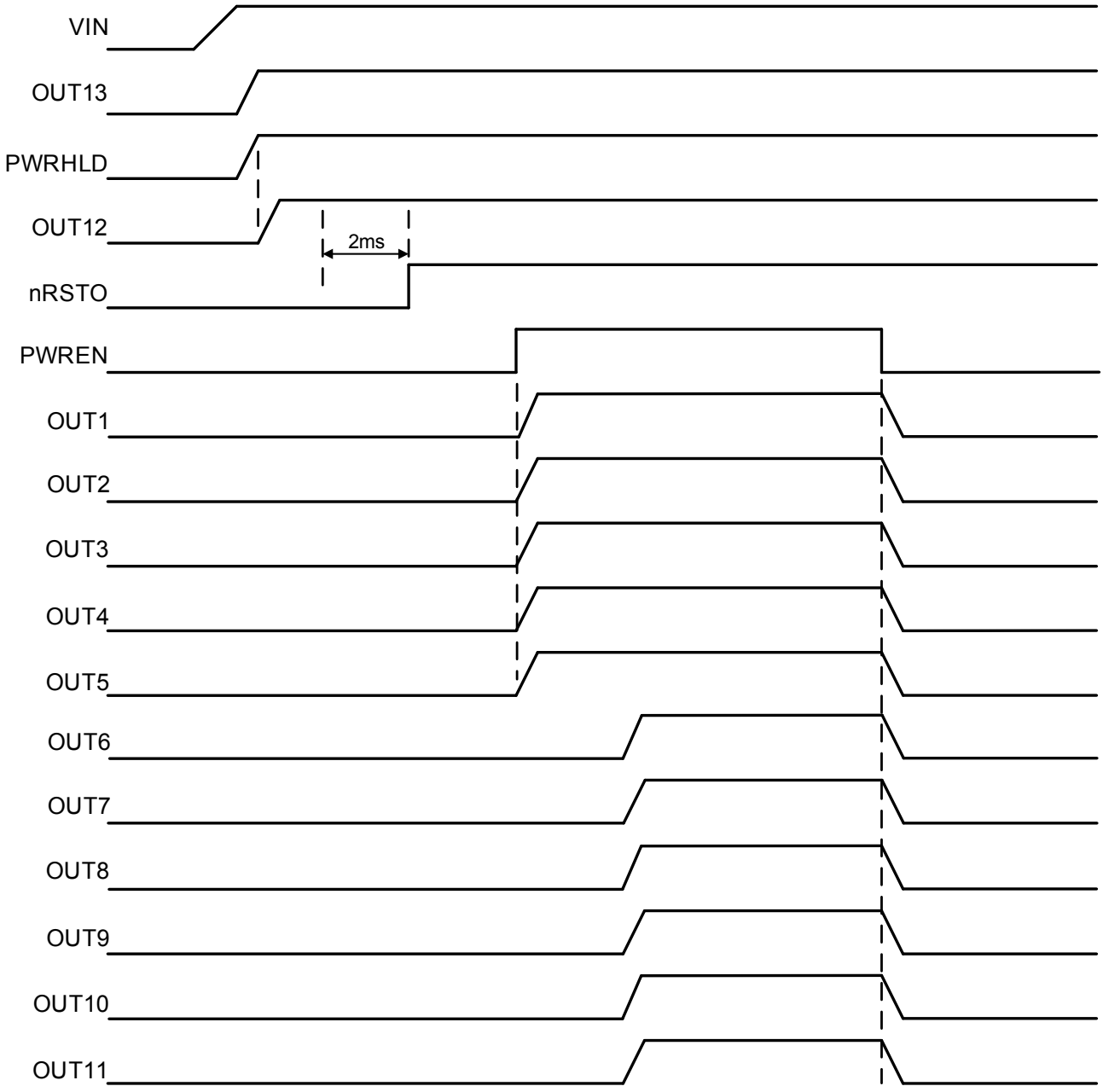
PWRHLD should be connected directly to OUT13. This automatically turns on OUT12 when the always-on OUT13 turns on after input power is applied.

PWREN should be connected to an SL3600 GPIO. Pulling PWREN high turns on OUT1/2/3/4/5. Pulling PWREN low turns off OUT1/2/3/4/5/6/7/8/9/10/11.

Startup

The ACT8846QM109-T automatically turns on OUT13 when power is applied. Connecting the PWRHLD pin to OUT13 automatically turns on OUT12 after OUT13 turns on. A processor GPIO connected to PWREN turns on OUT1/2/3/4/5 when the GPIO goes high. After OUT12/13 are turned on, the processor can turn OUT6/7/8/9/10/11 on and off via I²C while PWREN is held high.

CMI 109 Startup



Shutdown

The processor can turn OUT6/7/8/9/10/11 on and off via I²C when PWREN is held high. All outputs except OUT12/13 turn off when PWREN is pulled low. NOTE that I²C register bit WDSREN must set to 1 before pulling PWREN low. If WDSREN does is not set to 1, the outputs will not turn on when PWREN is pulled high again.

PWREN

Connect PWREN to the processor to control OUT1/2/3/4/5. Pulling PWREN high turns these outputs on. Pulling PWREN low turns off all outputs except OUT11/12.

nPBIN

nPBIN must be left floating. It does not provide pushbutton functionality with this CMI option.

NRSTO

nRSTO is gated by OUT12 and has a 2ms delay.

DVS

DVS functionality is only available via I²C.

VSELR2

VSELR2 should be tied to ground. VSELR2 does not have functionality with this CMI option.

GPIO1/2/3/4/5/6

These outputs are off by default but can be enabled via I²C. GPIO3 frequency and duty cycle are 256Hz and 50%. GPIO4/5/6 frequency and duty cycle are 0.25Hz and 6.25%.

Watchdog

All watchdog functionality is disabled by default.

CMI 111: ACT8846QM111

Sequencing

Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
OUT1	1.5	1.5	OUT7	0	400
OUT2	2.4	2.4	GPIO1	500	400
OUT3	1.2	1.2	OUT11	500	400
OUT4	3.0	3.0	I^2C	0	400
OUT5	3.0	n/a	I^2C	0	140
OUT6	3.3	n/a	I^2C	0	140
OUT7	1.8	n/a	OUT2	500	140
OUT8	3.3	n/a	OUT3	500	140
OUT9	3.3	n/a	OUT8	1000	140
OUT10	3.3	n/a	OUT8	500	100
OUT11	2.5	n/a	OUT1	500	100
OUT12	1.8	n/a	I^2C	0	100
OUT13	1.8	n/a	Always On	0	100

Hardware Configuration

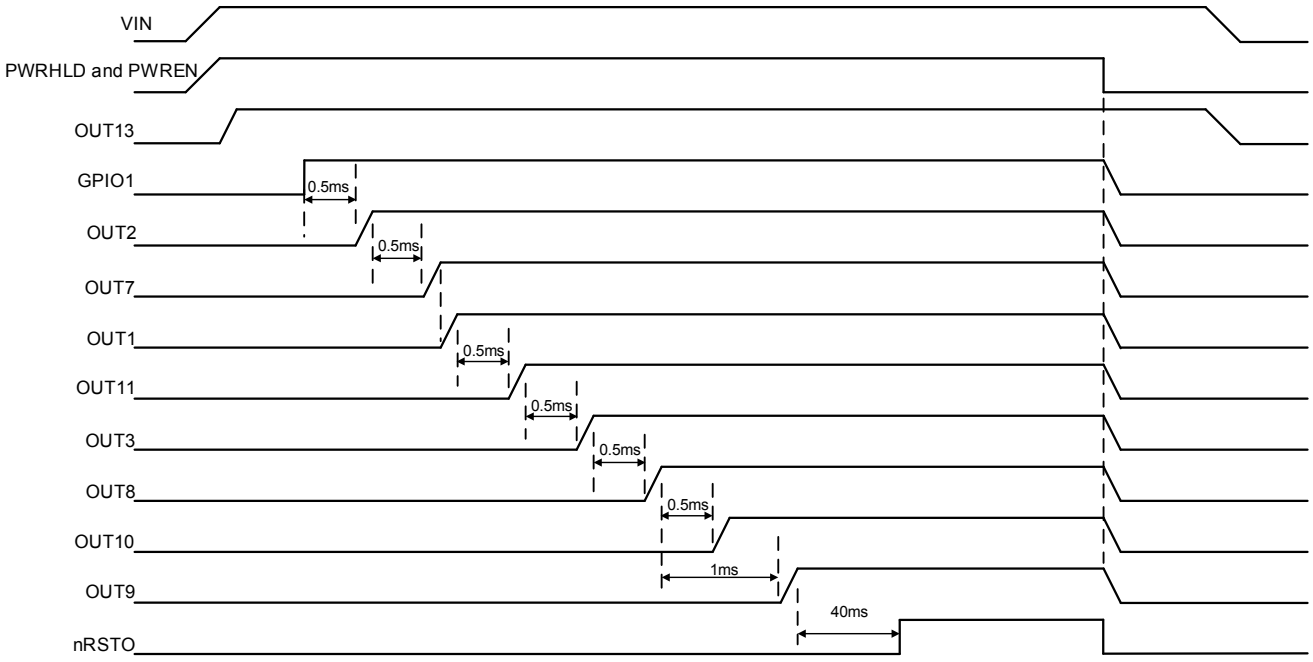
PWRHLD and PWREN must be connected together in CMI 111. They can be connected to VIN or to a microprocessor output.

GPIO1 can be connected to OUT13, or it can be connected to a microprocessor output.

Startup

The ACT8846QM111-T automatically turns on OUT13 when power is applied. Pulling PWREN and PWRHLD high enables the turn on sequencing, but does not actually start the sequencing. Pulling GPIO1 high starts the turn on sequencing for OUT2/7/1/11/3/8/10/9. After these outputs are on, the processor can turn OUT4/5/6/12 on and off via I^2C. Note that PWREN must be high for I^2C of OUT4/5/6/12.

CMI 111 Startup



Shutdown

The processor can turn OUT4/5/6/12 on and off via I²C when PWREN is held high. All outputs except OUT13 turn off when PWREN is pulled low.

PWREN

Connect PWREN to the processor or to OUT13 to control OUT2/7/1/11/3/8/10/9. Pulling PWREN high turns these outputs on. Pulling PWREN low turns off all outputs except OUT13.

nPBIN

nPBIN retains the short and long press functionality described earlier in the datasheet.

NRSTO

nRSTO is gated by OUT9 and has a 40ms delay.

DVS

DVS functionality is only available via I²C.

VSELR2

VSELR should be tied to ground. VSELR2 does not have functionality with this CMI option.

GPIO1

GPIO1 is the input trigger to OUT2. Pull GPIO1 high to start the turn on sequencing. After outputs OUT2/7/1/11/3/8/10/9 are turned on for greater than 0.5ms, GPIO1 can stay high or be pulled low. Pulling GPIO1 low does not turn off OUT2/7/1/11/3/8/10/9.

GPIO2/3/4/5/6

These outputs are off by default but can be enabled via I²C. GPIO3 frequency and duty cycle are 256Hz and 50%. GPIO4/5/6 frequency and duty cycle are 0.25Hz and 6.25%.

Watchdog

All watchdog functionality is disabled by default.

CMI 112: ACT8846QM112

CMI112 is optimized to power the Arm® Cortex® A7 processor. All buck converters are configured for forced PWM mode, but can be reconfigured to operate in power saving mode if desired.

Sequencing

Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
OUT1	1.8	1.8	OUT7	0	400
OUT2	0.9	0.9	GPIO1	500	400
OUT3	1.2	1.2	OUT11	500	400
OUT4	3.0	3.0	I^2C	0	400
OUT5	3.3	n/a	I^2C	0	140
OUT6	1.8	n/a	I^2C	0	140
OUT7	1.8	n/a	OUT2	500	140
OUT8	3.3	n/a	OUT3	500	140
OUT9	3.3	n/a	OUT8	1000	140
OUT10	3.3	n/a	OUT8	500	100
OUT11	2.5	n/a	OUT1	500	100
OUT12	3.3	n/a	I^2C	0	100
OUT13	1.8	n/a	Always On	0	100

Hardware Configuration

PWRHLD and PWREN must be connected together in CMI 112.

GPIO1 must be directly connected to OUT13 in CMI 112.

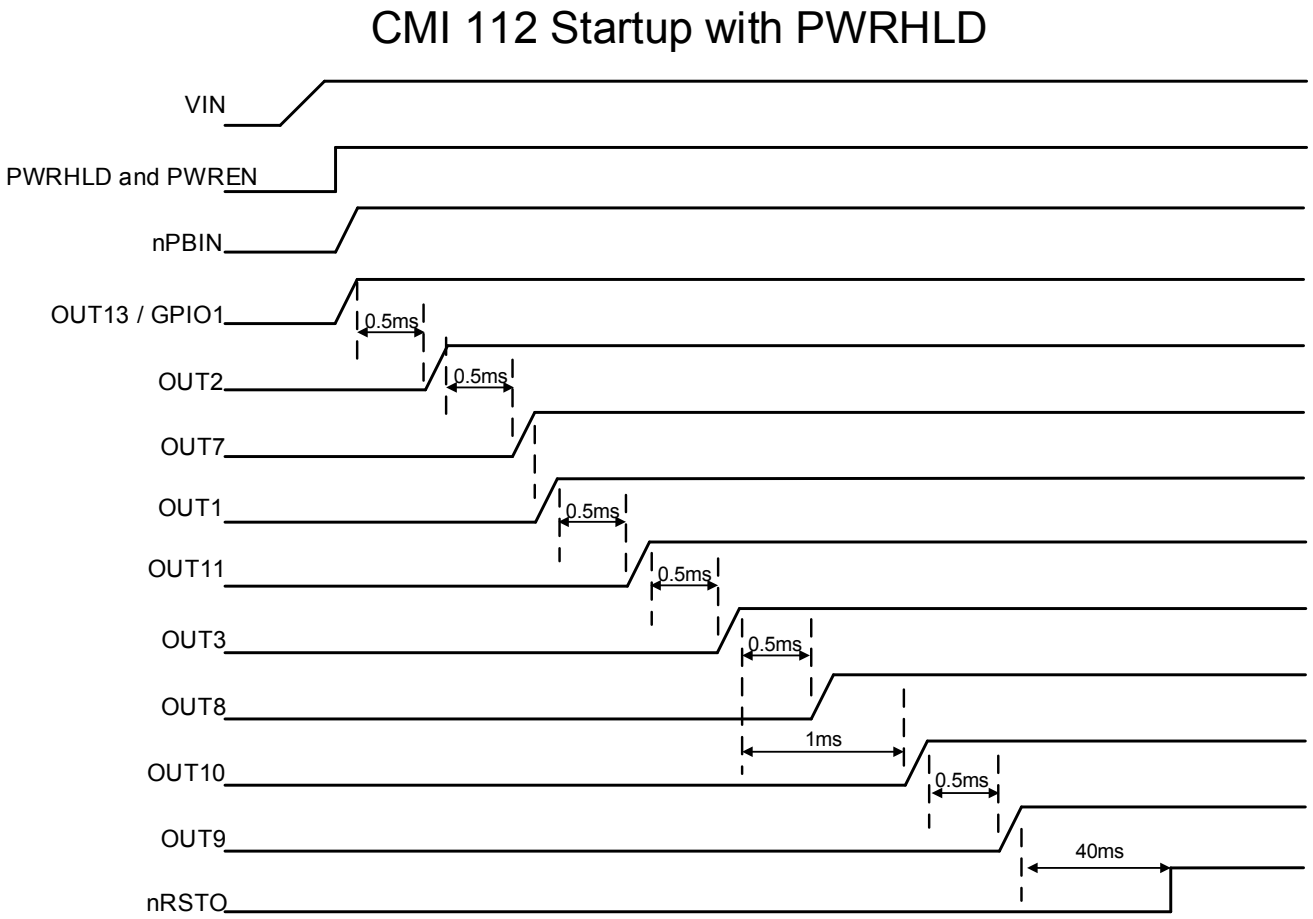
Startup

The ACT8846QM112-T has two startup sequences. The first is pushbutton startup. Asserting nPBIN low starts the startup sequence. nPBIN must stay low until after PWRHLD and PWREN are asserted high by an external source, usually a uP. If nPBIN goes high before PWRHLD goes high, the IC shuts down all outputs. The second startup sequence is with the PWREN and PWRHLD pins. After input power is applied, asserting PWREN high starts the startup sequence. Note that nPBIN should stay high in this application. In both startup conditions, OUT4/5/6/12 are off by default, but can be enabled via I^2C.

Power Save Mode

All buck regulators are programmed for forced PWM mode. This provides improved load transient response and maintains a constant output voltage ripple across the full load range.

CMI 112: ACT8846QM112 continued



Shutdown

The IC can be turned off by pulling nPBIN low through a 50kohm resistor to GA or by deasserting PWREN and PWRHLD pins low. The IC can also be turned off via I²C.

PWREN

Asserting PWREN high enables the IC. In pushbutton applications, if PWREN is not asserted high before the nPBIN pin goes high, the IC shuts down. Note that PWREN and PWRHLD must be connected together.

nPBIN

nPBIN retains the short and long press functionality described earlier in the datasheet.

NRSTO

nRSTO is gated by OUT9 and has a 40ms delay.

DVS

DVS functionality is only available via I²C.

CMI 112: ACT8846QM112 continued

VSELR/GPIO1/GPIO2

The VSELR/GPIO1/GPIO2 pins are not functional and should be permanently pulled high or low.

GPIO1/2/3/4/5/6

These outputs are off by default but can be enabled via I^2C. GPIO3 frequency and duty cycle are 256Hz and 50%. GPIO4/5/6 frequency and duty cycle are 0.25Hz and 6.25%.

Watchdog

All watchdog functionality is disabled by default.

CMI 113: ACT8846QM113

CMI113 is optimized for a custom processor. All buck converters are configured for forced PWM mode, but can be reconfigured to operate in power saving mode if desired.

Sequencing

Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)	Forced PWM
OUT1	1.5	1.35	OUT3	2000	400	On
OUT2	3.3	3.3	GPIO1	2000	400	On
OUT3	0.85	0.85	GPIO3	0	400	On
OUT4	1.8	1.8	OUT3	2000	400	On
OUT5	0.9	n/a	GPIO3	0	140	n/a
OUT6	1.2	n/a	GPIO3	0	140	n/a
OUT7	3.3	n/a	UVLO	0	140	n/a
OUT8	2.8	n/a	OUT9	2000	140	n/a
OUT9	1.5	n/a	OUT2	2000	140	n/a
OUT10	3.3	n/a	OUT1	2000	100	n/a
OUT11	3.3	n/a	GPIO5	0	100	n/a
OUT12	3.3	n/a	OUT1	2000	100	n/a
OUT13	1.8	n/a	OFF	0	100	n/a

Hardware Configuration

GPIO1 must be connected directly to nRESET.

PWRHLD must be connected directly to VIN.

Startup

The ACT8846QM113-T automatically turns on with the programmed startup sequencing when power is applied.

Power Save Mode

All buck regulators are programmed for forced PWM mode. This provides improved load transient response and maintains a constant output voltage ripple across the full load range.

CMI 113: ACT8846QM113 continued

CMI 113 Startup

Shutdown

The processor can turn the IC off with standard I²C commands. Another option for turning off the IC is to or assert nPBIN low for > 10s.

PWREN

PWREN must be connected directly to VIN for proper turn-on sequencing.

nPBIN

nPBIN should be left floating. It retains standard datasheet functionality and can be used to turn off the processor by asserting nPBIN low for > 10s

NRSTO

nRSTO is gated by OUT12 and has a 40ms delay. Connect nRSTO directly to GPIO1

DVS

DVS is only available for OUT1. GPIO2 is configured as the DVS input trigger for OUT1. When GPIO2 = 0, OUT1 = 1.5V. When GPIO2 = 1, OUT1 = 1.35V.

CMI 113: ACT8846QM113 continued

VSELR2

VSELR2 should be tied to ground. VSELR2 does not have functionality with this CMI option.

GPIO1

GPIO1 should be connected directly to nRSTO.

All watchdog functionality is disabled by default.

GPIO2

GPIO2 is the DVS is input trigger for OUT1. When GPIO2 = 0, Buck1 = 1.5V. When GPIO2 = 1, OUT1 = 1.35V.

GPIO3

GPIO3 is the input trigger for OUT3/5/6

GPIO4/6

These outputs are off by default but can be enabled via I^2C.

GPIO5

GPIO5 is the input trigger for OUT11. Note that OUT11 turns on with the AND of GPIO3 and GPIO5. GPIO5 is intended to be the output of a uP, and it can turn on OUT11 any time after nRSTO is high.

Watchdog

All watchdog functionality is disabled by default.

CMI 114: ACT8846QM114

CMI114 is optimized for a custom processor.

Sequencing

Rail	VSET0 Voltage (V)	VSET1 Voltage (V)	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)	Forced PWM
OUT1	1.35	1.35	OUT12	2000	400	Off
OUT2	1.0	1.0	UVLO	0	400	Off
OUT3	3.3	3.3	OUT4	2000	400	Off
OUT4	1.8	1.8	OUT10	2000	400	Off
OUT5	3.3	n/a	I2C	0	140	n/a
OUT6	3.3	n/a	OUT2	2000	140	n/a
OUT7	3.3	n/a	OUT2	2000	140	n/a
OUT8	1.8	n/a	OUT2	2000	140	n/a
OUT9	1.8	n/a	OUT2	2000	140	n/a
OUT10	1.8	n/a	OUT2	2000	100	n/a
OUT11	2.5	n/a	UVLO	0	100	n/a
OUT12	2.5	n/a	OUT4	2000	100	n/a
OUT13	1.8	n/a	I2C	N/A	100	n/a

Hardware Configuration

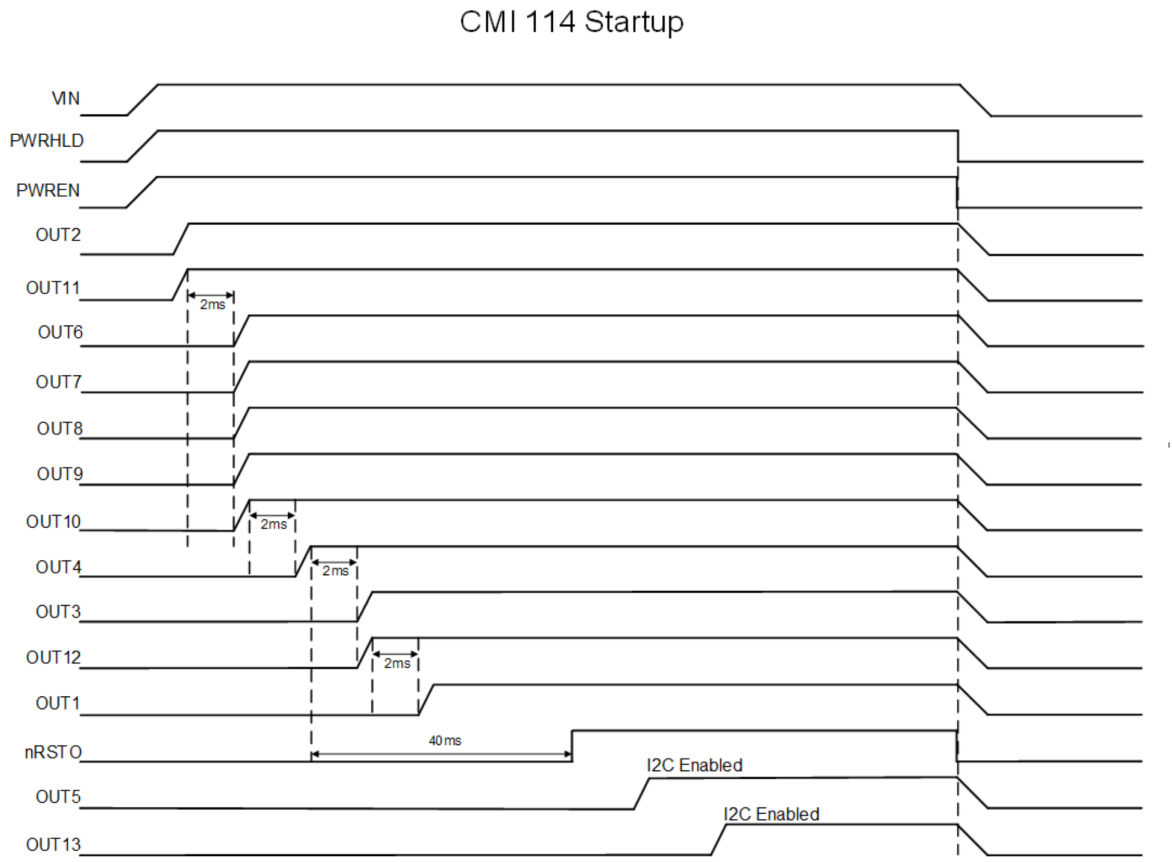
PWREN must be connected directly to VIN.

PWRHLD must be connected directly to VIN.

Startup

The ACT8846QM114-T automatically turns on with the programmed startup sequencing when power is applied.

CMI 114: ACT8846QM114 continued



Shutdown

The processor can turn the IC off with standard I²C commands.

PWREN

PWREN must be connected directly to VIN for proper turn-on sequencing.

nPBIN

nPBIN should be left floating. It should not be used with this CMI.

NRSTO

nRSTO is gated by OUT4 and has a 40ms delay.

DVS

DVS is not functional for this CMI.

VSELR2

VSELR2 should be tied to ground. VSELR2 does not have functionality with this CMI option.

CMI 114: ACT8846QM114 continued

GPIO1

GPIO1 should be connected directly to VIN.

GPIO2/3/4/5/6

GPIO2/3/4/5/6 should be left floating. They are not used with this CMI.

Watchdog

All watchdog functionality is disabled by default.

System Reset

The ACT8846QM114 can be power cycled in two ways.

The first is to set bit MR (bit 0, reg 0xD3) to 1. Then then set bit SIPC (bit 0 reg 0xC3) to 1 within 8ms. nRSTO will be asserted 8ms after MR is set, and Power Cycle is initiated 8ms after SIPC is set.

The second is to set bit WDPCEN (bit 0, register 0xC0) to 1. The IC will power cycle 4s after this bit is set. After the system powers up, set bit WDPCEN to 0.

ERRATA INFO

Errata Name:

ACT8846 creates I²C BUS contention.

Description:

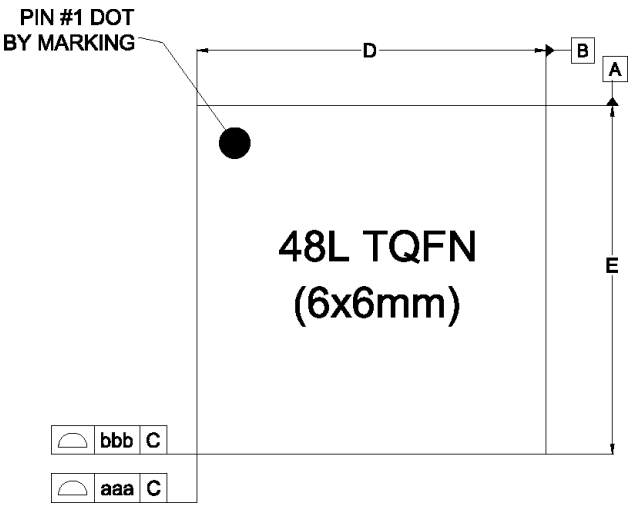
ACT8846 incorrectly detects its I²C slave address and pulls SDA low to acknowledge the address. This occurs under several conditions.

1. The IC is on a multi-slave I²C bus and the other slaves use multi-byte read or write commands, and the read/write data contains a string of bits that match the ACT8846 I²C address.
2. The host addresses a device with a 10 bit I²C address that contains a string of bits that match the ACT8846
   I²C address.

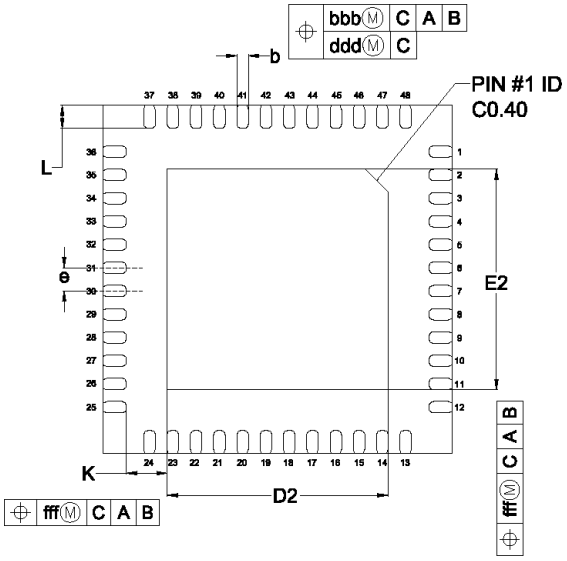
Work Around:

It is not possible to disable the ACT8846 I²C bus, so the recommended solution is to not put I²C devices that use multi-byte read or write commands on the ACT8846 I²C bus.

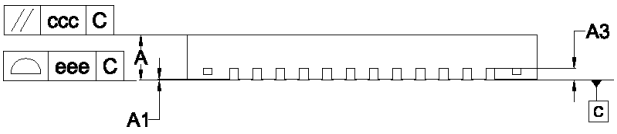
PACKAGE OUTLINE AND DIMENSIONS



Top View



Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	---	0.050
A3	0.203 Ref.		
D	6.0BSC		
E	6.0BSC		
D2	3.700	4.00	4.400
E2	3.700	4.000	4.400
--	--		
b	0.150	0.200	0.250
e	0.400 BSC		
L	0.300	0.400	0.500
K	0.700 Ref.		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Notes

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-2009.
2. All DIMENSIONS ARE IN MILLIMETERS.
3. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.