12-Bit RDC with Reference Oscillator

AD2S1205

FEATURES

Complete monolithic resolver-to-digital converter (RDC)
Parallel and serial 12-bit data ports
System fault detection
±11 arc minutes of accuracy
Input signal range: 3.15 V p-p ± 27%
Absolute position and velocity outputs
1250 rps maximum tracking rate, 12-bit resolution
Incremental encoder emulation (1024 pulses/rev)
Programmable sinusoidal oscillator on board
Single-supply operation (5.00 V ± 5%)
−40°C to +125°C temperature rating
44-lead LQFP
4 kV ESD protection
Qualified for automotive applications

APPLICATIONS

Automotive motion sensing and control
Hybrid-electric vehicles
Electric power steering
Integrated starter generator/alternator
Industrial motor control
Process control

FUNCTIONAL BLOCK DIAGRAM

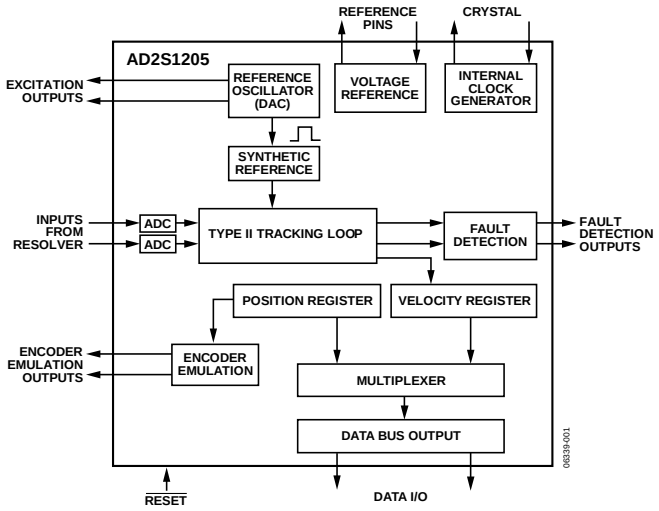

Figure 1.

GENERAL DESCRIPTION

The AD2S1205 is a complete 12-bit resolution tracking resolver-to-digital converter that contains an on-board programmable sinusoidal oscillator providing sine wave excitation for resolvers.

The converter accepts 3.15 V p-p ± 27% input signals on the Sin and Cos inputs. A Type II tracking loop is employed to track the inputs and convert the input Sin and Cos information into a digital representation of the input angle and velocity. The maximum tracking rate is a function of the external clock frequency. The performance of the AD2S105 is specified across a frequency range of 8.192 MHz ± 25%, allowing a maximum tracking rate of 1250 rps.

PRODUCT HIGHLIGHTS

1. Ratiometric Tracking Conversion. The Type II tracking loop provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.
2. System Fault Detection. A fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking.
3. Input Signal Range. The Sin and Cos inputs can accept differential input voltages of 3.15 V p-p ± 27%.
4. Programmable Excitation Frequency. Excitation frequency is easily programmable to 10 kHz, 12 kHz, 15 kHz, or 20 kHz by using the frequency select pins (the FS1 and FS2 pins).
5. Triple Format Position Data. Absolute 12-bit angular position data is accessed via either a 12-bit parallel port or a 3-wire serial interface. Incremental encoder emulation is in standard A-quad-B format with direction output available.
6. Digital Velocity Output. 12-bit signed digital velocity accessed via either a 12-bit parallel port or a 3-wire serial interface.

Rev. A

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REVISION HISTORY

5/10—Rev. 0 to Rev. A

Changes to Features Section ... 1
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1/07—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 5.0 V ± 5% at −40°C to +125°C, CLKIN = 8.192 MHz ± 25%, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Sin, Cos INPUTS[1]					
Voltage	2.3	3.15	4.0	V p-p	Sinusoidal waveforms, Sin − SinLO and Cos − CosLO, differential inputs
Input Bias Current			12	µA	V_{IN} = 4.5 V_{DC}, CLKIN = 10.24 MHz
Input Impedance	0.35			MΩ	V_{IN} = 4.5 V_{DC}
Common-Mode Voltage			100	mV peak	CMV with respect to REFOUT/2 at 10 kHz
Phase-Lock Range	−44		+44	Degrees	Sin/Cos vs. EXC output
ANGULAR ACCURACY					
Angular Accuracy			±11	Arc minutes	Zero acceleration, Y grade
			±22	Arc minutes	Zero acceleration, W grade
Resolution		12		Bits	Guaranteed no missing codes
Linearity INL			2	LSB	Zero acceleration, 0 rps to 1250 rps, CLKIN = 10.24 MHz
Linearity DNL			0.3	LSB	Guaranteed monotonic
Repeatability			1	LSB	
Hysteresis		1		LSB	
VELOCITY OUTPUT					
Velocity Accuracy			2	LSB	Zero acceleration
Resolution		11		Bits	
Linearity		1		LSB	Guaranteed by design, 2 LSB maximum
Offset		0	1	LSB	Zero acceleration
Dynamic Ripple		1		LSB	Zero acceleration
DYNAMIC PERFORMANCE					
Bandwidth	1000		2400	Hz	
Tracking Rate			750	rps	CLKIN = 6.144 MHz , guaranteed by design
			1000	rps	CLKIN = 8.192 MHz , guaranteed by design
			1250	rps	CLKIN = 10.24 MHz , guaranteed by design
Acceleration Error		30		Arc minutes	At 10,000 rps, CLKIN = 8.192 MHz
Settling Time 179° Step Input			5.2	ms	To within ±11 arc minutes, Y grade, CLKIN = 10.24 MHz
			4.0	ms	To within 1 degree, Y grade, CLKIN = 10.24 MHz
EXC, $\overline{EXC}$ OUTPUTS					
Voltage	3.34	3.6	3.83	V p-p	Load ±100 µA
Center Voltage	2.39	2.47	2.52	V	
Frequency		10		kHz	FS1 = high, FS2 = high, CLKIN = 8.192 MHz
		12		kHz	FS1 = high, FS2 = low, CLKIN = 8.192 MHz
		15		kHz	FS1 = low, FS2 = high, CLKIN = 8.192 MHz
		20		kHz	FS1 = low, FS2 = low, CLKIN = 8.192 MHz
EXC/$\overline{EXC}$ DC Mismatch			35	mV	
THD		−58		dB	First five harmonics
FAULT DETECTION BLOCK					
Loss of Signal (LOS)					
Sin/Cos Threshold	2.18	2.24	2.3	V p-p	DOS and LOT go low when Sin or Cos fall below threshold
Angular Accuracy (Worst Case)			57	Degrees	LOS indicated before angular output error exceeds limit (4.0 V p-p input signal and 2.18 V LOS threshold)
Angular Latency (Worst Case)			114	Degrees	Maximum electrical rotation before LOS is indicated (4.0 V p-p input signal and 2.18 V LOS threshold)
Time Latency			125	µs	

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Degradation of Signal (DOS)					
Sin/Cos Threshold	4.0	4.09	4.2	V p-p	DOS goes low when Sin or Cos exceeds threshold
Angular Accuracy (Worst Case)			33	Degrees	DOS indicated before angular output error exceeds limit
Angular Latency (Worst Case)			66	Degrees	Maximum electrical rotation before DOS is indicated
Time Latency			125	µs	
Sin/Cos Mismatch		385	420	mV	DOS latched low when Sin/Cos amplitude mismatch exceeds threshold
Loss of Tracking (LOT)					
Tracking Threshold		5		Degrees	LOT goes low when internal error signal exceeds threshold; guaranteed by design
Time Latency			1.1	ms	
Hysteresis	4			Degrees	Guaranteed by design
VOLTAGE REFERENCE					
REFOUT	2.39	2.47	2.52	V	$\pm I_{OUT}$ = 100 µA
Drift		70		ppm/°C	
PSRR		−60		dB	
CHARGE-PUMP OUTPUT (CPO)					
Frequency		204.8		kHz	Square wave output, CLKIN = 8.192 MHz
Duty Cycle		50		%	
POWER SUPPLY					
I_{DD} Dynamic			20	mA	
ELECTRICAL CHARACTERISTICS					
V_{IL}, Voltage Input Low			0.8	V	
V_{IH}, Voltage Input High	2.0			V	
V_{OL}, Voltage Output Low			0.4	V	+1 mA load
V_{OH}, Voltage Output High	4.0			V	−1 mA load
I_{IL}, Low Level Input Current (Non-Pull-Up)	−10		+10	µA	$\overline{\text{SAMPLE}}$, $\overline{\text{CS}}$, $\overline{\text{RDVEL}}$, CLKIN, $\overline{\text{SOE}}$ pins
I_{IL}, Low Level Input Current (Pull-Up)	−80		+80	µA	$\overline{\text{RD}}$, FS1, FS2, $\overline{\text{RESET}}$ pins
I_{IH}, High Level Input Current	−10		+10	µA	
I_{OZH}, High Level Three-State Leakage	−10		+10	µA	
I_{OZL}, Low Level Three-State Leakage	−10		+10	µA	

[1] The voltages for Sin, SinLO, Cos, and CosLO relative to AGND must be between 0.2 V and AV_{DD}.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	−0.3 V to +7.0 V
Supply Voltage (AV_{DD})	−0.3 V to +7.0 V
Input Voltage	−0.3 V to V_{DD} + 0.3 V
Output Voltage Swing	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range (Ambient)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

[1] Transient currents of up to 100 mA do not cause latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

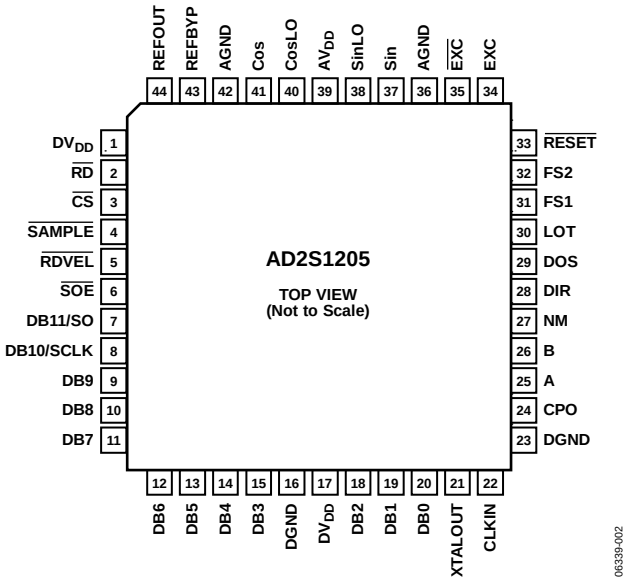

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 17	DV_{DD}	Digital Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD2S1205. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
2	$\overline{RD}$	Edge-Triggered Logic Input. This pin acts as a frame synchronization signal and output enable. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low.
3	$\overline{CS}$	Chip Select. Active low logic input. The device is enabled when $\overline{CS}$ is held low.
4	$\overline{SAMPLE}$	Sample Result. Logic input. Data is transferred from the position and velocity integrators to the position and velocity registers, respectively, after a high-to-low transition on the $\overline{SAMPLE}$ signal.
5	$\overline{RDVEL}$	Read Velocity. Logic input. $\overline{RDVEL}$ input is used to select between the angular position register and the angular velocity register. $\overline{RDVEL}$ is held high to select the angular position register and low to select the angular velocity register.
6	$\overline{SOE}$	Serial Output Enable. Logic input. This pin enables either the parallel or serial interface. The serial interface is selected by holding the $\overline{SOE}$ pin low, and the parallel interface is selected by holding the $\overline{SOE}$ pin high.
7	DB11/SO	Data Bit 11/Serial Data Output Bus. When the $\overline{SOE}$ pin is high, this pin acts as DB11, a three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$. When the $\overline{SOE}$ pin is low, this pin acts as SO, the serial data output bus controlled by $\overline{CS}$ and $\overline{RD}$. The bits are clocked out on the rising edge of SCLK.
8	DB10/SCLK	Data Bit 10/Serial Clock. In parallel mode this pin acts as DB10, a three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$. In serial mode this pin acts as the serial clock input.
9 to 15	DB9 to DB3	Data Bit 9 to Data Bit 3. Three-state data output pins controlled by $\overline{CS}$ and $\overline{RD}$.
16, 23	DGND	Digital Ground. These pins are ground reference points for digital circuitry on the AD2S1205. All digital input signals should be referred to this DGND voltage. Both of these pins can be connected to the AGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
18 to 20	DB2 to DB0	Data Bit 2 to Data Bit 0. Three-state data output pins controlled by $\overline{CS}$ and $\overline{RD}$.
21	XTALOUT	Crystal Output. To achieve the specified dynamic performance, an external crystal is recommended at the CLKIN and XTALOUT pins. The position and velocity accuracy are guaranteed for a frequency range of 8.192 MHz ± 25%.
22	CLKIN	Clock Input. To achieve the specified dynamic performance, an external crystal is recommended at the CLKIN and XTALOUT pins. The position and velocity accuracy are guaranteed for a frequency range of 8.192 MHz ± 25%.
24	CPO	Charge-Pump Output. Analog output. A 204.8 kHz square wave output with a 50% duty cycle is available at the CPO output pin. This square wave output can be used for negative rail voltage generation or to create a VCC rail.
25	A	Incremental Encoder Emulation Output A. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.

Pin No.	Mnemonic	Description
26	B	Incremental Encoder Emulation Output B. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
27	NM	North Marker Incremental Encoder Emulation Output. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
28	DIR	Direction. Logic output. This output is used in conjunction with the incremental encoder emulation outputs. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation.
29	DOS	Degradation of Signal. Logic output. Degradation of signal (DOS) is detected when either resolver input (Sin or Cos) exceeds the specified DOS Sin/Cos threshold. See the Signal Degradation Detection section. DOS is indicated by a logic low on the DOS pin and is not latched when the input signals exceed the maximum input level.
30	LOT	Loss of Tracking. Logic output. LOT is indicated by a logic low on the LOT pin and is not latched. See the Loss of Signal Detection section.
31	FS1	Frequency Select 1. Logic input. FSI in conjunction with FS2 allows the frequency of EXC/$\overline{\text{EXC}}$ to be programmed.
32	FS2	Frequency Select 2. Logic input. FS2 in conjunction with FS1 allows the frequency of EXC/$\overline{\text{EXC}}$ to be programmed.
33	$\overline{\text{RESET}}$	Reset. Logic input. The AD2S1205 requires an external reset signal to hold the $\overline{\text{RESET}}$ input low until V_{DD} is within the specified operating range of 4.5 V to 5.5 V. See the Supply Sequencing and Reset section.
34	EXC	Excitiation Frequency. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{\text{EXC}}$) to the resolver. The frequency of this reference signal is programmable via the FS1 and FS2 pins.
35	$\overline{\text{EXC}}$	Excitation Frequency Complement. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{\text{EXC}}$) to the resolver. The frequency of this reference signal is programmable via the FS1 and FS2 pins.
36, 42	AGND	Analog Ground. These pins are ground reference points for analog circuitry on the AD2S1205. All analog input signals and any external reference signal should be referred to this AGND voltage. Both of these pins should be connected to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
37	Sin	Positive Analog Input of Differential Sin/SinLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
38	SinLO	Negative Analog Input of Differential Sin/SinLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
39	AV_{DD}	Analog Supply Voltage, 4.75 V to 5.25 V. This pin is the supply voltage for all analog circuitry on the AD2S1205. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
40	CosLO	Negative Analog Input of Differential Cos/CosLO Pair.
41	Cos	Positive Analog Input of Differential Cos/CosLO Pair.
43	REFBYP	Reference Bypass. Reference decoupling capacitors should be connected here. Typical recommended values are 10 µF and 0.01 µF.
44	REFOUT	Voltage Reference Output, 2.39 V to 2.52 V.

RESOLVER FORMAT SIGNALS

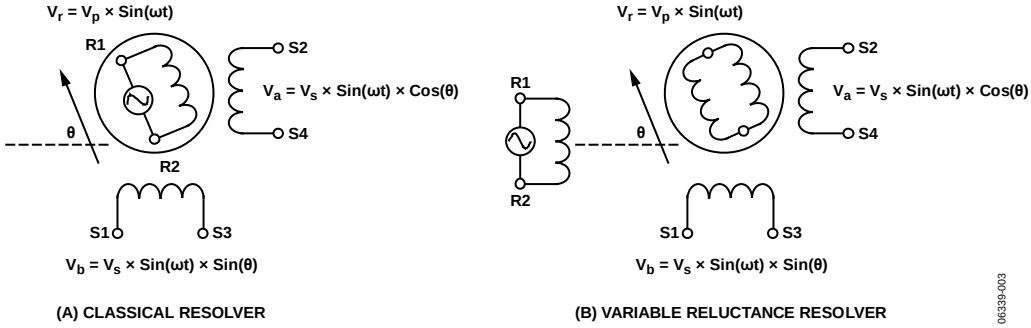

Figure 3. Classical Resolver vs. Variable Reluctance Resolver

A classical resolver is a rotating transformer that typically has a primary winding on the rotor and two secondary windings on the stator. A variable reluctance resolver, on the other hand, has the primary and secondary windings on the stator and no windings on the rotor, as shown in Figure 3; however, the saliency in this rotor design provides the sinusoidal variation in the secondary coupling with the angular position. For both designs, the resolver output voltages (S3 − S1, S2 − S4) are as follows:

$$S3 - S1 = E_0 Sin(\omega t) \times Sin\theta \quad (1)$$

$$S2 - S4 = E_0 Sin(\omega t) \times Cos\theta$$

where:
θ is the shaft angle.
$Sin(\omega t)$ is the rotor excitation frequency.
E_0 is the rotor excitation amplitude.

The stator windings are displaced mechanically by 90° (see Figure 3). The primary winding is excited with an ac reference. The amplitude of subsequent coupling onto the secondary windings is a function of the position of the rotor (shaft) relative to the stator. The resolver therefore produces two output voltages (S3 − S1, S2 − S4), modulated by the sine and cosine of the shaft angle. Resolver format signals refer to the signals derived from the output of a resolver, as shown in Equation 1. Figure 4 illustrates the output format.

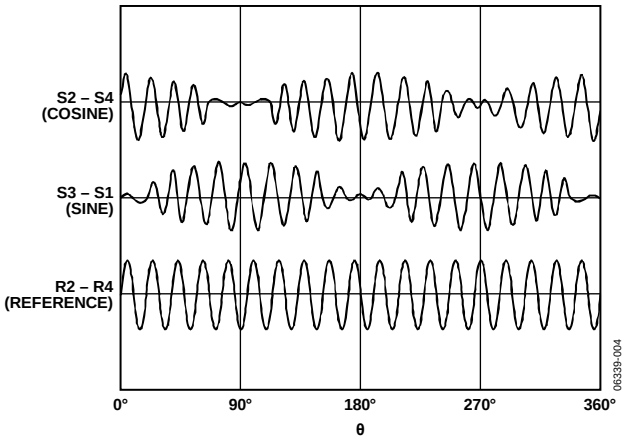

Figure 4. Electrical Resolver Representation

THEORY OF OPERATION

The AD2S1205's operation is based on a Type II tracking closed-loop principle. The digitally implemented tracking loop continually tracks the position and velocity of the resolver without the need for external convert and wait states. As the resolver moves through a position equivalent to the least significant bit weighting, the tracking loop output is updated by 1 LSB.

The converter tracks the shaft angle (θ) by producing an output angle (ϕ) that is fed back and compared with the input angle (θ); the difference between the two angles is the error, which is driven towards 0 when the converter is correctly tracking the input angle. To measure the error, S3 − S1 is multiplied by Cosϕ and S2 − S4 is multiplied by Sinϕ to give

$$\begin{aligned} &E_0 Sin(\omega t) \times Sin\theta Cos\varphi \quad \text{for S3 } - \text{S1} \\ &E_0 Sin(\omega t) \times Cos\theta Sin\varphi \quad \text{for S2 } - \text{S4} \end{aligned} \tag{2}$$

The difference is taken, giving

$$E_0 Sin(\omega t) \times (Sin\theta Cos\phi - Cos\theta Sin\varphi) \tag{3}$$

This signal is demodulated using the internally generated synthetic reference, yielding

$$E_0 (Sin\theta Cos\phi - Cos\theta Sin\phi) \tag{4}$$

Equation 4 is equivalent to $E_0 Sin(\theta - \phi)$, which is approximately equal to $E_0(\theta - \phi)$ for small values of $\theta - \phi$, where $\theta - \phi$ is the angular error.

The value $E_0(\theta - \phi)$ is the difference between the angular error of the rotor and the digital angle output of the converter.

A phase-sensitive demodulator, some integrators, and a compensation filter form a closed-loop system that seeks to null the error signal. If this is accomplished, ϕ equals the resolver angle, θ, within the rated accuracy of the converter. A Type II tracking loop is used so that constant velocity inputs can be tracked without inherent error.

For more information about the operation of the converter, see the Circuit Dynamics section.

FAULT DETECTION CIRCUIT

The AD2S1205 fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking; however, the position indicated by the AD2S1205 may differ significantly from the actual shaft position of the resolver.

MONITOR SIGNAL

The AD2S1205 generates a monitor signal by comparing the angle in the position register to the incoming Sin and Cos signals from the resolver. The monitor signal is created in a similar fashion to the error signal (described in the Theory of Operation section). The incoming Sinθ and Cosθ signals are multiplied by the Sin and Cos of the output angle, respectively, and then these values are added together:

$$Monitor = (A1 \times Sin\theta \times Sin\varphi) + (A2 \times Cos\theta \times Cos\varphi) \tag{5}$$

where:
$A1$ is the amplitude of the incoming Sin signal ($A1 \times Sin\theta$).
$A2$ is the amplitude of the incoming Cos signal ($A2 \times Cos\theta$).
θ is the resolver angle.
ϕ is the angle stored in the position register.

Note that Equation 5 is shown after demodulation with the carrier signal Sin(ωt) removed. Also note that for a matched input signal (that is, a no fault condition), A1 is equal to A2.

When A1 is equal to A2 and the converter is tracking (therefore, θ is equal to ϕ), the monitor signal output has a constant magnitude of A1 ($Monitor = A1 \times (Sin^2\theta + Cos^2\theta) = A1$), which is independent of the shaft angle. When A1 does not equal A2, the monitor signal magnitude alternates between A1 and A2 at twice the rate of the shaft rotation. The monitor signal is used to detect degradation or loss of input signals.

LOSS OF SIGNAL DETECTION

Loss of signal (LOS) is detected when either resolver input (Sin or Cos) falls below the specified LOS Sin/Cos threshold. The AD2S1205 detects this by comparing the monitor signal to a fixed minimum value. Without the use of external circuitry, the AD2S1205 can detect the loss of up to three of the four connections from the resolver. The addition of two external 68 kΩ resistors, as outlined in Figure 5, ensures that the loss of all 4 connections, that is, complete removal of the resolver, may also be detected. LOS is indicated by both DOS and LOT latching as logic low outputs. The DOS and LOT pins are reset to the no fault state by a rising edge of $\overline{\text{SAMPLE}}$. The LOS condition has priority over both the DOS and LOT conditions, as shown in Table 4. LOS is indicated within 57° of the angular output error (worst case).

SIGNAL DEGRADATION DETECTION

Degradation of signal (DOS) is detected when either resolver input (Sin or Cos) exceeds the specified DOS Sin/Cos threshold. The AD2S1205 detects this by comparing the monitor signal to a fixed maximum value. In addition, DOS is detected when the amplitudes of the Sin and Cos input signals are mismatched by more than the specified DOS Sin/Cos mismatch. This is identified because the AD2S1205 continuously stores the minimum and maximum magnitude of the monitor signal in internal registers and calculates the difference between these values. DOS is indicated by a logic low on the DOS pin and is not latched when the input signals exceed the maximum input level. When DOS is indicated due to mismatched signals, the output is latched low until a rising edge of $\overline{\text{SAMPLE}}$ resets the stored minimum and maximum values. The DOS condition has priority over the LOT condition, as shown in Table 4. DOS is indicated within 33° of the angular output error (worst case).

LOSS OF POSITION TRACKING DETECTION

Loss of tracking (LOT) is detected when

- The internal error signal of the AD2S1205 exceeds 5°.
- The input signal exceeds the maximum tracking rate.
- The internal position (at the position integrator) differs from the external position (at the position register) by more than 5°.

LOT is indicated by a logic low on the LOT pin and is not latched. LOT has a 4° hysteresis and is not cleared until the internal error signal or internal/external position mismatch is less than 1°. When the maximum tracking rate is exceeded, LOT is cleared only if the velocity is less than the maximum tracking rate and the internal/external position mismatch is less than 1°. LOT can be indicated for step changes in position (such as after a $\overline{\text{RESET}}$ signal is applied to the AD2S1205), or for accelerations of >~65,000 rps^2. It is also useful as a built-in test to indicate that the tracking converter is functioning properly. The LOT condition has lower priority than both the DOS and LOS conditions, as shown in Table 4. The LOT and DOS conditions cannot be indicated at the same time.

Table 4. Fault Detection Decoding

Condition	DOS Pin	LOT Pin	Order of Priority
Loss of Signal (LOS)	0	0	1
Degradation of Signal (DOS)	0	1	2
Loss of Tracking (LOT)	1	0	3
No Fault	1	1	

RESPONDING TO A FAULT CONDITION

If a fault condition (LOS, DOS, or LOT) is indicated by the AD2S1205, the output data is presumed to be invalid. Even if a $\overline{\text{RESET}}$ or $\overline{\text{SAMPLE}}$ pulse releases the fault condition and is not immediately followed by another fault, the output data may be corrupted. As discussed previously, there are some fault conditions with inherent latency. If the device fault is cleared, there may be some latency in the resolver's mechanical position before the fault condition is reindicated.

When a fault is indicated, all output pins still provide data, although the data may or may not be valid. The fault condition does not force the parallel, serial, or encoder outputs to a known state.

Response to specific fault conditions is a system-level requirement. The fault outputs of the AD2S1205 indicate that the device has sensed a potential problem with either the internal or external signals of the AD2S1205. It is the responsibility of the system designer to implement the appropriate fault-handling schemes within the control hardware and/or algorithm of a given application based on the indicated fault(s) and the velocity or position data provided by the AD2S1205.

FALSE NULL CONDITION

Resolver-to-digital converters that employ Type II tracking loops based on the previously stated error equation (see Equation 4 in the Theory of Operation section) can suffer from a condition known as a false null. This condition is caused by a metastable solution to the error equation when $\theta - \phi = 180°$. The AD2S1205 is not susceptible to this condition because its hysteresis is implemented external to the tracking loop. As a result of the loop architecture chosen for the AD2S1205, the internal error signal constantly has some movement (1 LSB per clock cycle); therefore, in a metastable state, the converter moves to an unstable condition within one clock cycle. This causes the tracking loop to respond to the false null condition as if it were a 180° step change in input position (the response time is the same, as specified in the Dynamic Performance section of Table 1). Therefore, it is impossible to enter the metastable condition after the start-up sequence if the resolver signals are valid.

ON-BOARD PROGRAMMABLE SINUSOIDAL OSCILLATOR

An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable to four standard frequencies (10 kHz, 12 kHz, 15 kHz, or 20 kHz) by using the FS1 and FS2 pins (see Table 5). FS1 and FS2 have internal pull-ups, so the default frequency is 10 kHz. The amplitude of this signal is centered on 2.5 V and has an amplitude of 3.6 V p-p.

Table 5. Excitation Frequency Selection

Frequency Selection (kHz)	FS1	FS2
10	1	1
12	1	0
15	0	1
20	0	0

The frequency of the reference signal is a function of the CLKIN frequency. By decreasing the CLKIN frequency, the minimum excitation frequency can also be decreased. This allows an excitation frequency of 7.5 kHz to be set when using a CLKIN frequency of 6.144 MHz, and it also decreases the maximum tracking rate to 750 rps.

The reference output of the AD2S1205 requires an external buffer amplifier to provide gain and additional current to drive the resolver. See Figure 6 for a suggested buffer circuit.

The AD2S1205 also provides an internal synchronous reference signal that is phase locked to its Sin and Cos inputs. Phase errors between the resolver's primary and secondary windings may degrade the accuracy of the RDC and are compensated for by using this synchronous reference signal. This also compensates for the phase shifts due to temperature and cabling, and it eliminates the need for an external preset phase-compensation circuit.

SYNTHETIC REFERENCE GENERATION

When a resolver undergoes a high rotation rate, the RDC tends to act as an electric motor and produces speed voltages in addition to the ideal Sin and Cos outputs. These speed voltages are in quadrature to the main signal waveform. Moreover, nonzero resistance in the resolver windings causes a nonzero phase shift between the reference input and the Sin and Cos outputs. The combination of the speed voltages and the phase shift causes a tracking error in the RDC that is approximated by

$$Error = Phase\,Shift \times \frac{Rotation\,Rate}{Reference\,Frequency} \quad (6)$$

To compensate for the described phase error between the resolver reference excitation and the Sin/Cos signals, an internal synthetic reference signal is generated in phase with the reference frequency carrier. The synthetic reference is derived using the internally filtered Sin and Cos signals. It is generated by determining the zero crossing of either the Sin or Cos (whichever signal is larger), which improves phase accuracy, and evaluating the phase of the resolver reference excitation. The synthetic reference reduces the phase shift between the reference and Sin/Cos inputs to less than 10° and can operate for phase shifts of ±45°.

CHARGE-PUMP OUTPUT

A 204.8 kHz square wave output with a 50% duty cycle is available at the CPO pin of the AD2S1205. This square wave output can be used for negative rail voltage generation or to create a V_{CC} rail.

CONNECTING THE CONVERTER

Ground is connected to the AGND and DGND pins (see Figure 5). A positive power supply (V_{DD}) of 5 V dc ± 5% is connected to the AV_{DD} and DV_{DD} pins, with typical values for the decoupling capacitors being 10 nF and 4.7 µF. These capacitors are then placed as close to the device pins as possible and are connected to both AV_{DD} and DV_{DD}. If desired, the reference oscillator frequency can be changed from the nominal value of 10 kHz using FS1 and FS2. Typical values for the oscillator decoupling capacitors are 20 pF, whereas typical values for the reference decoupling capacitors are 10 µF and 0.01 µF. As outlined in the Loss of Signal Detection section 68 kΩ resistors between the Sin and SinLO inputs and the Cos and CosLO inputs can be used to ensure loss of signal detection when all four inputs from resolver are disconnected.

In this recommended configuration, the converter introduces a $V_{REF}/2$ offset in the Sin and Cos signal outputs from the resolver. The SinLO and CosLO signals can each be connected to a different potential relative to ground if the Sin and Cos signals adhere to the recommended specifications. Note that because the EXC and $\overline{EXC}$ outputs are differential, there is an inherent gain of 2×. Figure 6 shows a suggested buffer circuit. Capacitor C1 may be used in parallel with Resistor R2 to filter out any noise that may exist on the EXC and $\overline{EXC}$ outputs. Care should be taken when selecting the cutoff frequency of this filter to ensure that phase shifts of the carrier caused by the filter do not exceed the phase lock range of the AD2S1205.

The gain of the circuit is

$$CarrierGain = -(R2/R1) \times (1/(1 + R2 \times C1 \times \omega)) \quad (7)$$

and

$$V_{OUT} = \left(V_{REF} \times \left(1 + \frac{R2}{R1}\right)\right) - \left(\frac{R2}{R1} \times (1/(1 + R2 \times C1 \times \omega))V_{IN}\right) \quad (8)$$

where:
ω is the radian frequency of the applied signal.

V_{REF}, a dc voltage, is set so that V_{OUT} is always a positive value, eliminating the need for a negative supply.

A separate screened twisted pair cable is recommended for analog inputs Sin/SinLO and Cos/CosLO. The screens should terminate to either REFOUT or AGND.

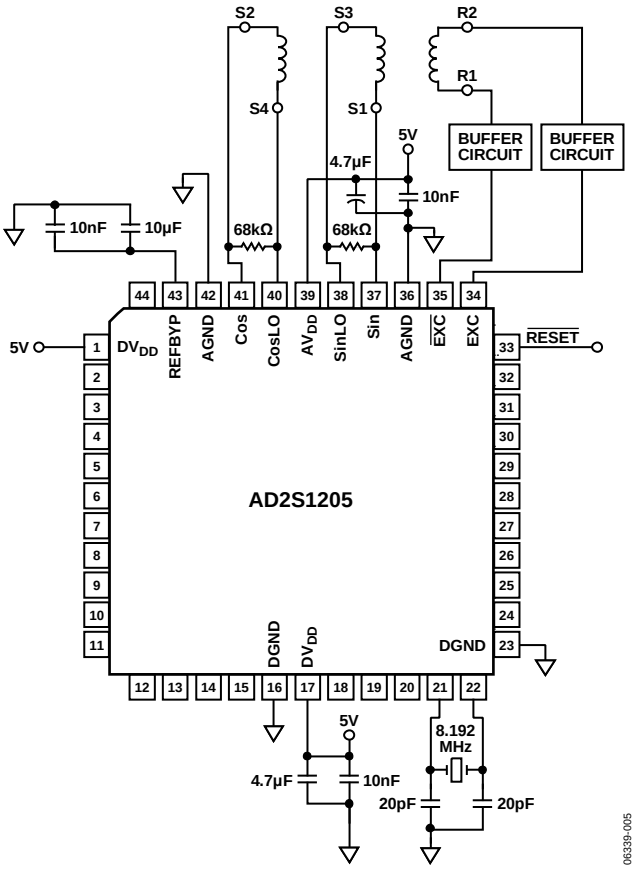

Figure 5. Connecting the AD2S1205 to a Resolver

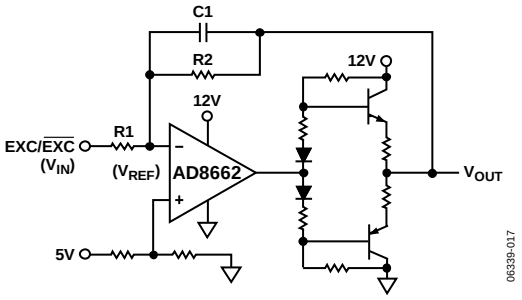

Figure 6. Buffer Circuit

CLOCK REQUIREMENTS

To achieve the specified dynamic performance, an external crystal is recommended at the CLKIN and XTALOUT pins. The position and velocity accuracy are guaranteed for a frequency range of 8.192 MHz ± 25%. However, the velocity outputs are scaled in proportion to the clock frequency so that if the clock is 25% greater than the nominal, the full-scale velocity is 25% greater than nominal. The maximum tracking rate, tracking loop bandwidth, and excitation frequency also vary with the clock frequency.

ABSOLUTE POSITION AND VELOCITY OUTPUT

The angular position and velocity are represented by binary data and can be extracted via either a 12-bit parallel interface or a 3-wire serial interface that operates at clock rates of up to 25 MHz.

$\overline{\text{SOE}}$ Input

The serial output enable pin ($\overline{\text{SOE}}$) is held high to enable the parallel interface and low to enable the serial interface. In the latter case, Pin DB0 to Pin DB9 are placed into a high impedance state while DB11 is the serial output (SO) and DB10 is the serial clock input (SCLK).

Data Format

The angular position data represents the absolute position of the resolver shaft as a 12-bit unsigned binary word. The angular velocity data is a 12-bit twos complement word, representing the velocity of the resolver shaft rotating in either a clockwise or counterclockwise direction.

PARALLEL INTERFACE

The angular position and velocity are available on the AD2S1205 in two 12-bit registers, accessed via the 12-bit parallel port. The parallel interface is selected by holding the $\overline{\text{SOE}}$ pin high. Data is transferred from the velocity and position integrators to the position and velocity registers, respectively, after a high-to-low transition on the $\overline{\text{SAMPLE}}$ pin. The $\overline{\text{RDVEL}}$ pin selects whether data from the position or velocity register is transferred to the output register. The $\overline{\text{CS}}$ pin must be held low to transfer data from the selected register to the output register. Finally, the $\overline{\text{RD}}$ input is used to read the data from the output register and to enable the output buffer. The timing requirements for the read cycle are shown in Figure 7.

$\overline{\text{SAMPLE}}$ Input

Data is transferred from the position and velocity integrators to the position and velocity registers, respectively, after a high-to-low transition on the $\overline{\text{SAMPLE}}$ signal. This pin must be held low for at least t_1 to guarantee correct latching of the data. $\overline{\text{RD}}$ should not be pulled low before this time because data will not be ready. The converter continues to operate during the read process. A rising edge of $\overline{\text{SAMPLE}}$ resets the internal registers that contain the minimum and maximum magnitude of the monitor signal.

$\overline{CS}$ Input

The device is enabled when $\overline{CS}$ is held low.

$\overline{RDVEL}$ Input

$\overline{RDVEL}$ input is used to select between the angular position register and the angular velocity register, as shown in Figure 7. $\overline{RDVEL}$ is held high to select the angular position register and low to select the angular velocity register. The $\overline{RDVEL}$ pin must be set (stable) at least t_4 before the $\overline{RD}$ pin is pulled low.

$\overline{RD}$ Input

The 12-bit data bus lines are normally in a high impedance state. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. A falling edge of the $\overline{RD}$ signal transfers data to the output buffer. The selected data is made available to the bus to be read within t_6 of the $\overline{RD}$ pin going low. The data pins return to a high impedance state when the $\overline{RD}$ pin returns to a high state within t_7. When reading data continuously, wait a minimum of t_3 after $\overline{RD}$ is released before reapplying it.

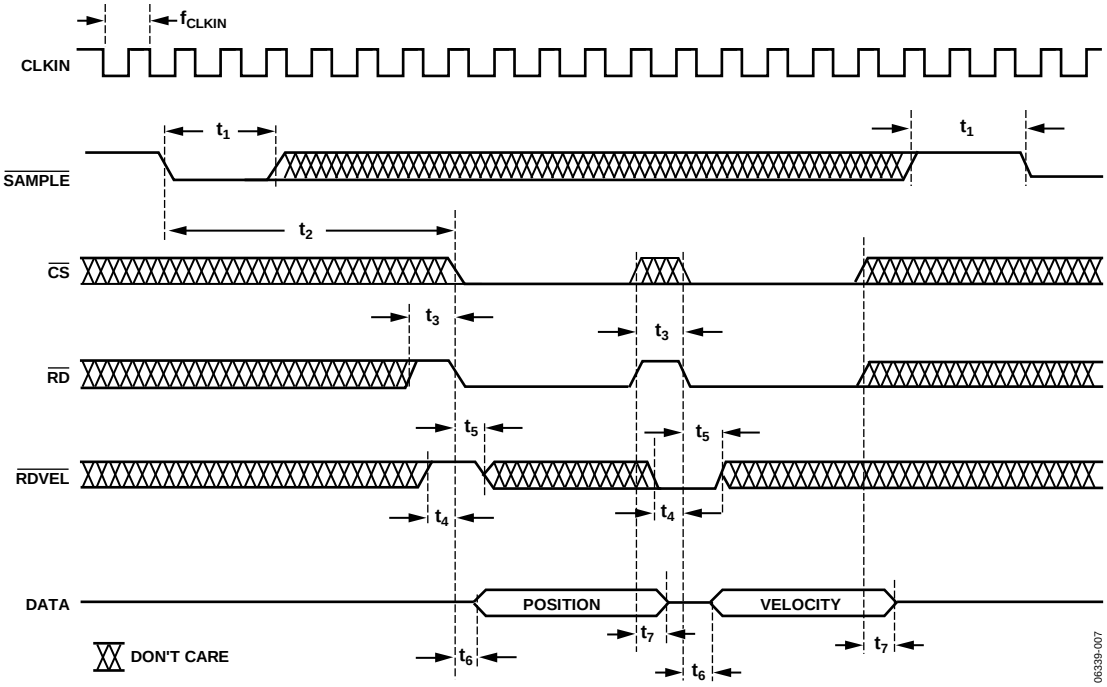

Figure 7. Parallel Port Read Timing

Table 6. Parallel Port Timing

Parameter	Description	Min	Typ	Max	Unit
f_{CLKIN}	Frequency of clock input	6.144	8.192	10.24	MHz
t_1	$\overline{SAMPLE}$ pulse width	$2 \times (1/f_{CLKIN}) + 20$			ns
t_2	Delay from $\overline{SAMPLE}$ before $\overline{RD}/\overline{CS}$ low	$6 \times (1/f_{CLKIN}) + 20$			ns
t_3	$\overline{RD}$ pulse width	18			ns
t_4	Set time $\overline{RDVEL}$ before $\overline{RD}/\overline{CS}$ low	5			ns
t_5	Hold time $\overline{RDVEL}$ after $\overline{RD}/\overline{CS}$ low	7			ns
t_6	Enable delay $\overline{RD}/\overline{CS}$ low to data valid			30	ns
t_7	Disable delay $\overline{RD}/\overline{CS}$ low to data high-Z			18	ns

SERIAL INTERFACE

The angular position and velocity are available on the AD2S1205 in two 12-bit registers. These registers can be accessed via a 3-wire serial interface (SO, $\overline{RD}$, and SCLK) that operates at clock rates of up to 25 MHz and is compatible with SPI and DSP interface standards. The serial interface is selected by holding the $\overline{SOE}$ pin low. Data from the position and velocity integrators are first transferred to the position and velocity registers using the $\overline{SAMPLE}$ pin. The $\overline{RDVEL}$ pin selects whether data is transferred from the position or velocity register to the output register, and the $\overline{CS}$ pin must be held low to transfer data from the selected register to the output register. Finally, the $\overline{RD}$ input is used to read the data that is clocked out of the output register and is available on the serial output pin (SO). When the serial interface is selected, DB11 is used as the serial output pin (SO), DB10 is used as the serial clock input (SCLK), and Pin DB0 to Pin DB9 are placed into the high impedance state. The timing requirements for the read cycle are described in Figure 8.

SO Output

The output shift register is 16 bits wide. Data is clocked out of the device as a 16-bit word by the serial clock input (SCLK). The timing diagram for this operation is shown in Figure 8. The 16-bit word consists of 12 bits of angular data (position or velocity, depending on $\overline{RDVEL}$ input), one $\overline{RDVEL}$ status bit, and three status bits (a parity bit, a degradation of signal bit, and a loss of tracking bit). Data is clocked out MSB first from the SO pin, beginning with DB15. DB15 through DB4 correspond to the angular information. The angular position data format is unsigned binary, with all 0s corresponding to 0° and all 1s corresponding to 360° − l LSB. The angular velocity data format is twos complement, with the MSB representing the rotation direction. DB3 is the $\overline{RDVEL}$ status bit, with a 1 indicating position and a 0 indicating velocity. DB2 is DOS, the degradation of signal flag (refer to the Fault Detection Circuit section). Bit 1 is LOT, the loss of tracking flag (refer to the Fault Detection Circuit section). Bit 0 is PAR, the parity bit. The position and velocity data are in odd parity format, and the data readback always contains an odd number of logic highs (1s).

$\overline{SAMPLE}$ Input

Data is transferred from the position and velocity integrators to the position and velocity registers, respectively, after a high-to-low transition on the $\overline{SAMPLE}$ signal. This pin must be held low for at least t_1 to guarantee correct latching of the data. $\overline{RD}$ should not be pulled low before this time because data will not be ready. The converter continues to operate during the read process.

$\overline{CS}$ Input

The device is enabled when $\overline{CS}$ is held low.

$\overline{RD}$ Input

The 12-bit data bus lines are normally in a high impedance state. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. The $\overline{RD}$ input is an edge-triggered input that acts as a frame synchronization signal and an output enable. On a falling edge of the $\overline{RD}$ signal, data is transferred to the output buffer. Data is then available on the serial output pin (SO); however, it is only valid after $\overline{RD}$ is held low for t_9. The serial data is clocked out of the SO pin on the rising edges of SCLK, and each data bit is available at the SO pin on the falling edge of SCLK. However, as the MSB is clocked out by the falling edge of $\overline{RD}$, the MSB is available at the SO pin on the first falling edge of SCLK. Each subsequent bit of the data-word is shifted out on the rising edge of SCLK and is available at the SO pin on the falling edge of SCLK for the next 15 clock pulses.

The high-to-low transition of $\overline{RD}$ must occur during the high time of the SCLK to avoid DB14 being shifted on the first rising edge of the SCLK, which would result in the MSB being lost. $\overline{RD}$ may rise high after the last falling edge of SCLK. If $\overline{RD}$ is held low and additional SCLKs are applied after DB0 has been read, then 0s will be clocked from the data output. When reading data continuously, wait a minimum of t_5 after $\overline{RD}$ is released before reapplying it.

$\overline{RDVEL}$ Input

$\overline{RDVEL}$ input is used to select between the angular position register and the angular velocity register. $\overline{RDVEL}$ is held high to select the angular position register and low to select the angular velocity register. The $\overline{RDVEL}$ pin must be set (stable) at least t_4 before the $\overline{RD}$ pin is pulled low.

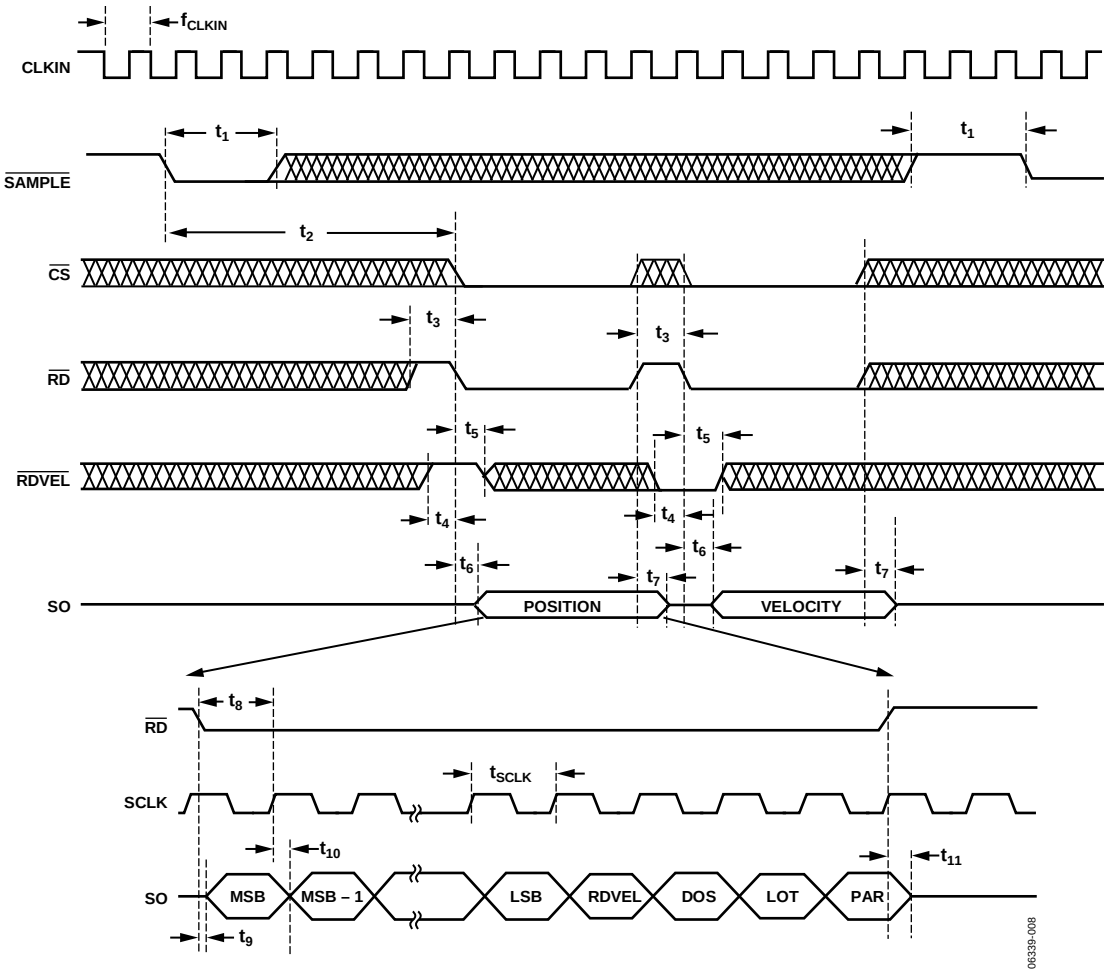

Figure 8. Serial Port Read Timing

Table 7. Serial Port Timing[1]

Parameter	Description	Min	Typ	Max	Unit
t_8	MSB read time $\overline{RD}/\overline{CS}$ to SCLK	15		t_{SCLK}	ns
t_9	SO enable time $\overline{RD}/\overline{CS}$ to DB valid			30	ns
t_{10}	Data access time, SCLK to DB valid			30	ns
t_{11}	Bus relinquish time $\overline{RD}/\overline{CS}$ to SO high-Z			18	ns
t_{SCLK}	Serial clock period (25 MHz maximum)	40			ns

[1] t_1 to t_7 are as defined in Table 6.

INCREMENTAL ENCODER OUTPUTS

The A, B, and NM incremental encoder emulation outputs are free running and are valid if the resolver format input signals applied to the converter are valid.

The AD2S1205 emulates a 1024-line encoder, meaning that, in terms of the converter resolution, one revolution produces 1024 A and B pulses. Pulse A leads Pulse B for increasing angular rotation (clockwise direction). The addition of the DIR output negates the need for external A and B direction decode logic. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation. DIR can be considered an asynchronous output that can make multiple changes in state between two consecutive LSB update cycles. This occurs when the direction of the rotation of the input changes but the magnitude of the rotation is less than 1 LSB.

The north marker pulse is generated as the absolute angular position passes through zero. The north marker pulse width is set internally for 90° and is defined relative to the A cycle. Figure 9 details the relationship between A, B, and NM.

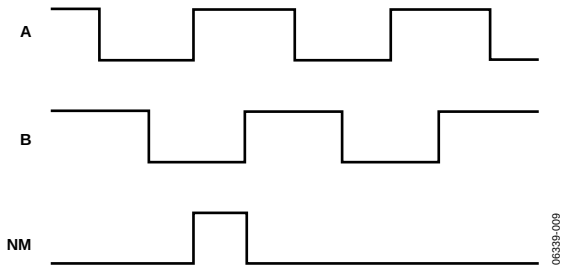

Figure 9. A, B, and NM Timing for Clockwise Rotation

Unlike incremental encoders, the AD2S1205 encoder output is not subject to error specifications such as cycle error, eccentricity, pulse and state width errors, count density, and phase ϕ. The maximum speed rating (n) of an encoder is calculated from its maximum switching frequency (f_{MAX}) and its pulses per revolution (PPR).

$$n = \frac{60 \times f_{MAX}}{PPR} \quad (9)$$

The A and B pulses of the AD2S1205 are initiated from the internal clock frequency, which is exactly half the external CLKIN frequency. With a nominal CLKIN frequency of 8.192 MHz, the internal clock frequency is 4.096 MHz. The equivalent encoder switching frequency is

$$1/4 \times 4.096 \text{ MHz} = 1.024 \text{ MHz (4 Updates} = 1 \text{ Pulse)} \quad (10)$$

For 12 bits, the PPR is 1024. Therefore, the maximum speed (n) of the AD2S1205 with a CLKIN of 8.192 MHz is

$$n = \frac{60 \times 1{,}024{,}000}{1024} = 60{,}000 \text{ rpm} \quad (11)$$

To achieve the maximum speed of 75,000 rpm, select an external CLKIN of 10.24 MHz to produce an internal clock frequency equal to 5.12 MHz.

This compares favorably with encoder specifications, which state f_{MAX} as 20 kHz (photo diodes) to 125 kHz (laser based), depending on the type of light system used. A 1024-line laser-based encoder has a maximum speed of 7300 rpm.

The inclusion of A and B outputs allows an AD2S1205 and resolver-based solution to replace optical encoders directly without the need to change or upgrade the user's existing application software.

SUPPLY SEQUENCING AND RESET

The AD2S1205 requires an external reset signal to hold the $\overline{\text{RESET}}$ input low until V_{DD} is within the specified operating range of 4.5 V to 5.5 V.

The $\overline{\text{RESET}}$ pin must be held low for a minimum of 10 µs after V_{DD} is within the specified range (shown as t_{RST} in Figure 10). Applying a $\overline{\text{RESET}}$ signal to the AD2S1205 initializes the output position to a value of 0x000 (degrees output through the parallel, serial, and encoder interfaces) and causes LOS to be indicated (LOT and DOS pins pulled low), as shown in Figure 10.

Failure to apply the correct power-up/reset sequence may result in an incorrect position indication.

After a rising edge on the $\overline{\text{RESET}}$ input, the device must be allowed at least 20 ms (shown as t_{TRACK} in Figure 10) for the internal circuitry to stabilize and the tracking loop to settle to the step change of the input position. After t_{TRACK}, a $\overline{\text{SAMPLE}}$ pulse must be applied, which in turn releases the LOT and DOT pins to the state determined by the fault detection circuitry and provides valid position data at the parallel and serial outputs. (Note that if position data is acquired via the encoder outputs, it can be monitored during t_{TRACK}.)

The $\overline{\text{RESET}}$ pin is then internally pulled up.

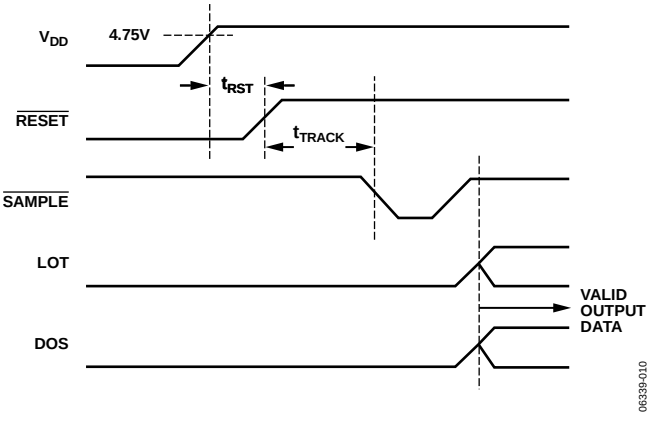

Figure 10. Power Supply Sequencing and Reset

CIRCUIT DYNAMICS

LOOP RESPONSE MODEL

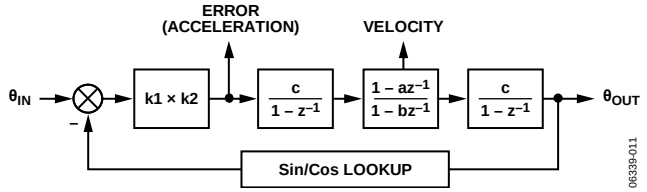

Figure 11. RDC System Response Block Diagram

The RDC is a mixed-signal device that uses two ADCs to digitize signals from the resolver and a Type II tracking loop to convert these to digital position and velocity words.

The first gain stage consists of the ADC gain on the Sin/Cos inputs and the gain of the error signal into the first integrator. The first integrator generates a signal proportional to velocity. The compensation filter contains a pole and a zero that are used to provide phase margin and reduce high frequency noise gain. The second integrator is the same as the first and generates the position output from the velocity signal. The Sin/Cos lookup has unity gain. The values for each section are as follows:

ADC gain parameter ($k1_{NOM}$ = 1.8/2.5)

$$k2 = \frac{V_{IN}(\mathrm{V_p})}{V_{REF}(\mathrm{V})} \tag{12}$$

Error gain parameter

$$k2 = 18 \times 10^6 \times 2\pi \tag{13}$$

Compensator zero coefficient

$$a = \frac{4095}{4096} \tag{14}$$

Compensator pole coefficient

$$b = \frac{4085}{4096} \tag{15}$$

Integrator gain parameter

$$c = \frac{1}{4{,}096{,}000} \tag{16}$$

INT1 and INT2 transfer function

$$I(z) = \frac{c}{1 - z^{-1}} \tag{17}$$

Compensation filter transfer function

$$C(z) = \frac{1 - az^{-1}}{1 - bz^{-1}} \tag{18}$$

R2D open-loop transfer function

$$G(z) = k1 \times k2 \times I(z)^2 \times C(z) \tag{19}$$

R2D closed-loop transfer function

$$H(z) = \frac{G(z)}{1 + G(z)} \tag{20}$$

The closed-loop magnitude and phase responses are that of a second-order low-pass filter (see Figure 12 and Figure 13).

To convert G(z) into the s-plane, an inverse bilinear transformation is performed by substituting the following equation for *z*:

$$z = \frac{\frac{2}{t} + s}{\frac{2}{t} - s} \tag{21}$$

where *t* is the sampling period (1/4.096 MHz ≈ 244 ns).

Substitution yields the open-loop transfer function G(s).

$$G(s) = \frac{k1 \times k2(1-a)}{a-b} \times \frac{1 + st + \frac{s^2t^2}{4}}{s^2} \times \frac{1 + s \times \frac{t(1+a)}{2(1-a)}}{1 + s \times \frac{t(1+b)}{2(1-b)}} \tag{22}$$

This transformation produces the best matching at low frequencies ($f < f_{SAMPLE}$). At such frequencies (within the closed-loop bandwidth of the AD2S1205), the transfer function can be simplified to

$$G(s) \cong \frac{K_a}{s^2} \times \frac{1 + st_1}{1 + st_2} \tag{23}$$

where:

$$t_1 = \frac{t(1+a)}{2(1-a)}$$

$$t_2 = \frac{t(1+b)}{2(1-b)}$$

$$K_a = \frac{k1 \times k2(1-a)}{a-b}$$

Solving for each value gives t_1 = 1 ms, t_2 = 90 µs, and $K_a \approx 7.4 \times 10^6$ s^{-2}. Note that the closed-loop response is described as

$$H(s) = \frac{G(s)}{1 + G(s)} \tag{24}$$

By converting the calculation to the s-domain, it is possible to quantify the open-loop dc gain (K_a). This value is useful to calculate the acceleration error of the loop (see the Sources of Error section).

The step response to a 10° input step is shown in Figure 14. Because the error calculation (see Equation 2) is nonlinear for large values of θ – ϕ, the response time for such large (90° to 180°) step changes in position typically takes three times as long as the response to a small (<20°) step change in position. In response to a step change in velocity, the AD2S1205 exhibits the same response characteristics as it does for a step change in position.

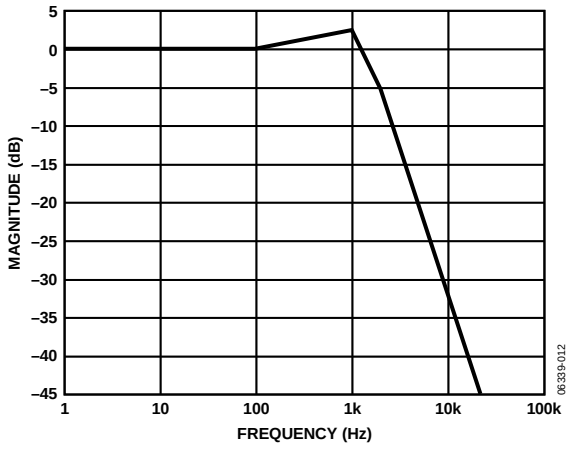

Figure 12. RDC System Magnitude Response

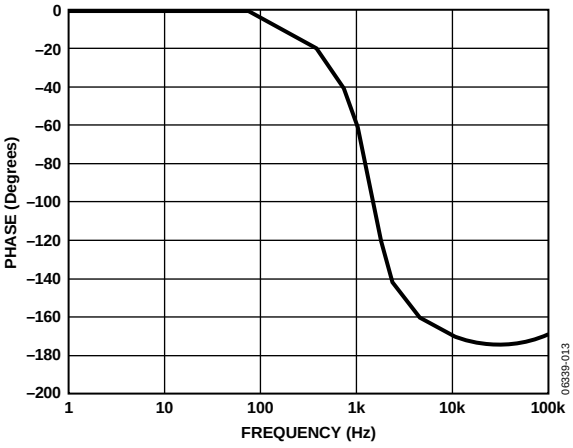

Figure 13. RDC System Phase Response

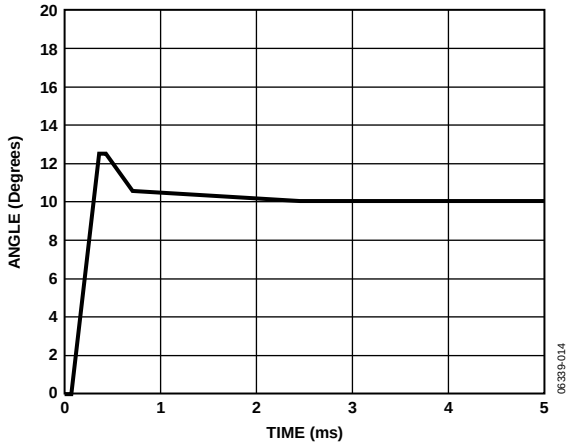

Figure 14. RDC Small Step Response

SOURCES OF ERROR

Acceleration

A tracking converter employing a Type II servo loop does not have a lag in velocity. There is, however, an error associated with acceleration. This error can be quantified using the acceleration constant (K_a) of the converter.

$$K_a = \frac{Input\ Acceleration}{Tracking\ Error} \tag{25}$$

Conversely,

$$Tracking\ Error = \frac{Input\ Acceleration}{K_a} \tag{26}$$

Figure 15 shows tracking error vs. acceleration for the AD2S1205.

The units of the numerator and denominator must be consistent. The maximum acceleration of the AD2S1205 is defined as the acceleration that creates an output position error of 5° (that is, when LOT is indicated). The maximum acceleration can be calculated as

$$Maximum\ Acceleration = \frac{K_a(\sec^{-2}) \times 5°}{360(°/\text{rev})} \cong 103{,}000\ \text{rps}^2 \tag{27}$$

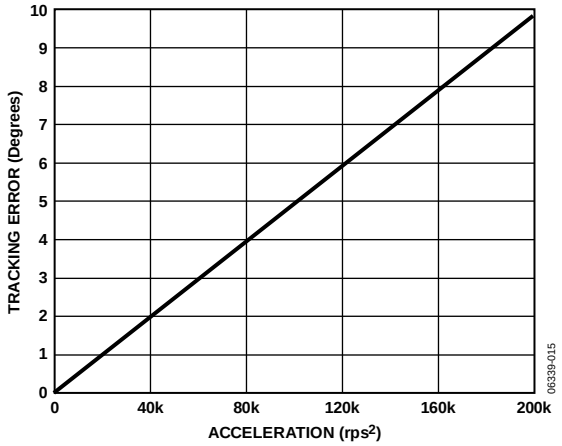

Figure 15. Tracking Error vs. Acceleration

CONNECTING TO THE DSP

The AD2S1205 serial port is ideally suited for interfacing to DSP-configured microprocessors. Figure 16 shows the AD2S1205 interfaced to an ADMC401, one of the DSP-based motor controllers.

The on-chip serial port of the ADMC401 is used in the following configuration

- Alternate framing transmit mode with internal framing (internally inverted)
- Normal framing receive mode with external framing (internally inverted)
- Internal serial clock generation

In this configuration, the internal TFS signal of ADMC401 is used as an external RFS to fully control the timing of data received, and the same TFS is connected to $\overline{RD}$ of the AD2S1205. In addition, the ADMC401 provides an internal continuous serial clock to the AD2S1205. The $\overline{SAMPLE}$ signal on the AD2S1205 can be provided either by using a PIO or by inverting the PWMSYNC signal to synchronize the position and velocity readings with the PWM switching frequency. $\overline{CS}$ and $\overline{RDVEL}$ can be obtained using two PIO outputs of the ADMC401. The 12 bits of significant data and the status bits are available on each consecutive negative edge of the clock after the $\overline{RD}$ signal goes low. Data is clocked from the AD2S1205 into the data receive register of the ADMC401. This is internally set to 16 bits (12 data bits, 4 status bits) because 16 bits are received overall. The serial port automatically generates an internal processor interrupt. This allows the ADMC401 to read all 16 bits and then continue to process data.

All ADMC401 products can interface to the AD2S1205 by using similar interface circuitry.

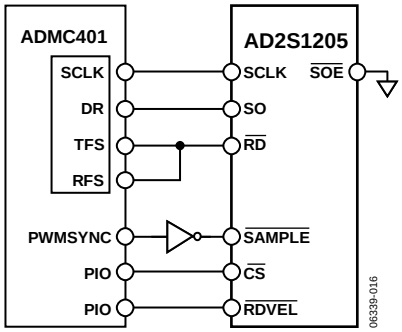

Figure 16. Connecting to the ADMC401