Dual Channel, 128-/256-Position, SPI, Nonvolatile Digital Potentiometer

Data Sheet

AD5122/AD5142

FEATURES

10 kΩ and 100 kΩ resistance options
Resistor tolerance: ±8% maximum
Wiper current: ±6 mA
Low temperature coefficient: 35 ppm/°C
Wide bandwidth: 3 MHz
Fast start-up time <75 µs
Linear gain setting mode
Single- and dual-supply operation
Independent logic supply: 1.8 V to 5.5 V
Wide operating temperature: −40°C to +125°C
3 mm × 3 mm package option
Qualified for automotive applications

APPLICATIONS

Portable electronics level adjustment
LCD panel brightness and contrast controls
Programmable filters, delays, and time constants
Programmable power supplies

GENERAL DESCRIPTION

The AD5122/AD5142 potentiometers provide a nonvolatile solution for 128-/256-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the Ax, Bx, and Wx pins.

The low resistor tolerance and low nominal temperature coefficient simplify open-loop applications as well as applications requiring tolerance matching.

The linear gain setting mode allows independent programming of the resistance between the digital potentiometer terminals through the R_{AW} and R_{WB} string resistors, allowing accurate resistor matching.

The high bandwidth and low total harmonic distortion (THD) ensure optimal performance for ac signals, making these devices suitable for filter design.

The low wiper resistance of only 40 Ω at the ends of the resistor array allows pin to pin connection.

The wiper values can be set through an SPI-compatible digital interface that also reads back the wiper register and EEPROM contents.

FUNCTIONAL BLOCK DIAGRAM

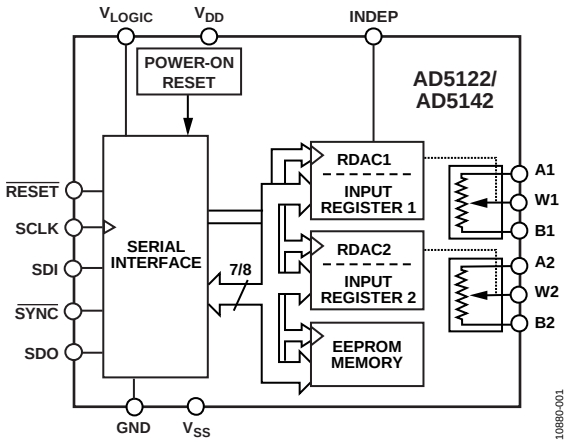

Figure 1.

The AD5122/AD5142 are available in a compact, 16-lead, 3 mm × 3 mm LFCSP and a 16-lead TSSOP. The devices are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Table 1. Family Models

Model	Channel	Position	Interface	Package
AD5123[1]	Quad	128	I²C	LFCSP
AD5124	Quad	128	SPI/I²C	LFCSP
AD5124	Quad	128	SPI	TSSOP
AD5143[1]	Quad	256	I²C	LFCSP
AD5144	Quad	256	SPI/I²C	LFCSP
AD5144	Quad	256	SPI	TSSOP
AD5144A	Quad	256	I²C	TSSOP
AD5122	Dual	128	SPI	LFCSP/TSSOP
AD5122A	Dual	128	I²C	LFCSP/TSSOP
AD5142	Dual	256	SPI	LFCSP/TSSOP
AD5142A	Dual	256	I²C	LFCSP/TSSOP
AD5121	Single	128	SPI/I²C	LFCSP
AD5141	Single	256	SPI/I²C	LFCSP

[1] Two potentiometers and two rheostats.

Rev. C
Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5122

V_{DD} = 2.3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.25 V to 2.75 V, V_{SS} = −2.25 V to −2.75 V; V_{LOGIC} = 1.8 V to 5.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		7			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ				
		V_{DD} ≥ 2.7 V	−1	±0.1	+1	LSB
		V_{DD} < 2.7 V	−2.5	±1	+2.5	LSB
		R_{AB} = 100 kΩ				
		V_{DD} ≥ 2.7 V	−0.5	±0.1	+0.5	LSB
		V_{DD} < 2.7 V	−1	±0.25	+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale				
		R_{AB} = 10 kΩ		55	125	Ω
		R_{AB} = 100 kΩ		130	400	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}					
		R_{AB} = 10 kΩ		40	80	Ω
		R_{AB} = 100 kΩ		60	230	Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = 0xFF	−1	±0.2	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL					
		R_{AB} = 10 kΩ	−0.5	±0.1	+0.5	LSB
		R_{AB} = 100 kΩ	−0.25	±0.1	+0.25	LSB
Differential Nonlinearity[4]	DNL		−0.25	±0.1	+0.25	LSB
Full-Scale Error	V_{WFSE}					
		R_{AB} = 10 kΩ	−1.5	−0.1		LSB
		R_{AB} = 100 kΩ	−0.5	±0.1	+0.5	LSB
Zero-Scale Error	V_{WZSE}					
		R_{AB} = 10 kΩ		1	1.5	LSB
		R_{AB} = 100 kΩ		0.25	0.5	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 100 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		25		pF
		R_{AB} = 100 kΩ		12		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		12		pF
		R_{AB} = 100 kΩ		5		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.6	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Power Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	µA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND	−5.5	−0.7		µA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		0.05	1.4	µA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		3.5		µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD}$ ± 10%, code = full scale		−66	−60	dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB				
		R_{AB} = 10 kΩ		3		MHz
		R_{AB} = 100 kΩ		0.43		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 100 kΩ		−90		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz				
		R_{AB} = 10 kΩ		7		nV/√Hz
		R_{AB} = 100 kΩ		20		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 100 kΩ		12		µs
Crosstalk (C_{W1}/C_{W2})	C_T	R_{AB} = 10 kΩ		10		nV-sec
		R_{AB} = 100 kΩ		25		nV-sec
Analog Crosstalk	C_{TA}			−90		dB
Endurance[10]		T_A = 25°C		1		Mcycles
			100			kcycles
Data Retention[11, 12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity (R-INL) error is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $(0.7 \times V_{DD})/R_{AB}$.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] Different from operating current; supply current for EEPROM program lasts approximately 30 ms.
[7] Different from operating current; supply current for EEPROM read lasts approximately 20 µs.
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{LOGIC} \times V_{LOGIC})$.
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.
[12] 50 years applies to an endurance of 1k cycles. An endurance of 100k cycles has an equivalent retention lifetime of 5 years.

ELECTRICAL CHARACTERISTICS—AD5142

V_{DD} = 2.3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.25 V to 2.75 V, V_{SS} = −2.25 V to −2.75 V; V_{LOGIC} = 1.8 V to 5.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		8			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ				
		V_{DD} ≥ 2.7 V	−2	±0.2	+2	LSB
		V_{DD} < 2.7 V	−5	±1.5	+5	LSB
		R_{AB} = 100 kΩ				
		V_{DD} ≥ 2.7 V	−1	±0.1	+1	LSB
		V_{DD} < 2.7 V	−2	±0.5	+2	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.2	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale				
		R_{AB} = 10 kΩ		55	125	Ω
		R_{AB} = 100 kΩ		130	400	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}					
		R_{AB} = 10 kΩ		40	80	Ω
		R_{AB} = 100 kΩ		60	230	Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = 0xFF	−1	±0.2	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL					
		R_{AB} = 10 kΩ	−1	±0.2	+1	LSB
		R_{AB} = 100 kΩ	−0.5	±0.1	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.2	+0.5	LSB
Full-Scale Error	V_{WFSE}					
		R_{AB} = 10 kΩ	−2.5	−0.1		LSB
		R_{AB} = 100 kΩ	−1	±0.2	+1	LSB
Zero-Scale Error	V_{WZSE}					
		R_{AB} = 10 kΩ		1.2	3	LSB
		R_{AB} = 100 kΩ		0.5	1	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 100 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		25		pF
		R_{AB} = 100 kΩ		12		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale				
		R_{AB} = 10 kΩ		12		pF
		R_{AB} = 100 kΩ		5		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.6	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Power Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	µA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND	−5.5	−0.7		µA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		0.05	1.4	µA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		3.5		µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD} \pm 10\%$, code = full scale		−66	−60	dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB				
		R_{AB} = 10 kΩ		3		MHz
		R_{AB} = 100 kΩ		0.43		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 100 kΩ		−90		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz				
		R_{AB} = 10 kΩ		7		nV/√Hz
		R_{AB} = 100 kΩ		20		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 100 kΩ		12		µs
Crosstalk (C_{W1}/C_{W2})	C_T	R_{AB} = 10 kΩ		10		nV-sec
		R_{AB} = 100 kΩ		25		nV-sec
Analog Crosstalk	C_{TA}			−90		dB
Endurance[10]		T_A = 25°C		1		Mcycles
			100			kcycles
Data Retention[11, 12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity (R-INL) error is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $(0.7 \times V_{DD})/R_{AB}$.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] Different from operating current; supply current for EEPROM program lasts approximately 30 ms.
[7] Different from operating current; supply current for EEPROM read lasts approximately 20 µs.
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{LOGIC} \times V_{LOGIC})$.
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.
[12] 50 years applies to an endurance of 1k cycles. An endurance of 100k cycles has an equivalent retention lifetime of 5 years.

INTERFACE TIMING SPECIFICATIONS

V_{LOGIC} = 1.8 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. SPI Interface[1]

Parameter[2]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_1	V_{LOGIC} > 1.8 V	20			ns	SCLK cycle time
	V_{LOGIC} = 1.8 V	30			ns	
t_2	V_{LOGIC} > 1.8 V	10			ns	SCLK high time
	V_{LOGIC} = 1.8 V	15			ns	
t_3	V_{LOGIC} > 1.8 V	10			ns	SCLK low time
	V_{LOGIC} = 1.8 V	15			ns	
t_4		10			ns	$\overline{SYNC}$ to SCLK falling edge setup time
t_5		5			ns	Data setup time
t_6		5			ns	Data hold time
t_7		10			ns	$\overline{SYNC}$ rising edge to next SCLK fall ignored
t_8[3]		20			ns	Minimum $\overline{SYNC}$ high time
t_9[4]			50		ns	SCLK rising edge to SDO valid
t_{10}				500	ns	$\overline{SYNC}$ rising edge to SDO pin disable

[1] Refer to the AN-1248 for additional information about the serial peripheral interface.
[2] All input signals are specified with $t_r = t_f$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] Refer to $t_{EEPROM\_PROGRAM}$ and $t_{EEPROM\_READBACK}$ for memory commands operations (see Table 5).
[4] R_{PULL_UP} = 2.2 kΩ to V_{DD} with a capacitance load of 168 pF.

Table 5. Control Pins

Parameter	Min	Typ	Max	Unit	Description
t_1	0.1		10	µs	$\overline{RESET}$ low time
$t_{EEPROM\_PROGRAM}$[1]		15	50	ms	Memory program time (not shown in Figure 5)
$t_{EEPROM\_READBACK}$		7	30	µs	Memory readback time (not shown in Figure 5)
t_{POWER_UP}[2]			75	µs	Start-up time (not shown in Figure 5)
t_{RESET}		30		µs	Reset EEPROM restore time (not shown in Figure 5)

[1] EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at lower temperatures and higher write cycles.
[2] Maximum time after $V_{DD} - V_{SS}$ is equal to 2.3 V.

SHIFT REGISTER AND TIMING DIAGRAMS

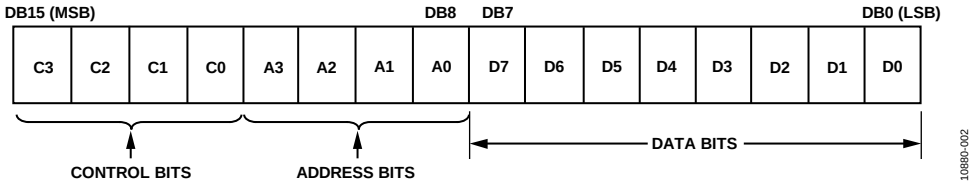


Figure 2. Input Shift Register Contents

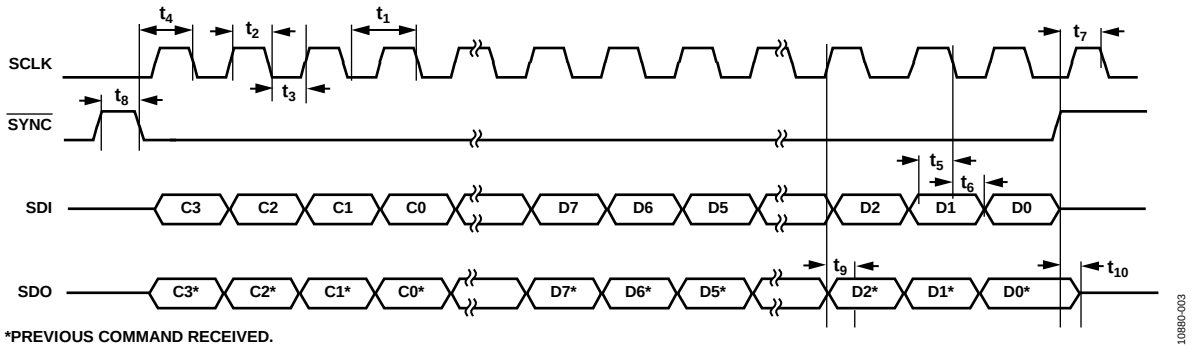


Figure 3. SPI Serial Interface Timing Diagram, Clock Polarity (CPOL) = 0, Clock Phase (CPHA) = 1

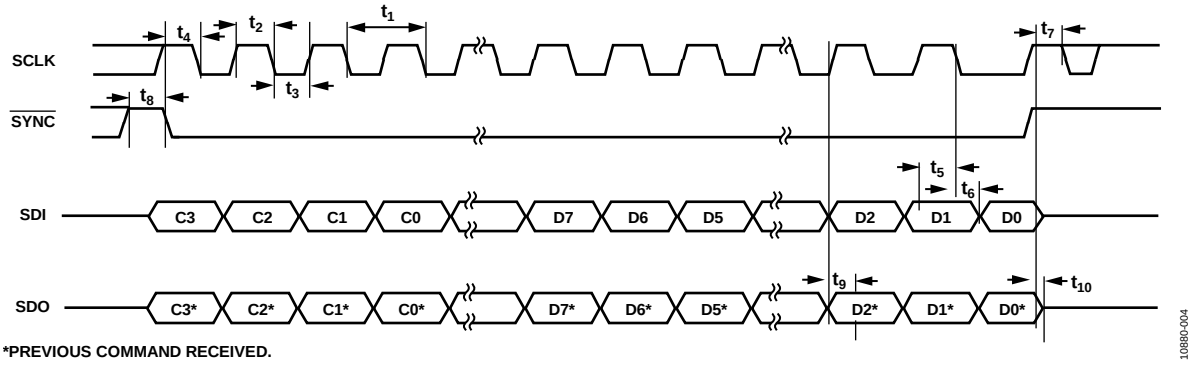


Figure 4. SPI Serial Interface Timing Diagram, Clock Polarity (CPOL) = 1, Clock Phase (CPHA) = 0

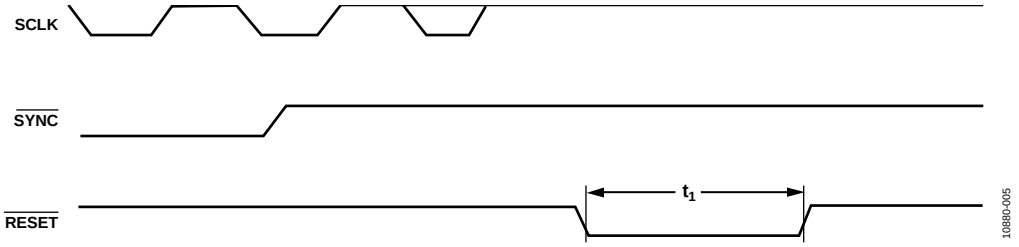


Figure 5. Control Pins Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_{LOGIC} to GND	−0.3 V to V_{DD} + 0.3 V or +7.0 V (whichever is less)
V_A, V_W, V_B to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V or +7.0 V (whichever is less)
I_A, I_W, I_B	
Pulsed[1]	
Frequency > 10 kHz	
R_{AW} = 10 kΩ	±6 mA/d^2
R_{AW} = 100 kΩ	±1.5 mA/d^2
Frequency ≤ 10 kHz	
R_{AW} = 10 kΩ	±6 mA/√d^2
R_{AW} = 100 kΩ	±1.5 mA/√d^2
Digital Inputs	−0.3 V to V_{LOGIC} + 0.3 V or +7 V (whichever is less)
Operating Temperature Range, T_A[3]	−40°C to +125°C
Maximum Junction Temperature, T_J Maximum	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
FICDM	1.5 kV

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] d = pulse duty factor.
[3] Includes programming of EEPROM memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP	89.5[1]	3	°C/W
16-Lead TSSOP	150.4[1]	27.6	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

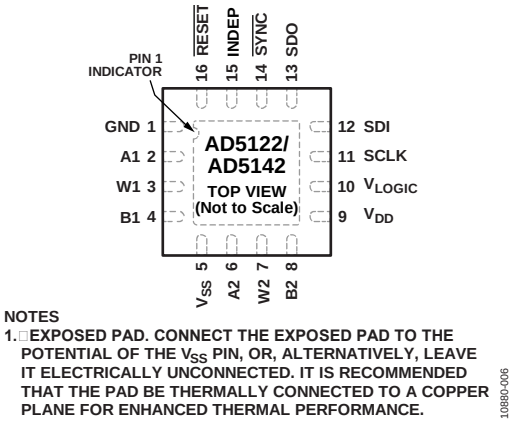


Figure 6. 16-Lead LFCSP Pin Configuration

Table 8. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin, Logic Ground Reference.
2	A1	Terminal A of RDAC1. $V_{SS} \le V_A \le V_{DD}$.
3	W1	Wiper Terminal of RDAC1. $V_{SS} \le V_W \le V_{DD}$.
4	B1	Terminal B of RDAC1. $V_{SS} \le V_B \le V_{DD}$.
5	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
6	A2	Terminal A of RDAC2. $V_{SS} \le V_A \le V_{DD}$.
7	W2	Wiper Terminal of RDAC2. $V_{SS} \le V_W \le V_{DD}$.
8	B2	Terminal B of RDAC2. $V_{SS} \le V_B \le V_{DD}$.
9	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
10	V_{LOGIC}	Logic Power Supply; 1.8 V to V_{DD}. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
11	SCLK	Serial Clock Line. Data is clocked in at the logic low transition.
12	SDI	Serial Data Input.
13	SDO	Serial Data Output. This is an open-drain output pin, and it needs an external pull-up resistor.
14	$\overline{\text{SYNC}}$	Synchronization Input, Active Low. When $\overline{\text{SYNC}}$ returns high, data is loaded into the input shift register.
15	INDEP	Linear Gain Setting Mode at Power-Up. Each string resistor is loaded independently from the associated memory location. If INDEP is enabled, it cannot be disabled by software.
16	$\overline{\text{RESET}}$	Hardware Reset Pin. Refresh the RDAC registers from EEPROM. $\overline{\text{RESET}}$ is activated at the logic low. If this pin is not used, tie $\overline{\text{RESET}}$ to V_{LOGIC}.
	EPAD	Exposed Pad. Connect this exposed pad to the potential of the V_{SS} pin, or, alternatively, leave it electrically unconnected. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

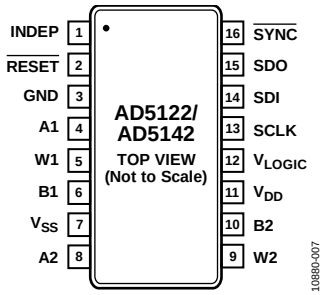


Figure 7. 16-Lead TSSOP, SPI Interface Pin Configuration

Table 9. 16-Lead TSSOP, SPI Interface Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INDEP	Linear Gain Setting Mode at Power-Up. Each string resistor is loaded independently from the associated memory location. If INDEP is enabled, it cannot be disabled by software.
2	$\overline{\text{RESET}}$	Hardware Reset Pin. Refresh the RDAC registers from EEPROM. $\overline{\text{RESET}}$ is activated at the logic low. If this pin is not used, tie $\overline{\text{RESET}}$ to V_{LOGIC}.
3	GND	Ground Pin, Logic Ground Reference.
4	A1	Terminal A of RDAC1. $V_{SS} \le V_A \le V_{DD}$.
5	W1	Wiper Terminal of RDAC1. $V_{SS} \le V_W \le V_{DD}$.
6	B1	Terminal B of RDAC1. $V_{SS} \le V_B \le V_{DD}$.
7	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
8	A2	Terminal A of RDAC2. $V_{SS} \le V_A \le V_{DD}$.
9	W2	Wiper Terminal of RDAC2. $V_{SS} \le V_W \le V_{DD}$.
10	B2	Terminal B of RDAC2. $V_{SS} \le V_B \le V_{DD}$.
11	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
12	V_{LOGIC}	Logic Power Supply; 1.8 V to V_{DD}. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
13	SCLK	Serial Clock Line. Data is clocked in at the logic low transition.
14	SDI	Serial Data Input.
15	SDO	Serial Data Output. This is an open-drain output pin, and it needs an external pull-up resistor.
16	$\overline{\text{SYNC}}$	Synchronization Input, Active Low. When $\overline{\text{SYNC}}$ returns high, data is loaded into the input shift register.

TYPICAL PERFORMANCE CHARACTERISTICS

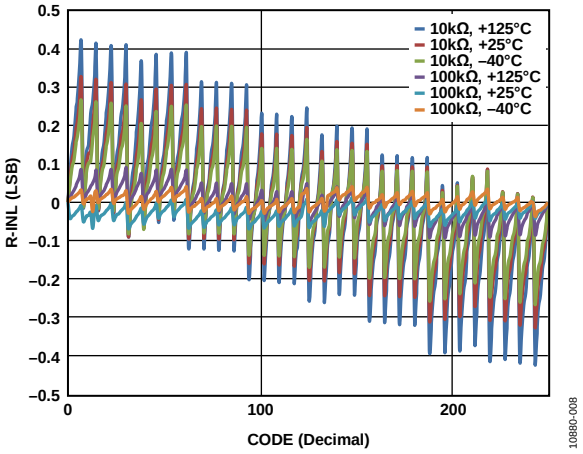


Figure 8. R-INL vs. Code (AD5142)

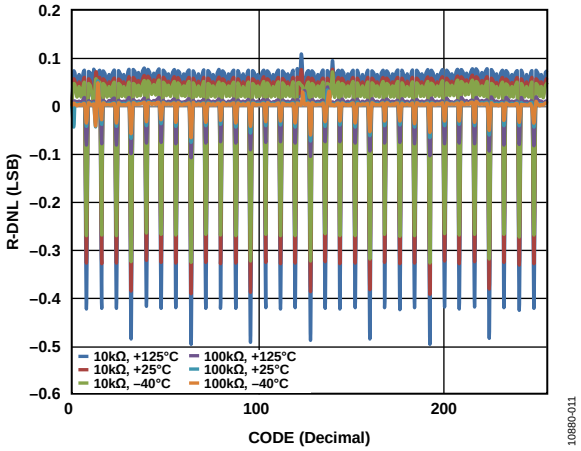


Figure 11. R-DNL vs. Code (AD5142)

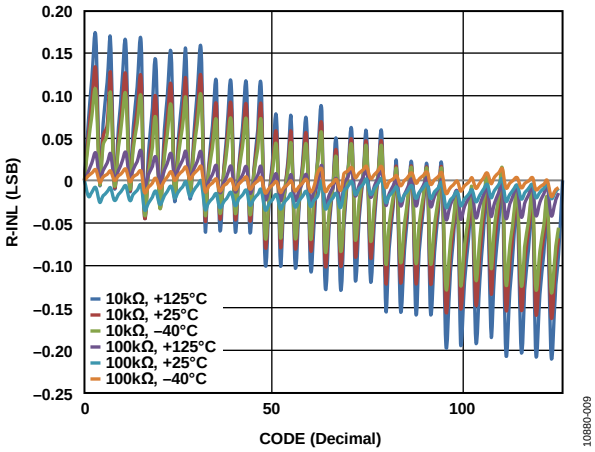


Figure 9. R-INL vs. Code (AD5122)

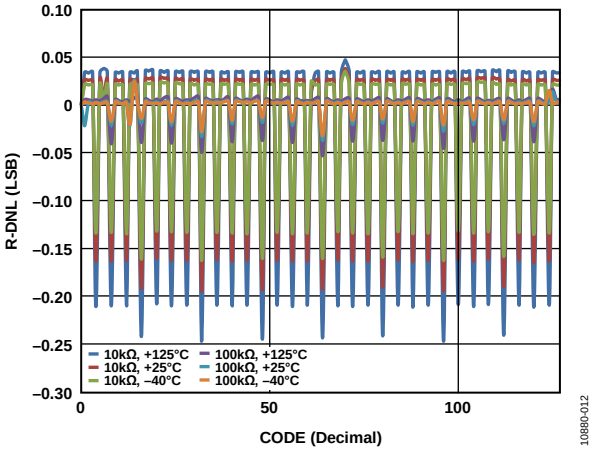


Figure 12. R-DNL vs. Code (AD5122)

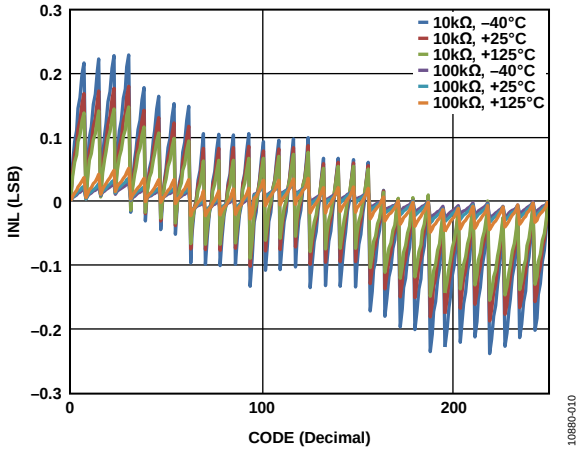


Figure 10. INL vs. Code (AD5142)

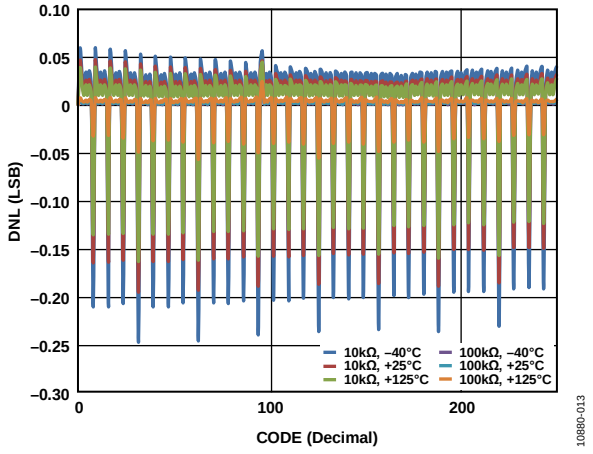


Figure 13. DNL vs. Code (AD5142)

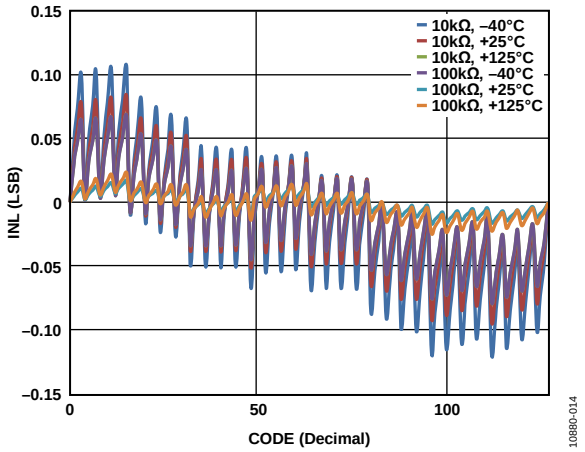


Figure 14. INL vs. Code (AD5122)

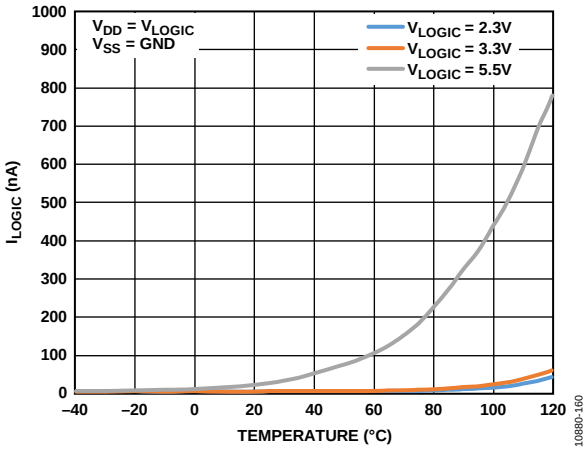


Figure 17. I_{LOGIC} vs. Temperature

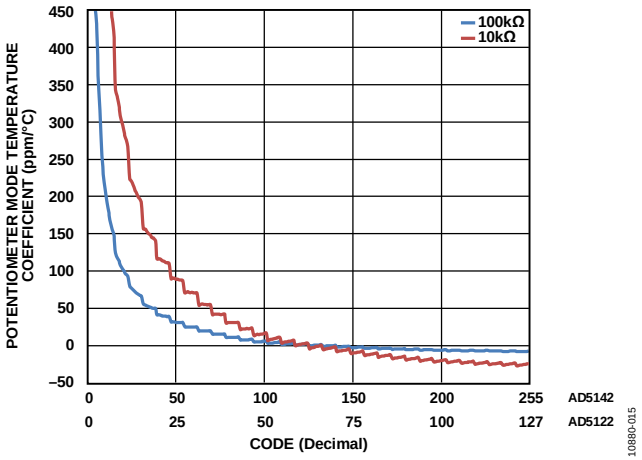


Figure 15. Potentiometer Mode Temperature Coefficient ($(\Delta V_W/V_W)/\Delta T \times 10^6$) vs. Code

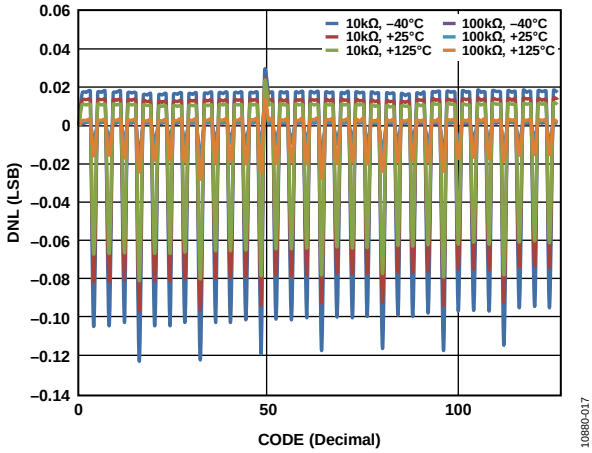


Figure 18. DNL vs. Code (AD5122)

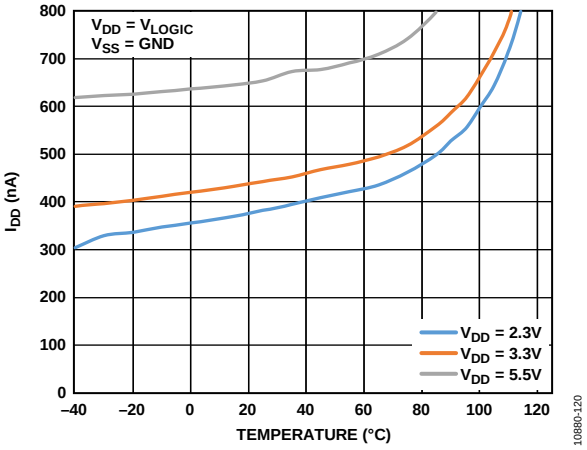


Figure 16. I_{DD} vs. Temperature

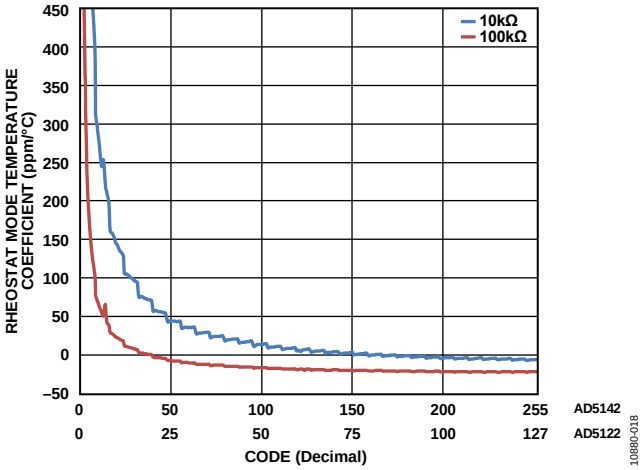


Figure 19. Rheostat Mode Temperature Coefficient ($(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$) vs. Code

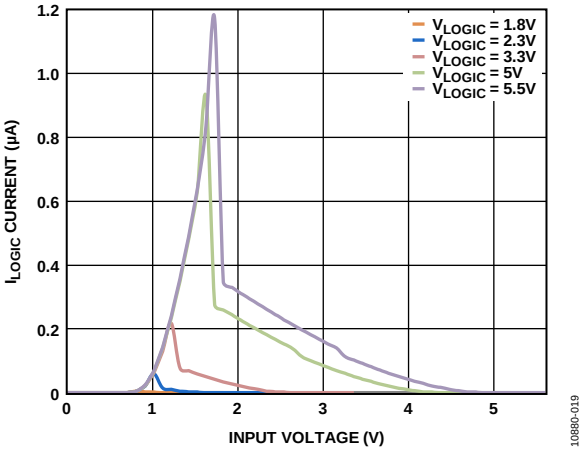


Figure 20. I_{LOGIC} Current vs. Digital Input Voltage

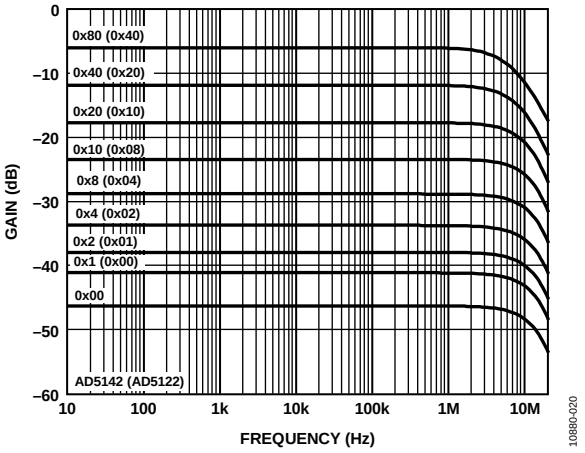


Figure 21. 10 kΩ Gain vs. Frequency vs. Code

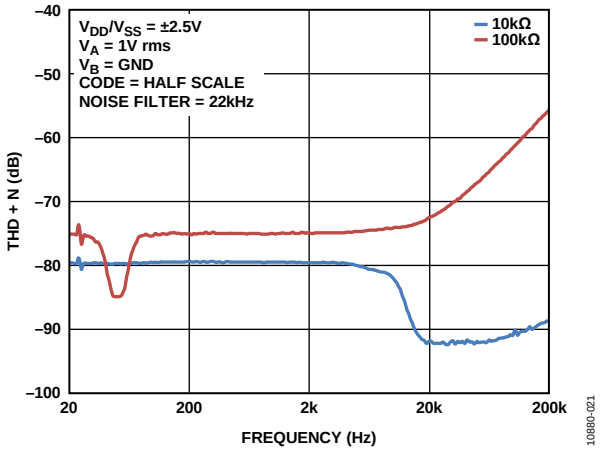


Figure 22. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency

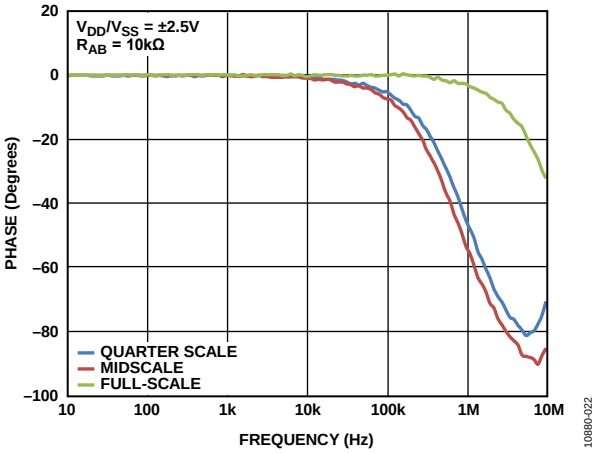


Figure 23. Normalized Phase Flatness vs. Frequency, R_{AB} = 10 kΩ

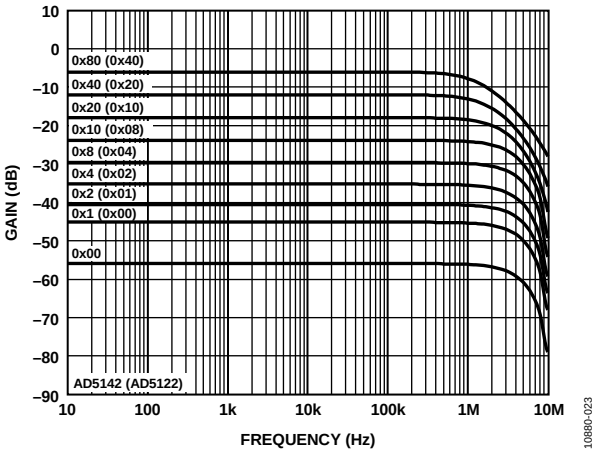


Figure 24. 100 kΩ Gain vs. Frequency vs. Code

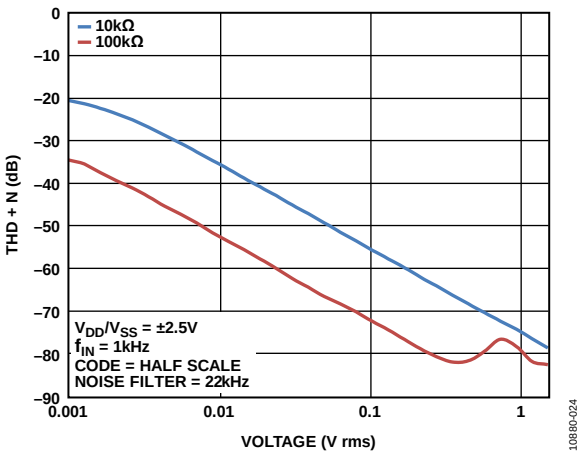


Figure 25. Total Harmonic Distortion Plus Noise (THD + N) vs. Amplitude

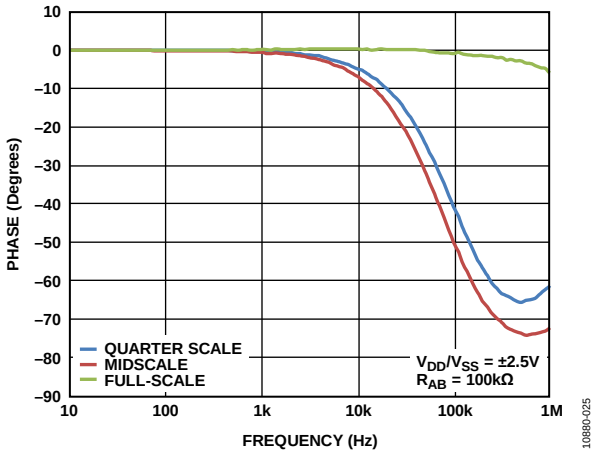


Figure 26. Normalized Phase Flatness vs. Frequency, R_{AB} = 100 kΩ

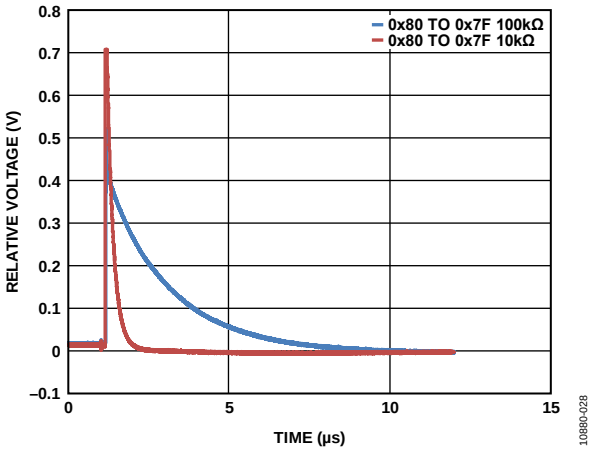


Figure 29. Maximum Transition Glitch

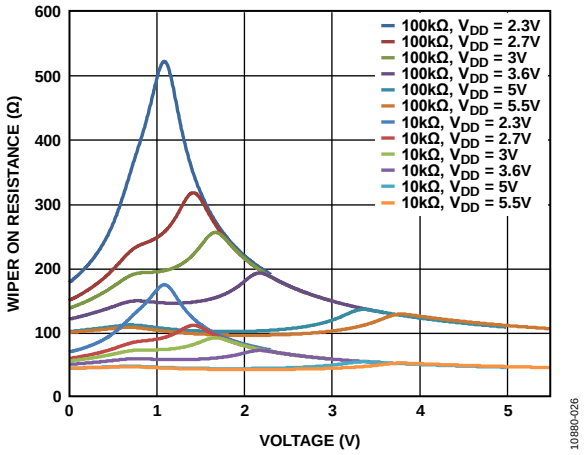


Figure 27. Incremental Wiper On Resistance vs. Positive Power Supply (V_{DD})

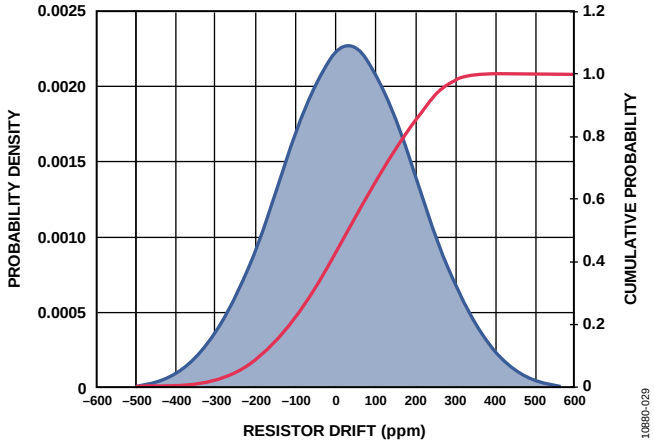


Figure 30. Resistor Lifetime Drift

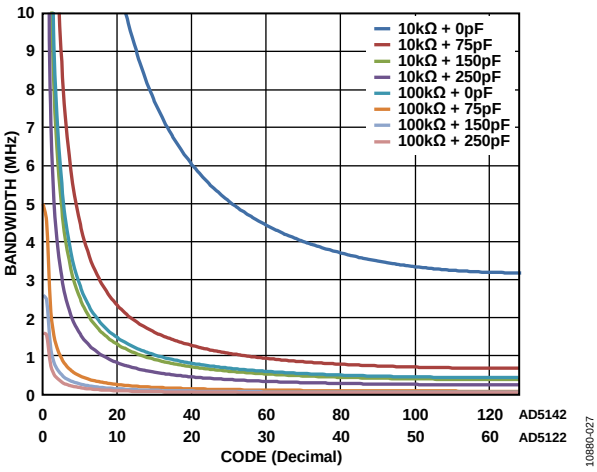


Figure 28. Maximum Bandwidth vs. Code vs. Net Capacitance

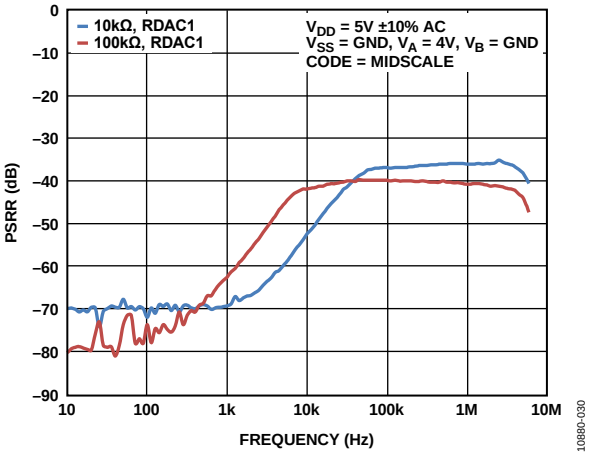


Figure 31. Power Supply Rejection Ratio (PSRR) vs. Frequency

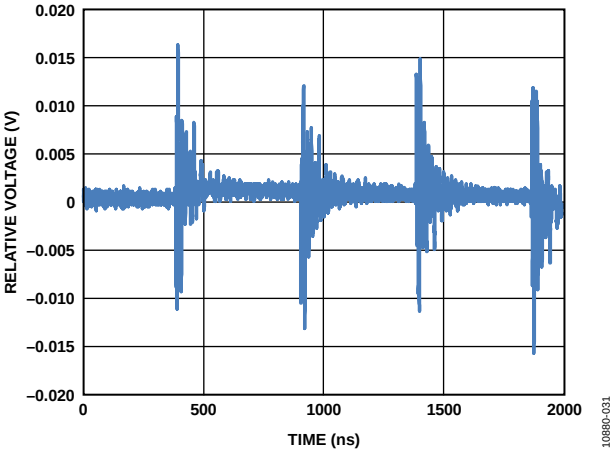


Figure 32. Digital Feedthrough

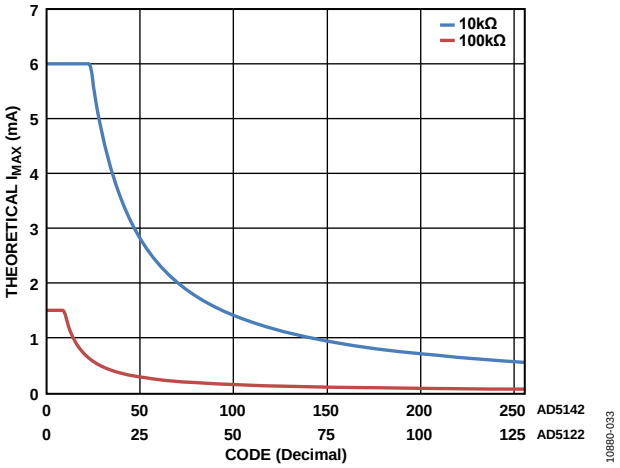


Figure 34. Theoretical Maximum Current vs. Code

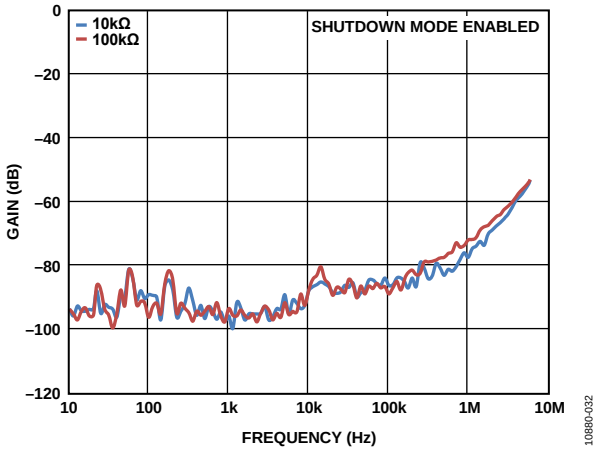


Figure 33. Shutdown Isolation vs. Frequency

TEST CIRCUITS

Figure 35 to Figure 39 define the test conditions used in the Specifications section.

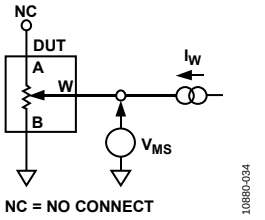


Figure 35. Resistor Integral Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

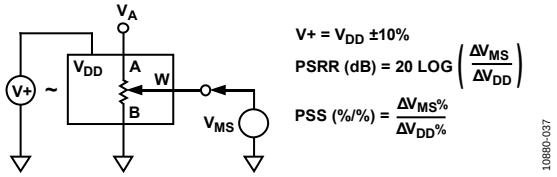


Figure 38. Power Supply Sensitivity and Power Supply Rejection Ratio (PSS, PSRR)

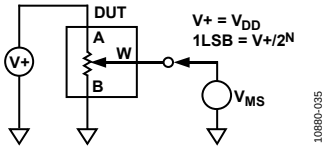


Figure 36. Potentiometer Divider Nonlinearity Error (INL, DNL)

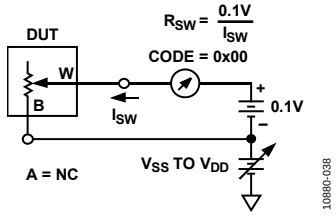


Figure 39. Incremental On Resistance

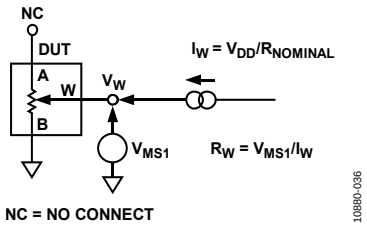


Figure 37. Wiper Resistance

THEORY OF OPERATION

The AD5122/AD5142 digital programmable potentiometers are designed to operate as true variable resistors for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register that allows unlimited changes of resistance settings. A secondary register (the input register) can preload the RDAC register data.

The RDAC register can be programmed with any position setting using the SPI interface (depending on the model). When a desirable wiper position is found, this value can be stored in the EEPROM memory. Thereafter, the wiper position is always restored to that position for subsequent power-ups. The storing of EEPROM data takes approximately 15 ms; during this time, the device is locked and does not acknowledge any new command, preventing any changes from taking place.

RDAC REGISTER AND EEPROM

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with 0x80 (AD5142, 256 taps), the wiper is connected to half scale of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

It is possible to both write to and read from the RDAC register using the digital interface (see Table 10).

The contents of the RDAC register can be stored to the EEPROM using Command 9 (see Table 16). Thereafter, the RDAC register always sets at that position for any future on-off-on power supply sequence. It is possible to read back data saved into the EEPROM with Command 3 (see Table 10).

Alternatively, the EEPROM can be written to independently using Command 11 (see Table 16).

INPUT SHIFT REGISTER

For the AD5122/AD5142, the input shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of four control bits, followed by four address bits and by eight data bits.

If the AD5122 RDAC or EEPROM registers are read from or written to, the lowest data bit (Bit 0) is ignored.

Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command as listed in Table 10 and Table 16.

SPI SERIAL DATA INTERFACE

The AD5122/AD5142 contain a 4-wire, SPI-compatible digital interface (SDI, $\overline{\text{SYNC}}$, SDO, and SCLK). The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word is loaded from the SDI pin. Data is loaded in at the SCLK falling edge transition, as shown in Figure 3 and Figure 4. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the instructions in Table 16.

To minimize power consumption in the digital input buffers when the device is enabled, operate all serial interface pins close to the V_{LOGIC} supply rails.

$\overline{\text{SYNC}}$ Interruption

In a standalone write sequence for the AD5122/AD5142, the $\overline{\text{SYNC}}$ line is kept low for 16 falling edges of SCLK, and the instruction is decoded when $\overline{\text{SYNC}}$ is pulled high. However, if the $\overline{\text{SYNC}}$ line is kept low for less than 16 falling edges of SCLK, the input shift register content is ignored, and the write sequence is considered invalid.

SDO Pin

The serial data output pin (SDO) serves two purposes: to read back the contents of the control, EEPROM, RDAC, and input registers using Command 3 (see Table 10 and Table 16), and to connect the AD5122/AD5142 to daisy-chain mode.

The SDO pin contains an internal open-drain output that needs an external pull-up resistor. The SDO pin is enabled when $\overline{\text{SYNC}}$ is pulled low, and the data is clocked out of SDO on the rising edge of SCLK, as shown in Figure 3 and Figure 4.

Daisy-Chain Connection

Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 40, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period can be increased because of the propagation delay of the line between subsequent devices. When two AD5122/AD5142 devices are daisy chained, 32 bits of data are required. The first 16 bits assigned to U2, and the second 16 bits assigned to U1, as shown in Figure 41. Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation. A typical connection is shown in Figure 40.

To prevent data from mislocking (for example, due to noise) the device includes an internal counter, if the clock falling edges count is not a multiple of 8, the device ignores the command. A valid clock count is 16, 24, or 32. The counter resets when $\overline{\text{SYNC}}$ returns high.

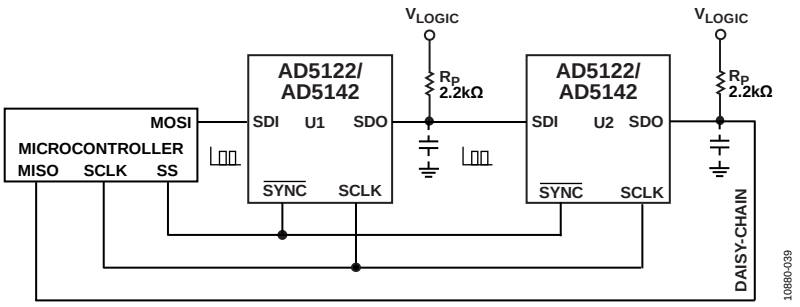


Figure 40. Daisy-Chain Configuration

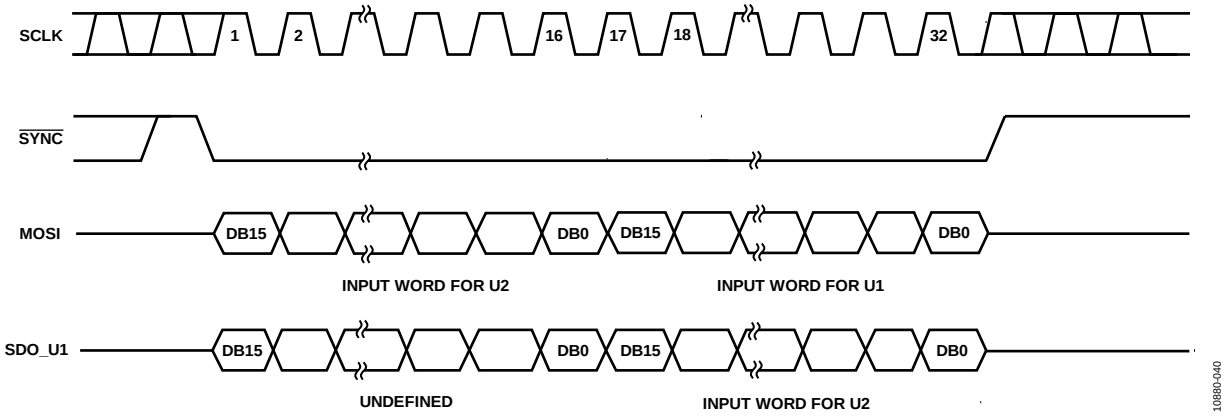


Figure 41. Daisy-Chain Diagram

Table 10. Reduced Commands Operation Truth Table

Command Number	Control Bits[DB15:DB12]				Address Bits[DB11:DB8][1]				Data Bits[DB7:DB0][1]								Operation
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: do nothing.
1	0	0	0	1	0	0	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC
2	0	0	1	0	0	0	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to input register
3	0	0	1	1	X	0	A1	A0	X	X	X	X	X	X	D1	D0	Read back contents
																	D1 / **D0** / **Data**: 0 / 1 / EEPROM; 1 / 1 / RDAC
9	0	1	1	1	0	0	0	A0	X	X	X	X	X	X	X	1	Copy RDAC register to EEPROM
10	0	1	1	1	0	0	0	A0	X	X	X	X	X	X	X	0	Copy EEPROM into RDAC
14	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Software reset
15	1	1	0	0	A3	0	0	A0	X	X	X	X	X	X	X	D0	Software shutdown
																	D0 / **Condition**: 0 / Normal mode; 1 / Shutdown mode

[1]X means don't care.

Table 11. Reduced Address Bits Table

A3	A2	A1	A0	Channel	Stored Channel Memory
1	X[1]	X[1]	X[1]	All channels	Not applicable
0	0	0	0	RDAC1	RDAC1
0	0	0	1	RDAC2	Not applicable
0	0	1	0	Not applicable	RDAC2

[1]X means don't care.

ADVANCED CONTROL MODES

The AD5122/AD5142 digital potentiometers include a set of user programming features to address the wide number of applications for these universal adjustment devices (see Table 16 and Table 18).

Key programming features include the following:

- Input register
- Linear gain setting mode
- Low wiper resistance feature
- Lineal increment and decrement instructions
- ±6 dB increment and decrement instructions
- Reset
- Shutdown mode

Input Register

The AD5122/AD5142 include one input register per RDAC register. These registers allow preloading of the value for the associated RDAC register. These registers can be written to using Command 2 and read back from using Command 3 (see Table 16).

This feature allows a synchronous update of one or all the RDAC registers at the same time.

The transfer from the input register to the RDAC register is done synchronously by Command 8 (see Table 16).

If new data is loaded into an RDAC register, this RDAC register automatically overwrites the associated input register.

Linear Gain Setting Mode

The proprietary architecture of the AD5122/AD5142 allows the independent control of each string resistor, R_{AW} and R_{WB}. To enable this feature, use Command 16 (see Table 16) to set Bit D2 of the control register (see Table 18).

This mode of operation can control the potentiometer as two independent rheostats connected at a single point, W terminal, as opposed to potentiometer mode where each resistor is complementary, $R_{AW} = R_{AB} - R_{WB}$.

This feature enables a second input and an RDAC register per channel, as shown in Table 17; however, the actual RDAC contents remain unchanged. The same operations are valid for potentiometer mode and linear gain setting mode.

If the INDEP pin is pulled high, the device powers up in linear gain setting mode and loads the values stored in the associated memory locations for each channel (see Table 17). The INDEP pin and D2 bit are connected internally to a logic or gate, if any or both are 1, the devices cannot operate in potentiometer mode.

Low Wiper Resistance Feature

The AD5122/AD5142 include two commands to reduce the wiper resistance between the terminals when the devices achieve full scale or zero scale. These extra positions are called bottom scale, BS, and top scale, TS. The resistance between Terminal A and Terminal W at top scale is specified as R_{TS}. Similarly, the bottom scale resistance between Terminal B and Terminal W is specified as R_{BS}.

The contents of the RDAC registers are unchanged by entering in these positions. There are three ways to exit from top scale and bottom scale: by using Command 12 or Command 13 (see Table 16); by loading new data in an RDAC register, which includes increment/decrement operations; or by entering shutdown mode, Command 15 (see Table 16).

Table 12 and Table 13 show the truth tables for the top scale position and the bottom scale position, respectively, when the potentiometer or linear gain setting mode is enabled.

Table 12. Top Scale Truth Table

Linear Gain Setting Mode		Potentiometer Mode	
R_{AW}	R_{WB}	R_{AW}	R_{WB}
R_{AB}	R_{AB}	R_{TS}	R_{AB}

Table 13. Bottom Scale Truth Table

Linear Gain Setting Mode		Potentiometer Mode	
R_{AW}	R_{WB}	R_{AW}	R_{WB}
R_{TS}	R_{BS}	R_{AB}	R_{BS}

Linear Increment and Decrement Instructions

The increment and decrement commands (Command 4 and Command 5 in Table 16) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send an increment or decrement command to the device. The adjustment can be individual or in a ganged potentiometer arrangement, where all wiper positions are changed at the same time.

For an increment command, executing Command 4 automatically moves the wiper to the next RDAC position. This command can be executed in a single channel or multiple channels.

±6 dB Increment and Decrement Instructions

Two programming instructions produce logarithmic taper increment or decrement of the wiper position control by an individual potentiometer or by a ganged potentiometer arrangement where all RDAC register positions are changed simultaneously. The +6 dB increment is activated by Command 6, and the −6 dB decrement is activated by Command 7 (see Table 16). For example, starting with the zero-scale position and executing Command 6 ten times moves the wiper in 6 dB steps to the full-scale position. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale position (see Table 14).

Incrementing the wiper position by +6 dB essentially doubles the RDAC register value, whereas decrementing the wiper position by −6 dB halves the register value. Internally, the AD5122/AD5142 use shift registers to shift the bits left and right to achieve a ±6 dB increment or decrement. These functions are useful for various audio/video level adjustments, especially for white LED brightness settings in which human visual responses are more sensitive to large adjustments than to small adjustments.

Table 14. Detailed Left Shift and Right Shift Functions for the ±6 dB Step Increment and Decrement

Left Shift (+6 dB/Step)	Right Shift (−6 dB/Step)
0000 0000	1111 1111
0000 0001	0111 1111
0000 0010	0011 1111
0000 0100	0001 1111
0000 1000	0000 1111
0001 0000	0000 0111
0010 0000	0000 0011
0100 0000	0000 0001
1000 0000	0000 0000
1111 1111	0000 0000

Reset

The AD5122/AD5142 can be reset through software by executing Command 14 (see Table 16) or through hardware on the low pulse of the $\overline{\text{RESET}}$ pin. The reset command loads the RDAC registers with the contents of the EEPROM and takes approximately 30 µs. The EEPROM is preloaded to midscale at the factory, and initial power-up is, accordingly, at midscale. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if the $\overline{\text{RESET}}$ pin is not used.

Shutdown Mode

The AD5122/AD5142 can be placed in shutdown mode by executing the software shutdown command, Command 15 (see Table 16); and by setting the LSB (D0) to 1. This feature places the RDAC in a special state. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 16 are supported while in shutdown mode. Execute Command 15 (see Table 16) and set the LSB (D0) to 0 to exit shutdown mode.

Table 15. Truth Table for Shutdown Mode

	Linear Gain Setting Mode		Potentiometer Mode	
A2	AW	WB	AW	WB
0	N/A[1]	Open	Open	R_{BS}
1	Open	N/A[1]	N/A[1]	N/A[1]

[1] N/A means not applicable.

EEPROM OR RDAC REGISTER PROTECTION

The EEPROM and RDAC registers can be protected by disabling any update to these registers. This can be done by using software. If these registers are protected by software, set Bit D0 and/or Bit D1 (see Table 18), which protects the EEPROM and RDAC registers independently.

When RDAC is protected, the only operation allowed is to copy the EEPROM into the RDAC register.

INDEP PIN

If the INDEP pin is pulled high at power-up, the device operates in linear gain setting mode, loading each string resistor, R_{AWx} and R_{WBx}, with the value stored into the EEPROM (see Table 17). If the pin is pulled low, the device powers up in potentiometer mode.

The INDEP pin and the D2 bit are connected internally to a logic OR gate, if any or both are 1, the device cannot operate in potentiometer mode (see Table 18).

Table 16. Advance Command Operation Truth Table

Command Number	Control Bits[DB15:DB12]				Address Bits[DB11:DB8][1]				Data Bits[DB7:DB0][1]								Operation
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: do nothing
1	0	0	0	1	0	A2	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC
2	0	0	1	0	0	A2	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to input register
3	0	0	1	1	0	A2	A1	A0	X	X	X	X	X	X	D1	D0	Read back contents D1 D0 Data 0 0 Input register 0 1 EEPROM 1 0 Control register 1 1 RDAC
4	0	1	0	0	A3	A2	0	A0	X	X	X	X	X	X	X	1	Linear RDAC increment
5	0	1	0	0	A3	A2	0	A0	X	X	X	X	X	X	X	0	Linear RDAC decrement
6	0	1	0	1	A3	A2	0	A0	X	X	X	X	X	X	X	1	+6 dB RDAC increment
7	0	1	0	1	A3	A2	0	A0	X	X	X	X	X	X	X	0	−6 dB RDAC decrement
8	0	1	1	0	A3	A2	0	A0	X	X	X	X	X	X	X	X	Copy input register to RDAC (software LRDAC)
9	0	1	1	1	0	A2	0	A0	X	X	X	X	X	X	X	1	Copy RDAC register to EEPROM
10	0	1	1	1	0	A2	0	A0	X	X	X	X	X	X	X	0	Copy EEPROM into RDAC
11	1	0	0	0	0	0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to EEPROM
12	1	0	0	1	A3	A2	0	A0	1	0	0	0	0	0	0	D0	Top scale D0 = 0; normal mode D0 = 1; shutdown mode
13	1	0	0	1	A3	A2	0	A0	0	0	0	0	0	0	0	D0	Bottom scale D0 = 1; enter D0 = 0; exit
14	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Software reset
15	1	1	0	0	A3	A2	0	A0	0	0	0	0	0	0	0	D0	Software shutdown D0 = 0; normal mode D0 = 1; device placed in shutdown mode
16	1	1	0	1	X	X	X	X	X	X	X	X	X	D2	D1	D0	Copy serial register data to control register

[1] X means don't care.

Table 17. Address Bits

A3	A2	A1	A0	Potentiometer Mode		Linear Gain Setting Mode		Stored Channel Memory
				Input Register	RDAC Register	Input Register	RDAC Register	
1	X[1]	X[1]	X[1]	All channels	All channels	All channels	All channels	Not applicable
0	0	0	0	RDAC1	RDAC1	R_{WB1}	R_{WB1}	RDAC1/R_{WB1}
0	1	0	0	Not applicable	Not applicable	R_{AW1}	R_{AW1}	Not applicable
0	0	0	1	RDAC2	RDAC2	R_{WB2}	R_{WB2}	R_{AW1}
0	1	0	1	Not applicable	Not applicable	R_{AW2}	R_{AW2}	Not applicable
0	0	1	0	Not applicable	Not applicable	Not applicable	Not applicable	RDAC2/R_{WB2}
0	0	1	1	Not applicable	Not applicable	Not applicable	Not applicable	R_{AW2}

[1] X means don't care.

Table 18. Control Register Bit Descriptions

Bit Name	Description
D0	RDAC register write protect 0 = wiper position frozen to value in EEPROM memory 1 = allows update of wiper position through digital interface (default)
D1	EEPROM program enable 0 = EEPROM program disabled 1 = enables device for EEPROM program (default)
D2	Lineal setting mode/potentiometer mode 0 = potentiometer mode (default) 1 = linear gain setting mode

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., uses a proprietary RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5122/AD5142 employ a three stage segmentation approach, as shown in Figure 42. The AD5122/AD5142 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from V_{DD} and V_{SS}.

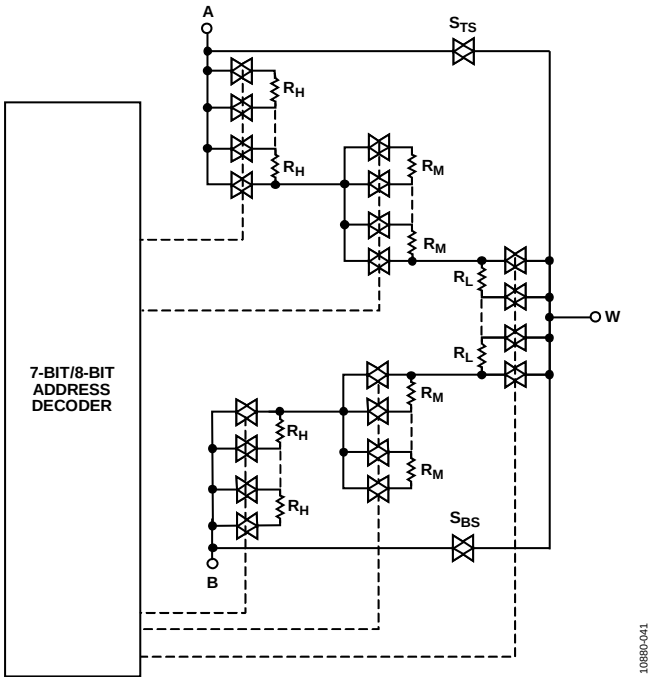


Figure 42. AD5122/AD5142 Simplified RDAC Circuit

Top Scale/Bottom Scale Architecture

In addition, the AD5122/AD5142 include new positions to reduce the resistance between terminals. These positions are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 130 Ω to 60 Ω (R_{AB} = 100 kΩ). At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB, and the total resistance is reduced to 60 Ω (R_{AB} = 100 kΩ).

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—±8% Resistor Tolerance

The AD5122/AD5142 operate in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W, as shown in Figure 43.

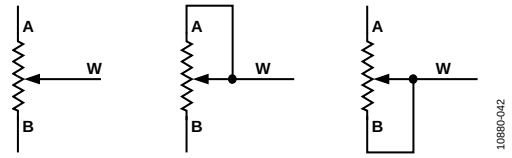


Figure 43. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is 10 kΩ or 100 kΩ, and has 128/256 tap points accessed by the wiper terminal. The 7-bit/8-bit data in the RDAC latch is decoded to select one of the 128/256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

AD5122:

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \qquad \text{From 0x00 to 0x7F} \quad (1)$$

AD5142:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \qquad \text{From 0x00 to 0xFF} \quad (2)$$

where:
D is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.

In potentiometer mode, similar to the mechanical potentiometer, the resistance between Terminal W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} also gives a maximum of 8% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

AD5122:

$$R_{AW}(D) = \frac{128 - D}{128} \times R_{AB} + R_W \qquad \text{From 0x00 to 0x7F} \quad (3)$$

AD5142:

$$R_{AW}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \qquad \text{From 0x00 to 0xFF} \quad (4)$$

where:
D is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.

If the device is configured in linear gain setting mode, the resistance between Terminal W and Terminal A is directly proportional to the code loaded in the associate RDAC register. The general equations for this operation are

AD5122:

$$R_{AW}(D) = \frac{D}{128} \times R_{AB} + R_W \qquad \text{From 0x00 to 0x7F} \quad (5)$$

AD5142:

$$R_{AW}(D) = \frac{D}{256} \times R_{AB} + R_W \qquad \text{From 0x00 to 0xFF} \quad (6)$$

where:
D is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.

In the bottom scale condition or top scale condition, a finite total wiper resistance of 40 Ω is present. Regardless of which setting the device is operating in, limit the current between Terminal A to Terminal B, Terminal W to Terminal A, and Terminal W to Terminal B, to the maximum continuous current of ±6 mA or to the pulse current specified in Table 6. Otherwise, degradation or possible destruction of the internal switch contact can occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A that is proportional to the input voltage at A to B, as shown in Figure 44.

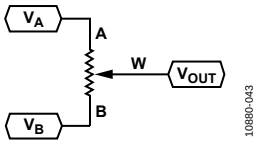


Figure 44. Potentiometer Mode Configuration

Connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 5 V. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B \quad (7)$$

where:
$R_{WB}(D)$ can be obtained from Equation 1 and Equation 2.
$R_{AW}(D)$ can be obtained from Equation 3 and Equation 4.

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

TERMINAL VOLTAGE OPERATING RANGE

The AD5122/AD5142 are designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on Terminal A, Terminal B, or Terminal W that exceed V_{DD} are clamped by the forward-biased diode. There is no polarity constraint between V_A, V_W, and V_B, but they cannot be higher than V_{DD} or lower than V_{SS}.

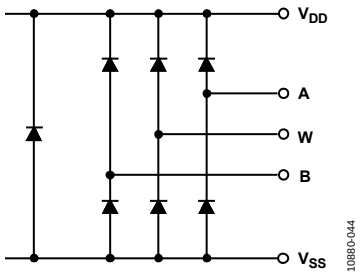


Figure 45. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 45), it is important to power up V_{DD} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally. The ideal power-up sequence is V_{SS}, V_{DD}, V_{LOGIC}, digital inputs, and V_A, V_B, and V_W. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{SS}, V_{DD}, and V_{LOGIC}. Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{LOGIC} is powered, the power-on preset activates, which restores EEPROM values to the RDAC registers.

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use a compact, minimum lead length layout design. Ensure that the leads to the input are as direct as possible with a minimum conductor length. Ground paths must have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Apply low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 46 illustrates the basic supply bypassing configuration for the AD5122/AD5142.

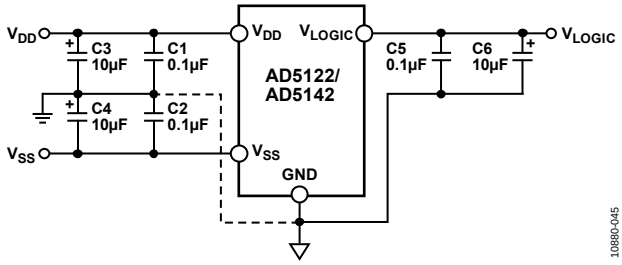
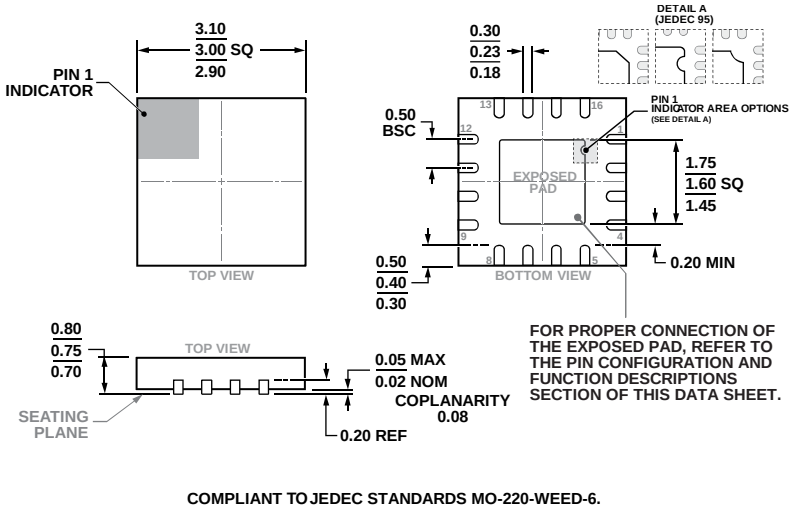


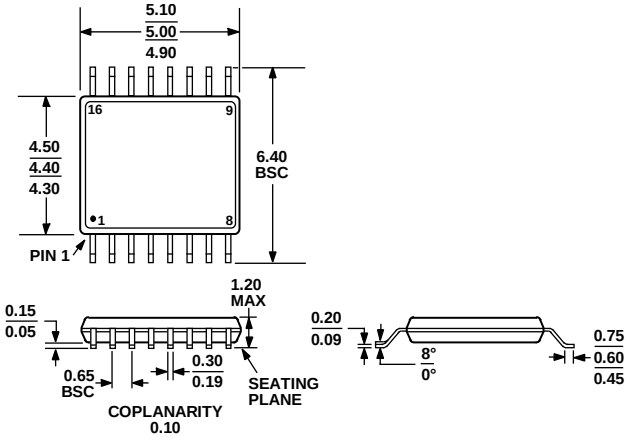
Figure 46. Power Supply Bypassing

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 47. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 48. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	R_{AB} (kΩ)	Resolution	Interface	Temperature Range	Package Description	Package Option	Branding
AD5122BCPZ10-RL7	10	128	SPI	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DH8
AD5122BCPZ100-RL7	100	128	SPI	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DH9
AD5122WBCPZ10-RL7	10	128	SPI	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DMY
AD5122BRUZ10	10	128	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5122BRUZ100	100	128	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5122BRUZ10-RL7	10	128	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5122WBRUZ10-RL7	10	128	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5122BRUZ100-RL7	100	128	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5142BCPZ10-RL7	10	256	SPI	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DH5
AD5142BCPZ100-RL7	100	256	SPI	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DH6
AD5142WBCPZ10-RL7	10	256	SPI	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	DN0
AD5142BRUZ10	10	256	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5142BRUZ100	100	256	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5142BRUZ10-RL7	10	256	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5142WBRUZ10-RL7	10	256	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
AD5142BRUZ100-RL7	100	256	SPI	−40°C to +125°C	16-Lead TSSOP	RU-16	
EVAL-AD5142DBZ					Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all of the available resistor value options.
[3] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD5122W and AD5142W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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