

Quad Channel, 128-/256-Position, I<sup>2</sup>C, Nonvolatile Digital Potentiometer

**FEATURES**

- ▶ 10 kΩ and 100 kΩ resistance options
- ▶ Resistor tolerance: 8% maximum
- ▶ Wiper current: ±6 mA
- ▶ Low temperature coefficient: 35 ppm/°C
- ▶ Wide bandwidth: 3 MHz
- ▶ Fast start-up time < 75 μs
- ▶ Linear gain setting mode
- ▶ Single- and dual-supply operation
- ▶ Wide operating temperature: -40°C to +125°C
- ▶ 3 mm × 3 mm package

**APPLICATIONS**

- ▶ Portable electronics level adjustment
- ▶ LCD panel brightness and contrast controls
- ▶ Programmable filters, delays, and time constants
- ▶ Programmable power supplies

**GENERAL DESCRIPTION**

The AD5123/AD5143<sup>1</sup> potentiometers provide a nonvolatile solution for 128-/256-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the Ax, Bx, and Wx pins.

The low resistor tolerance and low nominal temperature coefficient simplify open-loop applications as well as applications requiring tolerance matching.

The linear gain setting mode allows independent programming of the resistance between the digital potentiometer terminals, through the R<sub>AW</sub> and R<sub>WB</sub> string resistors, allowing very accurate resistor matching.

The high bandwidth and low total harmonic distortion (THD) ensure optimal performance for ac signals, making the devices suitable for filter design.

The low wiper resistance of only 40 Ω at the ends of the resistor array allows for pin to pin connection.

The wiper values can be set through an I<sup>2</sup>C-compatible digital interface that also reads back the wiper register and EEPROM contents.

The AD5123/AD5143 are available in a compact, 16-lead, 3 mm × 3 mm LFCSP. The devices are guaranteed to operate over the extended industrial temperature range of -40°C to +125°C.

**FUNCTIONAL BLOCK DIAGRAM**

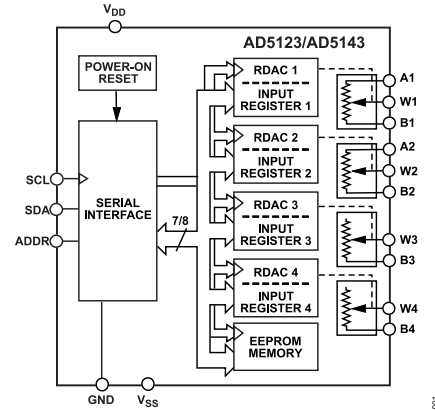


Figure 1.

Table 1. Family Models

Model	Channel	Position	Interface	Package
AD5123 <sup>1</sup>	Quad	128	I <sup>2</sup> C	LFCSP
AD5124	Quad	128	SPI/I <sup>2</sup> C	LFCSP
AD5124	Quad	128	SPI	TSSOP
AD5143	Quad	256	I <sup>2</sup> C	LFCSP
AD5144	Quad	256	SPI/I <sup>2</sup> C	LFCSP
AD5144	Quad	256	SPI	TSSOP
AD5144A	Quad	256	I <sup>2</sup> C	TSSOP
AD5122	Dual	128	SPI	LFCSP/TSSOP
AD5122A	Dual	128	I <sup>2</sup> C	LFCSP/TSSOP
AD5142	Dual	256	SPI	LFCSP/TSSOP
AD5142A	Dual	256	I <sup>2</sup> C	LFCSP/TSSOP
AD5121	Single	128	SPI/I <sup>2</sup> C	LFCSP
AD5141	Single	256	SPI/I <sup>2</sup> C	LFCSP

<sup>1</sup> Two potentiometers and two rheostats.

<sup>1</sup> Protected by U.S. Patent 7,688,240.

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## REVISION HISTORY

### 1/2022—Rev. B to Rev. C

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## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—AD5123

$V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ;  $V_{DD} = 2.25 \text{ V to } 2.75 \text{ V}$ ,  $V_{SS} = -2.25 \text{ V to } -2.75 \text{ V}$ ;  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		7			Bits
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{AB} = 10 \text{ k}\Omega$ $V_{DD} \geq 2.7 \text{ V}$	-1	$\pm 0.1$	+1	LSB
		$V_{DD} < 2.7 \text{ V}$ $R_{AB} = 100 \text{ k}\Omega$	-2.5	$\pm 1$	+2.5	LSB
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$V_{DD} \geq 2.7 \text{ V}$	-0.5	$\pm 0.1$	+0.5	LSB
		$V_{DD} < 2.7 \text{ V}$	-1	$\pm 0.25$	+1	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		-8	$\pm 1$	+8	%
Resistance Temperature Coefficient <sup>3</sup>	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance <sup>3</sup>	$R_W$	Code = zero scale $R_{AB} = 10 \text{ k}\Omega$		55	125	$\Omega$
		$R_{AB} = 100 \text{ k}\Omega$		130	400	$\Omega$
Bottom Scale or Top Scale	$R_{BS}$ or $R_{TS}$	$R_{AB} = 10 \text{ k}\Omega$		40	80	$\Omega$
		$R_{AB} = 100 \text{ k}\Omega$		60	230	$\Omega$
Nominal Resistance Match	$R_{AB1}/R_{AB2}$	Code = full scale	-1	$\pm 0.2$	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity <sup>4</sup>	INL	$R_{AB} = 10 \text{ k}\Omega$	-0.5	$\pm 0.1$	+0.5	LSB
		$R_{AB} = 100 \text{ k}\Omega$	-0.25	$\pm 0.1$	+0.25	LSB
Differential Nonlinearity <sup>4</sup>	DNL		-0.25	$\pm 0.1$	+0.25	LSB
Full-Scale Error	$V_{WFSE}$	$R_{AB} = 10 \text{ k}\Omega$	-1.5	-0.1		LSB
		$R_{AB} = 100 \text{ k}\Omega$	-0.5	$\pm 0.1$	+0.5	LSB
Zero-Scale Error	$V_{WZSE}$	$R_{AB} = 10 \text{ k}\Omega$		1	1.5	LSB
		$R_{AB} = 100 \text{ k}\Omega$		0.25	0.5	LSB
Voltage Divider Temperature Coefficient <sup>3</sup>	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		$\pm 5$		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous Current	$I_A$ , $I_B$ , and $I_W$	$R_{AB} = 10 \text{ k}\Omega$	-6		+6	mA
		$R_{AB} = 100 \text{ k}\Omega$	-1.5		+1.5	mA
Terminal Voltage Range <sup>5</sup>			$V_{SS}$		$V_{DD}$	V
Capacitance A, Capacitance B <sup>3</sup>	$C_A$ , $C_B$	$f = 1 \text{ MHz}$ , measured to GND, code = half scale $R_{AB} = 10 \text{ k}\Omega$		25		pF
		$R_{AB} = 100 \text{ k}\Omega$		12		pF
Capacitance W <sup>3</sup>	$C_W$	$f = 1 \text{ MHz}$ , measured to GND, code = half scale $R_{AB} = 10 \text{ k}\Omega$		12		pF
		$R_{AB} = 100 \text{ k}\Omega$		5		pF

## SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
Common-Mode Leakage Current <sup>3</sup>		$V_A = V_W = V_B$	-500	±15	+500	nA
<b>DIGITAL INPUTS</b>						
Input Logic <sup>3</sup>						
High	$V_{INH}$		$0.7 \times V_{DD}$			V
Low	$V_{INL}$				$0.2 \times V_{DD}$	V
Input Hysteresis <sup>3</sup>	$V_{HYST}$		$0.1 \times V_{DD}$			V
Input Current <sup>3</sup>	$I_{IN}$				±1	μA
Input Capacitance <sup>3</sup>	$C_{IN}$			5		pF
<b>DIGITAL OUTPUTS</b>						
Output High Voltage <sup>3</sup>	$V_{OH}$	$R_{PULL-UP} = 2.2 \text{ k}\Omega$ to $V_{DD}$		$V_{DD}$		V
Output Low Voltage <sup>3</sup>	$V_{OL}$	$I_{SINK} = 3 \text{ mA}$			0.4	V
		$I_{SINK} = 6 \text{ mA}$			0.6	V
Three-State Leakage Current			-1		+1	μA
Three-State Output Capacitance				2		pF
<b>POWER SUPPLIES</b>						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = \text{GND}$	2.3		5.5	V
Dual-Supply Power Range	$V_{DD}/V_{SS}$		±2.25		±2.75	V
Positive Supply Current	$I_{DD}$	$V_{IH} = V_{DD}$ or $V_{IL} = \text{GND}$ $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 2.3 \text{ V}$		0.7 400	5.5	μA nA
Negative Supply Current	$I_{SS}$	$V_{IH} = V_{DD}$ or $V_{IL} = \text{GND}$	-5.5	-0.7		μA
EEPROM Store Current <sup>3, 6</sup>	$I_{DD\_EEPROM\_STORE}$	$V_{IH} = V_{DD}$ or $V_{IL} = \text{GND}$		2		mA
EEPROM Read Current <sup>3, 7</sup>	$I_{DD\_EEPROM\_READ}$	$V_{IH} = V_{DD}$ or $V_{IL} = \text{GND}$		320		μA
Power Dissipation <sup>8</sup>	$P_{DISS}$	$V_{IH} = V_{DD}$ or $V_{IL} = \text{GND}$		3.5		μW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = V_{DD} \pm 10\%$ , code = full scale		-66	-60	dB
<b>DYNAMIC CHARACTERISTICS<sup>9</sup></b>						
Bandwidth	BW	-3 dB $R_{AB} = 10 \text{ k}\Omega$ $R_{AB} = 100 \text{ k}\Omega$		3 0.43		MHz MHz
Total Harmonic Distortion	THD	$V_{DD}/V_{SS} = \pm 2.5 \text{ V}$ , $V_A = 1 \text{ V rms}$ , $V_B = 0 \text{ V}$ , $f = 1 \text{ kHz}$ $R_{AB} = 10 \text{ k}\Omega$ $R_{AB} = 100 \text{ k}\Omega$		-80 -90		dB dB
Resistor Noise Density	$e_{N\_WB}$	Code = half scale, $T_A = 25^\circ\text{C}$ , $f = 10 \text{ kHz}$ $R_{AB} = 10 \text{ k}\Omega$ $R_{AB} = 100 \text{ k}\Omega$		7 20		nV/√Hz nV/√Hz
$V_W$ Settling Time	$t_s$	$V_A = 5 \text{ V}$ , $V_B = 0 \text{ V}$ , from zero-scale to full-scale, ±0.5 LSB error band $R_{AB} = 10 \text{ k}\Omega$ $R_{AB} = 100 \text{ k}\Omega$		2 12		μs μs
Crosstalk ( $C_{W1}/C_{W2}$ )	$C_T$	$R_{AB} = 10 \text{ k}\Omega$ $R_{AB} = 100 \text{ k}\Omega$		10 25		nV-sec nV-sec
Analog Crosstalk Endurance <sup>10</sup>	$C_{TA}$	$T_A = 25^\circ\text{C}$		-90 1		dB Mcycles
			100			kcycles

## SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
Data Retention <sup>11, 12</sup>				50		Years

<sup>1</sup> Typical values represent average readings at 25°C,  $V_{DD} = 5\text{ V}$ , and  $V_{SS} = 0\text{ V}$ .

<sup>2</sup> Resistor integral nonlinearity (R-INL) error is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to  $(0.7 \times V_{DD})/R_{AB}$ .

<sup>3</sup> Guaranteed by design and characterization, not subject to production test.

<sup>4</sup> INL and DNL are measured at  $V_{WB}$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ . DNL specification limits of  $\pm 1$  LSB maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.

<sup>6</sup> Different from operating current; supply current for EEPROM program lasts approximately 30 ms.

<sup>7</sup> Different from operating current; supply current for EEPROM read lasts approximately 20  $\mu\text{s}$ .

<sup>8</sup>  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ .

<sup>9</sup> All dynamic characteristics use  $V_{DD}/V_{SS} = \pm 2.5\text{ V}$ .

<sup>10</sup> Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>11</sup> Retention lifetime equivalent at junction temperature ( $T_J$ ) =  $125^\circ\text{C}$  per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

<sup>12</sup> 50 years applies to an endurance of 1k cycles. An endurance of 100k cycles have an equivalent retention lifetime of 5 years.

## ELECTRICAL CHARACTERISTICS—AD5143

$V_{DD} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ;  $V_{DD} = 2.25\text{ V}$  to  $2.75\text{ V}$ ,  $V_{SS} = -2.25\text{ V}$  to  $-2.75\text{ V}$ ;  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RDACs)						
Resolution	N		8			Bits
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{AB} = 10\text{ k}\Omega$				
		$V_{DD} \geq 2.7\text{ V}$	-2	$\pm 0.2$	+2	LSB
		$V_{DD} < 2.7\text{ V}$	-5	$\pm 1.5$	+5	LSB
		$R_{AB} = 100\text{ k}\Omega$				
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$V_{DD} \geq 2.7\text{ V}$	-1	$\pm 0.1$	+1	LSB
		$V_{DD} < 2.7\text{ V}$	-2	$\pm 0.5$	+2	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		-8	$\pm 1$	+8	%
Resistance Temperature Coefficient <sup>3</sup>	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/ $^\circ\text{C}$
Wiper Resistance <sup>3</sup>	$R_W$	Code = zero scale				
		$R_{AB} = 10\text{ k}\Omega$		55	125	$\Omega$
		$R_{AB} = 100\text{ k}\Omega$		130	400	$\Omega$
Bottom Scale or Top Scale	$R_{BS}$ or $R_{TS}$	$R_{AB} = 10\text{ k}\Omega$		40	80	$\Omega$
		$R_{AB} = 100\text{ k}\Omega$		60	230	$\Omega$
Nominal Resistance Match	$R_{AB1}/R_{AB2}$	Code = full scale	-1	$\pm 0.2$	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity <sup>4</sup>	INL	$R_{AB} = 10\text{ k}\Omega$	-1	$\pm 0.2$	+1	LSB
		$R_{AB} = 100\text{ k}\Omega$	-0.5	$\pm 0.1$	+0.5	LSB

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Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
Differential Nonlinearity <sup>4</sup>	DNL		-0.5	±0.2	+0.5	LSB
Full-Scale Error	V <sub>WFSE</sub>	R <sub>AB</sub> = 10 kΩ	-2.5	-0.1		LSB
		R <sub>AB</sub> = 100 kΩ	-1	±0.2	+1	LSB
Zero-Scale Error	V <sub>WZSE</sub>	R <sub>AB</sub> = 10 kΩ		1.2	3	LSB
		R <sub>AB</sub> = 100 kΩ		0.5	1	LSB
Voltage Divider Temperature Coefficient <sup>3</sup>	(ΔV <sub>W</sub> /V <sub>W</sub> )/ΔT × 10 <sup>6</sup>	Code = half scale		±5		ppm/°C
<b>RESISTOR TERMINALS</b>						
Maximum Continuous Current	I <sub>A</sub> , I <sub>B</sub> , and I <sub>W</sub>	R <sub>AB</sub> = 10 kΩ	-6		+6	mA
		R <sub>AB</sub> = 100 kΩ	-1.5		+1.5	mA
Terminal Voltage Range <sup>5</sup>			V <sub>SS</sub>		V <sub>DD</sub>	V
Capacitance A, Capacitance B <sup>3</sup>	C <sub>A</sub> , C <sub>B</sub>	f = 1 MHz, measured to GND, code = half scale				
		R <sub>AB</sub> = 10 kΩ		25		pF
		R <sub>AB</sub> = 100 kΩ		12		pF
Capacitance W <sup>3</sup>	C <sub>W</sub>	f = 1 MHz, measured to GND, code = half scale				
		R <sub>AB</sub> = 10 kΩ		12		pF
		R <sub>AB</sub> = 100 kΩ		5		pF
Common-Mode Leakage Current <sup>3</sup>		V <sub>A</sub> = V <sub>W</sub> = V <sub>B</sub>	-500	±15	+500	nA
<b>DIGITAL INPUTS</b>						
Input Logic <sup>3</sup>						
High	V <sub>INH</sub>		0.7 × V <sub>DD</sub>			V
Low	V <sub>INL</sub>				0.2 × V <sub>DD</sub>	V
Input Hysteresis <sup>3</sup>	V <sub>HYST</sub>		0.1 × V <sub>DD</sub>			V
Input Current <sup>3</sup>	I <sub>IN</sub>				±1	μA
Input Capacitance <sup>3</sup>	C <sub>IN</sub>			5		pF
<b>DIGITAL OUTPUTS</b>						
Output High Voltage <sup>3</sup>	V <sub>OH</sub>	R <sub>PULL-UP</sub> = 2.2 kΩ to V <sub>DD</sub>		V <sub>DD</sub>		V
Output Low Voltage <sup>3</sup>	V <sub>OL</sub>	I <sub>SINK</sub> = 3 mA			0.4	V
		I <sub>SINK</sub> = 6 mA			0.6	V
Three-State Leakage Current			-1		+1	μA
Three-State Output Capacitance				2		pF
<b>POWER SUPPLIES</b>						
Single-Supply Power Range	V <sub>DD</sub>	V <sub>SS</sub> = GND	2.3		5.5	V
Dual-Supply Power Range	V <sub>DD</sub> /V <sub>SS</sub>		±2.25		±2.75	V
Positive Supply Current	I <sub>DD</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND				
		V <sub>DD</sub> = 5.5 V		0.7	5.5	μA
		V <sub>DD</sub> = 2.3 V		400		nA
Negative Supply Current	I <sub>SS</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND	-5.5	-0.7		μA
EEPROM Store Current <sup>3, 6</sup>	I <sub>DD_EEPROM_STORE</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND		2		mA
EEPROM Read Current <sup>3, 7</sup>	I <sub>DD_EEPROM_READ</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND		320		μA
Power Dissipation <sup>8</sup>	P <sub>DISS</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND		3.5		μW
Power Supply Rejection Ratio	PSRR	ΔV <sub>DD</sub> /ΔV <sub>SS</sub> = V <sub>DD</sub> ± 10%, code = full scale		-66	-60	dB
<b>DYNAMIC CHARACTERISTICS<sup>9</sup></b>						
Bandwidth	BW		-3 dB			

## SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
Total Harmonic Distortion	THD	$R_{AB} = 10\text{ k}\Omega$		3		MHz
		$R_{AB} = 100\text{ k}\Omega$		0.43		MHz
Resistor Noise Density	$e_{N\_WB}$	$V_{DD}/V_{SS} = \pm 2.5\text{ V}$ , $V_A = 1\text{ V rms}$ , $V_B = 0\text{ V}$ , $f = 1\text{ kHz}$				
		$R_{AB} = 10\text{ k}\Omega$		-80		dB
$V_W$ Settling Time	$t_S$	$R_{AB} = 100\text{ k}\Omega$				
		Code = half scale, $T_A = 25^\circ\text{C}$ , $f = 10\text{ kHz}$				
Crosstalk ( $C_{W1}/C_{W2}$ )	$C_T$	$R_{AB} = 10\text{ k}\Omega$		7		nV/ $\sqrt{\text{Hz}}$
		$R_{AB} = 100\text{ k}\Omega$		20		nV/ $\sqrt{\text{Hz}}$
Analog Crosstalk	$C_{TA}$	$R_{AB} = 10\text{ k}\Omega$		2		$\mu\text{s}$
		$R_{AB} = 100\text{ k}\Omega$		12		$\mu\text{s}$
Endurance <sup>10</sup>		$R_{AB} = 10\text{ k}\Omega$		10		nV-sec
		$R_{AB} = 100\text{ k}\Omega$		25		nV-sec
Data Retention <sup>11, 12</sup>		$T_A = 25^\circ\text{C}$		1		Mcycles
			100			kcycles
				50		Years

<sup>1</sup> Typical values represent average readings at  $25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , and  $V_{SS} = 0\text{ V}$ .

<sup>2</sup> Resistor integral nonlinearity (R-INL) error is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to  $(0.7 \times V_{DD})/R_{AB}$ .

<sup>3</sup> Guaranteed by design and characterization, not subject to production test.

<sup>4</sup> INL and DNL are measured at  $V_{WB}$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ . DNL specification limits of  $\pm 1\text{ LSB}$  maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.

<sup>6</sup> Different from operating current; supply current for EEPROM program lasts approximately 30 ms.

<sup>7</sup> Different from operating current; supply current for EEPROM read lasts approximately 20  $\mu\text{s}$ .

<sup>8</sup>  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ .

<sup>9</sup> All dynamic characteristics use  $V_{DD}/V_{SS} = \pm 2.5\text{ V}$ .

<sup>10</sup> Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>11</sup> Retention lifetime equivalent at junction temperature ( $T_J$ ) =  $125^\circ\text{C}$  per JEDEC Standard 22, Method A117. Retention lifetime, based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

<sup>12</sup> 50 years applies to an endurance of 1k cycles. An endurance of 100k cycles have an equivalent retention lifetime of 5 years.

## INTERFACE TIMING SPECIFICATIONS

$V_{DD} = 2.3\text{ V}$  to  $5.5\text{ V}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 4. I<sup>2</sup>C Interface

Parameter <sup>1</sup>	Test Conditions/Comments	Min	Typ	Max	Unit	Description
$f_{SCL}$ <sup>2</sup>	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
$t_1$	Standard mode	4.0			$\mu\text{s}$	SCL high time, $t_{HIGH}$
	Fast mode	0.6			$\mu\text{s}$	
$t_2$	Standard mode	4.7			$\mu\text{s}$	SCL low time, $t_{LOW}$

## SPECIFICATIONS

Table 4. I<sup>2</sup>C Interface

Parameter <sup>1</sup>	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t <sub>3</sub>	Fast mode	1.3			μs	Data setup time, t <sub>SU</sub> ; DAT
	Standard mode	250			ns	
t <sub>4</sub>	Fast mode	100			ns	Data hold time, t <sub>HD</sub> ; DAT
	Standard mode	0		3.45	μs	
t <sub>5</sub>	Fast mode	0		0.9	μs	Setup time for a repeated start condition, t <sub>SU</sub> ; STA
	Standard mode	4.7			μs	
t <sub>6</sub>	Fast mode	0.6			μs	Hold time (repeated) for a start condition, t <sub>HD</sub> ; STA
	Standard mode	4			μs	
t <sub>7</sub>	Fast mode	0.6			μs	Bus free time between a stop and a start condition, t <sub>BUF</sub>
	Standard mode	4.7			μs	
t <sub>8</sub>	Fast mode	1.3			μs	Setup time for a stop condition, t <sub>SU</sub> ; STO
	Standard mode	4			μs	
t <sub>9</sub>	Fast mode	0.6			μs	Rise time of SDA signal, t <sub>RDA</sub>
	Standard mode			1000	ns	
t <sub>10</sub>	Fast mode	20 + 0.1 C <sub>L</sub>		300	ns	Fall time of SDA signal, t <sub>FDA</sub>
	Standard mode			300	ns	
t <sub>11</sub>	Fast mode	20 + 0.1 C <sub>L</sub>		300	ns	Rise time of SCL signal, t <sub>RCL</sub>
	Standard mode			1000	ns	
t <sub>11A</sub>	Fast mode	20 + 0.1 C <sub>L</sub>		300	ns	Rise time of SCL signal after a repeated start condition and after an acknowledge bit, t <sub>RCL1</sub> (not shown in Figure 3)
	Standard mode			1000	ns	
t <sub>12</sub>	Fast mode	20 + 0.1 C <sub>L</sub>		300	ns	Fall time of SCL signal, t <sub>FCL</sub>
	Standard mode			300	ns	
t <sub>SP</sub> <sup>3</sup>	Fast mode	0		50	ns	Pulse width of suppressed spike (not shown in Figure 3)
t <sub>EPROGRAM</sub> <sup>4</sup>			15	50	ms	Memory program time (not shown in Figure 3)
t <sub>EPROGRAM_READBACK</sub>			7	30	μs	Memory readback time (not shown in Figure 3)
t <sub>POWER_UP</sub> <sup>5</sup>				75	μs	Power-on EEPROM restore time (not shown in Figure 3)
t <sub>RESET</sub>			30		μs	Reset EEPROM restore time (not shown in Figure 3)

<sup>1</sup> Maximum bus capacitance is limited to 400 pF.

<sup>2</sup> The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate; however, it has a negative effect on the EMC behavior of the device.

<sup>3</sup> Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode.

<sup>4</sup> EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at lower temperatures and higher write cycles.

<sup>5</sup> Maximum time after V<sub>DD</sub> - V<sub>SS</sub> is equal to 2.3 V.

## SHIFT REGISTER AND TIMING DIAGRAMS

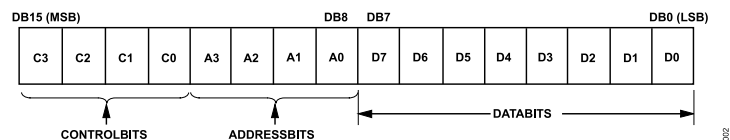


Figure 2. Input Shift Register Contents



SPECIFICATIONS

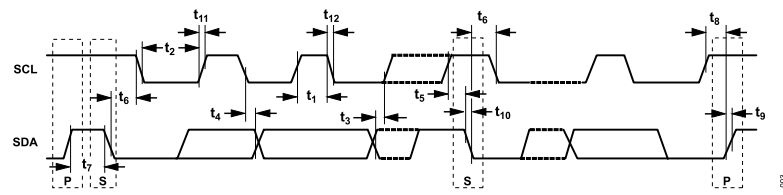


Figure 3. I<sup>2</sup>C Serial Interface Timing Diagram (Typical Write Sequence)

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7.0 V
$V_{SS}$ to GND	+0.3 V to -7.0 V
$V_{DD}$ to $V_{SS}$	7 V
$V_A, V_W, V_B$ to GND	$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V or +7.0 V (whichever is less)
$I_A, I_W, I_B$ Pulsed <sup>1</sup>	
Frequency > 10 kHz	
$R_{AW} = 10\text{ k}\Omega^2$	$\pm 6$ mA/d
$R_{AW} = 100\text{ k}\Omega^2$	$\pm 1.5$ mA/d
Frequency $\leq 10$ kHz	
$R_{AW} = 10\text{ k}\Omega^2$	$\pm 6$ mA/ $\sqrt{d}$
$R_{AW} = 100\text{ k}\Omega^2$	$\pm 1.5$ mA/ $\sqrt{d}$
Digital Inputs	-0.3 V to $V_{DD} + 0.3$ V or +7 V (whichever is less)
Operating Temperature Range, $T_A$ <sup>3</sup>	-40°C to +125°C
Maximum Junction Temperature, $T_J$ Maximum	150°C
Storage Temperature Range	-65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
FICDM	1.5 kV

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> d = pulse duty factor.

<sup>3</sup> Includes programming of EEPROM memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
16-Lead LFCSP	89.5 <sup>1</sup>	3	°C/W

<sup>1</sup> JEDEC 2S2P test board, still air (0 m/sec airflow).

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

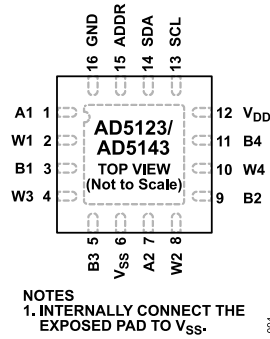


Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A1	Terminal A of RDAC1. $V_{SS} \leq V_A \leq V_{DD}$ .
2	W1	Wiper Terminal of RDAC1. $V_{SS} \leq V_W \leq V_{DD}$ .
3	B1	Terminal B of RDAC1. $V_{SS} \leq V_B \leq V_{DD}$ .
4	W3	Wiper Terminal of RDAC3. $V_{SS} \leq V_W \leq V_{DD}$ .
5	B3	Terminal B of RDAC3. $V_{SS} \leq V_B \leq V_{DD}$ .
6	$V_{SS}$	Negative Power Supply. Decouple this pin with 0.1 $\mu\text{F}$ ceramic capacitors and 10 $\mu\text{F}$ capacitors.
7	A2	Terminal A of RDAC2. $V_{SS} \leq V_A \leq V_{DD}$ .
8	W2	Wiper Terminal of RDAC2. $V_{SS} \leq V_W \leq V_{DD}$ .
9	B2	Terminal B of RDAC2. $V_{SS} \leq V_B \leq V_{DD}$ .
10	W4	Wiper Terminal of RDAC4. $V_{SS} \leq V_W \leq V_{DD}$ .
11	B4	Terminal B of RDAC4. $V_{SS} \leq V_B \leq V_{DD}$ .
12	$V_{DD}$	Positive Power Supply. Decouple this pin with 0.1 $\mu\text{F}$ ceramic capacitors and 10 $\mu\text{F}$ capacitors.
13	SCL	Serial Clock Line. Data is clocked in at the logic low transition.
14	SDA	Serial Data Input/Output.
15	ADDR	Programmable Address for Multiple Package Decoding.
16	GND	Ground Pin, Logic Ground Reference.
	EPAD	Internally Connect the Exposed Paddle to $V_{SS}$ .

TYPICAL PERFORMANCE CHARACTERISTICS

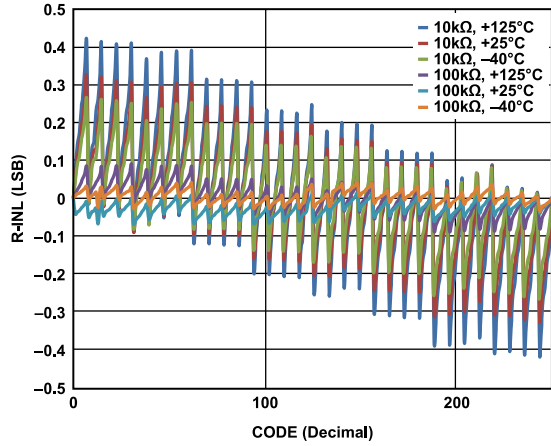


Figure 5. R-INL vs. Code (AD5143)

105

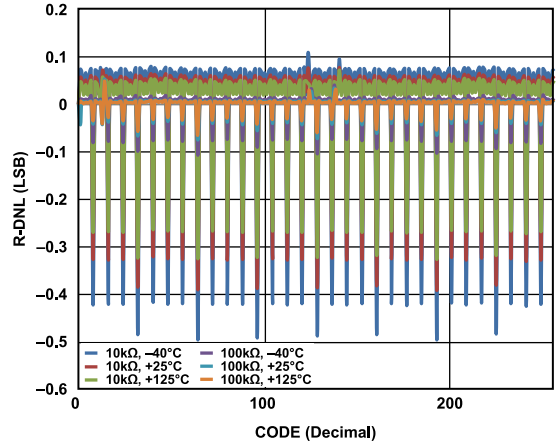


Figure 8. R-DNL vs. Code (AD5143)

108

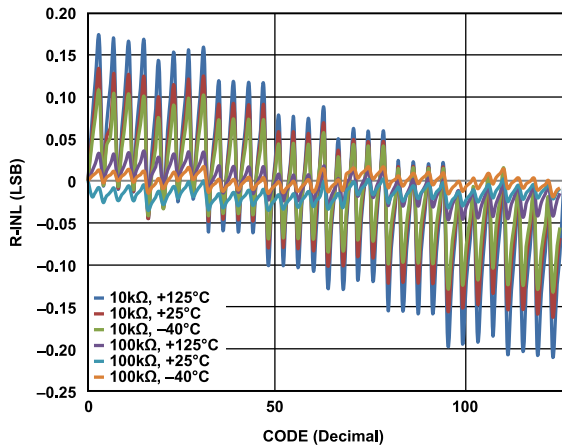


Figure 6. R-INL vs. Code (AD5123)

106

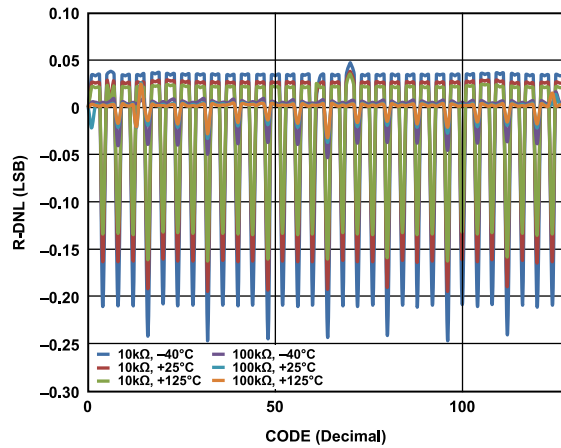


Figure 9. R-DNL vs. Code (AD5123)

109

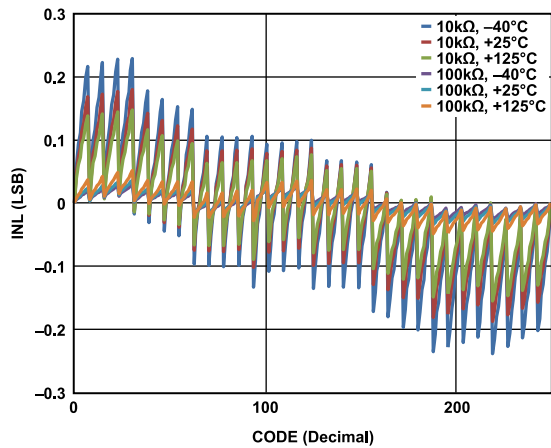


Figure 7. INL vs. Code (AD5143)

107

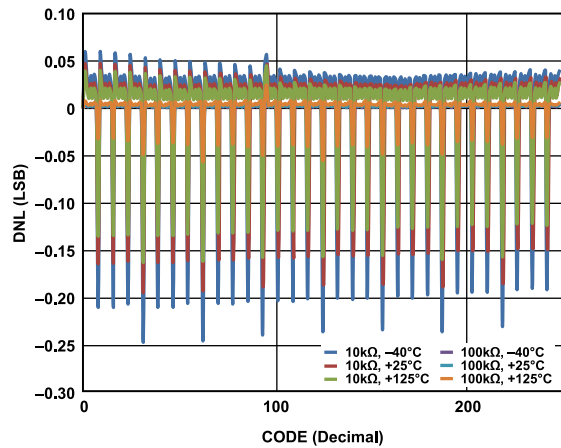


Figure 10. DNL vs. Code (AD5143)

110

TYPICAL PERFORMANCE CHARACTERISTICS

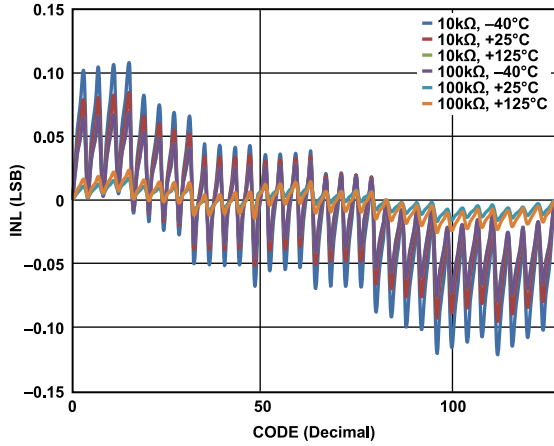


Figure 11. INL vs. Code (AD5123)

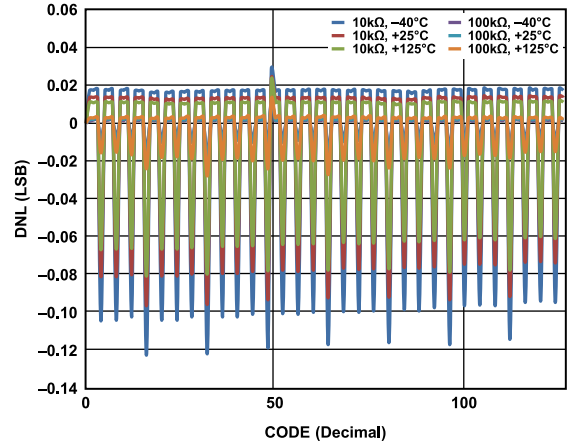


Figure 14. DNL vs. Code (AD5123)

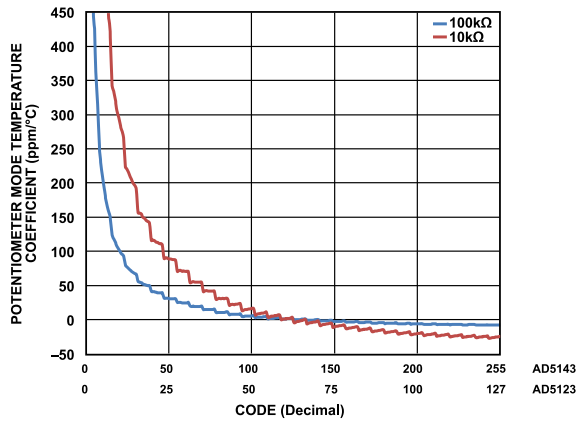


Figure 12. Potentiometer Mode Temperature Coefficient  $((\Delta V_W/V_W)/\Delta T \times 10^6)$  vs. Code

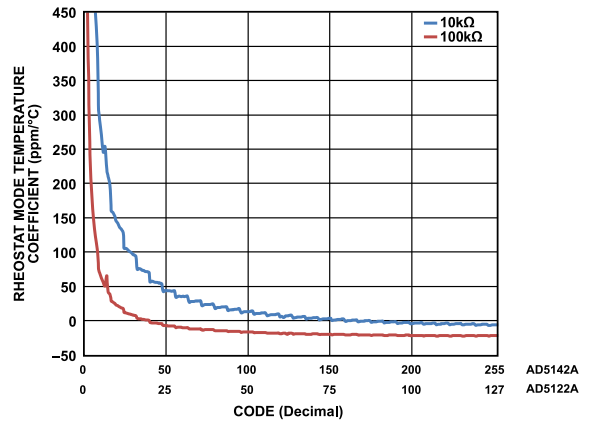


Figure 15. Rheostat Mode Temperature Coefficient  $((\Delta R_{WB}/R_{WB})/\Delta T \times 10^6)$  vs. Code

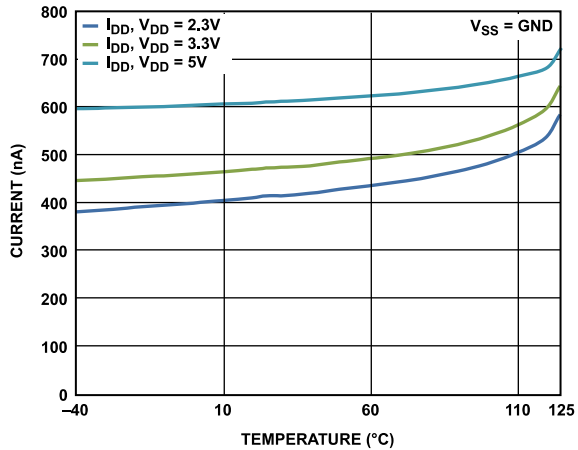


Figure 13. Supply Current vs. Temperature

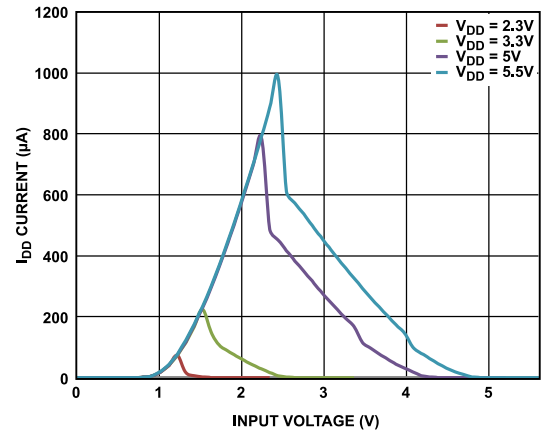


Figure 16.  $I_{DD}$  Current vs. Digital Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

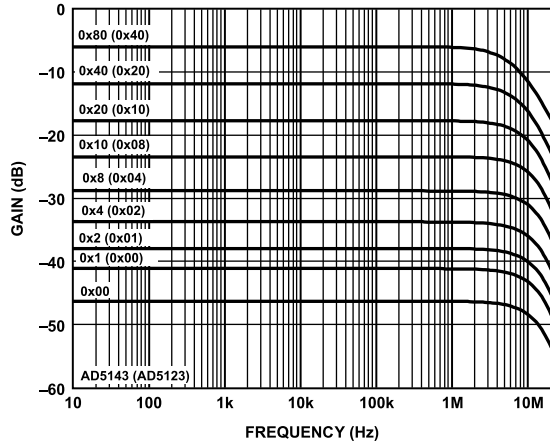


Figure 17. 10 kΩ Gain vs. Frequency and Code

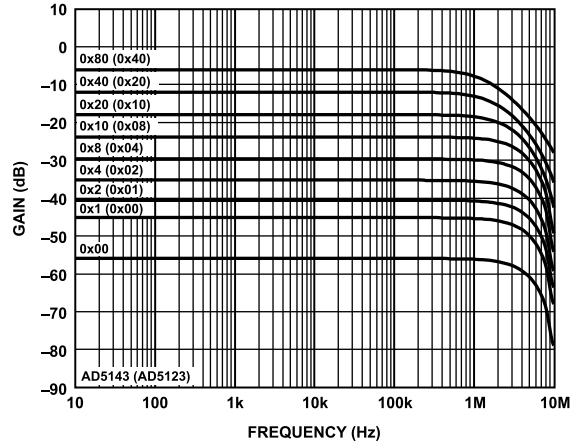


Figure 20. 100 kΩ Gain vs. Frequency and Code

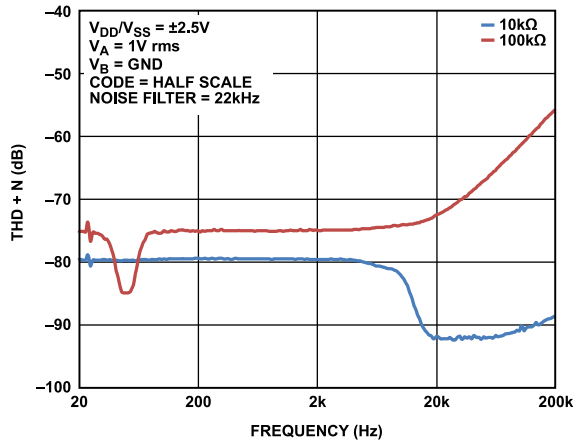


Figure 18. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency

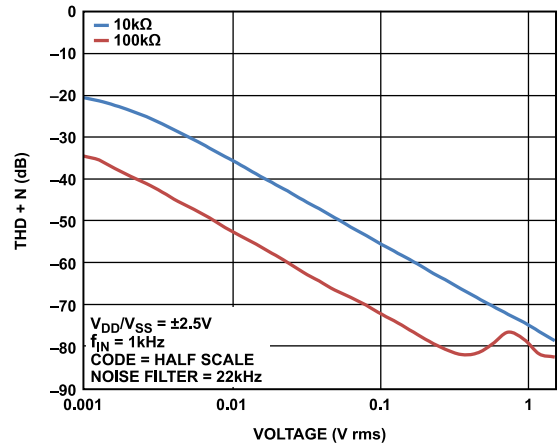


Figure 21. Total Harmonic Distortion Plus Noise (THD + N) vs. Amplitude

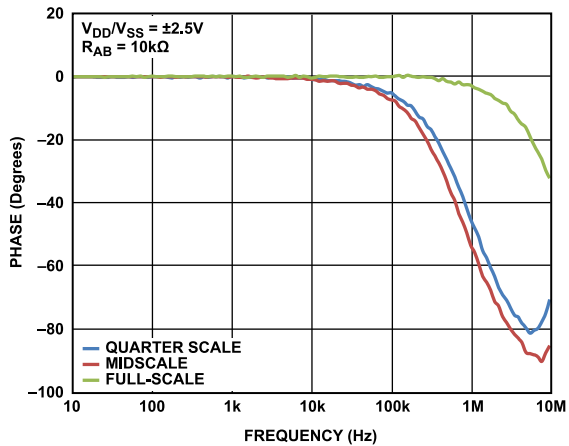


Figure 19. Normalized Phase Flatness vs. Frequency,  $R_{AB} = 10\text{ k}\Omega$

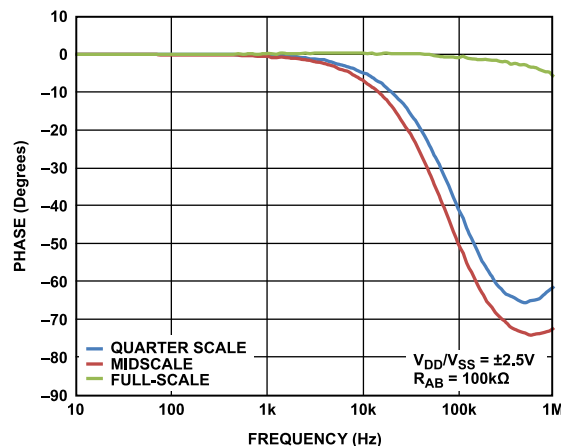


Figure 22. Normalized Phase Flatness vs. Frequency,  $R_{AB} = 100\text{ k}\Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

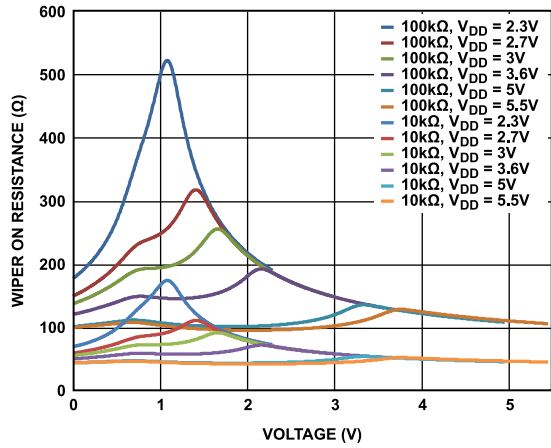


Figure 23. Incremental Wiper On Resistance vs. Positive Power Supply ( $V_{DD}$ )

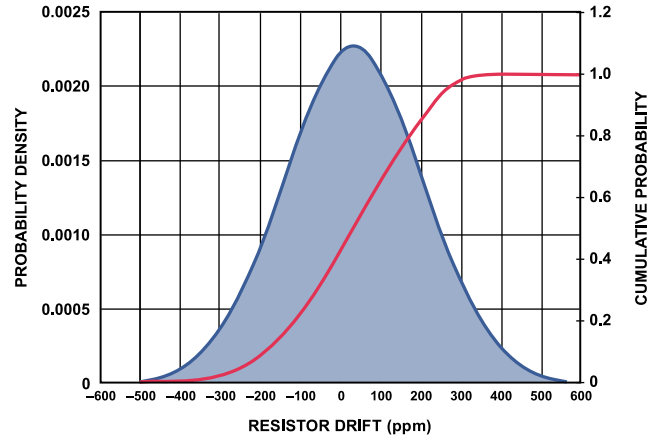


Figure 26. Resistor Lifetime Drift

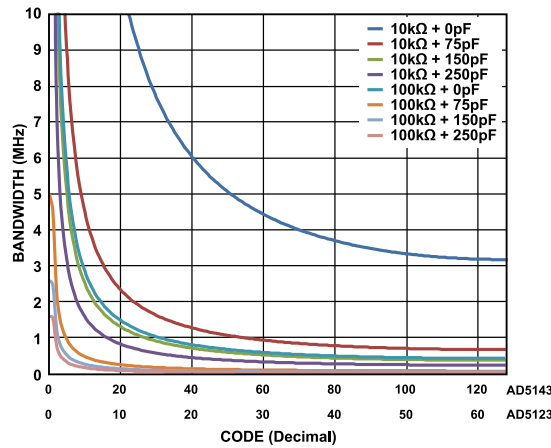


Figure 24. Maximum Bandwidth vs. Code and Net Capacitance

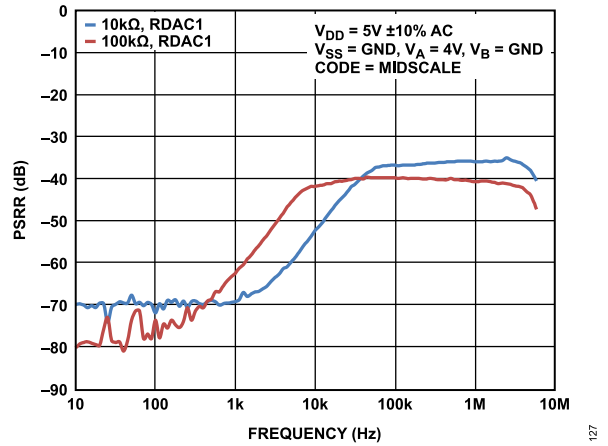


Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency

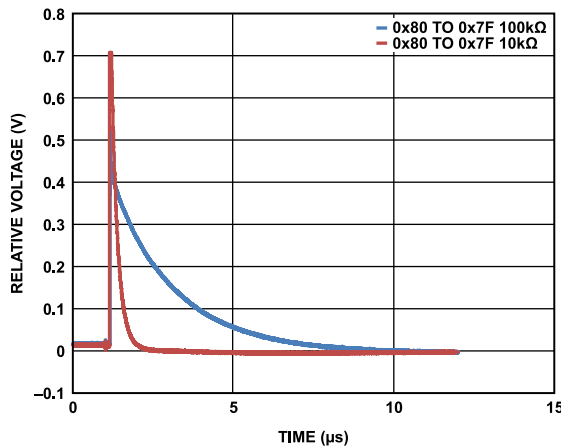


Figure 25. Maximum Transition Glitch

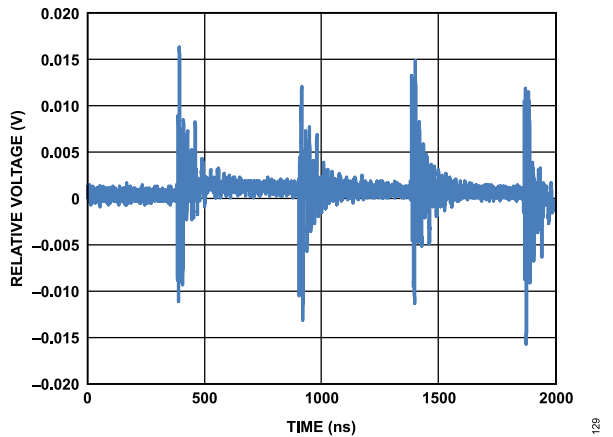


Figure 28. Digital Feedthrough

TYPICAL PERFORMANCE CHARACTERISTICS

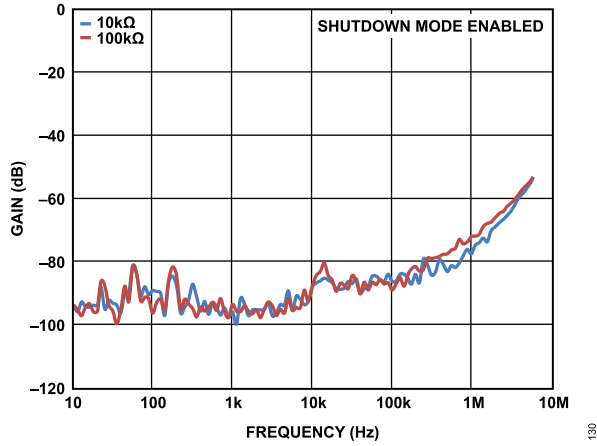


Figure 29. Shutdown Isolation vs. Frequency

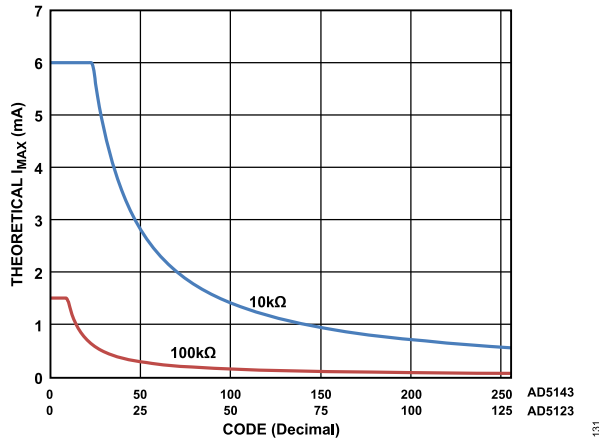


Figure 30. Theoretical Maximum Current vs. Code



TEST CIRCUITS

Figure 31 to Figure 35 define the test conditions used in the Specifications section.

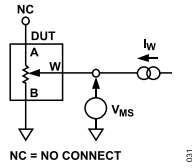


Figure 31. Resistor Integral Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

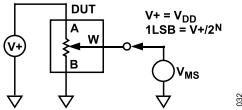


Figure 32. Potentiometer Divider Nonlinearity Error (INL, DNL)

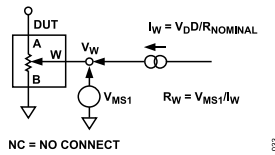


Figure 33. Wiper Resistance

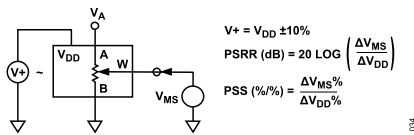


Figure 34. Power Supply Sensitivity and Power Supply Rejection Ratio (PSS, PSRR)

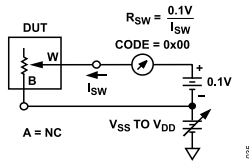


Figure 35. Incremental On Resistance

## THEORY OF OPERATION

The AD5123/AD5143 digital programmable potentiometers are designed to operate as true variable resistors for analog signals within the terminal voltage range of  $V_{SS} < V_{TERM} < V_{DD}$ . The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register that allows unlimited changes of resistance settings. A secondary register (the input register) can preload the RDAC register data.

The RDAC register can be programmed with any position setting using the I<sup>2</sup>C interface (depending on the model). When a desirable wiper position is found, this value can be stored in the EEPROM memory. Thereafter, the wiper position is always restored to that position for subsequent power-ups. The storing of EEPROM data takes approximately 15 ms; during this time, the device is locked and does not acknowledge any new command, preventing any changes from taking place.

## RDAC REGISTER AND EEPROM

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with

0x80 (AD5143, 256 taps), the wiper is connected to half scale of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

It is possible to both write to and read from the RDAC register using the digital interface (see Table 8).

The contents of the RDAC register can be stored to the EEPROM using Command 9 (see Table 8). Thereafter, the RDAC register always sets at that position for any future on off on power supply sequence. It is possible to read back data saved into the EEPROM with Command 3 (see Table 8).

Alternatively, the EEPROM can be written to independently using Command 11 (see Table 11).

**Table 8. Reduced Commands Operation Truth Table**

Command Number	Control Bits[DB15:DB12]				Address Bits[DB11:DB8] <sup>1</sup>				Data Bits[DB7:DB0] <sup>1</sup>								Operation									
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0										
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: do nothing									
1	0	0	0	1	0	0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC									
2	0	0	1	0	0	0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to input register									
3	0	0	1	1	0	0	A1	A0	X	X	X	X	X	X	D1	D0	Read back contents									
																	<table border="1"> <thead> <tr> <th>D1</th> <th>D0</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>EEPROM</td> </tr> <tr> <td>1</td> <td>1</td> <td>RDAC</td> </tr> </tbody> </table>	D1	D0	Data	0	1	EEPROM	1	1	RDAC
D1	D0	Data																								
0	1	EEPROM																								
1	1	RDAC																								
9	0	1	1	1	0	0	A1	A0	X	X	X	X	X	X	X	1	Copy RDAC register to EEPROM									
10	0	1	1	1	0	0	A1	A0	X	X	X	X	X	X	X	0	Copy EEPROM into RDAC									
14	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Software reset									
15	1	1	0	0	A3	A2	A1	A0	X	X	X	X	X	X	X	D0	Software shutdown									
																	<table border="1"> <thead> <tr> <th>D0</th> <th>Condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal mode</td> </tr> <tr> <td>1</td> <td>Shutdown mode</td> </tr> </tbody> </table>	D0	Condition	0	Normal mode	1	Shutdown mode			
D0	Condition																									
0	Normal mode																									
1	Shutdown mode																									

<sup>1</sup> X means don't care.

**Table 9. Reduced Address Bits Table**

A3	A2	A1	A0	Channel	Stored Channel Memory
1	X <sup>1</sup>	X <sup>1</sup>	X <sup>1</sup>	All channels	Not applicable
0	0	0	0	RDAC1	RDAC1
0	0	0	1	RDAC2	RDAC2
0	0	1	0	RDAC3	RDAC3
0	0	1	1	RDAC4	RDAC4

<sup>1</sup> X means don't care.

## THEORY OF OPERATION

### INPUT SHIFT REGISTER

For the AD5123/AD5143, the input shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of four control bits, followed by four address bits and by eight data bits.

If the AD5123 RDAC or EEPROM registers are read from or written to, the lowest data bit (Bit 0) is ignored.

Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command, as listed in Table 8 and Table 11.

### I<sup>2</sup>C SERIAL DATA INTERFACE

The AD5123/AD5143 have 2-wire, I<sup>2</sup>C-compatible serial interfaces. These devices can be connected to an I<sup>2</sup>C bus as a slave device, under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD5123/AD5143 support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The 2-wire serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address and an R/ $\bar{W}$  bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, the shift register.  
If the R/ $\bar{W}$  bit is set high, the master reads from the slave device. However, if the R/ $\bar{W}$  bit is set low, the master writes to the slave device.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read from or written to, a stop condition is established. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then high again during the tenth clock pulse to establish a stop condition.

### I<sup>2</sup>C ADDRESS

The facility to make hardwired changes to ADDR allows the user to incorporate up to three of these devices on one bus as outlined in Table 10.

Table 10. I<sup>2</sup>C Address Selection

ADDR Pin	7-Bit I <sup>2</sup> C Device Address
V <sub>DD</sub>	0101000
No connect <sup>1</sup>	0101010
GND	0101011

<sup>1</sup> Not available in bipolar mode (V<sub>SS</sub> < 0 V).

### ADVANCED CONTROL MODES

The AD5123/AD5143 digital potentiometers include a set of user programming features to address the wide number of applications for these universal adjustment devices (see Table 11 and Table 13).

Key programming features include the following:

- ▶ Input register
- ▶ Linear gain setting mode
- ▶ Low wiper resistance feature
- ▶ Linear increment and decrement instructions
- ▶ ±6 dB increment and decrement instructions
- ▶ Burst mode (I<sup>2</sup>C only)
- ▶ Reset
- ▶ Shutdown mode

Table 11. Advance Commands Operation Truth Table

Command Number	Control Bits[DB15:DB12]				Address Bits[DB11:DB8] <sup>1</sup>				Data Bits[DB7:DB0] <sup>1</sup>								Operation															
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0																
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: do nothing															
1	0	0	0	1	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC															
2	0	0	1	0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to input register															
3	0	0	1	1	X	A2	A1	A0	X	X	X	X	X	X	D1	D0	Read back contents															
																	<table border="1"> <thead> <tr> <th>D1</th> <th>D0</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Input register</td> </tr> <tr> <td>0</td> <td>1</td> <td>EEPROM</td> </tr> <tr> <td>1</td> <td>0</td> <td>Control register</td> </tr> <tr> <td>1</td> <td>1</td> <td>RDAC</td> </tr> </tbody> </table>	D1	D0	Data	0	0	Input register	0	1	EEPROM	1	0	Control register	1	1	RDAC
D1	D0	Data																														
0	0	Input register																														
0	1	EEPROM																														
1	0	Control register																														
1	1	RDAC																														
4	0	1	0	0	A3	A2	A1	A0	X	X	X	X	X	X	X	1	Linear RDAC increment															

## THEORY OF OPERATION

Table 11. Advance Commands Operation Truth Table

Command Number	Control Bits[DB15:DB12]				Address Bits[DB11:DB8] <sup>1</sup>				Data Bits[DB7:DB0] <sup>1</sup>								Operation
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
5	0	1	0	0	A3	A2	A1	A0	X	X	X	X	X	X	X	0	Linear RDAC decrement
6	0	1	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	1	+6 dB RDAC increment
7	0	1	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	0	-6 dB RDAC decrement
8	0	1	1	0	A3	A2	A1	A0	X	X	X	X	X	X	X	X	Copy input register to RDAC (software LRDAC)
9	0	1	1	1	0	0	A1	A0	X	X	X	X	X	X	X	1	Copy RDAC register to EEPROM
10	0	1	1	1	0	0	A1	A0	X	X	X	X	X	X	X	0	Copy EEPROM into RDAC
11	1	0	0	0	0	0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to EEPROM
12	1	0	0	1	A3	A2	A1	A0	1	X	X	X	X	X	X	D0	Top scale D0 = 0; normal mode D0 = 1; shutdown mode
13	1	0	0	1	A3	A2	A1	A0	0	X	X	X	X	X	X	D0	Bottom scale D0 = 1; enter D0 = 0; exit
14	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Software reset
15	1	1	0	0	A3	A2	A1	A0	X	X	X	X	X	X	X	D0	Software shutdown D0 = 0; normal mode D0 = 1; device placed in shutdown mode
16	1	1	0	1	X	X	X	X	X	X	X	X	D3	D2	D1	D0	Copy serial register data to control register

<sup>1</sup> X means don't care.

Table 12. Address Bits

A3	A2	A1	A0	Potentiometer Mode		Linear Gain Setting Mode		Stored RDAC Memory
				Input Register	RDAC Register	Input Register	RDAC Register	
1	X <sup>1</sup>	X <sup>1</sup>	X <sup>1</sup>	All channels	All channels	All channels	All channels	Not applicable
0	0	0	0	RDAC1	RDAC1	R <sub>WB1</sub>	R <sub>WB1</sub>	RDAC1
0	1	0	0	Not applicable	Not applicable	R <sub>AW1</sub>	R <sub>AW1</sub>	Not applicable
0	0	0	1	RDAC2	RDAC2	R <sub>WB2</sub>	R <sub>WB2</sub>	RDAC2
0	1	0	1	Not applicable	Not applicable	R <sub>AW2</sub>	R <sub>AW2</sub>	Not applicable
0	0	1	0	RDAC3	RDAC3	R <sub>WB3</sub>	R <sub>WB3</sub>	RDAC3
0	1	1	0	Not applicable	Not applicable	R <sub>AW3</sub>	R <sub>AW3</sub>	Not applicable
0	0	1	1	RDAC4	RDAC4	R <sub>WB4</sub>	R <sub>WB4</sub>	RDAC4
0	1	1	1	Not applicable	Not applicable	R <sub>AW4</sub>	R <sub>AW4</sub>	Not applicable

<sup>1</sup> X means don't care.

Table 13. Control Register Bit Descriptions

Bit Name	Description
D0	RDAC register write protect 0 = wiper position frozen to value in EEPROM memory 1 = allows update of wiper position through digital interface (default)
D1	EEPROM program enable 0 = EEPROM program disabled 1 = enables device for EEPROM program (default)

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**Table 13. Control Register Bit Descriptions**

Bit Name	Description
D2	Linear setting mode/potentiometer mode 0 = potentiometer mode (default) 1 = linear gain setting mode
D3	Burst mode 0 = disabled (default) 1 = enabled (no disable after stop or repeat start condition)

### Input Register

The AD5123/AD5143 include one input register per RDAC register. These registers allow preloading of the value for the associated RDAC register. These registers can be written to using Command 2 and read back using Command 3 (see Table 11).

This feature allows a synchronous and asynchronous update of one or all of the RDAC registers at the same time.

The transfer from the input register to the RDAC register is done synchronously by Command 8 (see Table 11).

If new data is loaded in an RDAC register, this RDAC register automatically overwrites the associated input register.

### Linear Gain Setting Mode

The patented architecture of the AD5123/AD5143 allows the independent control of each string resistor,  $R_{AW}$ , and  $R_{WB}$ . To enable linear gain setting mode, use Command 16 (see Table 11) to set Bit D2 of the control register (see Table 13).

This mode of operation can control the potentiometer as two independent rheostats connected at a single point, W terminal, as opposed to potentiometer mode where each resistor is complementary,  $R_{AW} = R_{AB} - R_{WB}$ .

This mode enables a second input and an RDAC register per channel, as shown in Table 12; however, the actual RDAC contents remain unchanged. The same operations are valid for potentiometer and linear setting gain modes. The devices restore in potentiometer mode after a reset or power-up.

### Low Wiper Resistance Feature

The AD5123/AD5143 include two commands to reduce the wiper resistance between the terminals when the devices achieve full scale or zero scale. These extra positions are called bottom scale, BS, and top scale, TS. The resistance between Terminal A and Terminal W at top scale is specified as  $R_{TS}$ . Similarly, the bottom scale resistance between Terminal B and Terminal W is specified as  $R_{BS}$ .

The contents of the RDAC registers are unchanged by entering in these positions. There are three ways to exit from top scale and bottom scale: by using Command 12 or Command 13 (see Table 11); by loading new data in an RDAC register, which includes

increment/decrement operations; or by entering shutdown mode, Command 15 (see Table 11).

Table 14 and Table 15 show the truth tables for the top scale position and the bottom scale position, respectively, when the potentiometer or linear gain setting mode is enabled.

**Table 14. Top Scale Truth Table**

Linear Gain Setting Mode		Potentiometer Mode	
$R_{AW}$	$R_{WB}$	$R_{AW}$	$R_{WB}$
$R_{AB}$	$R_{AB}$	$R_{TS}$	$R_{AB}$

**Table 15. Bottom Scale Truth Table**

Linear Gain Setting Mode		Potentiometer Mode	
$R_{AW}$	$R_{WB}$	$R_{AW}$	$R_{WB}$
$R_{TS}$	$R_{BS}$	$R_{AB}$	$R_{BS}$

### Linear Increment and Decrement Instructions

The increment and decrement commands (Command 4 and Command 5 in Table 11) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send an increment or decrement command to the device. The adjustment can be individual or in a ganged potentiometer arrangement, where all wiper positions are changed at the same time.

For an increment command, executing Command 4 automatically moves the wiper to the next resistance RDAC position. This command can be executed in a single channel or multiple channels.

### ±6 dB Increment and Decrement Instructions

Two programming instructions produce logarithmic taper increment or decrement of the wiper position control by an individual potentiometer or by a ganged potentiometer arrangement where all RDAC register positions are changed simultaneously. The +6 dB increment is activated by Command 6, and the -6 dB decrement is activated by Command 7 (see Table 11). For example, starting with the zero-scale position and executing Command 6 ten times moves the wiper in 6 dB steps to the full-scale position. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale position (see Table 16).

Incrementing the wiper position by +6 dB essentially doubles the RDAC register value, whereas decrementing the wiper position by

## THEORY OF OPERATION

-6 dB halves the register value. Internally, the AD5123/AD5143 use shift registers to shift the bits left and right to achieve a  $\pm 6$  dB increment or decrement. These functions are useful for various audio/video level adjustments, especially for white LED brightness settings in which human visual responses are more sensitive to large adjustments than to small adjustments.

**Table 16. Detailed Left Shift and Right Shift Functions for the  $\pm 6$  dB Step Increment and Decrement**

Left Shift (+6 dB/Step)	Right Shift (-6 dB/Step)
0000 0000	1111 1111
0000 0001	0111 1111
0000 0010	0011 1111
0000 0100	0001 1111
0000 1000	0000 1111
0001 0000	0000 0111
0010 0000	0000 0011
0100 0000	0000 0001
1000 0000	0000 0000
1111 1111	0000 0000

### Burst Mode

By enabling the burst mode, multiple data bytes can be sent to the device consecutively. After the command byte, the device interprets the consecutive bytes as data bytes for the command.

A new command can be sent by generating a repeat start or by a stop and start condition.

The burst mode is activated by setting Bit D3 of the control register (see Table 13).

### Reset

The AD5123/AD5143 can be reset through software by executing Command 14 (see Table 11). The reset command loads the RDAC registers with the contents of the EEPROM and takes approximately 30  $\mu$ s. The EEPROM is preloaded to midscale at the factory, and initial power-up is, accordingly, at midscale.

### Shutdown Mode

The AD5123/AD5143 can be placed in shutdown mode by executing the software shutdown command, Command 15 (see Table 11), and setting the LSB (D0) to 1. This feature places the RDAC in a zero power consumption state where the device operates in potentiometer mode, Terminal A is open-circuited, and the wiper, Terminal W, is connected to Terminal B; however, a finite wiper resistance of 40  $\Omega$  is present. When the device is configured in linear gain setting mode, the resistor addressed,  $R_{AW}$  or  $R_{WB}$ , is internally placed at high impedance. Table 17 shows the truth table depending on the device operating mode. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 11 are supported while in

shutdown mode. Execute Command 15 (see Table 11) and set the LSB (D0) to 0 to exit shutdown mode.

**Table 17. Truth Table for Shutdown Mode**

Linear Gain Setting Mode		Potentiometer Mode	
$R_{AW}$	$R_{WB}$	$R_{AW}$	$R_{WB}$
High impedance	High impedance	High impedance	$R_{BS}$

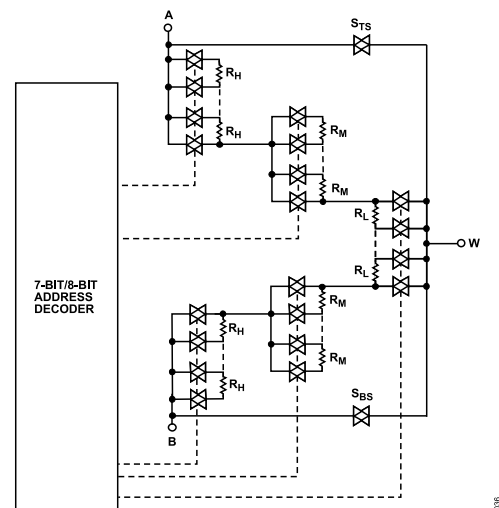
### EEPROM OR RDAC REGISTER PROTECTION

The EEPROM and RDAC registers can be protected by disabling any update to these registers. This can be done by using software or by using hardware. If these registers are protected by software, set Bit D0 and/or Bit D1 (see Table 13), which protects the RDAC and EEPROM registers independently.

When RDAC is protected, the only operation allowed is to copy the EEPROM into the RDAC register.

### RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5123/AD5143 employ a three-stage segmentation approach, as shown in Figure 36. The AD5123/AD5143 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from  $V_{DD}$  and  $V_{SS}$ .



**Figure 36. AD5123/AD5143 Simplified RDAC Circuit**

### Top Scale/Bottom Scale Architecture

In addition, the AD5123/AD5143 include new positions to reduce the resistance between terminals. These positions are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 130  $\Omega$  to 60  $\Omega$  ( $R_{AB} = 100$  k $\Omega$ ). At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB, and the total resistance is reduced to 60  $\Omega$  ( $R_{AB} = 100$  k $\Omega$ ).

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## PROGRAMMING THE VARIABLE RESISTOR

## Rheostat Operation—±8% Resistor Tolerance

The AD5123/AD5143 operate in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W, as shown in Figure 37.

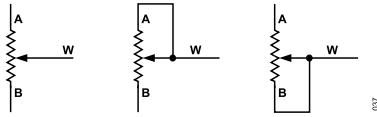


Figure 37. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B,  $R_{AB}$ , is 10 k $\Omega$  or 100 k $\Omega$ , and has 128/256 tap points accessed by the wiper terminal. The 7-bit/8-bit data in the RDAC latch is decoded to select one of the 128/256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

AD5123:

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \quad \text{From } 0x00 \text{ to } 0x7F \quad (1)$$

AD5143:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad \text{From } 0x00 \text{ to } 0xFF \quad (2)$$

where:

$D$  is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.

$R_{AB}$  is the end to end resistance.

$R_W$  is the wiper resistance.

In potentiometer mode, similar to the mechanical potentiometer, the resistance between Terminal W and Terminal A also produces a digitally controlled complementary resistance,  $R_{WA}$ .  $R_{WA}$  also gives a maximum of 8% absolute.  $R_{WA}$  starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

AD5123:

$$R_{AW}(D) = \frac{128-D}{128} \times R_{AB} + R_W \quad \text{From } 0x00 \text{ to } 0x7F \quad (3)$$

AD5143:

$$R_{AW}(D) = \frac{256-D}{256} \times R_{AB} + R_W \quad \text{From } 0x00 \text{ to } 0xFF \quad (4)$$

where:

$D$  is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.

$R_{AB}$  is the end to end resistance.

$R_W$  is the wiper resistance.

If the device is configured in linear gain setting mode, the resistance between Terminal W and Terminal A is directly proportional

to the code loaded in the associate RDAC register. The general equations for this operation are

AD5123:

$$R_{AW}(D) = \frac{D}{128} \times R_{AB} + R_W \quad \text{From } 0x00 \text{ to } 0x7F \quad (5)$$

AD5123:

$$R_{AW}(D) = \frac{D}{256} \times R_{AB} + R_W \quad \text{From } 0x00 \text{ to } 0xFF \quad (6)$$

where:

$D$  is the decimal equivalent of the binary code in the 7-bit/8-bit RDAC register.

$R_{AB}$  is the end to end resistance.

$R_W$  is the wiper resistance.

In the bottom scale condition or top scale condition, a finite total wiper resistance of 40  $\Omega$  is present. Regardless of which setting the device is operating in, limit the current between Terminal A to Terminal B, Terminal W to Terminal A, and Terminal W to Terminal B, to the maximum continuous current of  $\pm 6$  mA or to the pulse current specified in Table 5. Otherwise, degradation or possible destruction of the internal switch contact can occur.

## PROGRAMMING THE POTENTIOMETER DIVIDER

## Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B, as shown in Figure 38.

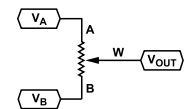


Figure 38. Potentiometer Mode Configuration

Connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 5 V. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B \quad (7)$$

where:

$R_{WB}(D)$  can be obtained from Equation 1 and Equation 2.

$R_{AW}(D)$  can be obtained from Equation 3 and Equation 4.

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors,  $R_{AW}$  and  $R_{WB}$ , and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/ $^{\circ}$ C.

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### TERMINAL VOLTAGE OPERATING RANGE

The AD5123/AD5143 are designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on Terminal A, Terminal B, or Terminal W that exceed  $V_{DD}$  are clamped by the forward-biased diode. There is no polarity constraint between  $V_A$ ,  $V_W$ , and  $V_B$ , but they cannot be higher than  $V_{DD}$  or lower than  $V_{SS}$ .

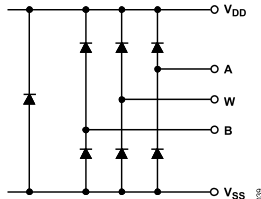


Figure 39. Maximum Terminal Voltages Set by  $V_{DD}$  and  $V_{SS}$

### POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 39), it is important to power up  $V_{DD}$  first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that  $V_{DD}$  is powered unintentionally. The ideal power-up sequence is  $V_{SS}$ ,  $V_{DD}$ , digital inputs, and  $V_A$ ,  $V_B$ , and  $V_W$ . The order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and digital inputs is not important as long as they are powered after  $V_{SS}$  and  $V_{DD}$ . Regardless of the power-up sequence and the ramp rates of the power supplies, once  $V_{DD}$  is powered, the power-on preset activates, which restores EEPROM values to the RDAC registers.

### LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use a compact, minimum lead length layout design. Ensure that the leads to the input are as direct as possible with a minimum conductor length. Ground paths must have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Apply low equivalent series resistance (ESR)  $1\ \mu\text{F}$  to  $10\ \mu\text{F}$  tantalum or electrolytic capacitors at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 40 illustrates the basic supply bypassing configuration for the AD5123/AD5143.

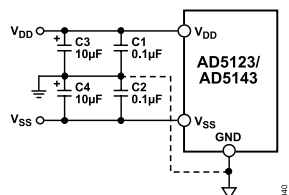


Figure 40. Power Supply Bypassing