64-Position OTP Digital Potentiometer

AD5171

FEATURES

64 position
One-time programmable (OTP) set-and-forget resistance setting—low cost alternative over EEMEM
Unlimited adjustments prior to OTP activation
5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ end-to-end resistance
Low temperature coefficient: 5 ppm/°C in potentiometer mode
Low temperature coefficient: 35 ppm/°C in rheostat mode
Compact standard 8-lead SOT-23 package
Low power: I_{DD} = 10 µA maximum
Fast settling time: t_S = 5 µs typical in power-up
I^{2}C-compatible digital interface
Computer software replaces microcontroller in factory programming applications
Full read/write of wiper register
Extra I^{2}C device address pin
Low operating voltage: 2.7 V to 5.5 V
OTP validation check function
Automotive temperature range: –40°C to +125°C

APPLICATIONS

System calibrations
Electronics level settings
Mechanical trimmers and potentiometer replacements
Automotive electronics adjustments
Gain control and offset adjustments
Transducer circuit adjustments
Programmable filters up to 1.5 MHz BW[1]

GENERAL DESCRIPTION

The AD5171 is a 64-position, one-time programmable (OTP) digital potentiometer[2] that uses fuse link technology to achieve the memory retention of the resistance setting function. OTP is a cost-effective alternative over the EEMEM approach for users who do not need to reprogram new memory settings in the digital potentiometer. This device performs the same electronic adjustment function as most mechanical trimmers and variable resistors. The AD5171 is programmed using a 2-wire, I^{2}C®-compatible digital control. It allows unlimited adjustments before permanently setting the resistance value. During the OTP activation, a permanent fuse blown command is sent after the final value is determined, freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer).

FUNCTIONAL BLOCK DIAGRAM

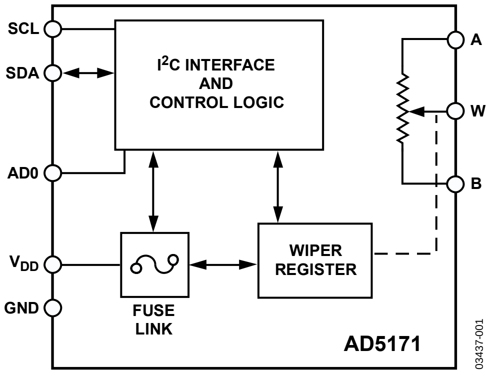

Figure 1.

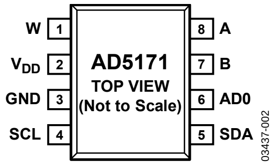

Figure 2. Pin Configuration

When this permanent setting is achieved, the value does not change regardless of supply variations or environmental stresses under normal operating conditions. To verify the success of permanent programming, Analog Devices, Inc., patterned the OTP validation such that the fuse status can be discerned from two validation bits in read mode.

For applications that program the AD5171 in factories, Analog Devices offers device programming software that operates across Windows® 95 to XP platforms, including Windows NT. This software application effectively replaces the need for external I^{2}C controllers or host processors and, therefore, significantly reduces the development time of the users.

An AD5171 evaluation kit includes the software, connector, and cable that can be converted for factory programming applications.

The AD5171 is available in a compact 8-lead SOT-23 package. All parts are guaranteed to operate over the automotive temperature range of –40°C to +125°C. Besides its unique OTP feature, the AD5171 lends itself well to other general-purpose digital potentiometer applications due to its temperature performance, small form factor, and low cost.

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[1] Applies to 5 kΩ parts only.
[2] The terms digital potentiometer and RDAC are used interchangeably.

Rev. D

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS: 5 kΩ, 10 kΩ, 50 kΩ, AND 100 kΩ

V_{DD} = 3 V to 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect, R_{AB} = 10 kΩ, 50 kΩ, and 100 kΩ	−0.5	±0.1	+0.5	LSB
		R_{WB}, V_A = no connect, R_{AB} = 5 kΩ	−1	±0.25	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect, R_{AB} = 10 kΩ, 50 kΩ, and 100 kΩ	−1.5	±0.35	+1.5	LSB
		R_{WB}, V_A = no connect, R_{AB} = 5 kΩ	−1.5	±0.5	+1.5	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$		−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		60	115	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE (SPECIFICATIONS APPLY TO ALL RDACs)						
Resolution	N				6	Bits
Differential Nonlinearity[4]	DNL		−0.5	±0.1	+0.5	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x20		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x3F, R_{AB} = 10 kΩ, 50 kΩ, and 100 kΩ	−1	−0.5	0	LSB
Full-Scale Error	V_{WFSE}	Code = 0x3F, R_{AB} = 5 kΩ	−1.5		0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00, R_{AB} =10 kΩ, 50 kΩ, and 100 kΩ	0	0.5	1	LSB
		Code = 0x00, R_{AB} = 5 kΩ	0		2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W	With respect to GND			V_{DD}	V
Capacitance A, B[6]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x20		25		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x20		55		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS						
Input Logic High (SDA and SCL)[7]	V_{IH}		0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)[7]	V_{IL}		−0.5		+0.3 V_{DD}	V
Input Logic High (AD0)	V_{IH}	V_{DD} = 3 V	3.0		V_{DD}	V
Input Logic Low (AD0)	V_{IL}	V_{DD} = 3 V	0		1.0	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[8]	C_{IL}			3		pF
DIGITAL OUTPUTS						
Output Logic Low (SDA)	V_{OL}	I_{OL} = 6 mA			0.4	V
Three-State Leakage Current (SDA)	I_{OZ}	V_{IN} = 0 V or 5 V			±1	µA
Output Capacitance[8]	C_{OZ}			3		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply[7, 9]	V_{DD_OTP}	T_A = 25°C	4.75	5	5.25	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		4	10	µA
OTP Supply Current[7, 10, 11]	I_{DD_OTP}	V_{DD_OTP} = 5 V, T_A = 25°C		100		mA
Power Dissipation[12]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.02	0.055	mW
Power Supply Sensitivity	PSSR		−0.025	+0.001	+0.025	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[8, 13, 14]						
–3 dB Bandwidth	BW_5k	R_{AB} = 5 kΩ, code = 0x20		1500		kHz
	BW_10k	R_{AB} = 10 kΩ, code = 0x20		600		kHz
	BW_50k	R_{AB} = 50 kΩ, code = 0x20		110		kHz
	BW_100k	R_{AB} = 100 kΩ, code = 0x20		60		kHz
Total Harmonic Distortion	THD	V_A = 1 V rms, R_{AB} = 10 kΩ, V_B = 0 V dc, f = 1 kHz		0.05		%
Adjustment Settling Time	t_{S1}	V_A = 5 V ± 1 LSB error band, V_B = 0 V, measured at V_W		5		μs
Power-Up Settling Time After Fuses Blown	t_{S2}	V_A = 5 V ±1 LSB error band, V_B = 0 V, measured at V_W		5		μs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 5 kΩ, f = 1 kHz, code = 0x20		8		nV/√Hz
		R_{AB} = 10 kΩ, f = 1 kHz, code = 0x20		12		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.

[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

[3] V_{AB} = V_{DD}, Wiper (V_W) = no connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[5] The A, B, and W resistor terminals have no limitations on polarity with respect to each other.

[6] Guaranteed by design; not subject to production test.

[7] The minimum voltage requirement on the V_{IH} is 0.7 V × V_{DD}. For example, V_{IH} minimum = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

[8] Guaranteed by design; not subject to production test.

[9] Different from operating power supply; power supply for OTP is used one time only.

[10] Different from operating current; supply current for OTP lasts approximately 400 ms for one-time need only.

[11] See Figure 24 for the energy plot during the OTP program.

[12] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[13] Bandwidth, noise, and settling time depend on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

[14] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS: 5 kΩ, 10 kΩ, 50 kΩ, AND 100 kΩ

V_{DD} = 3 V to 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS (APPLY TO ALL PARTS[2, 3])						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time Between Start and Stop	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Start Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL Signals	t_9				0.3	µs
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs
OTP Program Time	t_{11}			400		ms

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design; not subject to production test.
[3] All dynamic characteristics use V_{DD} = 5 V.

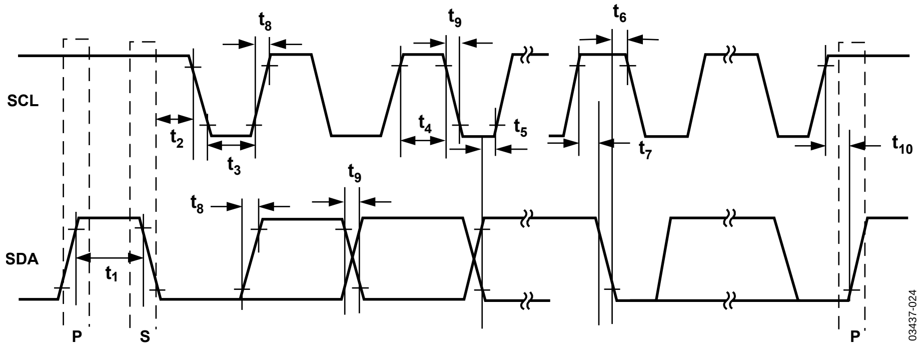


Figure 3. Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, and V_W to GND	GND to V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous ($R_{WB} \leq 1$ kΩ, A Open)[1]	±5 mA
I_{WA} Continuous ($R_{WA} \leq 1$ kΩ, B Open)[1]	±5 mA
Digital Inputs and Output Voltage to GND	0 V to V_{DD}
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance θ_{JA}[2]	230°C/W

[1] Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance; the maximum current handling of the switches, and the maximum power dissipation of the package. $V_{DD} = 5$ V.

[2] Package power dissipation = (T_J max – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

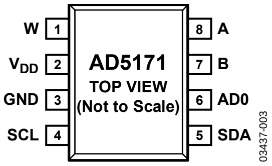


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	W	Wiper Terminal W. GND ≤ V_W ≤ V_{DD}.
2	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be within the 4.75 V and 5.25 V range and capable of driving 100 mA.
3	GND	Common Ground.
4	SCL	Serial Clock Input. Requires a pull-up resistor. If it is driven direct from a logic controller without the pull-up resistor, ensure that the V_{IH} minimum is 0.7 V × V_{DD}.
5	SDA	Serial Data Input/Output. Requires a pull-up resistor. If it is driven direct from a logic controller without a pull-up resistor, ensure that the V_{IH} minimum is 0.7 V × V_{DD}.
6	AD0	I^2C Device Address Bit. Allows a maximum of two AD5171s to be addressed.
7	B	Resistor Terminal B. GND ≤ V_B ≤ V_{DD}.
8	A	Resistor Terminal A. GND ≤ V_A ≤ V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

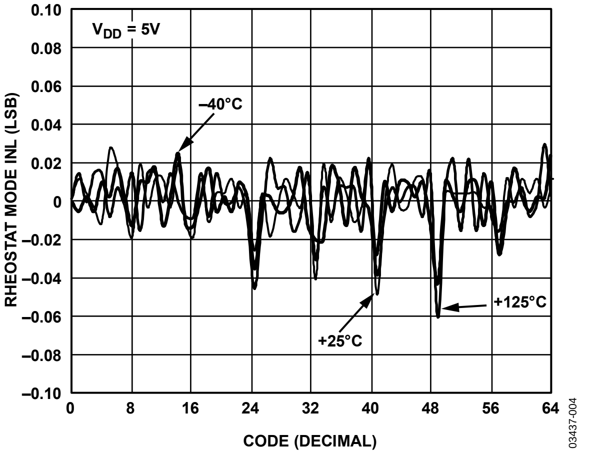


Figure 5. R-INL vs. Code vs. Temperature

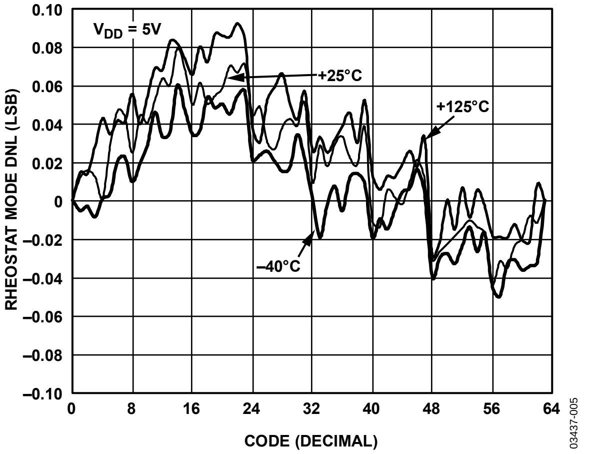


Figure 6. R-DNL vs. Code vs. Temperature

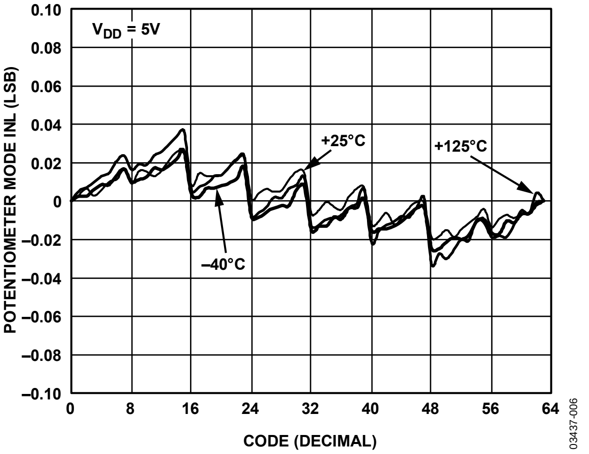


Figure 7. INL vs. Code vs. Temperature

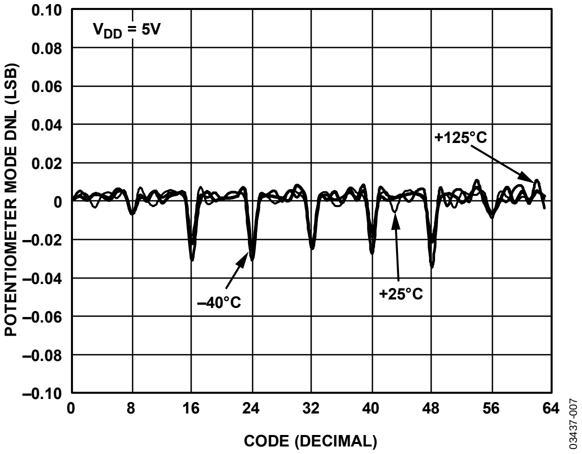


Figure 8. DNL vs. Code vs. Temperature

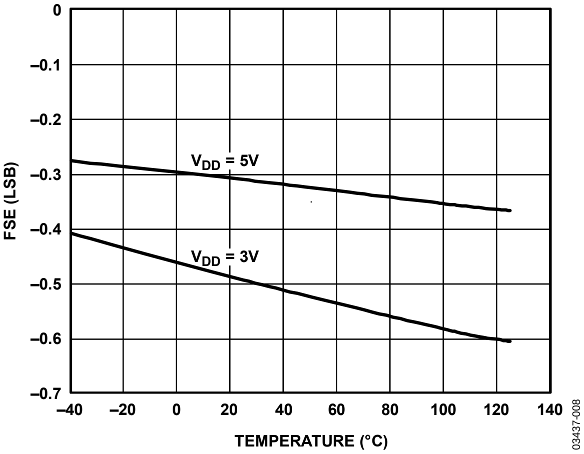


Figure 9. Full-Scale Error (FSE) vs. Temperature

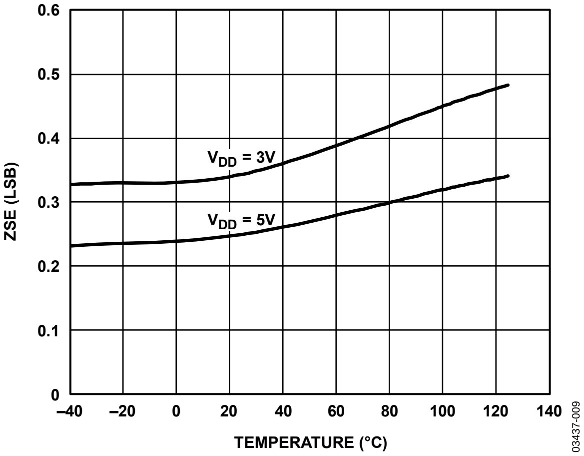


Figure 10. Zero-Scale Error (ZSE) vs. Temperature

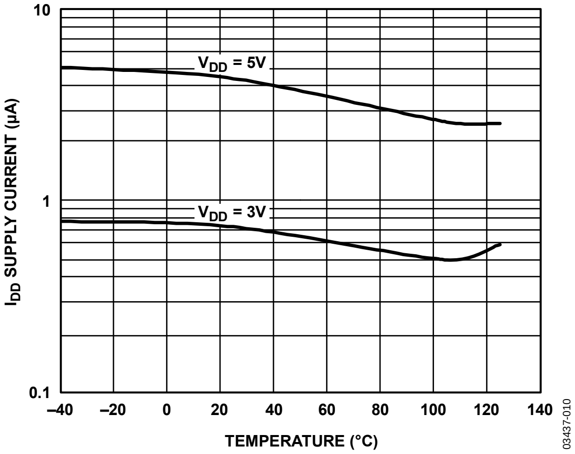


Figure 11. I_{DD} Supply Current vs. Temperature

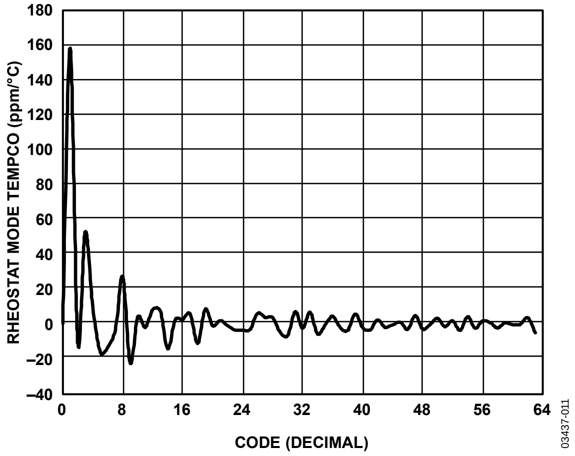


Figure 12. Rheostat Mode Tempco ($\Delta R_{AB}/R_{AB}$)/ΔT vs. Code

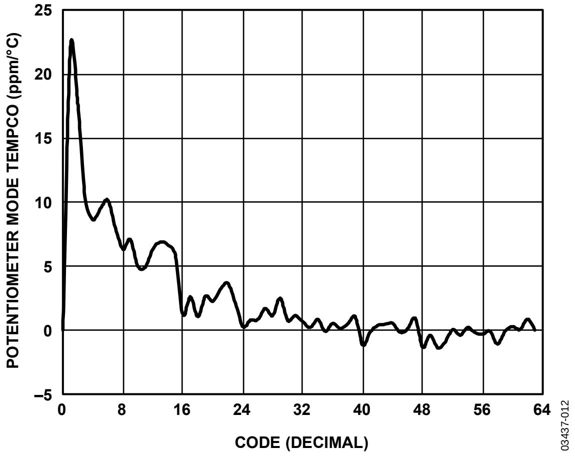


Figure 13. Potentiometer Mode Tempco ($\Delta V_W/V_W$)/ΔT vs. Code

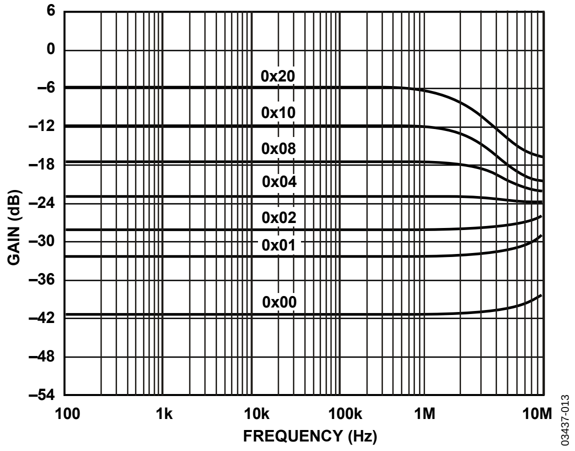


Figure 14. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

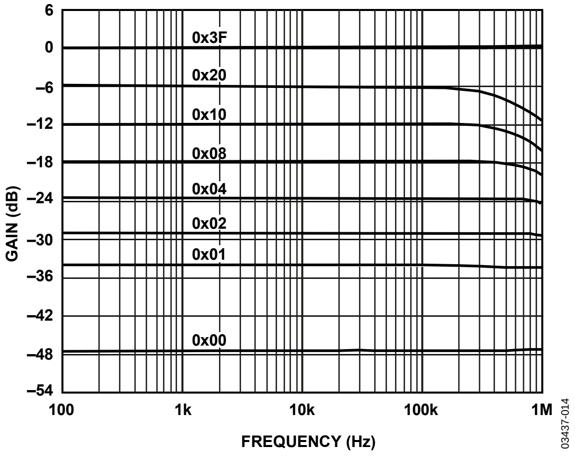


Figure 15. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

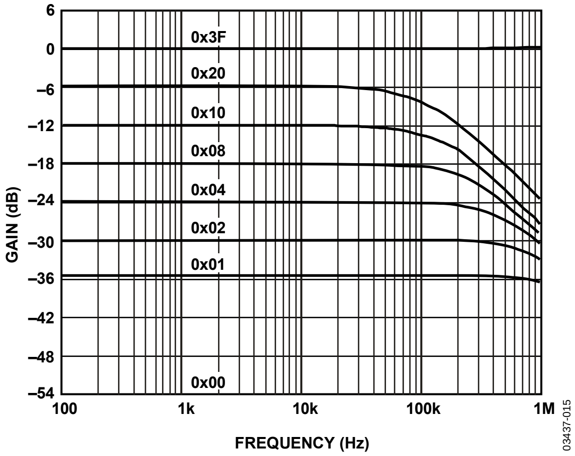


Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 50 Ω

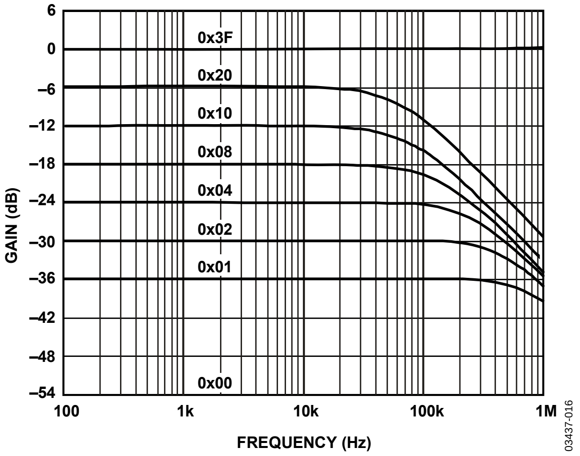


Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

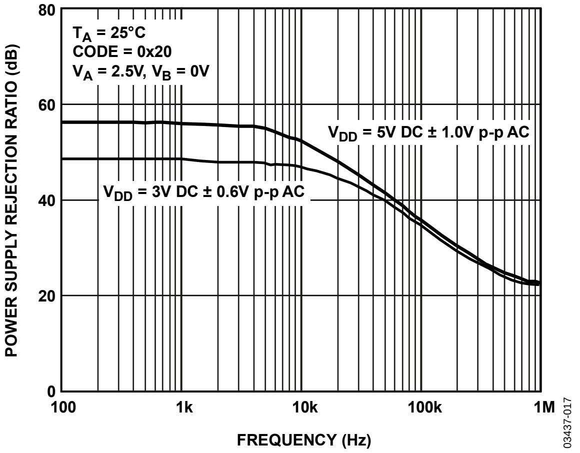


Figure 18. Power Supply Rejection Ratio vs. Frequency

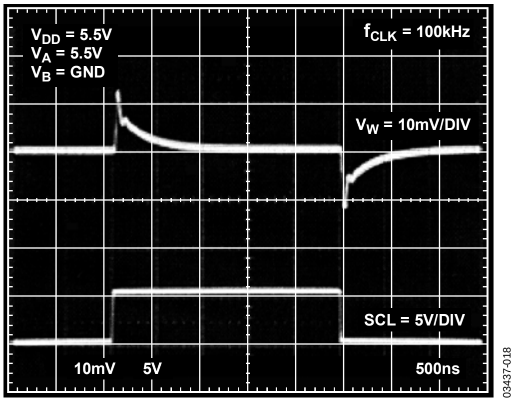


Figure 19. Digital Feedthrough vs. Time

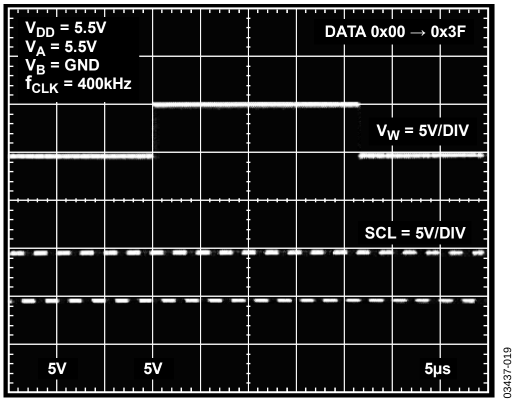


Figure 20. Settling Time

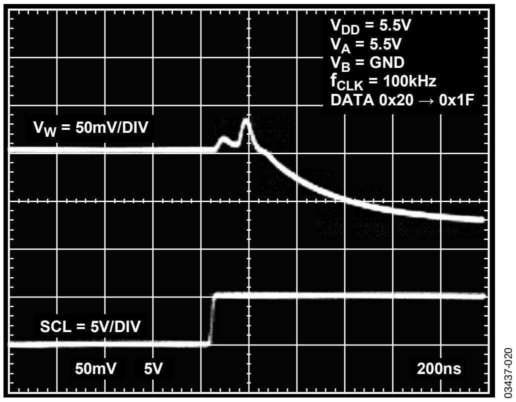


Figure 21. Midscale Glitch Energy

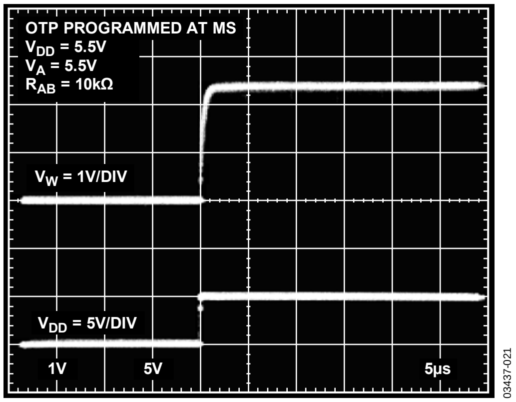


Figure 22. Power-Up Settling Time After Fuses Blown

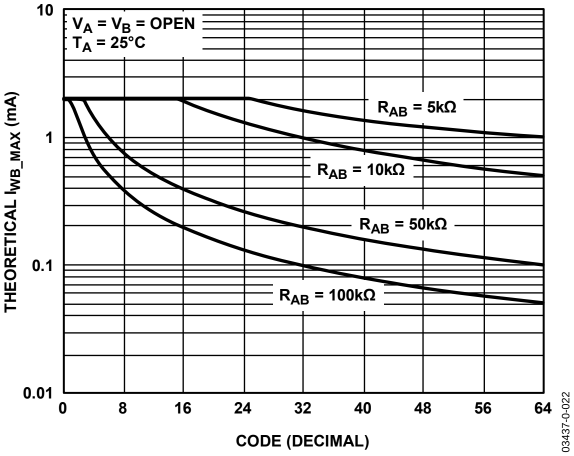


Figure 23. Theoretical I_{WB_MAX} vs. Code

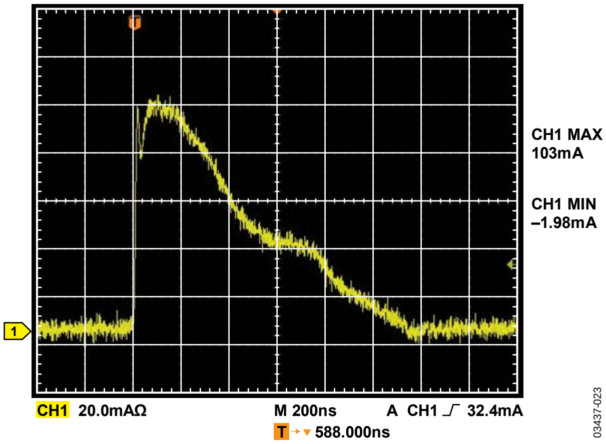


Figure 24. OTP Program Energy Plot for Single Fuse

THEORY OF OPERATION

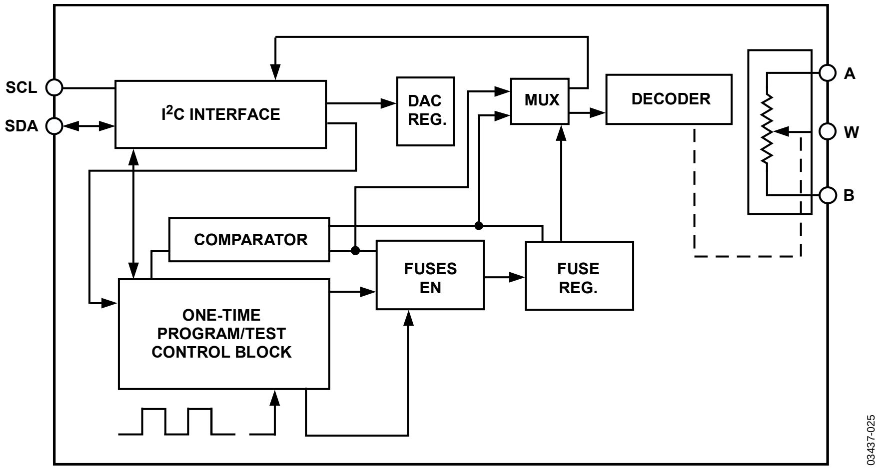


Figure 25. Detailed Functional Block Diagram

The AD5171 allows unlimited 6-bit adjustments, except for the one-time programmable, set-and-forget resistance setting. OTP technology is a proven, cost-effective alternative over EEMEM in one-time memory programming applications. The AD5171 employs fuse link technology to achieve the memory retention of the resistance setting function. It has six data fuses that control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are blown.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5171 presets to midscale during initial power-on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit high along with the proper coding (see Table 8 and Table 9) and one-time V_{DD_OTP}. The fuse link technology of the AD517x family of digital potentiometers requires V_{DD_OTP} between 4.75 V and 5.25 V to blow the fuses to achieve a given nonvolatile setting. On the other hand, V_{DD} can be 2.7 V to 5.5 V during operation. As a result, a system supply that is lower than 4.75 V requires external supply for OTP. In addition, the user is only allowed one attempt in blowing the fuses. If the user fails to blow the fuses at the first attempt, the fuse structures may change so that they may never be blown regardless of the energy applied at subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back to check the programming status (see Table 5). Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses are blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting.

Table 5. Validation Status

E1	E0	Status
0	0	Ready for programming.
0	1	Test fuse not blown successfully. For factory setup checking purpose only. Users should not see these combinations.
1	0	Fatal error. Some fuses are not blown. Do not retry. Discard the unit.
1	1	Successful. No further programming is possible.

This section discusses the fuse operation in detail. When the OTP T bit is set, the internal clock is enabled. The program then attempts to blow a test fuse. The operation stops if the test fuse is not properly blown. The validation bits, E1 and E0, show 01. This status is intended for factory setup checking purposes only; users should not see this status. If the test fuse is properly blown, the data fuses can be programmed. The six data fuses are programmed in six clock cycles. The output of the fuses is compared with the code stored in the RDAC register. If they do not match, E1 and E0 of 10 are issued as fatal errors and the operation stops. Users should never try blowing the fuses more than once because the fuse structure may have changed prohibiting further programming. As a result, the unit must be discarded. This error status can also occur if the OTP supply voltage goes above or drops below the V_{DD_OTP} requirement, the OTP supply current is limited, or both the voltage and current ramp times are slow. If the output and stored code match, the programming lock fuse is blown so that no further programming is possible. In the meantime, E1 and E0 issue 11, indicating the lock fuse is properly blown. All the fuse latches are enabled at power-on; therefore, from this point on, the output corresponds to the stored setting. Figure 25 shows a detailed functional block diagram.

VARIABLE RESISTANCE AND VOLTAGE FOR RHEOSTAT MODE

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused terminal can be opened or shorted with Terminal W. This operation is called rheostat mode (see Figure 26).

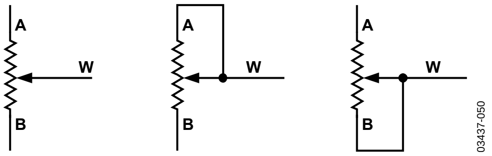


Figure 26. Rheostat Mode Configuration

The nominal resistance (R_{AB}) of the RDAC has 64 contact points accessed by the wiper terminal, plus Terminal B contact if R_{WB} is considered. The 6-bit data in the RDAC latch is decoded to select one of the 64 settings. Assuming that a 10 kΩ part is used, the first connection of the wiper starts at Terminal B for Data 0x00. Such a connection yields a minimum of 60 Ω resistance between Terminal W and Terminal B due to the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 219 Ω ($R_{WB} = 1 \times R_{AB}/63 + R_W$) for Data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,060 Ω ($63 \times R_{AB}/63 + R_W$). Figure 27 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining R_{WB} is

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \tag{1}$$

where:

D is the decimal equivalent of the 6-bit binary code.

R_{AB} is the end-to-end resistance.

R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Table 6. R_{WB} vs. Codes: R_{AB} = 10 kΩ; Terminal A Open

D (Dec)	R_{WB} (Ω)	Output State
63	10060	Full-scale (R_{AB} + R_W)
32	5139	Midscale
1	219	1 LSB
0	60	Zero-scale (wiper contact resistance)

Because a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between Terminal W and Terminal B in this state to a maximum pulse current 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper (Terminal W) and Terminal A also produces a complementary resistance, R_{WA}. When these terminals are used, Terminal B can be opened or shorted to Terminal W. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{63 - D}{63} \times R_{AB} + R_W \tag{2}$$

Table 7. R_{WA} vs. Codes: R_{AB} = 10 kΩ; Terminal B Open

D (Dec)	R_{WA} (Ω)	Output State
63	60	Full-scale
32	4980	Midscale
1	9901	1 LSB
0	10060	Zero-scale

The typical distribution of the resistance tolerance from device to device is process-lot dependent; it is possible to have ±30% tolerance.

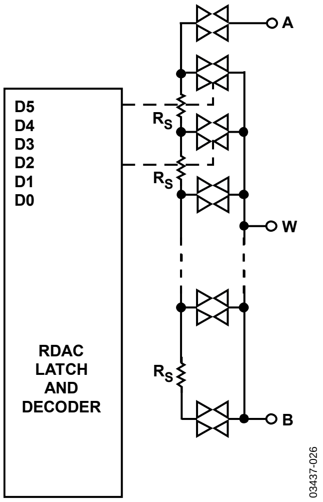


Figure 27. AD5171 Equivalent RDAC Circuit

VARIABLE RESISTANCE AND VOLTAGE FOR POTENTIOMETER MODE

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (see Figure 28).

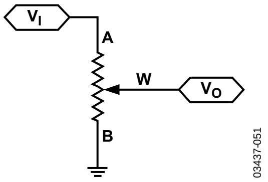


Figure 28. Potentiometer Mode Configuration

Ignoring the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{63} V_A \tag{3}$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{\frac{D}{63} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \tag{4}$$

Unlike in rheostat mode where the absolute tolerance is high, potentiometer mode yields an almost ratiometric function of D/63 with a relatively small error contributed by the R_W terms; thus, the tolerance effect is almost cancelled. Although the thin film step resistor (R_S) and CMOS switches resistance (R_W) have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode includes other operations such as op amp input, feedback resistor networks, and voltage scaling applications. Terminal A, Terminal W, and Terminal B can, in fact, be input or output terminals provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} to GND.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the OTP and normal operating voltage supplies share the same V_{DD} terminal of the AD5171. The AD5171 employs fuse link technology that requires 4.75 V to 5.25 V for blowing the internal fuses to achieve a given setting, but normal V_{DD} can be anywhere between 2.7 V and 5.5 V after the fuse programming process. As a result, dual voltage supplies and isolation are needed if system V_{DD} is lower than the required V_{DD_OTP}. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 4.75 V to 5.25 V and able to provide a 100 mA current for 400 ms for successful one-time programming. Once fuse programming is complete, the V_{DD_OTP} supply must be removed to allow normal operation at 2.7 V to 5.5 V; the device then consumes current in the μA range.

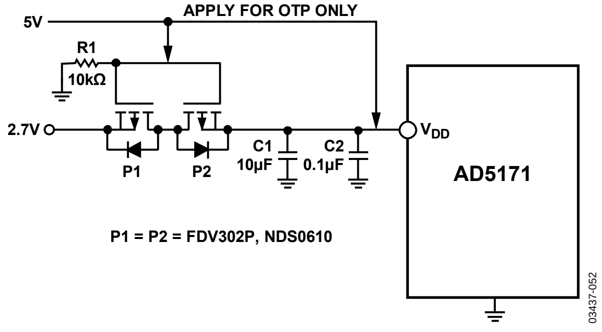


Figure 29. 5 V OTP Supply Isolated from the 2.7 V Normal Operating Supply; the V_{DD_OTP} supply must be removed once OTP is complete.

When operating at 2.7 V, use of the bidirectional low threshold P-Ch MOSFETs is recommended for the isolation of the supply. As shown in Figure 29, this assumes that the 2.7 V system voltage is applied first, and the P1 and P2 gates are pulled to ground, thus turning on P1 and, subsequently, P2. As a result, V_{DD} of the AD5171 approaches 2.7 V. When the AD5171 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFETs gates, thus turning off P1 and P2. The OTP command should be executed at this time to program the AD5171 while the 2.7 V source is protected. Once the fuse programming is complete, the tester withdraws the V_{DD_OTP} and the setting of the AD5171 is permanently fixed.

The AD5171 achieves the OTP function through blowing internal fuses. Users should always apply the 4.75 V to 5.25 V one-time program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement may lead to a change in the fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between 0.7 V × V_{DD} and V_{DD}. Refer to the Level Shifting for Different Voltage Operation section.

Poor PCB layout introduces parasitics that may affect the fuse programming. Therefore, it is recommended that a 10 μF tantalum capacitor be added in parallel with a 1 nF ceramic capacitor as close as possible to the V_{DD} pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides both a fast response and larger supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, while C2 reduces high frequency noise during normal operation.

ESD PROTECTION

Digital inputs SDA and SCL are protected with a series input resistor and parallel Zener ESD structures (see Figure 30).

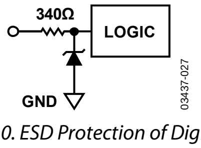


Figure 30. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

There are also ESD protection diodes between V_{DD} and the RDAC terminals; therefore, the V_{DD} of the AD5171 defines their voltage boundary conditions (see Figure 31). Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} are clamped by the internal forward-biased diodes and should be avoided.

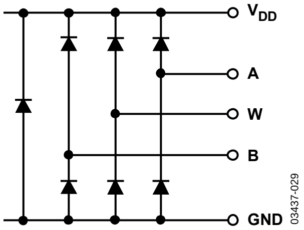


Figure 31. Maximum Terminal Voltages Set by V_{DD}

POWER-UP/POWER-DOWN SEQUENCES

Similarly, because of the ESD protection diodes, it is important to power V_{DD} first before applying any voltages to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and can affect the remainder of the users' circuits. The ideal power-up sequence is the following order: GND, V_{DD}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}. Similarly, V_{DD} should be powered down last.

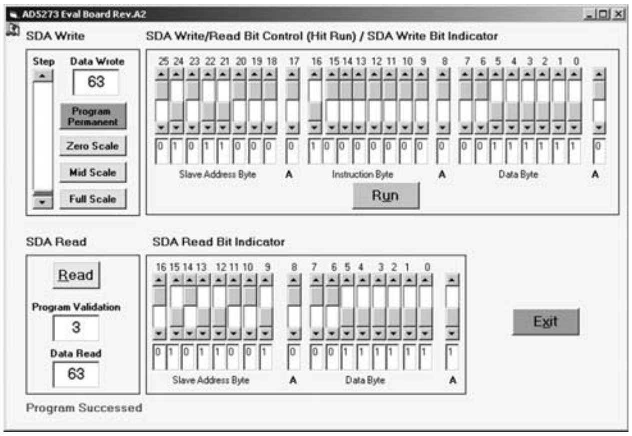
CONTROLLING THE AD5171

There are two ways of controlling the AD5171. Users can either program the devices with computer software or employ external I^{2}C controllers.

SOFTWARE PROGRAMMING

Due to the advantage of the one-time programmable feature, users may consider programming the device in the factory before shipping it to the end users. Analog Devices offers device programming software that can be implemented in the factory on PCs running Windows 95 to Windows XP platforms. As a result, external controllers are not required, which significantly reduces development time.

The program is an executable file that does not require the user to know any programming languages or programming skills. It is easy to set up and use. Figure 32 shows the software interface. The software can be downloaded from the AD5171 product page.



Data Wrote: 63

Program Validation: 3

Data Read: 63

Program Successed

Figure 32. Software Interface

Write

The AD5171 starts at midscale after power-up prior to the OTP programming. To increment or decrement the resistance, move the scrollbar on the left. To write any specific values, use the bit pattern control in the upper screen and click **Run**. The format of writing data to the device is shown in Table 8. Once the desired setting is found, click **Program Permanent** to blow the internal fuse links for permanent setting. The user can also set the programming bit pattern in the upper screen and click **Run** to achieve the same result.

Read

To read the validation bits and data from the device, click **Read**. The user may also set the bit pattern in the upper screen and click **Run**. The format of reading data out from the device is shown in Table 9.

DEVICE PROGRAMMING

To apply the device programming software in the factory, users need to modify a parallel port cable and configure Pin 2, Pin 3, Pin 15, and Pin 25 for SDA_write, SCL, SDA_read, and DGND, respectively, for the control signals (see Figure 33). In addition, lay out the PCB of the AD5171 with SCL and SDA pads, as shown in Figure 34, such that pogo pins can be inserted for the factory programming.

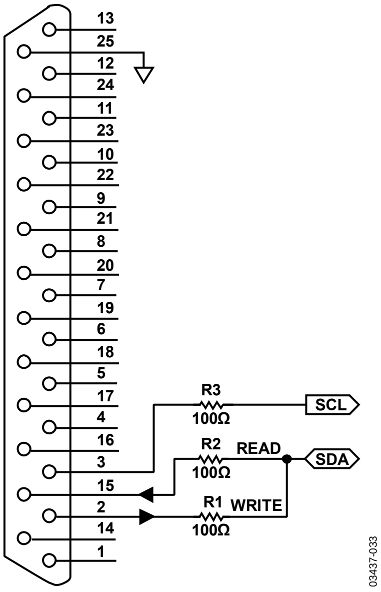


Figure 33. Parallel Port Connection: Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND

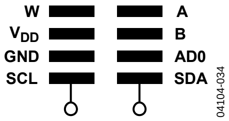


Figure 34. Recommended AD5171 PCB Layout

Table 8. SDA Write Mode Bit Format

S	0	1	0	1	1	0	AD0	0	A	T	X	X	X	X	X	X	X	A	X	X	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 9. SDA Read Mode Bit Format

S	0	1	0	1	1	0	AD0	1	A	E1	E0	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

Table 10. SDA Bits Definitions and Descriptions

Bit	Description
S	Start Condition.
P	Stop Condition.
A	Acknowledge.
AD0	I²C Device Address Bit. Allows a maximum of two AD5171s to be addressed.
X	Don't Care.
T	OTP Programming Bit. Logic 1 programs the wiper position permanently.
D5, D4, D3, D2, D1, D0	Data Bits.
E1, E0	OTP Validation Bits: 0, 0 = Ready to Program. 0, 1 = Test Fuse Not Blown Successfully. For factory setup checking purpose only. Users should not see these combinations. 1, 0 = Fatal Error. Do not retry. Discard the unit. 1, 1 = Programmed Successfully. No further adjustments are possible.

I²C CONTROLLER PROGRAMMING

Write Bit Patterns

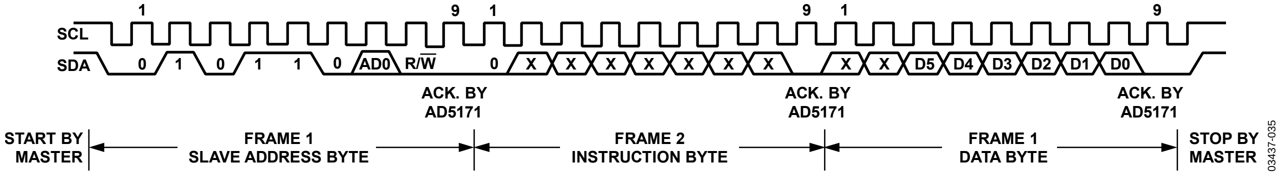


Figure 35. Writing to the RDAC Register

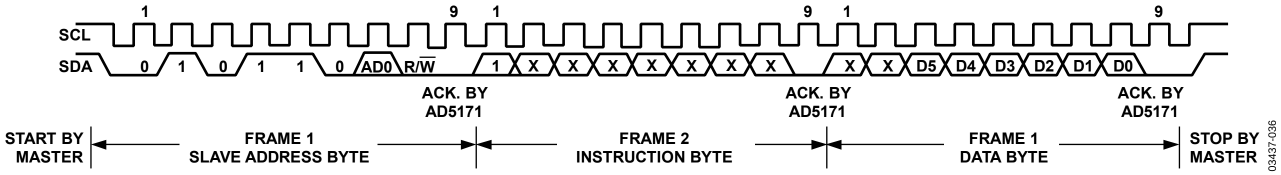


Figure 36. Activating One-Time Programming

Read Bit Pattern

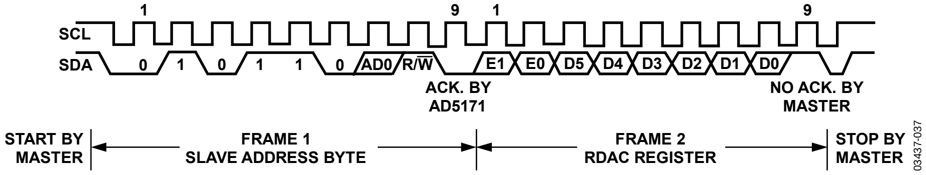


Figure 37. Reading Data from RDAC Register

I²C-COMPATIBLE 2-WIRE SERIAL BUS

For users who prefer to use external controllers, the AD5171 can be controlled via an I²C-compatible serial bus; the part is connected to this bus as a slave device. The following section describes how the 2-wire I²C serial bus protocol operates (see Figure 35, Figure 36, and Figure 37).

The master initiates data transfer by establishing a start condition, which is when SDA goes from high to low while SCL is high (see Figure 35 and Figure 36). The following byte is the slave address byte, which consists of the 6 MSBs as a slave address defined as 010110. The next bit is AD0, which is an I²C device address bit. Depending on the states of their AD0 bits, two AD5171s can be addressed on the same bus (see Figure 38). The last LSB is the R/W̄ bit, which determines whether data is read from, or written to, the slave device.

The slave address corresponding to the transmitted address bit responds by pulling the SDA line low during the 9th clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register.

The write operation contains one instruction byte more than the read operation. The instruction byte in the write mode follows the slave address byte. The MSB of the instruction byte labeled T is the one-time programming bit. After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 35).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (note the slight difference from the write mode; there are eight data bits followed by a no acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 37).

When all data bits are read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In the write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 35 and Figure 36). In the read mode, the master issues a no acknowledge for the 9th clock pulse, that is, the SDA line remains high. The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 37).

A repeated write function gives the user flexibility to update the RDAC output a number of times, except after permanent programming, addressing, and instructing the part only once. During the write cycle, each data byte updates the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output updates after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte updates the output of the selected slave device. If different instructions are needed, the write mode has to be started with a new slave address, instruction, and data bytes. Similarly, a repeated read function of the RDAC is also allowed.

CONTROLLING TWO DEVICES ON ONE BUS

Figure 38 shows two AD5171 devices on the same serial bus. Each has a different slave address because the state of each AD0 pin is different, which allows each device to be independently operated. The master device output bus line drivers are open-drain pull-downs in a fully I^{2}C-compatible interface.

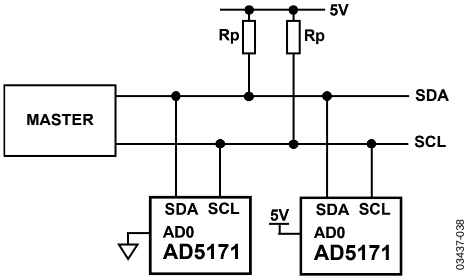


Figure 38. Two AD5171 Devices on One Bus

APPLICATIONS INFORMATION

DAC

It is common to buffer the output of the digital potentiometer as a DAC unless the load is much larger than R_{WB}. The buffer can impede conversion and deliver higher current, if needed.

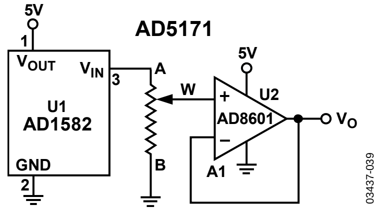


Figure 39. Programmable Voltage Reference (DAC)

GAIN CONTROL COMPENSATION

The digital potentiometers are commonly used in gain controls or sensor transimpedance amplifier signal conditioning applications (see Figure 40). To avoid gain peaking, or in worst-case oscillation due to step response, a compensation capacitor is needed. In general, C2 in the range of a few picofarads to a few tenths of a picofarad is adequate for the compensation.

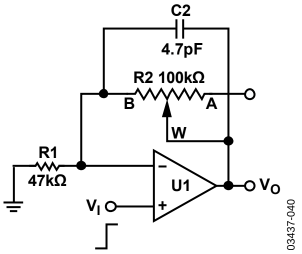


Figure 40. Typical Noninverting Gain Amplifier

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 41).

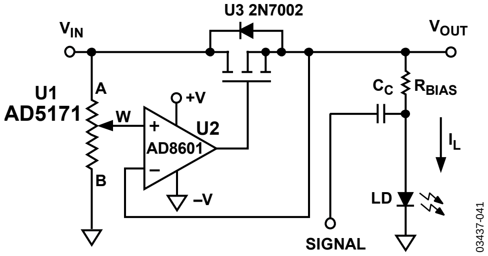


Figure 41. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N_1. N_1 power handling must be adequate to dissipate $(V_I - V_O) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference, such as the ADR421, ADR03, or ADR370, can be applied at Terminal A of the digital potentiometer.

LEVEL SHIFTING FOR DIFFERENT VOLTAGE OPERATION

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum V_{IH} level (0.7 V × V_{DD}), level shift the signals for read/write communications between the AD5171 and the controller. Figure 42 shows one of the implementations. For example, when SDA1 is at 2.5 V, M1 turns off, and SDA2 becomes 5 V. When SDA1 is at 0 V, M1 turns on, and SDA2 approaches 0 V. As a result, proper level shifting is established. M1 and M2 should be low threshold N-Ch power MOSFETs, such as FDV301N.

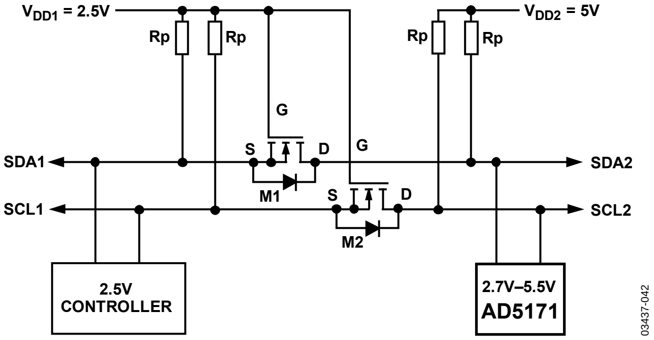


Figure 42. Level Shifting for Different Voltage Operation

RESISTANCE SCALING

The AD5171 offers 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ nominal resistances. For users who need to optimize the resolution with an arbitrary full range resistance, the following techniques can be used. By paralleling a discrete resistor, a proportionately lower voltage appears at Terminal A to Terminal B, which is applicable only to the voltage divider mode (see Figure 43).

This translates into a finer degree of precision because the step size at Terminal W is smaller. The voltage can be found as

$$V_W(D) = \frac{(R_{AB} \,||\, R2)}{R3 + R_{AB} \,||\, R2} \times \frac{D}{64} \times V_{DD} \qquad (5)$$

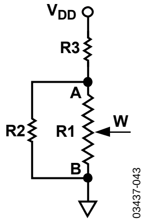


Figure 43. Lowering the Nominal Resistance

For log taper adjustment, such as volume control, Figure 44 shows another way of resistance scaling. In this circuit, the smaller the R2 with respect to R_{AB}, the more it behaves like the pseudo log taper characteristic. The wiper voltage is simply

$$V_W(D) = \frac{(R_{WB} \,||\, R2)}{R_{WA} + R_{WB} \,||\, R2} \times V_I \tag{6}$$

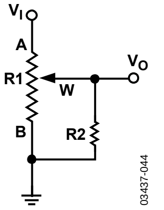


Figure 44. Resistor Scaling with Log Adjustment Characteristics

RESOLUTION ENHANCEMENT

The resolution can be doubled in the potentiometer mode of operation by using three digital potentiometers. Borrowed from the Analog Devices patented RDAC segmentation technique, users can configure three AD5171s to double the resolution (see Figure 45). First, U3 must be parallel with a discrete resistor, R_P, which is chosen to be equal to a step resistance ($R_P = R_{AB}/64$). Adjusting U1 and U2 together forms the coarse 6-bit adjustment, and adjusting U3 alone forms the finer 6-bit adjustment. As a result, the effective resolution becomes 12-bit.

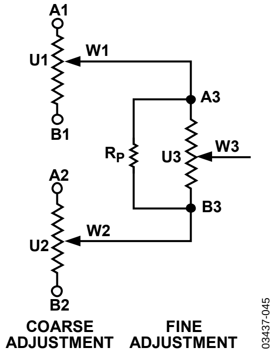


Figure 45. Doubling the Resolution

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentiometers. Configured as a potentiometer divider, the −3 dB bandwidth of the AD5171 (5 kΩ resistor) measures 1.5 MHz at half scale. Figure 14 to Figure 17 provide the large signal BODE plot characteristics of the four available resistor versions: 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. A parasitic simulation model is shown in Figure 46. Listing 1 provides a macro model net list for the 10 kΩ device.

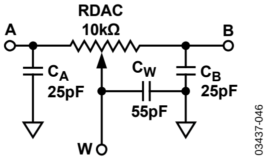


Figure 46. Circuit Simulation Model for RDAC = 10 kΩ

Listing 1. Macro Model Net List for RDAC

```
.PARAM D=64, RDAC=10E3

*

.SUBCKT DPOT (A,W,B)
*
CA     A     0     25E-12
RWA    A     W     {(1-D/64)*RDAC+60}
CW     W     0     55E-12
RWB    W     B     {D/64*RDAC+60}
CB     B     0     25E-12

*

.ENDS DPOT
```

EVALUATION BOARD

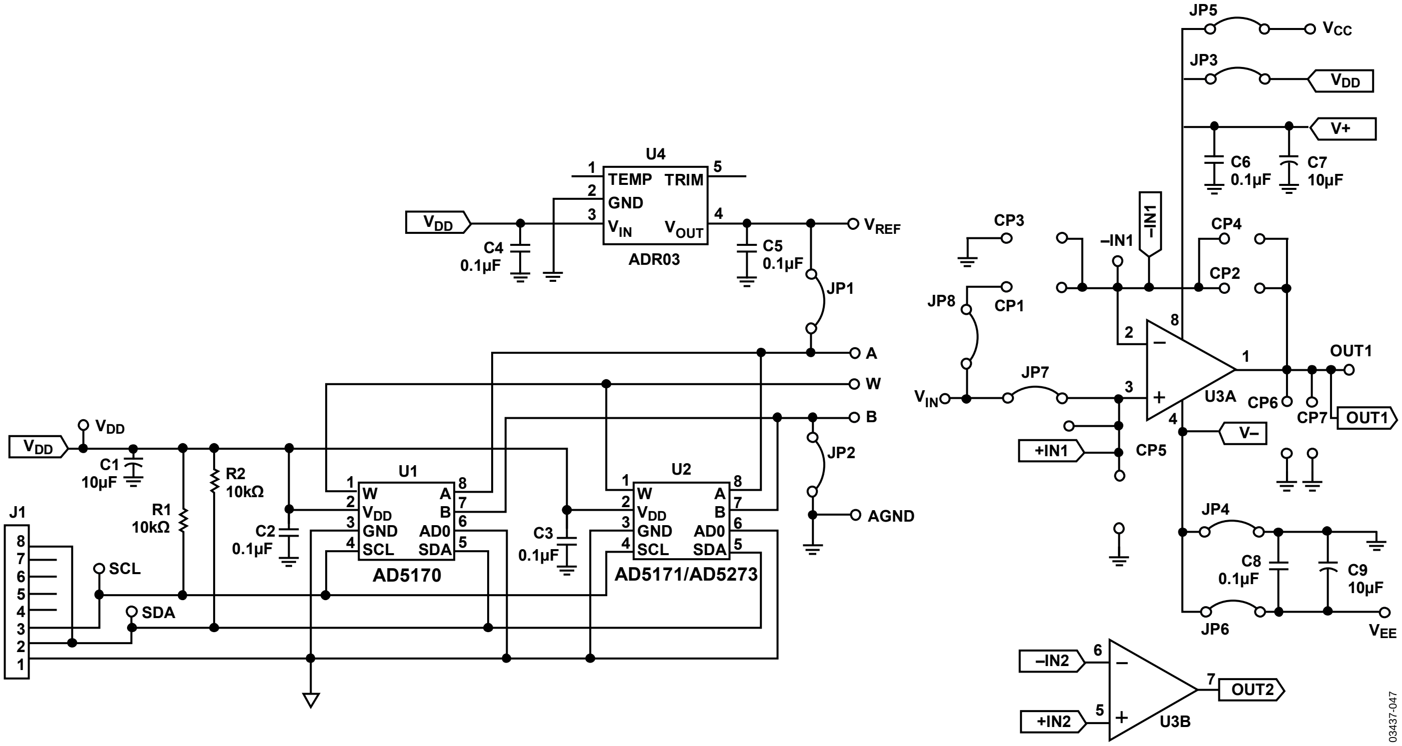


Figure 47. Evaluation Board Schematic

The AD5171 evaluation board comes with a dual op amp AD822 and a 2.5 V reference ADR03. Users can configure many building block circuits with minimal components needed. Figure 48 shows one of the examples. There is space available on the board where users can build additional circuits for further evaluations as shown in Figure 49.

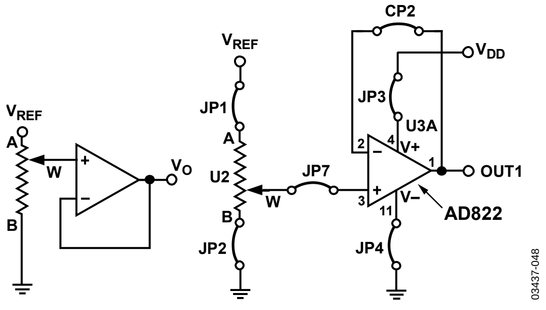


Figure 48. Programmable Voltage Reference

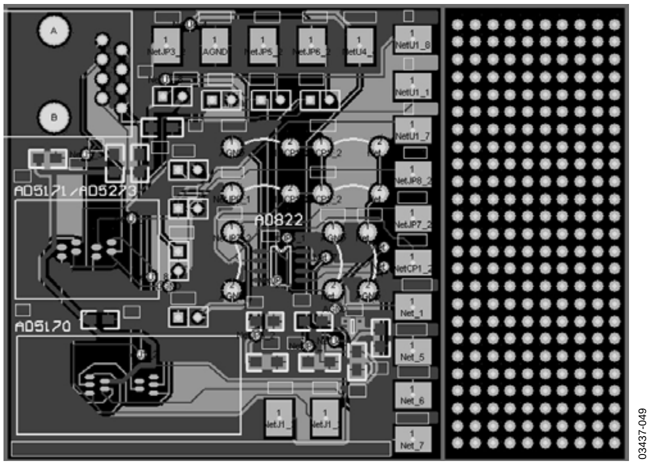
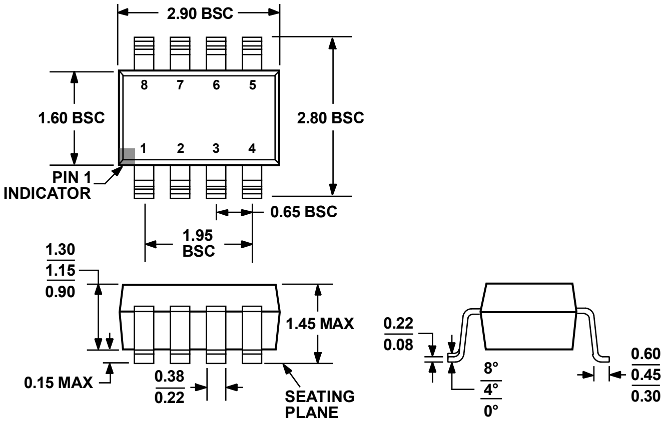


Figure 49. Evaluation Board

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 50. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD5171BRJ5-R2	5	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D12
AD5171BRJ5-RL7	5	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D12
AD5171BRJZ5-R2[2]	5	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D12#
AD5171BRJZ5-R7[2]	5	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D12#
AD5171BRJ10-R2	10	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D13
AD5171BRJ10-RL7	10	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D13
AD5171BRJZ10-R2[2]	10	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D13#
AD5171BRJZ10-R7[2]	10	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D13#
AD5171BRJ50-R2	50	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D14
AD5171BRJ50-RL7	50	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D14
AD5171BRJZ50-R2[2]	50	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D14#
AD5171BRJZ50-R7[2]	50	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D14#
AD5171BRJ100-R2	100	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D15
AD5171BRJ100-RL7	100	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D15
AD5171BRJZ100-R2[2]	100	−40°C to +125°C	8-Lead SOT-23	RJ-8	250	D15#
AD5171BRJZ100-R7[2]	100	−40°C to +125°C	8-Lead SOT-23	RJ-8	3000	D15#
AD5171EVAL[3]	10		Evaluation Board		1	

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[1] Parts have a YWW or #YWW marking on the bottom of the package. Y shows the year that the part was made, for example, Y = 5 for 2005. WW shows the work week that the part was made.

[2] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked.

[3] The evaluation board is shipped with three pieces of 10 kΩ parts. Users should order extra samples or different resistance options if needed.

NOTES