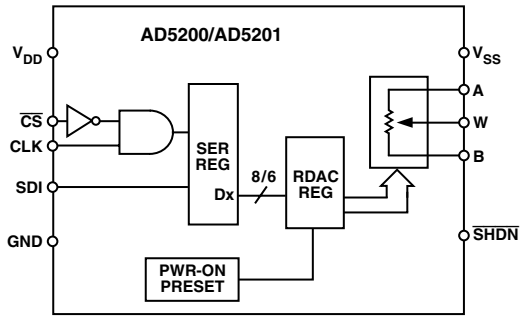
256-Position and 33-Position Digital Potentiometers

AD5200/AD5201

FEATURES
AD5200—256-Position
AD5201—33-Position
10 kΩ, 50 kΩ
3-Wire SPI-Compatible Serial Data Input
Single Supply 2.7 V to 5.5 V or
Dual Supply ±2.7 V for AC or Bipolar Operations
Internal Power-On Midscale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage-to-Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5200 and AD5201 are programmable resistor devices, with 256 positions and 33 positions respectively, that can be digitally controlled through a 3-wire SPI serial interface. The terms programmable resistor, variable resistor (VR), and RDAC are commonly used interchangeably to refer to digital potentiometers. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Both AD5200/AD5201 contain a single variable resistor in the compact MSOP package. Each device contains a fixed wiper resistance at the wiper contact that taps the programmable resistance at a point determined by a digital code. The code is loaded in the serial input register. The resistance between the wiper and either end point of the programmable resistor varies linearly with respect to the digital code transferred into the VR latch. Each variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper, or the B terminal and the wiper. The fixed A-to-B terminal resistance of 10 kΩ or 50 kΩ has a nominal temperature coefficient of 500 ppm/°C. The VR has a VR latch that holds its programmed resistance value. The VR latch is updated from an SPI-compatible serial-to-parallel shift register that is loaded from a standard 3-wire serial-input digital interface. Eight data bits for the AD5200 and six data bits for the AD5201 make up the data word that is clocked into the serial input register. The internal preset forces the wiper to the midscale position by loading 80_H and 10_H into AD5200 and AD5201 VR latches respectively. The $\overline{SHDN}$ pin forces the resistor to an end-to-end open-circuit condition on the A terminal and shorts the wiper to the B terminal, achieving a microwatt power shutdown state. When $\overline{SHDN}$ is returned to logic high, the previous latch setting puts the wiper in the same resistance setting prior to shutdown. The digital interface is still active during shutdown so that code changes can be made that will produce a new wiper position when the device is returned from shutdown.

All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

REV. D

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AD5200/AD5201–SPECIFICATIONS

AD5200 ELECTRICAL CHARACTERISTICS

(V_{DD} = 5 V ± 10%, or 3 V ± 10%, V_{SS} = 0 V, V_A = +V_{DD}, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity [2]	R-DNL	R_{WB}, V_A = No Connect	–1	±0.25	+1	LSB
Resistor Integral Nonlinearity [2]	R-INL	R_{WB}, V_A = No Connect	–2	±0.5	+2	LSB
Nominal Resistor Tolerance [3]	ΔR_{AB}	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs.)						
Resolution	N		8			Bits
Differential Nonlinearity [4]	DNL		–1	±1/4	+1	LSB
Integral Nonlinearity [4]	INL		–2	±1/2	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–1.5	–0.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+0.5	+1.5	LSB
RESISTOR TERMINALS						
Voltage Range [5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance [6] A, B	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 80_H		45		pF
Capacitance [6] W	C_W	f = 1 MHz, Measured to GND, Code = 80_H		60		pF
Shutdown Supply Current [7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	5	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V, V_{SS} = 0 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V, V_{SS} = 0 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance [6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_{LOGIC}		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	–0.3		5.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V		15	40	µA
Negative Supply Current	I_{SS}	V_{SS} = –5 V		15	40	µA
Power Dissipation [8]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = 0 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale	–0.01	0.001	+0.01	%/%
DYNAMIC CHARACTERISTICS [6, 9]						
Bandwidth –3 dB	BW_10 kΩ	R_{AB} = 10 kΩ, Code = 80_H		600		kHz
	BW_50 kΩ	R_{AB} = 50 kΩ, Code = 80_H		100		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.003		%
V_W Settling Time (10 kΩ/50 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ± 1 LSB Error Band		2/9		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, RS = 0		9		nV$\sqrt{Hz}$

NOTES

[1]Typicals represent average readings at 25°C and V_{DD} = 5 V, V_{SS} = 0 V.

[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. I_W = V_{DD}/R for both V_{DD} = +2.7 V, V_{SS} = –2.7 V.

[3]V_{AB} = V_{DD}, Wiper (V_W) = No connect.

[4]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions.

[5]Resistor Terminals A, B, W have no limitations on polarity with respect to each other.

[6]Guaranteed by design and not subject to production test.

[7]Measured at the A terminal. A terminal is open-circuited in shutdown mode.

[8]P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[9]All dynamic characteristics use V_{DD} = 5 V, V_{SS} = 0 V.

Specifications subject to change without notice.

AD5201 ELECTRICAL CHARACTERISTICS

(V_{DD} = 5 V ± 10%, or 3 V ± 10%, V_{SS} = 0 V, V_A = +V_{DD}, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity [2]	R-DNL	R_{WB}, V_A = No Connect	–0.5	±0.05	+0.5	LSB
Resistor Integral Nonlinearity [2]	R-INL	R_{WB}, V_A = No Connect	–1	±0.1	+1	LSB
Nominal Resistor Tolerance [3]	ΔR_{AB}	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs.)						
Resolution [4]	N		6			Bits
Differential Nonlinearity [5]	DNL		–0.5	±0.01	+0.5	LSB
Integral Nonlinearity [5]	INL		–1	±0.02	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 10_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 20_H	–1/2	–1/4	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+1/4	+1/2	LSB
RESISTOR TERMINALS						
Voltage Range [6]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance [7] A, B	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 10_H		45		pF
Capacitance [7] W	C_W	f = 1 MHz, Measured to GND, Code = 10_H		60		pF
Shutdown Supply Current [8]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	5	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = $V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V, V_{SS} = 0 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V, V_{SS} = 0 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance [7]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_{LOGIC}		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	–0.3		5.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V		15	40	µA
Negative Supply Current	I_{SS}	V_{SS} = –5 V		15	40	µA
Power Dissipation [9]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = –5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%	–0.01	0.001	+0.01	%/%
DYNAMIC CHARACTERISTICS [7,10]						
Bandwidth –3 dB	BW_10 kΩ	R_{AB} = 10 kΩ, Code = 10_H		600		kHz
	BW_50 kΩ	R_{AB} = 50 kΩ, Code = 10_H		100		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.003		%
V_W Settling Time (10 kΩ/50 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ± 1 LSB Error Band		2/9		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, RS = 0		9		nV$\sqrt{Hz}$

NOTES

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V, V_{SS} = 0 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. I_W = V_{DD}/R for both V_{DD} = +2.7 V, V_{SS} = –2.7 V.

[3] V_{AB} = V_{DD}, Wiper (V_W) = No connect.

[4] Six bits are needed for 33 positions even though it is not a 64-position device.

[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions.

[6] Resistor Terminals A, B, W have no limitations on polarity with respect to each other.

[7] Guaranteed by design and not subject to production test.

[8] Measured at the A terminal. A terminal is open-circuited in shutdown mode.

[9] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[10] All dynamic characteristics use V_{DD} = 5 V, V_{SS} = 0 V.

Specifications subject to change without notice.

AD5200/AD5201–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, or 3 V ± 10%, V_{SS} = 0 V, V_A = $+V_{DD}$, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS (Applies to All Parts [Notes 2, 3])						
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock Level High or Low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		40			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES
[1]Typicals represent average readings at 25°C and V_{DD} = 5 V, V_{SS} = 0 V.
[2]Guaranteed by design and not subject to production test.
[3]See timing diagram for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_{LOGIC} = 5 V.

Specifications subject to change without notice.

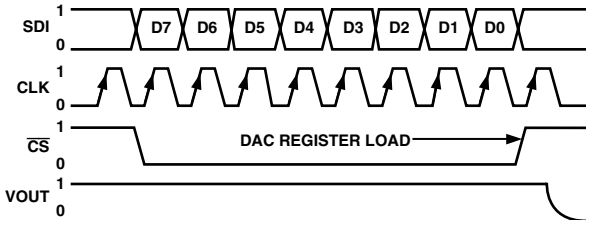


Figure 1a. AD5200 Timing Diagram

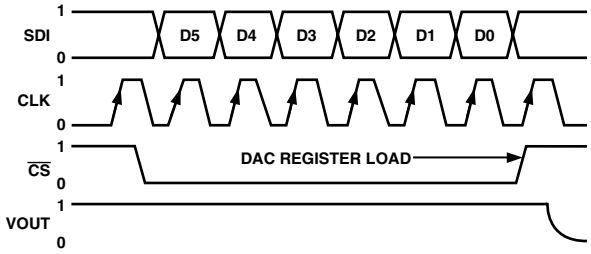


Figure 1b. AD5201 Timing Diagram

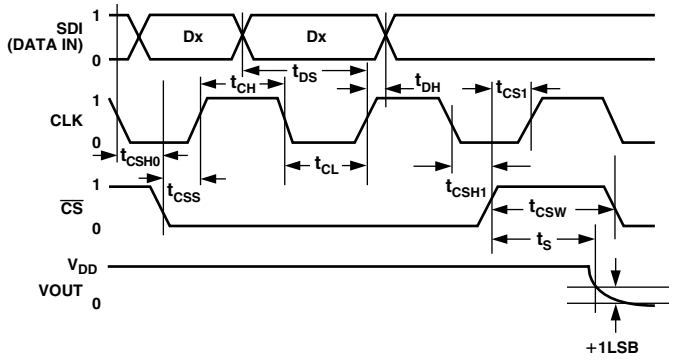


Figure 1c. Detail Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted)

V_{DD} to V_{SS} . . . . . 7 V
V_{DD} to GND . . . . . –0.3, +7 V
V_{SS} to GND . . . . . 0 V, –7 V
V_A, V_B, V_W to GND . . . . . V_{SS}, V_{DD}
I_{MAX} . . . . . ±20 mA[2]
Digital Inputs and Output Voltage to GND . . . . . 0 V, 7 V
Operating Temperature Range . . . . . –40°C to +85°C
Maximum Junction Temperature (T_J Max) . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Thermal Resistance θ_{JA}, MSOP . . . . . 200°C/W
Package Power Dissipation = (T_J Max – T_A)/θ_{JA}

NOTES

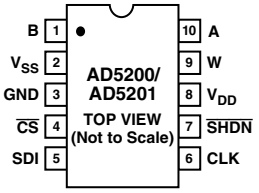
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Max current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance. Please refer to TPC 31 and TPC 32 for detail.

PIN FUNCTION DESCRIPTIONS

Pin	Name	Description
1	B	B Terminal.
2	V_{SS}	Negative Power Supply, specified for operation from 0 V to –2.7 V.
3	GND	Ground.
4	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the DAC register.
5	SDI	Serial Data Input.
6	CLK	Serial Clock Input, positive edge triggered.
7	$\overline{SHDN}$	Active Low Input. Terminal A open circuit. Shutdown controls Variable Resistors of RDAC to temporary infinite.
8	V_{DD}	Positive Power Supply (Sum of V_{DD} + V_{SS} ≤ 5.5 V).
9	W	Wiper Terminal.
10	A	A Terminal.

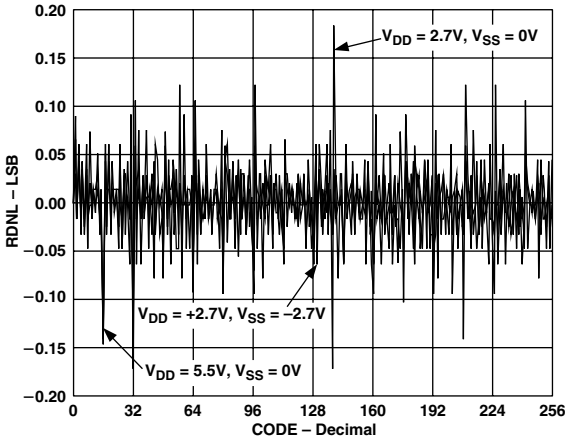
PIN CONFIGURATION



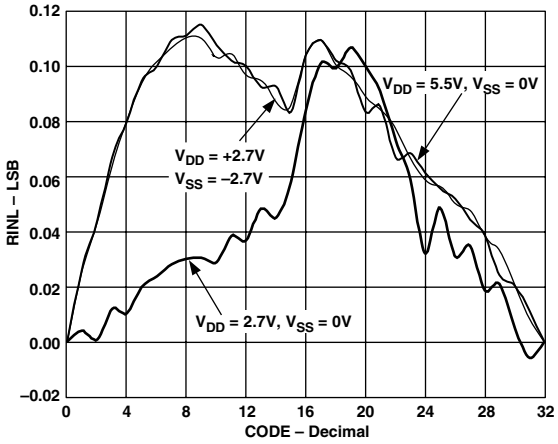
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5200/AD5201 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

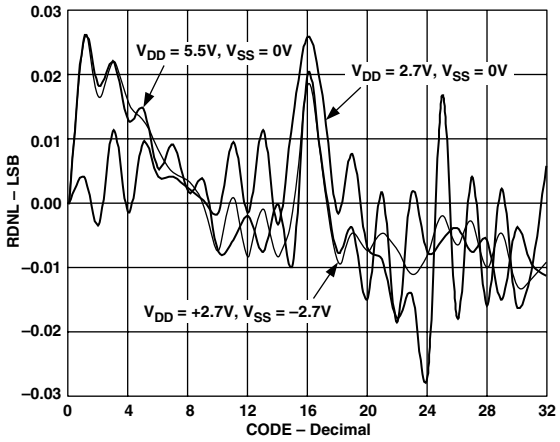
AD5200/AD5201–Typical Performance Characteristics



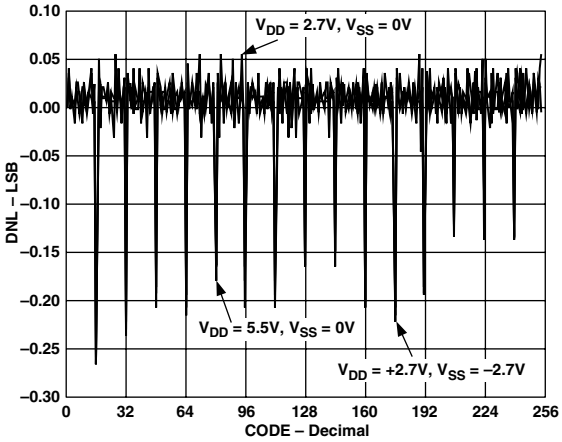
TPC 1. AD5200 10 kΩ RDNL vs. Code



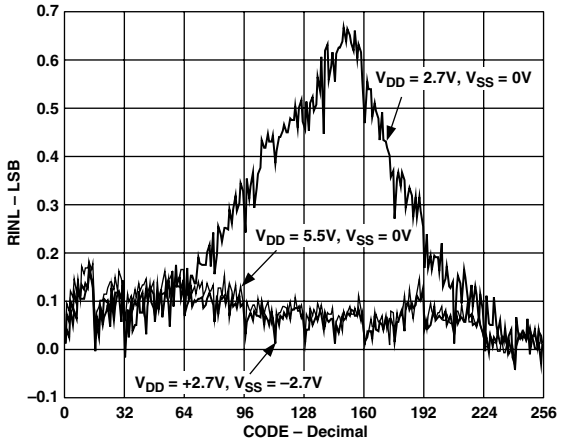
TPC 4. AD5201 10 kΩ RINL vs. Code



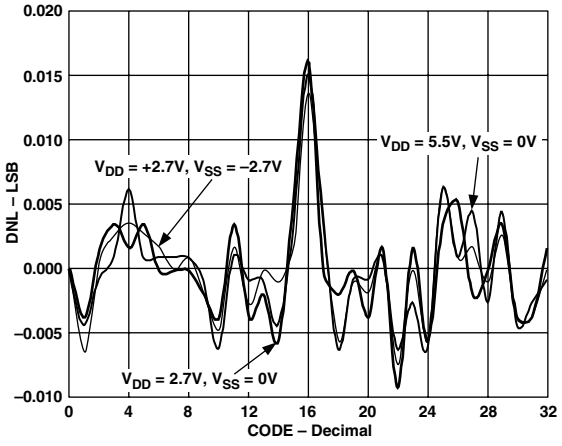
TPC 2. AD5201 10 kΩ RDNL vs. Code



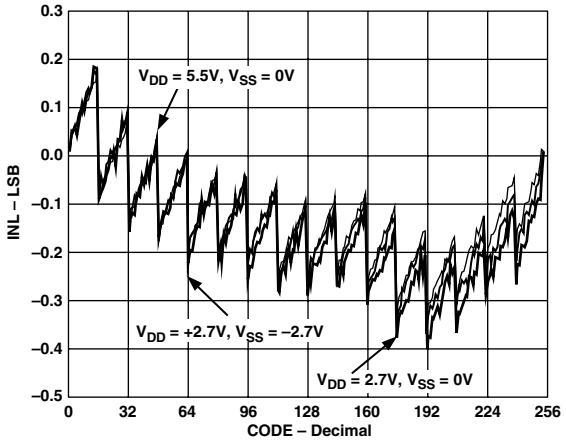
TPC 5. AD5200 10 kΩ DNL vs. Code



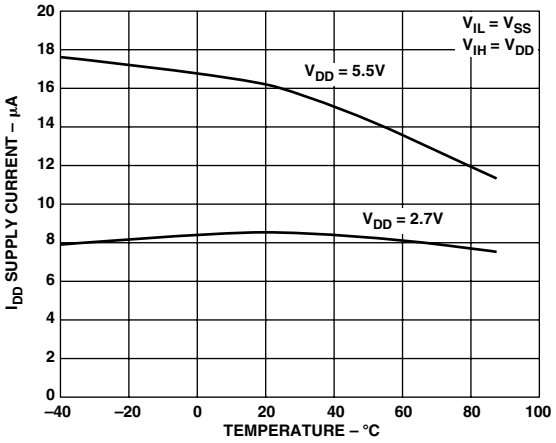
TPC 3. AD5200 10 kΩ RINL vs. Code



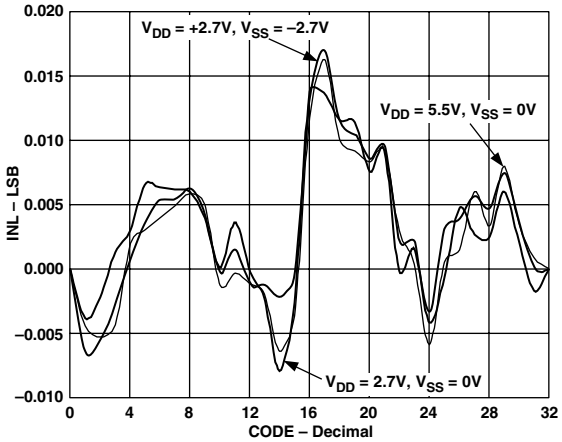
TPC 6. AD5201 10 kΩ DNL vs. Code



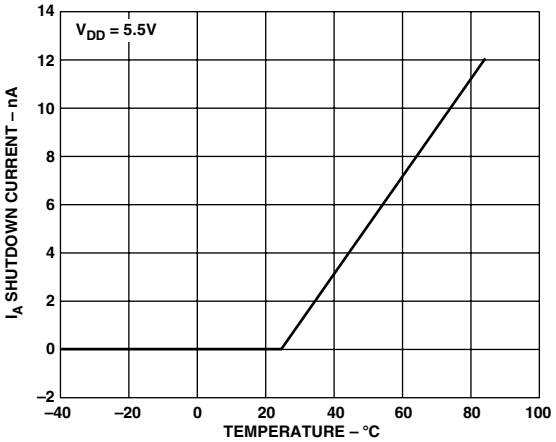
TPC 7. AD5200 10 kΩ INL vs. Code



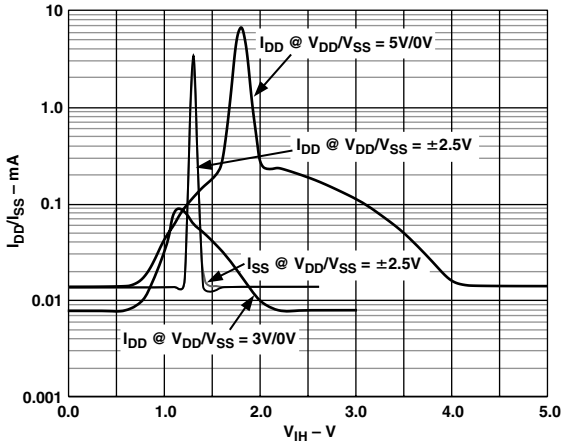
TPC 10. Supply Current vs. Temperature



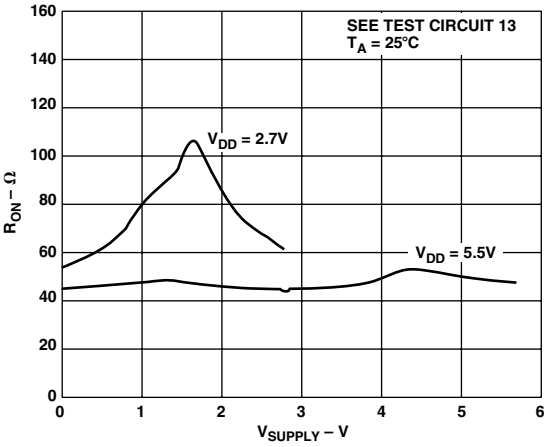
TPC 8. AD5201 10 kΩ INL vs. Code



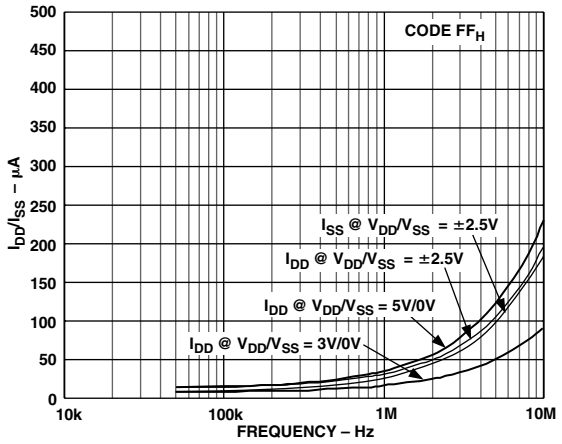
TPC 11. Shutdown Current vs. Temperature



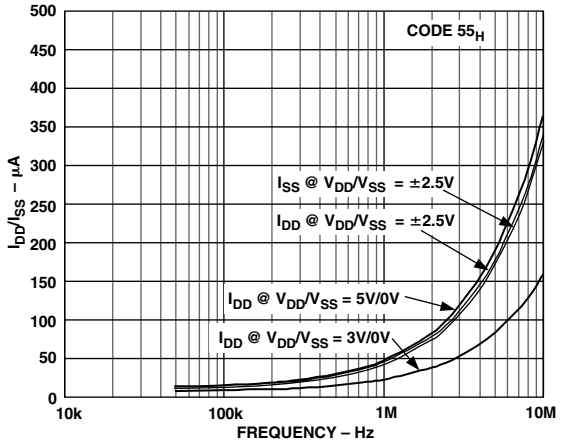
TPC 9. Supply Current vs. Logic Input Voltage



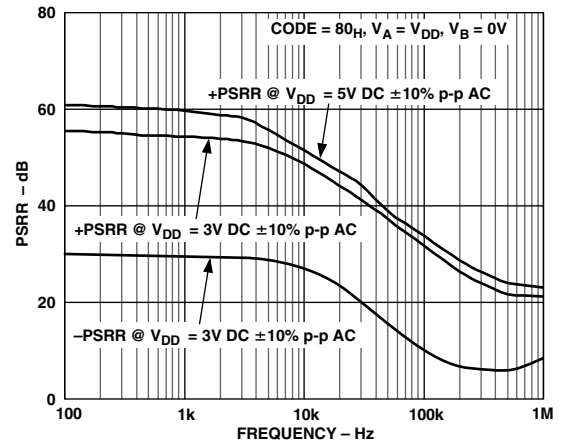
TPC 12. Wiper ON Resistance vs. V_{SUPPLY}



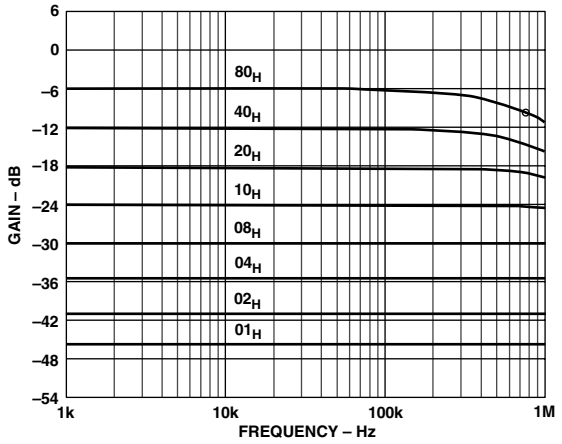
TPC 13. AD5200 10 kΩ Supply Current vs. Clock Frequency



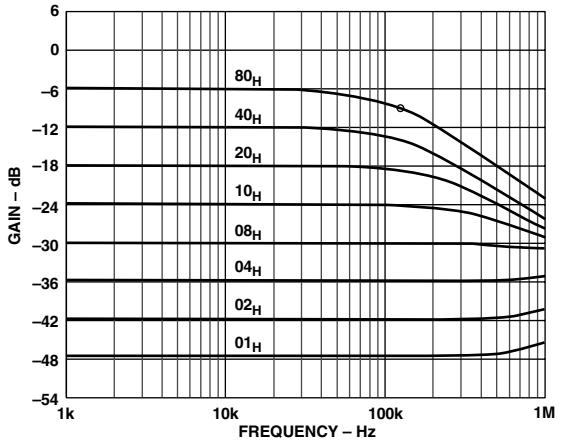
TPC 14. AD5200 10 kΩ Supply Current vs. Clock Frequency



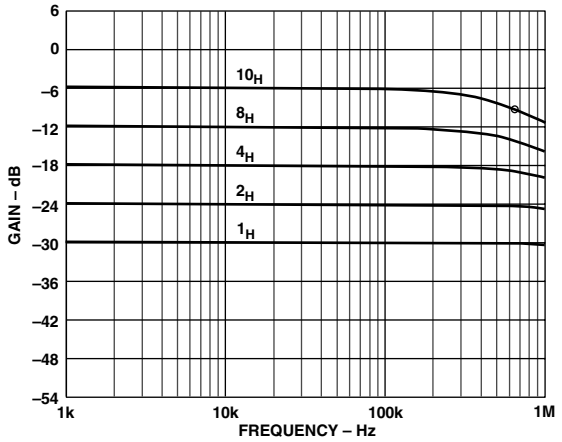
TPC 15. Power Supply Rejection Ratio vs. Frequency



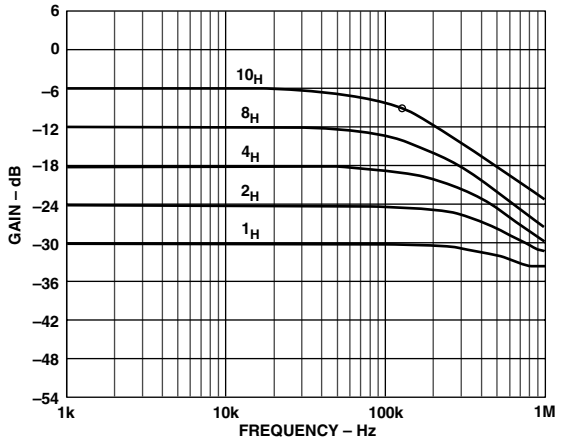
TPC 16. AD5200 10 kΩ Gain vs. Frequency vs. Code



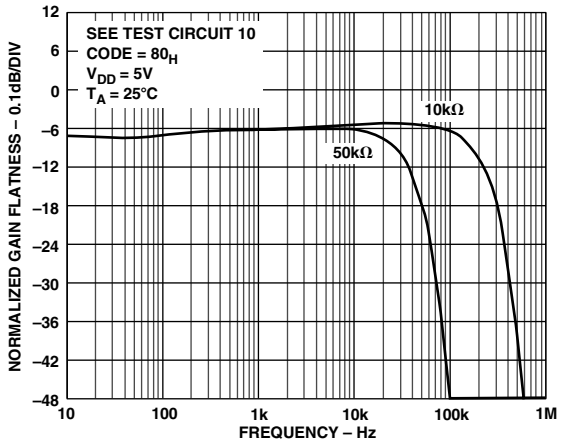
TPC 17. AD5200 50 kΩ Gain vs. Frequency vs. Code



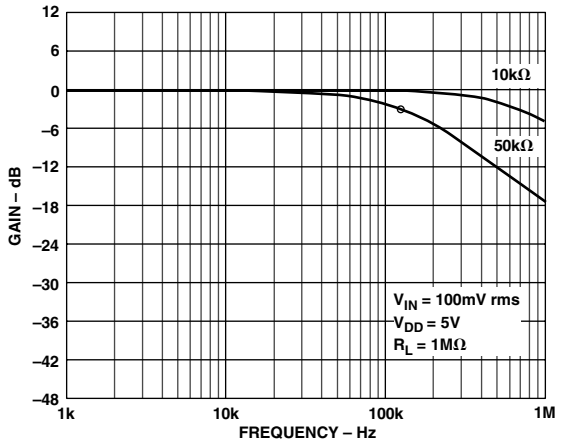
TPC 18. AD5201 10 kΩ Gain vs. Frequency vs. Code



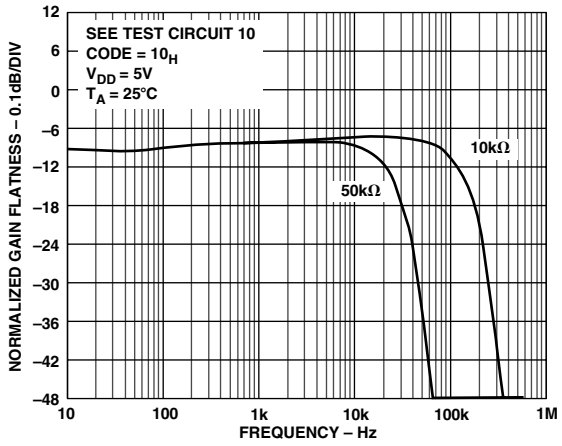
TPC 19. AD5201 50 kΩ Gain vs. Frequency vs. Code



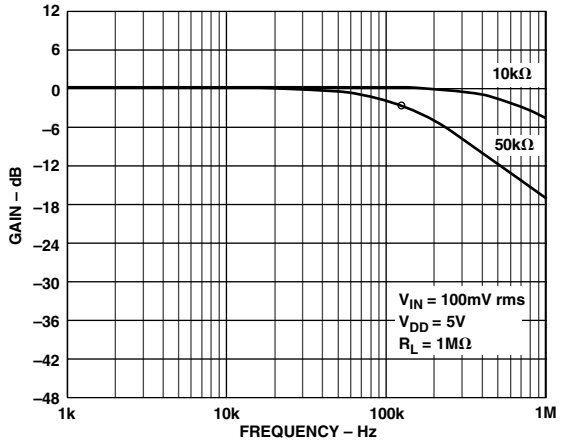
TPC 22. Normalized Gain Flatness vs. Frequency



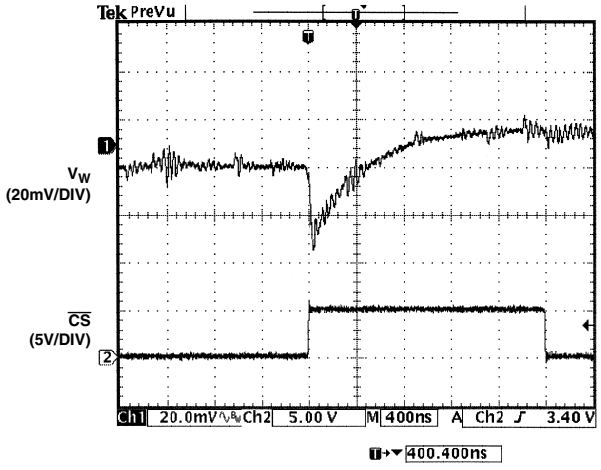
TPC 20. AD5200 –3 dB Bandwidth



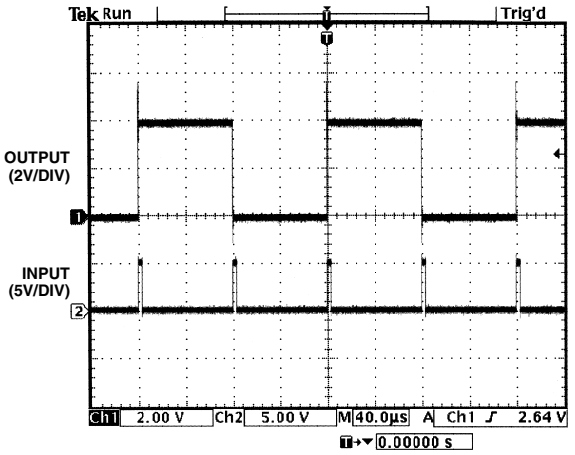
TPC 23. AD5201 Normalized Gain Flatness vs. Frequency



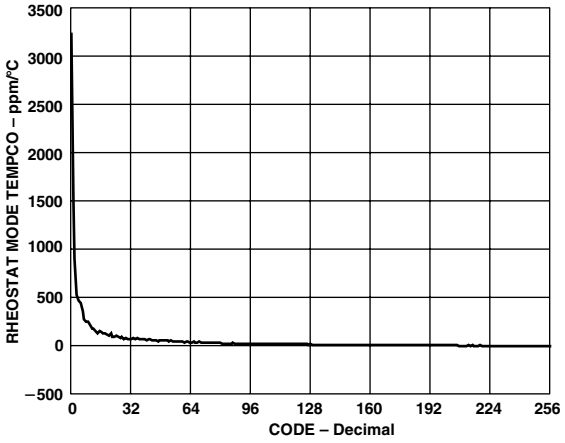
TPC 21. AD5201 –3 dB Bandwidth



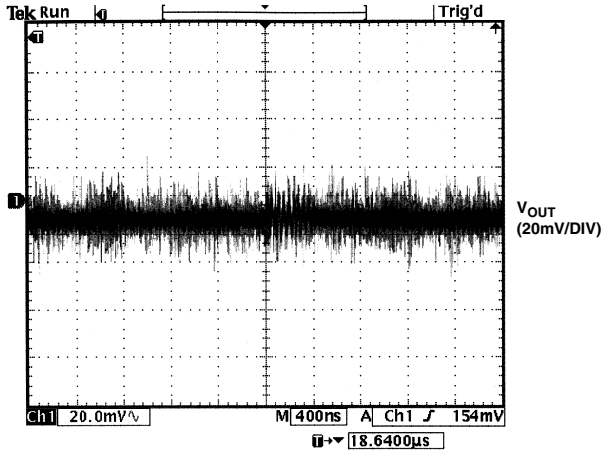
TPC 24. One Position Step Change at Half Scale



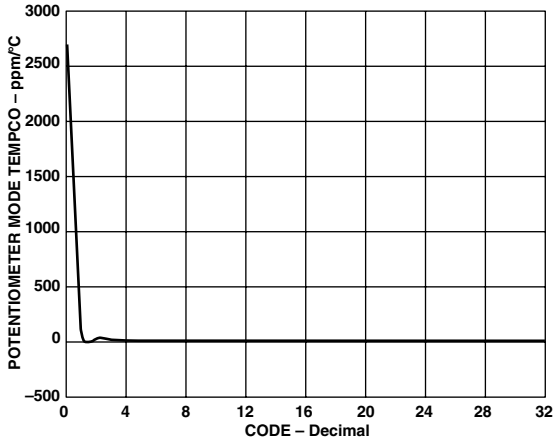
TPC 25. Large Signal Settling Time



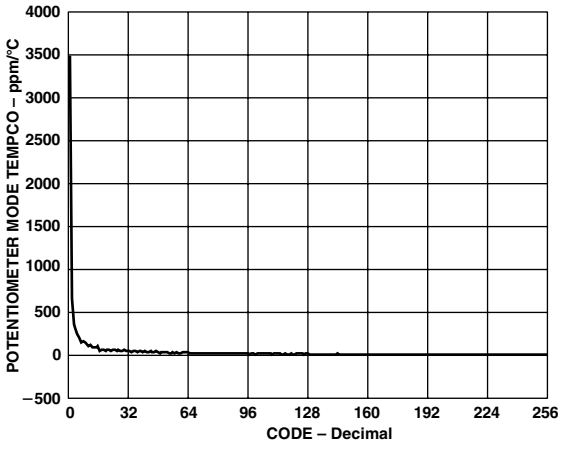
TPC 28. AD5200 $\Delta R_{WB}/\Delta T$ Rheostat Mode Temperature Coefficient



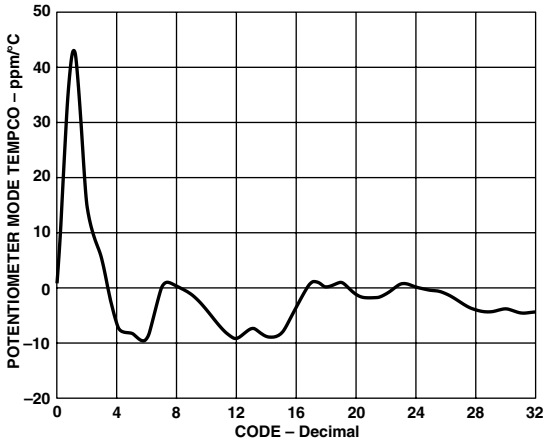
TPC 26. Digital Feedthrough vs. Time



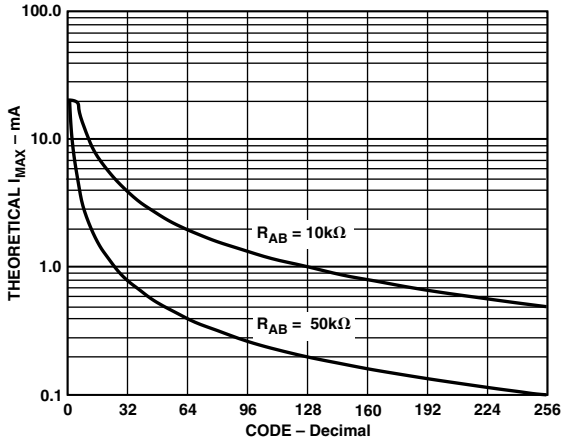
TPC 29. AD5201 Potentiometer Mode Temperature Coefficient



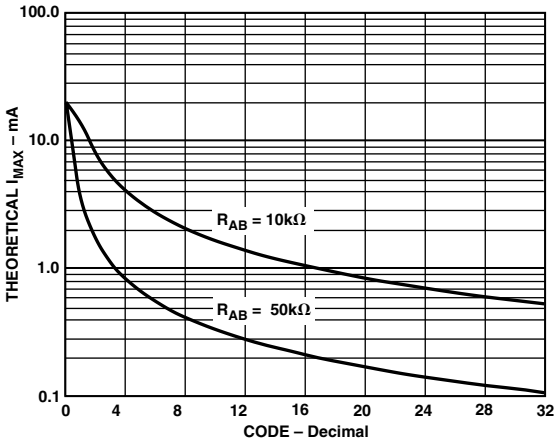
TPC 27. AD5200 $\Delta V_{WB}/\Delta T$ Potentiometer Mode Temperature Coefficient



TPC 30. AD5201 $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco



TPC 31. AD5200 I_{MAX} vs. Code



TPC 32. AD5201 I_{MAX} vs. Code

OPERATION

The AD5200/AD5201 provide 255 and 33 positions digitally-controlled variable resistor (VR) devices. Changing the programmed VR settings is accomplished by clocking in an 8-bit serial data word for AD5200, and a 6-bit serial data word for AD5201, into the SDI (Serial Data Input) pins. Table I provides the serial register data word format. The AD5200/AD5201 are preset to a midscale internally during power-on condition. In addition, the AD5200/AD5201 contain power shutdown $\overline{\text{SHDN}}$ pins that place the RDAC in a zero power consumption state where the immediate switches next to Terminals A and B are open-circuited. Meanwhile, the wiper W is connected to B terminal, resulting in only leakage current consumption in the VR structure. During shutdown, the VR latch contents are maintained when the RDAC is inactive. When the part is returned from shutdown, the stored VR setting will be applied to the RDAC.

Table I. AD5200 Serial-Data Word Format

B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MSB							**LSB**
2^7							2^0

Table II. AD5201 Serial-Data Word Format

B5*	**B4**	**B3**	**B2**	**B1**	**B0**
D5*	**D4**	**D3**	**D2**	**D1**	**D0**
MSB					**LSB**
2^5					2^0

*Six data bits are needed for 33 positions.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B are available with values of 10 kΩ and 50 kΩ. The final two digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10 and 50 kΩ = 50. The nominal resistance (R_{AB}) of AD5200 has 256 contact points accessed by the wiper terminal. The 8-bit data word in the RDAC latch of AD5200 is decoded to select one of the 256 possible settings. In both parts, the wiper's first connection starts at the B terminal for data 00_H. This B-terminal connection has a wiper contact resistance of 50 Ω as long as valid V_{DD}/V_{SS} is applied, regardless of the nominal resistance. For a 10 kΩ part, the second connection of AD5200 is the first tap point with 89 Ω [$R_{WB} = R_{AB}/255 + R_W = 39\ \Omega + 50\ \Omega$] for data 01_H. The third connection is the next tap point representing 78 + 50 = 128 Ω for data 02_H. Due to its unique internal structure, AD5201 has 5-bit + 1 resolution, but needs a 6-bit data word to achieve the full 33 steps resolution. The 6-bit data word in the RDAC latch is decoded to select one of the 33 possible settings. Data 34 to 63 will automatically be equal to Position 33. The wiper 00_H connection of AD5201 gives 50 Ω. Similarly, for a 10 kΩ part, the first tap point of AD5201 yields 363 Ω for data 01_H, 675 Ω for data 02_H. For both AD5200 and AD5201, each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached. Figures 2a and 2b show the simplified diagrams of the equivalent RDAC circuits.

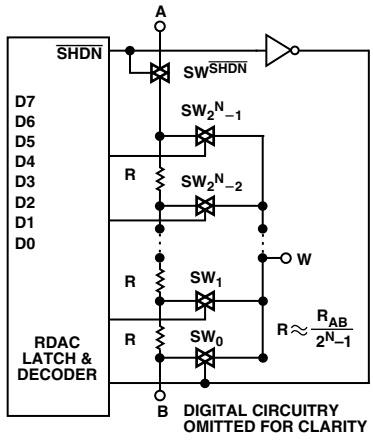


Figure 2a. AD5200 Equivalent RDAC Circuit. 255 positions can be achieved up to Switch SW $_{2^N-1}$.

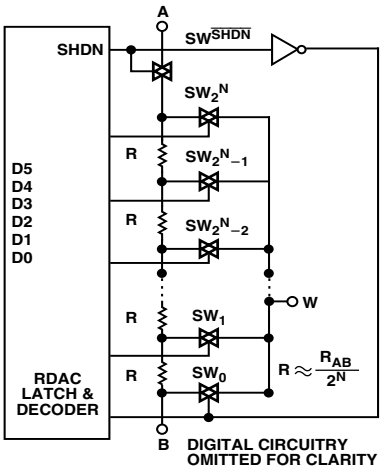


Figure 2b. AD5201 Equivalent RDAC Circuit. Unlike AD5200, 33 positions can be achieved all the way to Switch SW $_{2^N}$.

The general equation determining the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{255}R_{AB} + 50\ \Omega \qquad \text{for AD5200} \qquad (1)$$

$$R_{WB}(D) = \frac{D}{32}R_{AB} + 50\ \Omega \qquad \text{for AD5201} \qquad (2)$$

where:

D is the decimal equivalent of the data contained in RDAC latch.

R_{AB} is the nominal end-to-end resistance.

R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Note *D* in AD5200 is between 0 to 255 for 256 positions. On the other hand, *D* in AD5201 is between 0 to 32 so that 33 positions can be achieved due to the slight internal structure difference, Figure 2b.

Again if R_{AB} = 10 kΩ and A terminal can be opened or tied to W, the following output resistance between W to B will be set for the following RDAC latch codes:

AD5200 Wiper-to-B Resistance

D (DEC)	R_{WB} (Ω)	Output State
255	10050	Full-Scale (R_{AB} + R_W)
128	5070	Midscale
1	89	1 LSB
0	50	Zero-Scale (Wiper Contact Resistance)

AD5201 Wiper-to-B Resistance

D (DEC)	R_{WB} (Ω)	Output State
32	10050	Full-Scale (R_{AB} + R_W)
16	5050	Midscale
1	363	1 LSB
0	50	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 50 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than ±20 mA to avoid degradation or possible destruction of the internal switch contact.

Like the mechanical potentiometer the RDAC replaces, it is totally symmetrical. The resistance between the wiper W and Terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used, the B terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{(255 - D)}{255}R_{AB} + 50\ \Omega \qquad \text{for AD5200} \qquad (3)$$

$$R_{WA}(D) = \frac{(32 - D)}{32}R_{AB} + 50\ \Omega \qquad \text{for AD5201} \qquad (4)$$

Similarly, *D* in AD5200 is between 0 to 255, whereas D in AD5201 is between 0 to 32.

For R_{AB} = 10 kΩ and B terminal is opened or tied to the wiper W, the following output resistance between W and A will be set for the following RDAC latch codes:

AD5200 Wiper-to-A Resistance

D (DEC)	R_{WA} (Ω)	Output State
255	50	Full-Scale (R_W)
128	5030	Midscale
1	10011	1 LSB
0	10050	Zero-Scale (R_{AB} + R_W)

AD5201 Wiper-to-A Resistance

D (DEC)	R_{WA} (Ω)	Output State
32	50	Full-Scale (R_W)
16	5050	Midscale
1	9738	1 LSB
0	10050	Zero-Scale (R_{AB} + R_W)

The tolerance of the nominal resistance can be ±30% due to process lot dependance. If users apply the RDAC in rheostat (variable resistance) mode, they should be aware of such specification of tolerance. The change in R_{AB} with temperature has a 500 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates output voltages at wiper-to-B and wiper-to-A to be proportional to the input voltage at A to B.

Unlike the polarity of $V_{DD} - V_{SS}$, which must be positive, voltage across A–B, W–A, and W–B can be at either polarity.

If ignoring the effects of the wiper resistance for an approximation, connecting A terminal to 5 V and B terminal to ground produces an output voltage at the wiper which can be any value starting at almost zero to almost full scale with the minor deviation contributed by the wiper resistance. Each LSB of voltage is equal to the voltage applied across Terminal AB divided by the 2^N-1 and 2^N position resolution of the potentiometer divider for AD5200 and AD5201 respectively. The general equation defining the output voltage with respect to ground for any valid input voltage applied to Terminals A and B is:

$$V_W(D) = \frac{D}{255} V_{AB} + V_B \qquad \text{for AD5200} \tag{5}$$

$$V_W(D) = \frac{D}{32} V_{AB} + V_B \qquad \text{for AD5201} \tag{6}$$

where D in AD5200 is between 0 to 255 and D in AD5201 is between 0 to 32.

For more accurate calculation, including the effects of wiper resistance, V_W can be found as:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \tag{7}$$

where $R_{WB}(D)$ and $R_{WA}(D)$ can be obtained from Equations 1 to 4.

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors and not the absolute values; therefore, the drift reduces to 15 ppm/°C.

DIGITAL INTERFACING

The AD5200/AD5201 contain a standard three-wire serial input control interface. The three inputs are clock (CLK), $\overline{CS}$, and serial data input (SDI). The positive-edge-sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. Figure 3 shows more detail of the internal digital circuitry. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Table III).

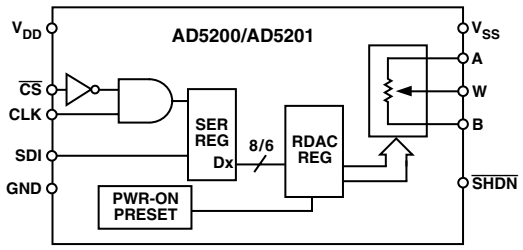


Figure 3. Block Diagram

Table III. Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{SHDN}$	Register Activity
L	L	H	No SR effect.
P	L	H	Shift one bit in from the SDI pin.
X	P	H	Load SR data into RDAC latch.
X	H	H	No operation.
X	H	L	Open circuit on A terminal and short circuit between W to B terminals.

NOTE
P = positive edge, X = don't care, SR = shift register.

All digital inputs are protected with a series input resistor and parallel Zener ESD structure shown in Figure 4. Applies to digital input pins $\overline{CS}$, SDI, $\overline{SHDN}$, CLK.

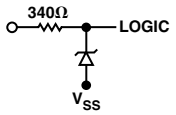


Figure 4. ESD Protection of Digital Pins

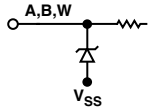


Figure 5. ESD Protection of Resistor Terminals

TEST CIRCUITS

Figures 6 to 14 define the test conditions used in the product specification table.

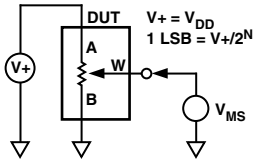


Figure 6. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

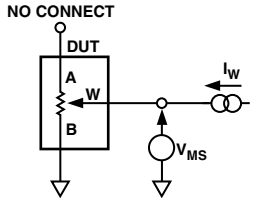


Figure 7. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

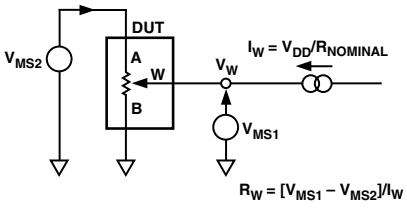


Figure 8. Wiper Resistance Test Circuit

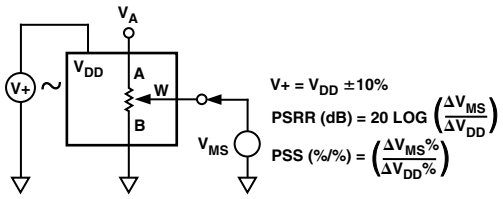


Figure 9. Power Supply Sensitivity Test Circuit (PSS, PSRR)

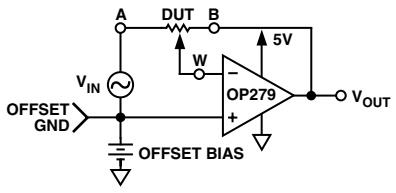


Figure 10. Inverting Gain Test Circuit

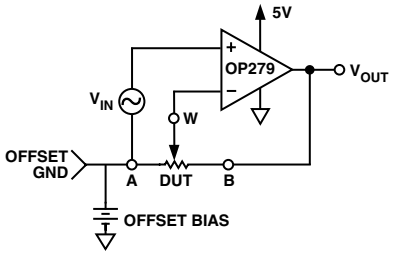


Figure 11. Noninverting Gain Test Circuit

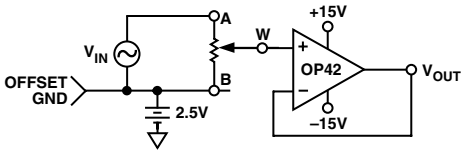


Figure 12. Gain vs. Frequency Test Circuit

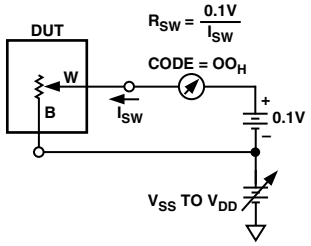


Figure 13. Incremental ON Resistance Test Circuit

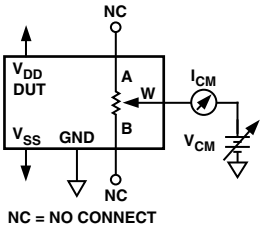


Figure 14. Common-Mode Leakage Current Test Circuit