Data Sheet

AD5204/AD5206

4-/6-Channel Digital Potentiometers

FEATURES

- 256 positions
- Multiple independently programmable channels
  - AD5204—4-channel
  - AD5206—6-channel
- Potentiometer replacement
- Terminal resistance of 10 kΩ, 50 kΩ, 100 kΩ
- 3-wire SPI-compatible serial data input
- +2.7 V to +5.5 V single-supply operation; ±2.7 V dual-supply operation
- Power-on midscale preset

APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation: gain, offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, time constants
- Line impedance matching

FUNCTIONAL BLOCK DIAGRAMS

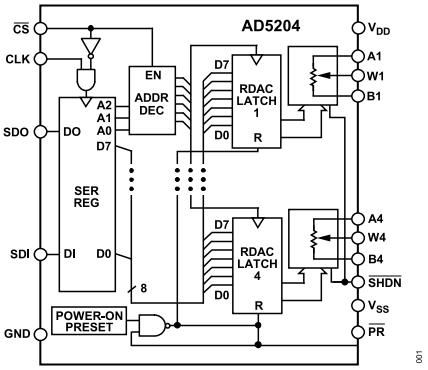

Figure 1.

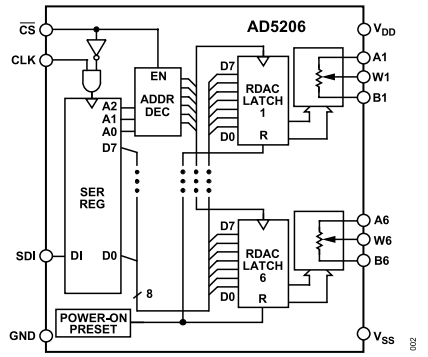

Figure 2.

GENERAL DESCRIPTION

The AD5204/AD5206 provide 4-/6-channel, 256-position digitally controlled variable resistor (VR) devices. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Each channel of the AD5204/AD5206 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial-input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance between the A terminal and the wiper or the B terminal and the wiper. The fixed A-to-B terminal resistance of 10 kΩ, 50 kΩ, or 100 kΩ has a nominal temperature coefficient of 700 ppm/°C.

Each VR has its own VR latch that holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial-input digital interface. Eleven data bits make up the data-word clocked into the serial input register. The first three bits are decoded to determine which VR latch is loaded with the last eight bits of the data-word when the $\overline{CS}$ strobe is returned to logic high. A serial data output pin at the opposite end of the serial register (AD5204 only) allows simple daisy chaining in multiple VR applications without requiring additional external decoding logic.

An optional reset ($\overline{PR}$) pin forces all the AD5204 wipers to the midscale position by loading 0x80 into the VR latch.

The AD5204/AD5206 are available in the 24-lead surface-mount SOIC and TSSOP packages. The AD5204 is also available in a 32-lead, 5 mm × 5 mm LFCSP package. All parts are guaranteed to operate over the extended industrial temperature range of −40°C to +85°C. For additional single-, dual-, and quad-channel devices, see the AD8400/AD8402/AD8403 data sheets.

Rev. F

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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5/2022—Rev. E to Rev. F

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Changes to VW Settling Time Parameter, Input Logic High Parameter, and Input Logic Low Parameter, Table 1 ... 3
Deleted PDIP (N-24-1) Parameter, Table 2 ... 6
Added Electrostatic Discharge (ESD) Ratings Section ... 6
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V ± 10% or 3 V ± 10%, V_{SS} = 0 V, V_A = V_{DD}, V_B = 0 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE[2]						
Resistor Differential NL[3]	R-DNL	R_{WB}, V_A = no connect	−1	±0.25	+1	LSB
Resistor Nonlinearity Error[3]	R-INL	R_{WB}, V_A = no connect	−2	±0.5	+2	LSB
Nominal Resistor Tolerance[4]	ΔR_{AB}	T_A = 25°C	−30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, wiper = no connect		700		ppm/°C
Nominal Resistance Match	$\Delta R/R_{AB}$	Channel 1 to Channel 2, Channel 3, and Channel 4, or to Channel 5 and Channel 6; V_{AB} = V_{DD}		0.25	1.5	%
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = 5 V		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE[2]						
Resolution	N		8			Bits
Differential Nonlinearity[5]	DNL		−1	±0.25	+1	LSB
Integral Nonlinearity[5]	INL		−2	±0.5	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = midscale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−2	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0	1	2	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance[7] Ax, Bx	C_A, C_B	f = 1 MHz, measured to GND, code = midscale		45		pF
Capacitance[7] Wx	C_W	f = 1 MHz, measured to GND, code = midscale		60		pF
Shutdown Current[8]	I_{A_SD}			0.01	5	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_W = 0, V_{DD} = +2.7 V, V_{SS} = −2.5 V		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
		V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.6	V
Output Logic High	V_{OH}	$R_{PULL-UP}$ = 1 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[7]	C_{IL}			5		pF
POWER SUPPLIES						
Power Single-Supply Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Power Dual-Supply Range	V_{DD}/V_{SS}		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		12	60	µA
Negative Supply Current	I_{SS}	V_{SS} = −2.5 V, V_{DD} = +2.7 V		12	60	µA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V			0.3	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = 5 V ± 10%		0.0002	0.005	%/%
DYNAMIC CHARACTERISTICS[7, 10]						
Bandwidth −3 dB	BW_10K	R_{AB} = 10 kΩ		721		kHz
	BW_50K	R_{AB} = 50 kΩ		137		kHz

SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
	BW_100K	R_{AB} = 100 kΩ		69		kHz
Total Harmonic Distortion	THD_W	V_A = 1.414 V rms, V_B = 0 V dc, f = 1 kHz		0.004		%
VW Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band				
		R_{AB} = 10 kΩ		2		µs
		R_{AB} = 50 kΩ		9		µs
		R_{AB} = 100 kΩ		18		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz, $\overline{PR}$ = 0		9		nV/√Hz
INTERFACE TIMING CHARACTERISTICS[7, 11, 12]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
CLK-to-SDO Propagation Delay[13]	t_{PD}	R_L = 2 kΩ , C_L < 20 pF	1		150	ns
Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		40			ns
Reset Pulse Width	t_{RS}		90			ns
CLK Fall to $\overline{CS}$ Fall Setup	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.

[2] Applies to all VRs.

[3] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal position between successive tap positions. Parts are guaranteed monotonic. See the test circuit in Figure 24. I_W = V_{DD}/R for both V_{DD} = 3 V and V_{DD} = 5 V.

[4] V_{AB} = V_{DD}, wiper (V_W) = no connect.

[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic at operating conditions. See the test circuit in Figure 23.

[6] Resistor Terminal A, Terminal B, and Wiper W have no limitations on polarity with respect to each other.

[7] Guaranteed by design and not subject to production test.

[8] Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.

[9] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[10] All dynamic characteristics use V_{DD} = 5 V.

[11] Applies to all parts.

[12] See the timing diagrams (Figure 3 to Figure 5) for the location of the measured values. All input control voltages are specified with t_R = t_F = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and V_{DD} = 5 V.

[13] The propagation delay depends on the values of V_{DD}, R_L, and C_L (see the Theory of Operation section).

TIMING DIAGRAMS

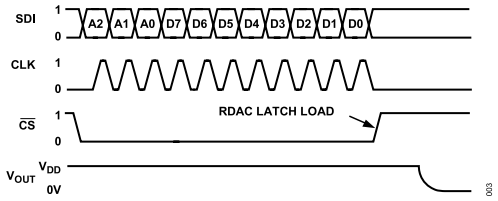

Figure 3. Timing Diagram

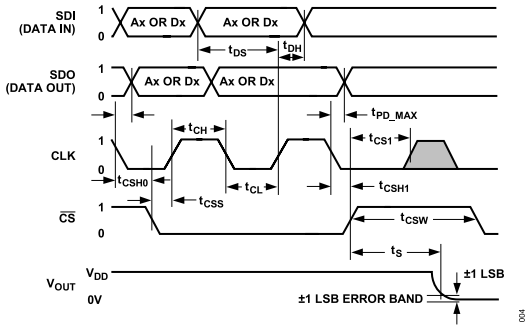

Figure 4. Detailed Timing Diagram

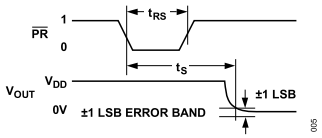

Figure 5. AD5204 Preset Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	0 V to −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
I_A, I_B, I_W	
Pulsed[1]	±20 mA
Continuous	
10 kΩ End-to-End Resistance	±11 mA
50 kΩ and 100 kΩ End-to-End Resistance	±2.5 mA
Digital Input and Output Voltage to GND	−0.3 V to (V_{DD} + 0.3 V) or 7 V (whichever is less)
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Thermal Resistance, θ_{JA}[2]	
SOIC (RW-24)	52°C/W
TSSOP (RU-24)	50°C/W
LFCSP (CP-32-13)	32.5°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Thermal resistance (JEDEC 4-layer (2S2P) board). Paddle soldered to board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD RATINGS FOR AD5204/AD5206

Table 3. AD5204/AD5206, 24-Lead TSSOP, 24-Lead SOIC, and 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	1000 V	1C
FICDM	1500 V	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

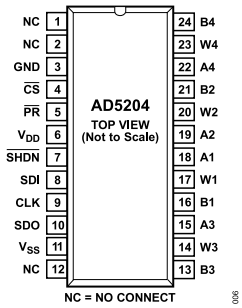

Figure 6. AD5204 SOIC/TSSOP Pin Configuration

Table 4. AD5204 SOIC/TSSOP Pin Function Descriptions

Pin No.	Name	Description
1, 2, 12	NC	Not Connected.
3	GND	Ground.
4	$\overline{CS}$	Chip Select Input (Active Low). When $\overline{CS}$ returns high, data in the serial input register is decoded based on the address bits, and then it is loaded into the target RDAC latch.
5	$\overline{PR}$	Preset to Midscale (Active Low). This pin sets the RDAC registers to 0x80.
6	V_{DD}	Positive Power Supply. This pin is specified for operation at both 3 V and 5 V. It is the sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.
7	$\overline{SHDN}$	Terminal A Open-Circuit Shutdown (Active Low Input). This pin controls VR 1 through VR 4.
8	SDI	Serial Data Input. Data is input MSB first.
9	CLK	Serial Clock Input. This pin is positive edge triggered.
10	SDO	Serial Data Output. This pin is an open-drain transistor and requires a pull-up resistor.
11	V_{SS}	Negative Power Supply. This pin is specified for operation at both 0 V and −2.7 V. It is the sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.
13	B3	Terminal B RDAC 3.
14	W3	Wiper RDAC 3. Address = 010_2.
15	A3	Terminal A RDAC 3.
16	B1	Terminal B RDAC 1.
17	W1	Wiper RDAC 1. Address = 000_2.
18	A1	Terminal A RDAC 1.
19	A2	Terminal A RDAC 2.
20	W2	Wiper RDAC 2. Address = 001_2.
21	B2	Terminal B RDAC 2.
22	A4	Terminal A RDAC 4.
23	W4	Wiper RDAC 4. Address = 011_2.
24	B4	Terminal B RDAC 4.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

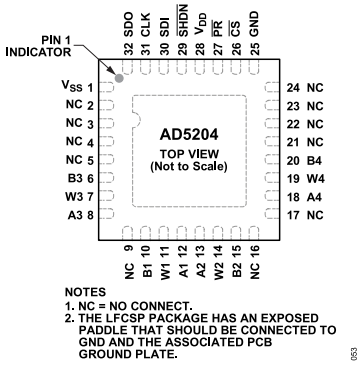

Figure 7. AD5204 LFCSP Pin Configuration

Table 5. AD5204 LFCSP Pin Function Descriptions

Pin No.	Name	Description
1	V_{SS}	Negative Power Supply. This pin is specified for operation at both 0 V and −2.7 V. It is the sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.
2 to 5, 9, 16, 17, 21 to 24	NC	Not Connected.
6	B3	Terminal B RDAC 3.
7	W3	Wiper RDAC 3. Address = 010_2.
8	A3	Terminal A RDAC 3.
10	B1	Terminal B RDAC 1.
11	W1	Wiper RDAC 1. Address = 000_2.
12	A1	Terminal A RDAC 1.
13	A2	Terminal A RDAC 2.
14	W2	Wiper RDAC 2. Address = 001_2.
15	B2	Terminal B RDAC 2.
18	A4	Terminal A RDAC 4.
19	W4	Wiper RDAC 4. Address = 011_2.
20	B4	Terminal B RDAC 4.
25	GND	Ground.
26	$\overline{CS}$	Chip Select Input (Active Low). When $\overline{CS}$ returns high, data in the serial input register is decoded based on the address bits, and then it is loaded into the target RDAC latch.
27	$\overline{PR}$	Preset to Midscale (Active Low). This pin sets the RDAC registers to 0x80.
28	V_{DD}	Positive Power Supply. This pin is specified for operation at both 3 V and 5 V. It is the sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.
29	$\overline{SHDN}$	Terminal A Open-Circuit Shutdown (Active Low Input). This pin controls VR 1 through VR 4.
30	SDI	Serial Data Input. Data is input MSB first.
31	CLK	Serial Clock Input. This pin is positive edge triggered.
32	SDO	Serial Data Output. This pin is an open-drain transistor and requires a pull-up resistor.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

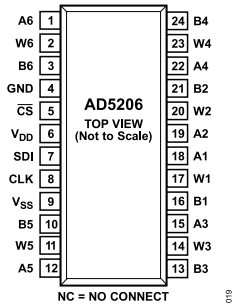

Figure 8. AD5206 SOIC/TSSOP Pin Configuration

Table 6. AD5206 Pin Function Descriptions

Pin No.	Name	Description
1	A6	Terminal A RDAC 6.
2	W6	Wiper RDAC 6. Address = 101_2.
3	B6	Terminal B RDAC 6.
4	GND	Ground.
5	$\overline{CS}$	Chip Select Input (Active Low). When $\overline{CS}$ returns high, data in the serial input register is decoded based on the address bits, and then it is loaded into the target RDAC latch.
6	V_{DD}	Positive Power Supply. This pin is specified for operation at both 3 V and 5 V. It is the sum of $\lvert V_{DD}\rvert + \lvert V_{SS}\rvert < 5.5$ V.
7	SDI	Serial Data Input. Data is input MSB first.
8	CLK	Serial Clock Input. This pin is positive edge triggered.
9	V_{SS}	Negative Power Supply. This pin is specified for operation at both 0 V and −2.7 V. It is the sum of $\lvert V_{DD}\rvert + \lvert V_{SS}\rvert < 5.5$ V.
10	B5	Terminal B RDAC 5.
11	W5	Wiper RDAC 5. Address = 100_2.
12	A5	Terminal A RDAC 5.
13	B3	Terminal B RDAC 3.
14	W3	Wiper RDAC 3. Address = 010_2.
15	A3	Terminal A RDAC 3.
16	B1	Terminal B RDAC 1.
17	W1	Wiper RDAC 1. Address = 000_2.
18	A1	Terminal A RDAC 1.
19	A2	Terminal A RDAC 2.
20	W2	Wiper RDAC 2. Address = 001_2.
21	B2	Terminal B RDAC 2.
22	A4	Terminal A RDAC 4.
23	W4	Wiper RDAC 4. Address = 011_2.
24	B4	Terminal B RDAC 4.

TYPICAL PERFORMANCE CHARACTERISTICS

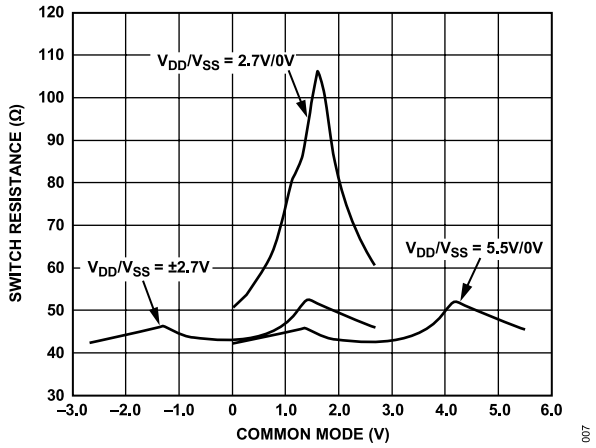

Figure 9. Incremental On Resistance of the Wiper vs. Voltage

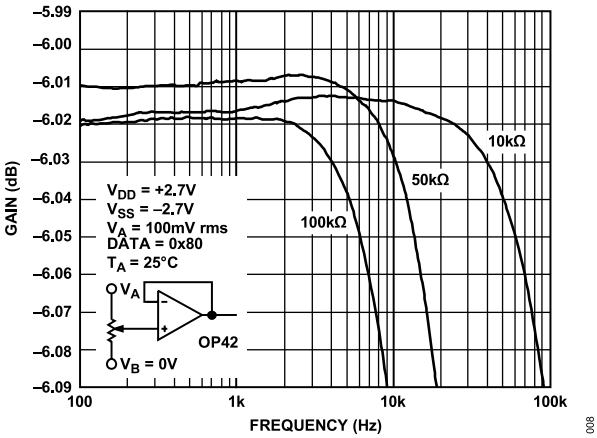

Figure 10. Gain Flatness vs. Frequency

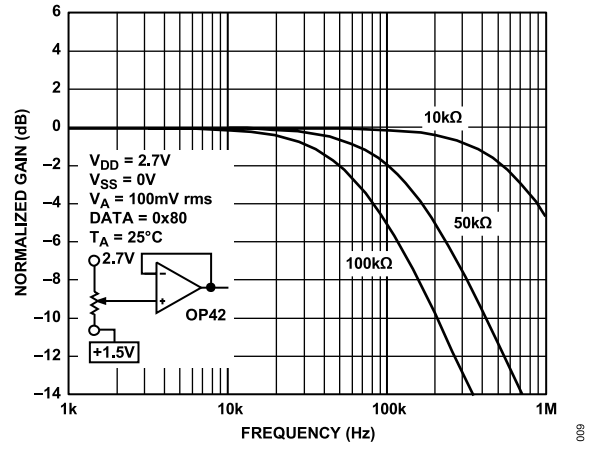

Figure 11. −3 dB Bandwidth vs. Terminal Resistance, 2.7 V Single-Supply Operation

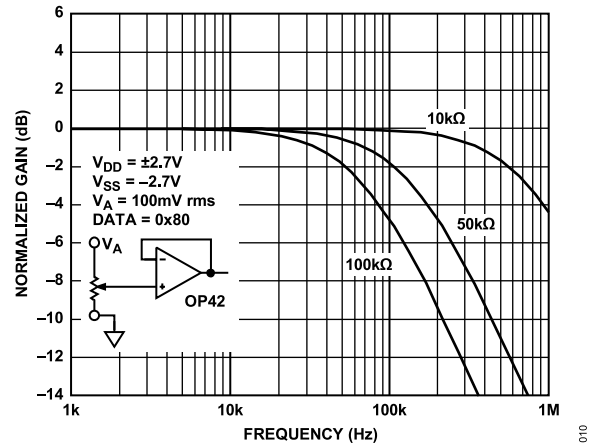

Figure 12. −3 dB Bandwidth vs. Terminal Resistance, ±2.7 V Dual-Supply Operation

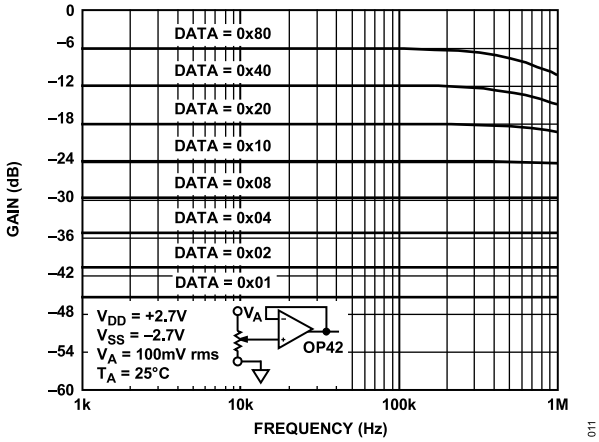

Figure 13. Bandwidth vs. Code, 10 kΩ Version

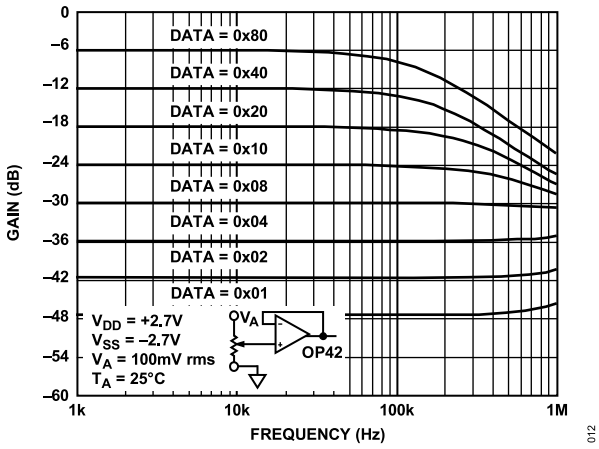

Figure 14. Bandwidth vs. Code, 50 kΩ Version

TYPICAL PERFORMANCE CHARACTERISTICS

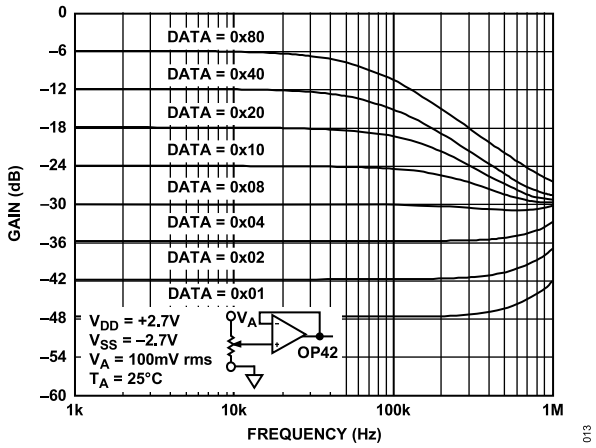

Figure 15. Bandwidth vs. Code, 100 kΩ Version

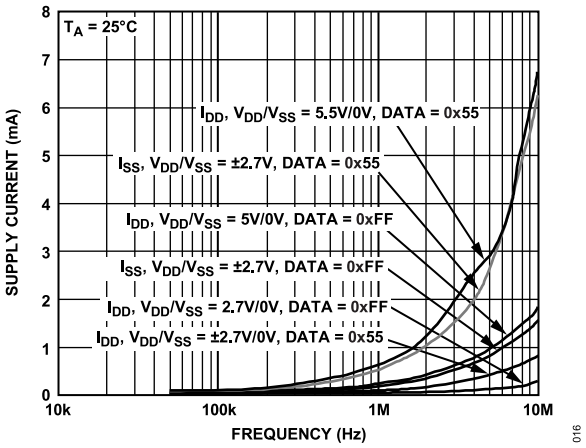

Figure 18. Supply Current vs. Clock Frequency

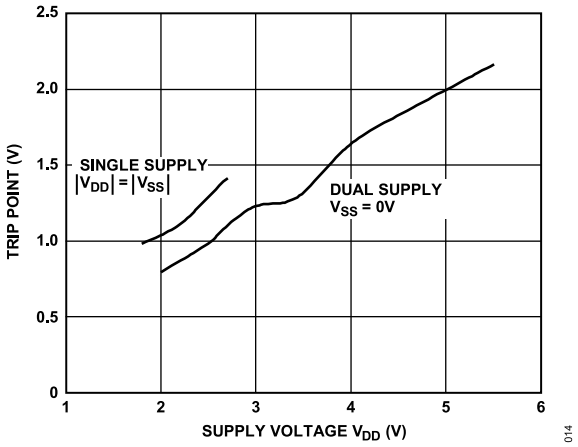

Figure 16. Digital Input Trip Point vs. Supply Voltage

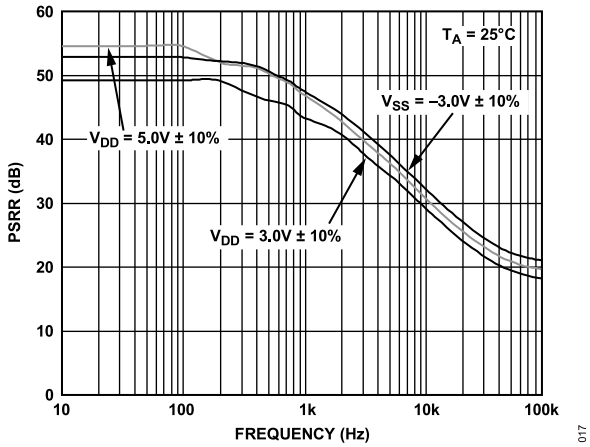

Figure 19. Power Supply Rejection vs. Frequency

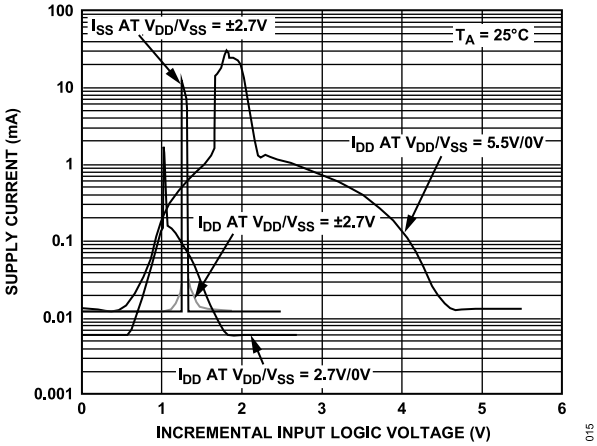

Figure 17. Supply Current vs. Input Logic Voltage

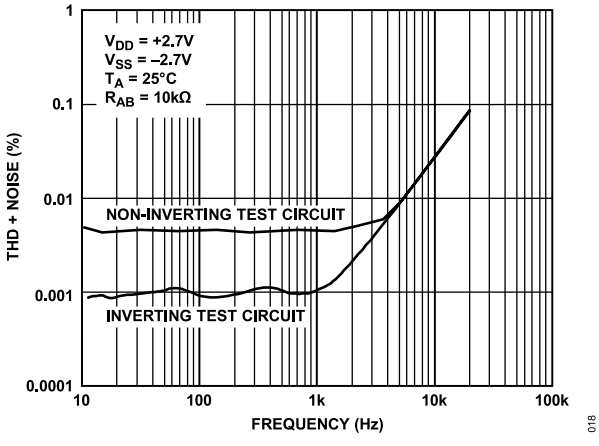

Figure 20. Total Harmonic Distortion Plus Noise vs. Frequency

TEST CIRCUITS

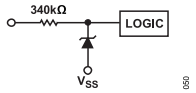

Figure 21. ESD Protection of Digital Pins

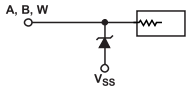

Figure 22. ESD Protection of Resistor Terminals

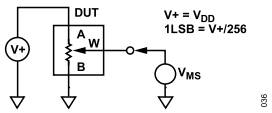

Figure 23. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

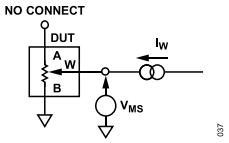

Figure 24. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

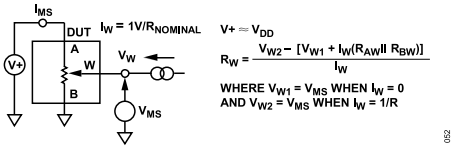

Figure 25. Wiper Resistance Test Circuit

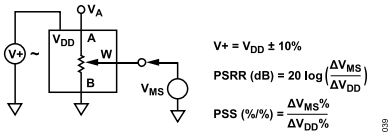

Figure 26. Power Supply Sensitivity Test Circuit (PSS, PSRR)

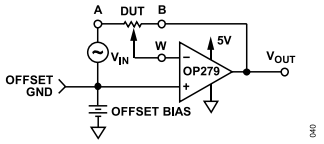

Figure 27. Inverting Programmable Gain Test Circuit

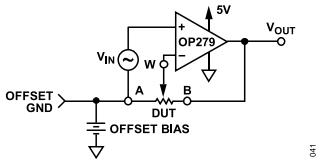

Figure 28. Noninverting Programmable Gain Test Circuit

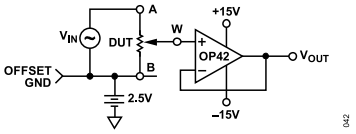

Figure 29. Gain vs. Frequency Test Circuit

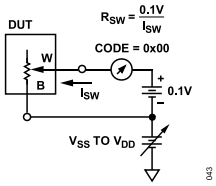

Figure 30. Incremental On-Resistance Test Circuit

THEORY OF OPERATION

The AD5204 provides a 4-channel, 256-position digitally controlled VR device, and the AD5206 provides a 6-channel, 256-position digitally controlled VR device. Changing the programmed VR settings is accomplished by clocking an 11-bit serial data-word into the SDI pin. The format of this data-word is three address bits, MSB first, followed by eight data bits, MSB first. Table 7 provides the serial register data-word format.

Table 7. Serial Data-Word Format

Address			Data							
B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB		LSB	MSB							LSB
2^{10}		2^8	2^7							2^0

See Table 11 for the AD5204/AD5206 address assignments to decode the location of the VR latch receiving the serial register data in Bit B7 through Bit B0. The VR outputs can be changed one at a time in random sequence. The AD5204 presets to midscale by asserting the $\overline{PR}$ pin, simplifying fault condition recovery at power up. Both parts have an internal power-on preset that places the wiper in a preset midscale condition at power on. In addition, the AD5204 contains a power shutdown pin ($\overline{SHDN}$) that places the RDAC in a zero power consumption state, where terminals Ax are open circuited and wipers Wx are connected to terminals Bx, resulting in only leakage currents being consumed in the VR structure. In shutdown mode, the VR latch settings are maintained so that the VR settings return to their previous resistance values when the device is returned to operational mode from power shutdown.

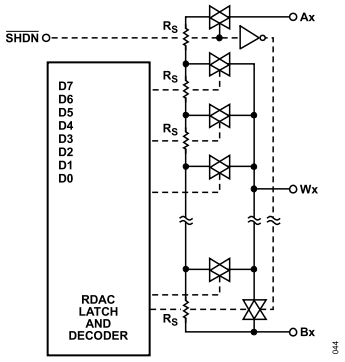

Figure 31. AD5204/AD5206 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available with values of 10 kΩ, 50 kΩ, and 100 kΩ. The last digits of the part number determine the nominal resistance value; for example, 10 kΩ = 10 and 100 kΩ = 100. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus Terminal B contact. The 8-bit data-word in the RDAC latch is decoded to select one of the 256 possible settings.

The first connection of the wiper starts at Terminal B for the 0x00 data. This Terminal B connection has a wiper contact resistance of 45 Ω. The second connection (for a 10 kΩ part) is the first tap point, located at 84 Ω [= R_{AB} (nominal resistance)/256 + R_W = 39 Ω + 45 Ω] for the 0x01 data. The third connection is the next tap point, representing 78 + 45 = 123 Ω for the 0x02 data. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,006 Ω. The wiper does not directly connect to Terminal A. See Figure 31 for a simplified diagram of the equivalent RDAC circuit.

The general transfer equation determining the digitally programmed output resistance between the Wx and Bx terminals is

$$R_{WB}(Dx) = (Dx)/256 \times R_{AB} + R_W \quad (1)$$

where Dx is the data contained in the 8-bit RDACx latch, and R_{AB} is the nominal end-to-end resistance.

For example, when V_B = 0 V and Terminal A is open circuited, the output resistance values are set as outlined in Table 8 for the RDAC latch codes (applies to the 10 kΩ potentiometer).

Table 8. Output Resistance Values for the RDAC Latch Codes—V_B = 0 V and Terminal A = Open Circuited

D (Dec)	R_{WB} (Ω)	Output State
255	10006	Full scale
128	5045	Midscale ($\overline{PR}$ = 0 condition)
1	84	1 LSB
0	45	Zero scale (wiper contact resistance)

In the zero-scale condition, a finite total wiper resistance of 45 Ω is present. Regardless of which setting the part is operating in, care should be taken to limit the current between Terminal A to Terminal B, Wiper W to Terminal A, and Wiper W to Terminal B, to the maximum continuous current of ±5.65 mA(10 kΩ) or ±1.35 mA(50 kΩ and 100 kΩ) or pulse current of ±20 mA. Otherwise, degradation or possible destruction of the internal switch contact, can occur.

Like the mechanical potentiometer that the RDAC replaces, the RDAC is completely symmetrical. The resistance between Wiper W and Terminal A produces a digitally controlled resistance, R_{WA}. When these terminals are used, Terminal B should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded to the latch is increased in value. The general transfer equation for this operation is

$$R_{WA}(Dx) = (256 - Dx)/256 \times R_{AB} + R_W \quad (2)$$

where Dx is the data contained in the 8-bit RDACx latch, and R_{AB} is the nominal end-to-end resistance.

For example, when V_A = 0 V and Terminal B is tied to Wiper W, the output resistance values outlined in Table 9 are set for the RDAC latch codes.

THEORY OF OPERATION

Table 9. Output Resistance Values for the RDAC Latch Codes—V_A = 0 V and Terminal B Tied to Wiper W

D (DEC)	R_{WA} (Ω)	Output State
255	84	Full scale
128	5045	Midscale ($\overline{PR}$ = 0 condition)
1	10006	1 LSB
0	10045	Zero scale

The typical distribution of R_{AB} from channel to channel matches to within ±1%. However, device-to-device matching is process lot dependent, having a ±30% variation. The change in R_{AB} in terms of temperature has a 700 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the wiper that can be any value from 0 V up to 1 LSB less than +5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256-position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to Terminal A and Terminal B is

$$V_W(Dx) = Dx/256 \times V_{AB} + V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. In this mode, the output voltage is dependent on the ratio of the internal resistors, not the absolute value; therefore, the drift improves to 15 ppm/°C.

DIGITAL INTERFACING

The AD5204/AD5206 each contain a standard 3-wire serial input control interface. The three inputs are clock (CLK), chip select input ($\overline{CS}$), and serial data input (SDI). The positive-edge-sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or by other suitable means. Figure 32 shows more detail of the internal digital circuitry. When $\overline{CS}$ is taken active low, the clock loads data into the serial register on each positive clock edge (see Table 10). When using a positive (V_{DD}) and negative (V_{SS}) supply voltage, the logic levels are still referenced to digital ground (GND).

The serial data output (SDO) pin contains an open-drain n-channel FET. This output requires a pull-up resistor to transfer data to the SDI pin of the next package. The pull-up resistor termination voltage can be larger than the V_{DD} supply of the AD5204. For example, the AD5204 can operate at V_{DD} = 3.3 V, and the pull-up for the interface to the next device can be set at 5 V. This allows for daisy chaining several RDACs from a single-processor serial data line.

If a pull-up resistor is used to connect the SDI pin of the next device in the series, the clock period must be increased. Capacitive loading at the daisy-chain node (where SDO and SDI are connected) between the devices must be accounted for to successfully transfer data. When daisy chaining is used, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers, ensuring that the address bits and data bits are in the proper decoding locations. This requires 22 bits of address and data complying with the data-word format outlined in Table 7 if two AD5204 4-channel RDACs are daisy-chained. During shutdown ($\overline{SHDN}$), the SDO output pin is forced to the off (logic high state) position to disable power dissipation in the pull-up resistor. See Figure 34 for the equivalent SDO output circuit schematic.

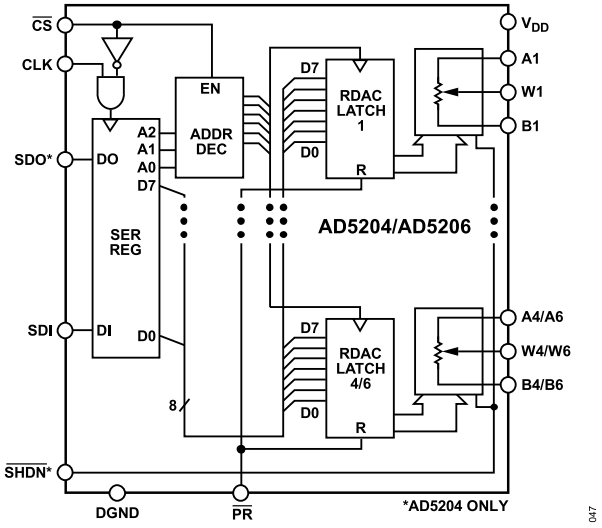

Figure 32. Block Diagram

Table 10. Input Logic Control Truth Table[1]

CLK	$\overline{CS}$	$\overline{PR}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect; enables SDO pin.
P	L	H	H	Shift one bit in from the SDI pin. The 11th bit entered is shifted out of the SDO pin.
X	P	H	H	Load SR data into the RDAC latch based on A2, A1, A0 decode (Table 11).
X	H	H	H	No operation.
X	X	L	H	Sets all RDAC latches to midscale; wiper centered and SDO latch cleared.
X	H	P	H	Latches all RDAC latches to 0x80.
X	H	H	L	Open circuits all A resistor terminals, connects Wiper W to Terminal B, and turns off the SDO output transistor.

[1] P = positive edge, X = don't care, SR = shift register.

THEORY OF OPERATION

Table 11. Address Decode Table

A2	A1	A0	Latch Decoded
0	0	0	RDAC 1
0	0	1	RDAC 2
0	1	0	RDAC 3
0	1	1	RDAC 4
1	0	0	RDAC 5 AD5206 only
1	0	1	RDAC 6 AD5206 only

The data setup and data hold times in the specification table determine the data valid time requirements. The last 11 bits of the data-word entered into the serial register are held when $\overline{CS}$ returns high. When $\overline{CS}$ goes high, the address decoder is gated, enabling one of four or six positive-edge-triggered RDAC latches (see Figure 33 for details).

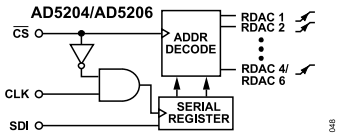

Figure 33. Equivalent Input Control Logic

The target RDAC latch is loaded with the last eight bits of the serial data-word, completing one DAC update. Four separate 8-bit data-words must be clocked in to change all four VR settings.

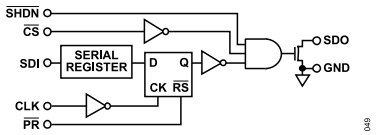

Figure 34. Detail SDO Output Schematic of the AD5204

All digital pins ($\overline{CS}$, SDI, SDO, $\overline{PR}$, $\overline{SHDN}$, and CLK) are protected with a series input resistor and a parallel Zener ESD structure (see Figure 21).

OUTLINE DIMENSIONS

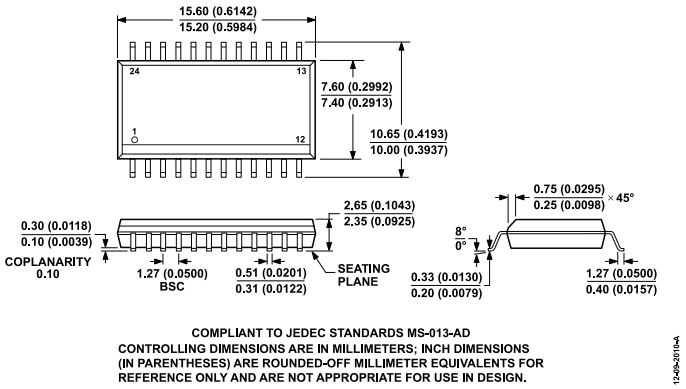

Figure 35. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)

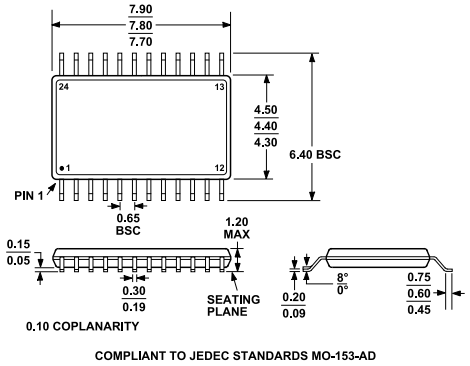

Figure 36. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

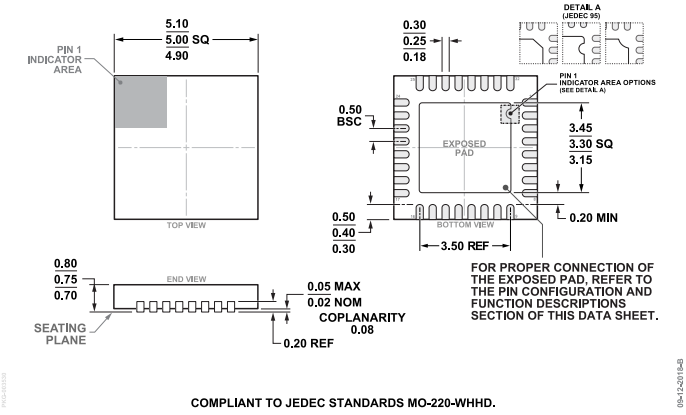

Figure 37. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-13)
Dimensions shown in millimeters