Data Sheet

AD5241/AD5242

I²C-Compatible 256-Position Digital Potentiometers

FEATURES

- 256 positions
- 10 kΩ, 100 kΩ, 1 MΩ
- Low temperature coefficient: 30 ppm/°C
- Internal power on midscale preset
- Single-supply 2.7 V to 5.5 V or dual-supply ±2.7 V for ac or bipolar operation
- I²C-compatible interface with readback capability
- Extra programmable logic outputs
- Self contained shutdown feature
- Extended temperature range: −40°C to +105°C

APPLICATIONS

- Multimedia, video, and audio
- Communications
- Mechanical potentiometer replacement
- Instrumentation: gain, offset adjustment
- Programmable voltage-to-current conversion
- Line impedance matching

FUNCTIONAL BLOCK DIAGRAM

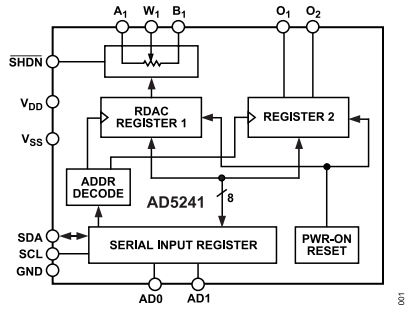

Figure 1. AD5241 Functional Block Diagram

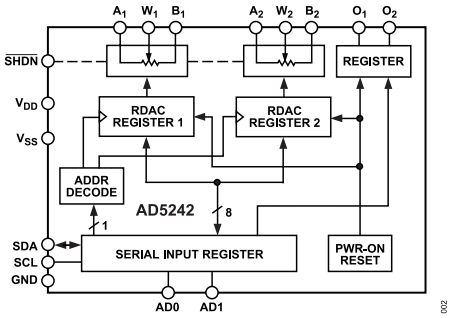

Figure 2. AD5242 Functional Block Diagram

GENERAL DESCRIPTION

The AD5241/AD5242[1] provide a single-/dual-channel, 256-position, digitally controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a potentiometer, trimmer, or variable resistor. Each VR offers a completely programmable value of resistance between the A terminal and the wiper, or the B terminal and the wiper. For the AD5242, the fixed A-to-B terminal resistance of 10 kΩ, 100 kΩ, or 1 MΩ has a 1% channel-to-channel matching tolerance. The nominal temperature coefficient of both parts is 30 ppm/°C.

Wiper position programming defaults to midscale at system power on. When powered, the VR wiper position is programmed by an I²C-compatible, 2-wire serial data interface. Both parts have two extra programmable logic outputs available that enable users to drive digital loads, logic gates, LED drivers, and analog switches in their system.

The AD5241/AD5242 are available in surface-mount, 14-lead SOIC and 16-lead SOIC packages and, for ultracompact solutions, 14-lead TSSOP and 16-lead TSSOP packages. All parts are guaranteed to operate over the extended temperature range of −40°C to +105°C.

[1] Patent Number 5,495,245 applies.

Rev. E

TABLE OF CONTENTS

REVISION HISTORY

1/2022—Rev. D to Rev. E

Deleted Interface Timing Characteristics Parameter, Table 1 ... 3
Changes to Power Single-Supply Range Parameter and Power Dual-Supply Range Parameter, Table 1 ... 3
Added Timing Specifications Section and Table 2; Renumbered Sequentially ... 4
Moved Figure 32 ... 14
Changes to Ordering Guide ... 17

SPECIFICATIONS

10 KΩ, 100 KΩ, 1 MΩ VERSION

V_{DD} = 2.7 V to 5.5 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE (SPECIFICATIONS APPLY TO ALL VRs)						
Resolution	N		8			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.4	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±0.5	+2	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	T_A = 25°C, R_{AB} = 10 kΩ	−30		+30	%
		T_A = 25°C, R_{AB} = 100 kΩ/1 MΩ	−30		+50	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	$V_{AB} = V_{DD}$, wiper = no connect		30		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$		60	120	Ω
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE (SPECIFICATIONS APPLY TO ALL VRs)						
Resolution	N		8			Bits
Differential Nonlinearity[3]	DNL		−1	±0.4	+1	LSB
Integral Nonlinearity[3]	INL		−2	±0.5	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = 0x80		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−1	−0.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	0.5	1	LSB
RESISTOR TERMINALS						
Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance (A, B)[5]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance (W)[5]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS						
Input Logic High (SDA and SCL)	V_{IH}		0.7 × V_{DD}		V_{DD} + 0.5 V	V
Input Logic Low (SDA and SCL)	V_{IL}		−0.5		+0.3 × V_{DD}	V
Input Logic High (AD0 and AD1)	V_{IH}	V_{DD} = 5 V	2.4		V_{DD}	V
Input Logic Low (AD0 and AD1)	V_{IL}	V_{DD} = 5 V	0		0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1		V_{DD}	V
Input Logic Low	V_{IL}	V_{DD} = 3 V	0		0.6	V
Input Current	I_{IL}	V_{IH} = 5 V or V_{IL} = GND			1	µA
Input Capacitance[5]	C_{IL}			3		pF
DIGITAL OUTPUT	V_{OL}	I_{OL} = 3 mA			0.4	V
Output Logic Low (SDA)	V_{OL}	I_{OL} = 6 mA			0.6	V
Output Logic Low (O_1 and O_2)	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
Output Logic High (O_1 and O_2)	V_{OH}	I_{SOURCE} = 40 µA	4			V
Three-State Leakage Current (SDA)	I_{OZ}	V_{IH} = 5 V or V_{IL} = GND			±1	µA
Output Capacitance[5]	C_{OZ}			3	8	pF
POWER SUPPLIES						
Power Single-Supply Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Power Dual-Supply Range	V_{DD}/V_{SS}		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = GND		0.1	50	µA
Negative Supply Current	I_{SS}	V_{SS} = −2.5 V, V_{DD} = +2.5 V		+0.1	−50	µA

SPECIFICATIONS

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Power Dissipation[6]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND, V_{DD} = 5 V		0.5	250	µW
Power Supply Sensitivity	PSS		−0.01	+0.002	+0.01	%/%
DYNAMIC CHARACTERISTICS[5, 7, 8]						
−3 dB Bandwidth	BW_10 kΩ	R_{AB} = 10 kΩ, code = 0x80		650		kHz
	BW_100 kΩ	R_{AB} = 100 kΩ, code = 0x80		69		kHz
	BW_1 MΩ	R_{AB} = 1 MΩ, code = 0x80		6		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.005		%
V_W Settling Time	t_S	V_A = V_{DD}, V_B = 0 V, ± 1 LSB error band, R_{AB} = 10 kΩ		2		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		14		nV√Hz

1 Typicals represent average readings at 25°C, V_{DD} = 5 V.

2 Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Test Circuits.

3 INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See Figure 37.

4 Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.

5 Guaranteed by design, not subject to production test.

6 P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

7 Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

8 All dynamic characteristics use V_{DD} = 5 V.

TIMING SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INTERFACE TIMING CHARACTERISTICS (APPLIES TO ALL PARTS[1, 2])						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between Stop and Start, t_{BUF}	t_1		1.3			µs
Hold Time (Repeated Start), $t_{HD;\ STA}$	t_2	After this period, the first clock pulse is generated	600			ns
Low Period of SCL Clock, t_{LOW}	t_3		1.3			µs
High Period of SCL Clock, t_{HIGH}	t_4		0.6		50	µs
Setup Time for Repeated Start Condition, $t_{SU;\ STA}$	t_5		600			ns
Data Hold Time, $t_{HD;\ DAT}$	t_6				900	ns
Data Setup Time, $t_{SU;\ DAT}$	t_7		100			ns
Rise Time of Both SDA and SCL Signals, t_R	t_8				300	ns
Fall Time of Both SDA and SCL Signals, t_F	t_9				300	ns
Setup Time for Stop Condition, $t_{SU;\ STO}$	t_{10}		0.6			µs

1 Guaranteed by design, not subject to production test.

2 See timing diagram in Figure 3 for location of measured values.

SPECIFICATIONS

TIMING DIAGRAMS

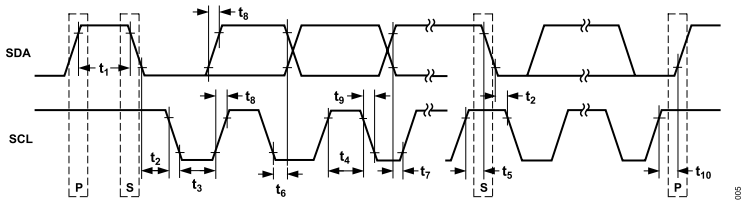

Figure 3. Detail Timing Diagram

Data of AD5241/AD5242 is accepted from the I²C bus in the following serial format.

Table 3.

S	0	1	0	1	1	AD1	AD0	R/$\overline{W}$	A	$\overline{A}$/B	R S	SD	O_1	O_2	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

where:
S = start condition
P = stop condition
A = acknowledge
X = don't care
AD1, AD0 = Package pin programmable address bits. Must be matched with the logic states at Pin AD1 and Pin AD0.
R/$\overline{W}$ = Read enable at high and output to SDA. Write enable at low.
$\overline{A}$/B = RDAC subaddress select; 0 for RDAC1 and 1 for RDAC2.
RS = Midscale reset, active high.
SD = Shutdown in active high. Same as except inverse logic.
O_1, O_2 = Output logic pin latched values
D7, D6, D5, D4, D3, D2, D1, D0 = data bits.

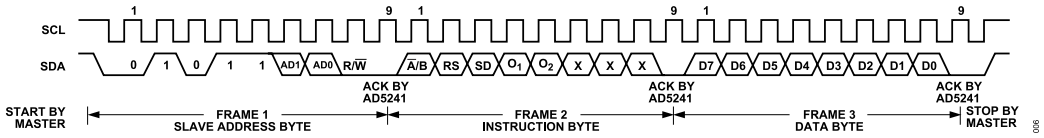

Figure 4. Writing to the RDAC Serial Register

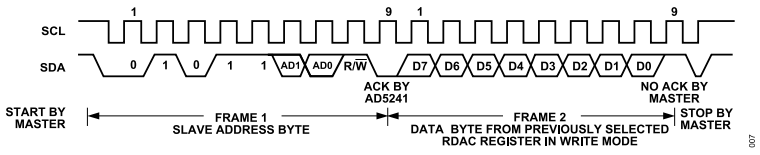

Figure 5. Reading Data from a Previously Selected RDAC Register in Write Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	0 V to −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS} to V_{DD}
I_A, I_B, I_W	
R_{AB} = 10 kΩ in TSSOP-14	5.0 mA[1]
R_{AB} = 100 kΩ in TSSOP-14	1.5 mA[1]
R_{AB} = 1 MΩ in TSSOP-14	0.5 mA[1]
Digital Input Voltage to GND	0 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Thermal Resistance θ_{JA}	
14-Lead SOIC	158°C/W
16-Lead SOIC	73°C/W
14-Lead TSSOP	206°C/W
16-Lead TSSOP	180°C/W
Maximum Junction Temperature (T_J max)	150°C
Package Power Dissipation	$P_D = (T_J \text{ max} - T_A)/\theta_{JA}$
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Vapor Phase, 60 sec	215°C
Infrared, 15 sec	220°C

[1] Maximum current increases at lower resistance and different packages.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

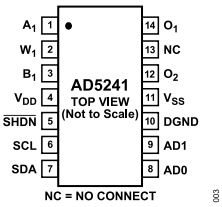

Figure 6. AD5241 Pin Configuration

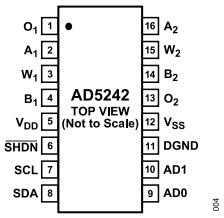

Figure 7. AD5242 Pin Configuration

Table 5. AD5241 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A_1	Resistor Terminal A_1.
2	W_1	Wiper Terminal W_1.
3	B_1	Resistor Terminal B_1.
4	V_{DD}	Positive Power Supply, Specified for Operation from 2.2 V to 5.5 V.
5	$\overline{SHDN}$	Active low, asynchronous connection of Wiper W to Terminal B, and open circuit of Terminal A. RDAC register contents unchanged. $\overline{SHDN}$ should tie to V_{DD} if not used.
6	SCL	Serial Clock Input.
7	SDA	Serial Data Input/Output.
8	AD0	Programmable Address Bit for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
9	AD1	Programmable Address Bit for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
10	DGND	Common Ground.
11	V_{SS}	Negative Power Supply, Specified for Operation from 0 V to −2.7 V.
12	O_2	Logic Output Terminal O_2.
13	NC	No Connect.
14	O_1	Logic Output Terminal O_1.

Table 6. AD5242 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	O_1	Logic Output Terminal O_1.
2	A_1	Resistor Terminal A_1.
3	W_1	Wiper Terminal W_1.
4	B_1	Resistor Terminal B_1.
5	V_{DD}	Positive Power Supply, Specified for Operation from 2.2 V to 5.5 V.
6	$\overline{SHDN}$	Active Low, Asynchronous Connection of Wiper W to Terminal B, and Open Circuit of Terminal A. RDAC register contents unchanged. $\overline{SHDN}$ should tie to V_{DD}, if not used.
7	SCL	Serial Clock Input.
8	SDA	Serial Data Input/Output.
9	AD0	Programmable Address Bit for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
10	AD1	Programmable Address Bit for Multiple Package Decoding. Bit AD0 and Bit AD1 provide four possible addresses.
11	DGND	Common Ground.
12	V_{SS}	Negative Power Supply, Specified for Operation from 0 V to −2.7 V.
13	O_2	Logic Output Terminal O_2.
14	B_2	Resistor Terminal B_2.
15	W_2	Wiper Terminal W_2.
16	A_2	Resistor Terminal A_2.

TYPICAL PERFORMANCE CHARACTERISTICS

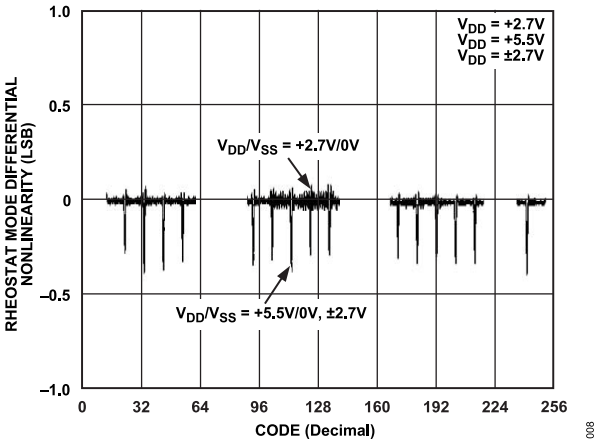

Figure 8. RDNL vs. Code

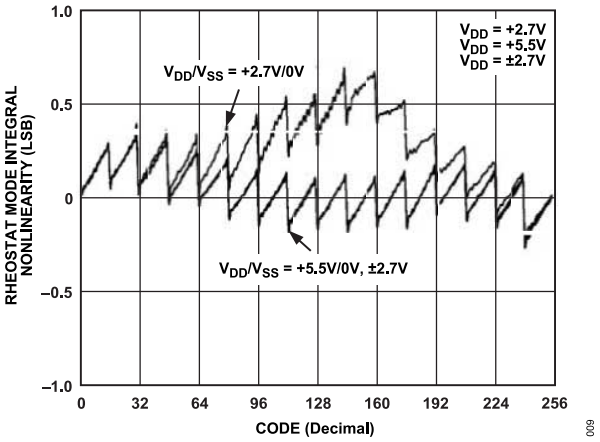

Figure 9. RINL vs. Code

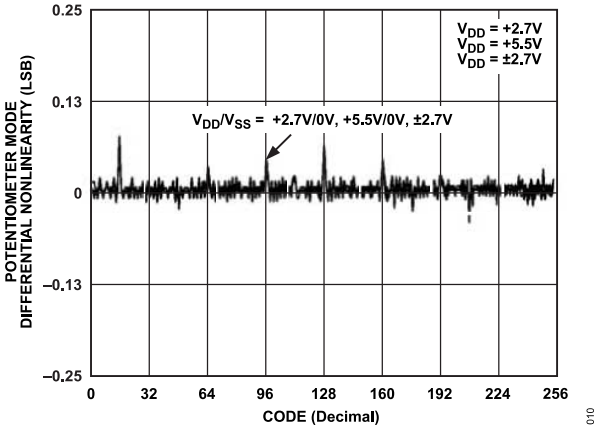

Figure 10. DNL vs. Code

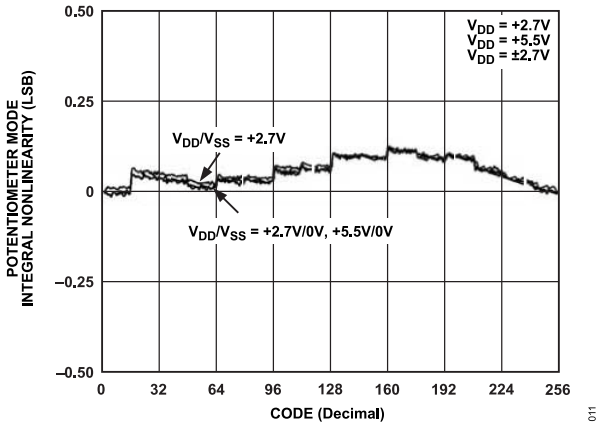

Figure 11. INL vs. Code

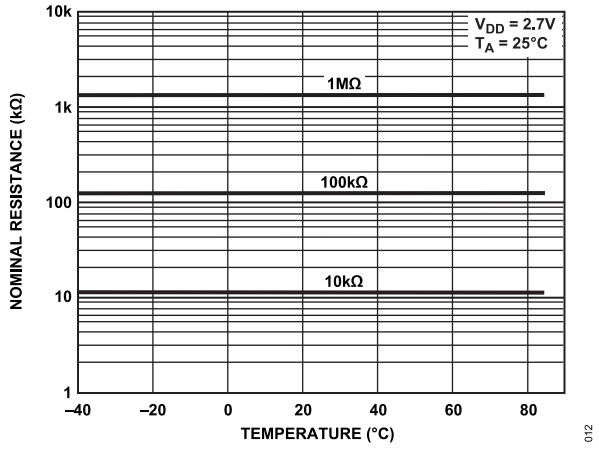

Figure 12. Nominal Resistance vs. Temperature

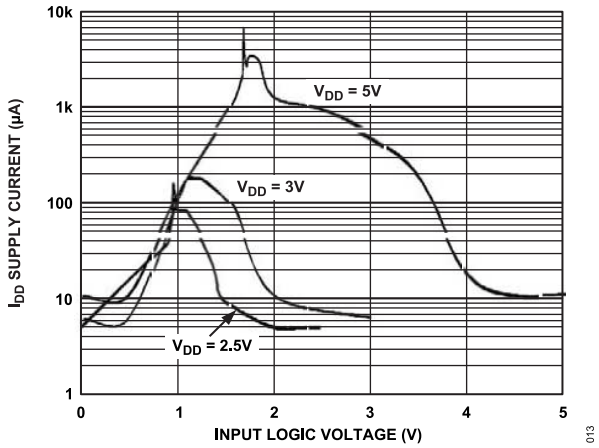

Figure 13. Supply Current vs. Input Logic Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

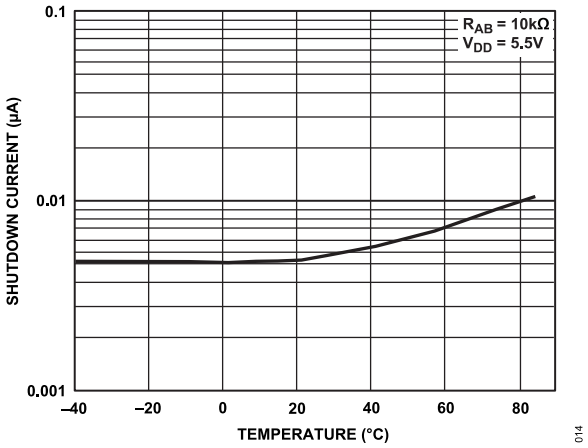

Figure 14. Shutdown Current vs. Temperature

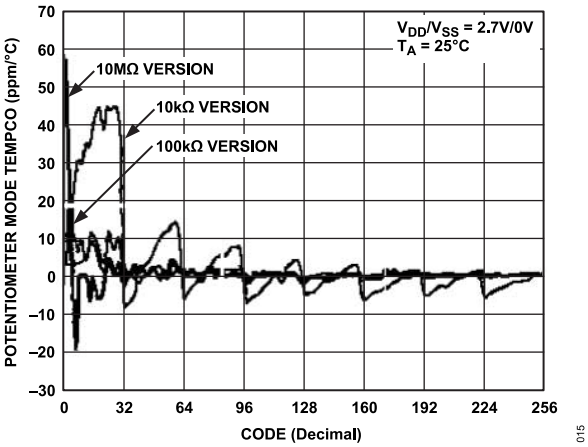

Figure 15. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Temperature Coefficient

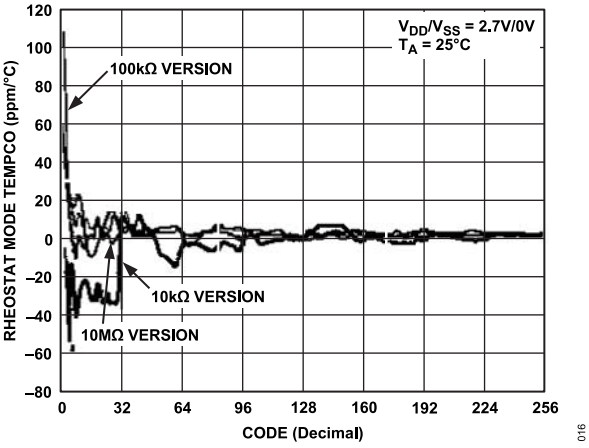

Figure 16. $\Delta R_{WB}/\Delta T$ Rheostat Mode Temperature Coefficient

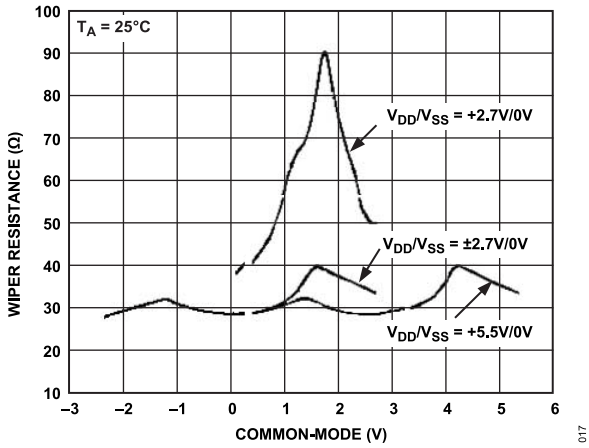

Figure 17. Incremental Wiper Contact vs. V_{DD}/V_{SS}

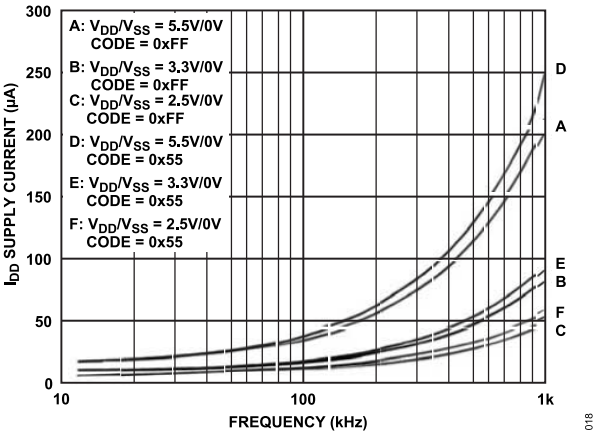

Figure 18. Supply Current vs. Frequency

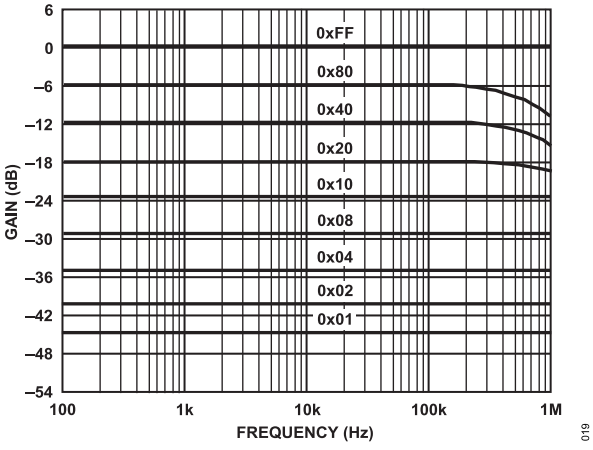

Figure 19. AD5242 10 k Ω Gain vs. Frequency vs. Code

TYPICAL PERFORMANCE CHARACTERISTICS

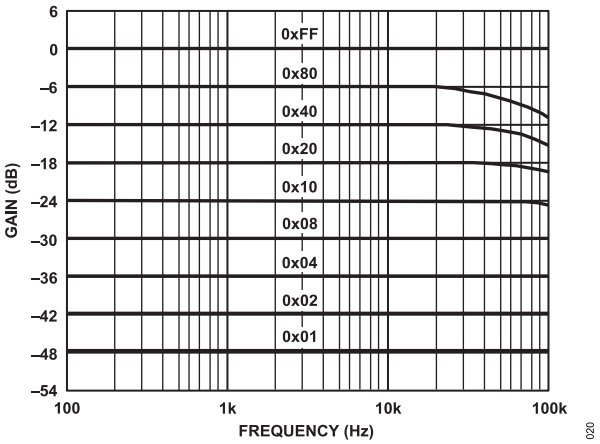

Figure 20. AD5242 100 kΩ Gain vs. Frequency vs. Code

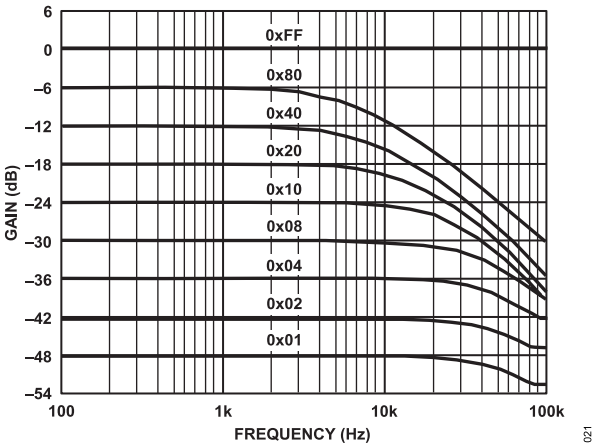

Figure 21. AD5242 1 MΩ Gain vs. Frequency vs. Code

TEST CIRCUITS

Figure 22 to Figure 30 define the test conditions used in the product specifications table.

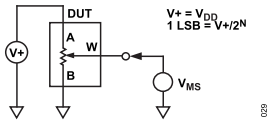

Figure 22. Potentiometer Divider Nonlinearity Error (INL, DNL)

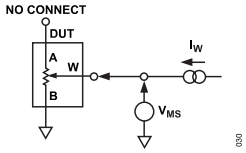

Figure 23. Resistor Position Nonlinearity Error(Rheostat Operation; R-INL, R-DNL)

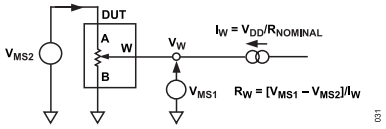

Figure 24. Wiper Resistance

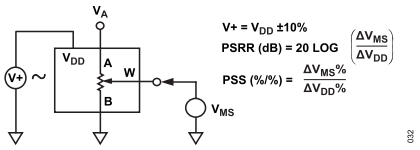

Figure 25. Power Supply Sensitivity (PSS, PSRR)

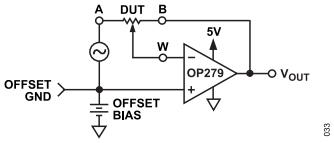

Figure 26. Inverting Gain

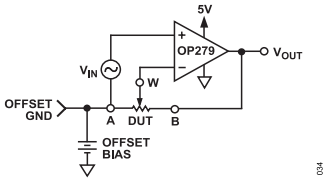

Figure 27. Noninverting Gain

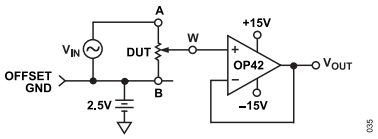

Figure 28. Gain vs. Frequency

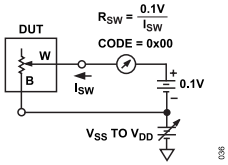

Figure 29. Incremental On Resistance

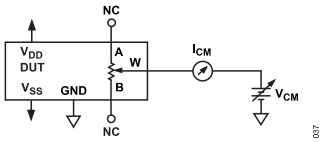

Figure 30. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5241/AD5242 provide a single-/dual-channel, 256-position digitally controlled variable resistor (VR) device. The terms VR, RDAC, and programmable resistor are commonly used interchangeably to refer to digital potentiometer.

To program the VR settings, refer to the Digital Interface section. Both parts have an internal power-on preset that places the wiper in midscale during power-on that simplifies the fault condition recovery at power-up. In addition, the shutdown pin ($\overline{SHDN}$) of AD5241/AD5242 places the RDAC in an almost zero power consumption state where Terminal A is open circuited and Wiper W is connected to Terminal B, resulting in only leakage current being consumed in the VR structure. During shutdown, the VR latch contents are maintained when the RDAC is inactive. When the part returns from shutdown, the stored VR setting is applied to the RDAC.

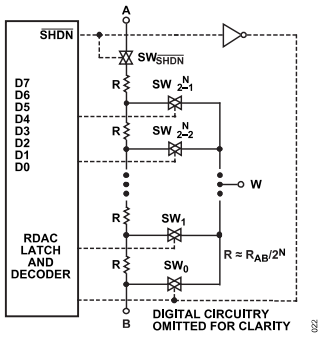

Figure 31. Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 10 kΩ, 100 kΩ, and 1 MΩ. The final two or three digits of the part number determine the nominal resistance value, for example, 10 kΩ = 10, 100 kΩ = 100, and 1 MΩ = 1 M. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 kΩ part is used; the first connection of the wiper starts at the B terminal for Data 0x00. Because there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between Terminal W and Terminal B. The second connection is the first tap point that corresponds to 99 Ω (R_{WB} = R_{AB}/256 + R_W = 39 + 60) for Data 0x01. The third connection is the next tap point representing 138 Ω (39 × 2 + 60) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,021 Ω [R_{AB} – 1 LSB + R_W].

Figure 31 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string is not accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code between 0 and 255, which is loaded in the 8-bit RDAC register.
R_{AB} is the nominal end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

Again, if R_{AB} = 10 kΩ, Terminal A can be either open circuit or tied to W. Table 7 shows the R_{WB} resistance based on the code set in the RDAC latch.

Table 7. R_{WB} (D) at Selected Codes for R_{AB} = 10 kΩ

D (DEC)	R_{WB} (Ω)	Output State
255	10,021	Full-scale (R_{WB} – 1 LSB + R_W)
128	5060	Midscale
1	99	1 LSB
0	60	Zero-scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled resistance, R_{WA}. When these terminals are used, Terminal B can be opened or tied to the wiper terminal. The minimum R_{WA} resistance is for Data 0xFF and increases as the data loaded in the latch decreases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For R_{AB} = 10 kΩ, Terminal B can be either open circuit or tied to W. Table 8 shows the R_{WA} resistance based on the code set in the RDAC latch.

Table 8. R_{WA} (D) at Selected Codes for R_{AB} = 10 kΩ

D (DEC)	R_{WA} (Ω)	Output State
255	99	Full-scale
128	5060	Midscale
1	10,021	1 LSB
0	10,060	Zero-scale

The typical distribution of the nominal resistance R_{AB} from channel to channel matches within ±1% for AD5242. Device-to-device matching is process lot dependent, and it is possible to have ±30% variation. Because the resistance element is processed in thin film

THEORY OF OPERATION

technology, the change in R_{AB} with temperature has no more than a 30 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates output voltages at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} /V_{SS}, which must be positive, voltage across terminal A to terminal B, terminal W to terminal A, and terminal W to terminal B can be at either polarity provided that V_{SS} is powered by a negative supply.

If ignoring the effect of the wiper resistance for approximation, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal AB divided by the 256 positions of the potentiometer divider. Because AD5241/AD5242 can be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \quad (3)$$

which can be simplified to

$$V_W(D) = \frac{D}{256}V_{AB} + V_B \quad (4)$$

where *D* is the decimal equivalent of the binary code between 0 to 255 that is loaded in the 8-bit RDAC register.

For a more accurate calculation, including the effects of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (5)$$

where $R_{WB}(D)$ and $R_{WA}(D)$ can be obtained from Equation 1 and Equation 2.

Operation of the digital potentiometer in divider mode results in a more accurate operation over temperature. Unlike rheostat mode, the output voltage is dependent on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values; therefore, the temperature drift reduces to 5 ppm/°C.

DIGITAL INTERFACE

2-Wire Serial Bus

The AD5241/AD5242 are controlled via an I²C-compatible serial bus. The RDACs are connected to this bus as slave devices.

Referring to Figure 3 and Figure 4, the first byte of AD5241/AD5242 is a slave address byte. It has a 7-bit slave address and an R/ bit. The five MSBs are 01011 and the following two bits are determined by the state of the AD0 and AD1 pins of the device. AD0 and AD1 allow users to use up to four of these devices on one bus.

The 2-wire, I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 4). The following byte is the Frame 1, slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device).
2. The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. If the R/$\overline{W}$ bit is low, the master writes to the slave device.
3. A write operation contains an extra instruction byte more than the read operation. The Frame 2 instruction byte in write mode follows the slave address byte. The MSB of the instruction byte labeled $\overline{A}$/B is the RDAC subaddress select. A low selects RDAC1 and a high selects RDAC2 for the dual-channel AD5242. Set $\overline{A}$/B to low for the AD5241. The second MSB, RS, is the midscale reset. A logic high of this bit moves the wiper of a selected RDAC to the center tap where R_{WA} = R_{WB}. The third MSB, SD, is a shutdown bit. A logic high on SD causes the RDAC to open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost a 0 Ω rheostat mode or 0 V in potentiometer mode. This SD bit serves the same function as the $\overline{SHDN}$ pin except that the $\overline{SHDN}$ pin reacts to active low. The following two bits are O_2 and O_1. They are extra programmable logic outputs that users can use to drive other digital loads, logic gates, LED drivers, analog switches, and the like. The three LSBs are don't care (see Figure 4).
4. After acknowledging the instruction byte, the last byte in write mode is the, Frame 3 data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 4).
5. Unlike the write mode, the data byte follows immediately after the acknowledgment of the slave address byte in Frame 2 read mode. Data is transmitted over the serial bus in sequences of nine clock pulses (slightly different from the write mode, there are eight data bits followed by a no acknowledge Logic 1 bit in read mode). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 5).
6. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition (see Figure 4). In read mode,

THEORY OF OPERATION

the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, which goes high to establish a stop condition (see Figure 5).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. During the write cycle, each data byte updates the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output is updated. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte updates the output of the selected slave device. If different instructions are needed, the write mode has to start a completely new sequence with a new slave address, instruction, and data bytes transferred again. Similarly, a repeated read function of the RDAC is also allowed.

READBACK RDAC VALUE

Specific to the AD5242 dual-channel device, the channel of interest is the one that was previously selected in the write mode. In addition, to read both RDAC values consecutively, users have to perform two write-read cycles. For example, users may first specify the RDAC1 subaddress in write mode (it is not necessary to issue the data byte and stop condition), and then change to read mode to read the RDAC1 value. To continue reading the RDAC2 value, users have to switch back to write mode, specify the subaddress, and then switch once again to read mode to read the RDAC2 value. It is not necessary to issue the write mode data byte or the first stop condition for this operation. Users should refer to Figure 4 and Figure 5 for the programming format.

MULTIPLE DEVICES ON ONE BUS

Figure 32 shows four AD5242 devices on the same serial bus. Each has a different slave address because the state of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C-compatible interface. Note, a device is addressed properly only if the bit information of AD0 and AD1 in the slave address byte matches with the logic inputs at the AD0 and AD1 pins of that particular device.

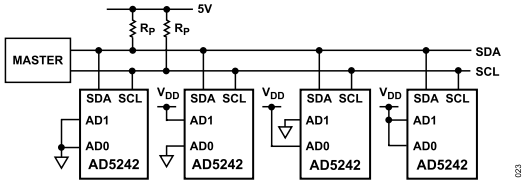

Figure 32. Multiple AD5242 Devices on One Bus

LEVEL-SHIFT FOR BIDIRECTIONAL INTERFACE

While most old systems can operate at one voltage, a new component may be optimized at another. When they operate the same signal at two different voltages, a proper method of level-shifting is needed. For instance, a 3.3 V E²PROM can be used to interface with a 5 V digital potentiometer. A level-shift scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E²PROM. Figure 33 shows one of the techniques. M1 and M2 can be N-channel FETs (2N7002) or low threshold FDV301N if V_{DD} falls below 2.5 V.

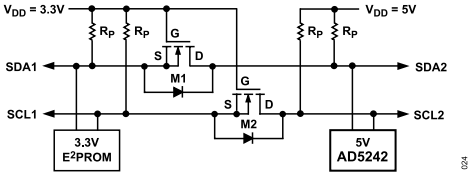

Figure 33. Level-Shift for Different Voltage Devices Operation

ADDITIONAL PROGRAMMABLE LOGIC OUTPUT

The AD5241/AD5242 feature additional programmable logic outputs, O_1 and O_2, that can be used to drive digital load, analog switches, and logic gates. They can also be used as a self-contained shutdown preset to Logic 0 that is further explained in the Shutdown Function section. O_1 and O_2 default to Logic 0 during power-up. The logic states of O_1 and O_2 can be programmed in Frame 2 under the write mode (see Figure 4). Figure 34 shows the output stage of O_1, which employs large P-channel and N-channel MOSFETs in push-pull configuration. As shown in Figure 34, the output is equal to V_{DD} or V_{SS}, and these logic outputs have adequate current driving capability to drive milliamperes of load.

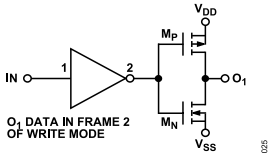

Figure 34. Output Stage of Logic Output, O_1

Users can also activate O_1 and O_2 in the following three different ways without affecting the wiper settings:

1. Start, slave address byte, acknowledge, instruction byte with O_1 and O_2 specified, acknowledge, stop.
2. Complete the write cycle with stop, then start, slave address byte, acknowledge, instruction byte with O_1 and O_2 specified, acknowledge, stop.
3. Do not complete the write cycle by not issuing the stop, then start, slave address byte, acknowledge, instruction byte with O_1 and O_2 specified, acknowledge, stop.

THEORY OF OPERATION

All digital inputs are protected with a series input resistor and the parallel Zener ESD structures shown in Figure 36. This applies to the digital input pins, SDA, SCL, and $\overline{SHDN}$.

SHUTDOWN FUNCTION

Shutdown can be activated by strobing the $\overline{SHDN}$ pin or programming the SD bit in the write mode instruction byte (see Table 3). If the RDAC Register 1 or RDAC Register 2 (AD5242 only) is placed in shutdown mode by the software, SD bit, the part returns the wiper to its prior position when a new command is received.

In addition, shutdown can be implemented with the device digital output, as shown in Figure 35. In this configuration, the device is shutdown during power-up but users are allowed to program the device. Thus, when O_1 is programmed high, the device exits shutdown mode and responds to the new setting. This self-contained shutdown function allows absolute shutdown during power-up, which is crucial in hazardous environments, and it does not add extra components.

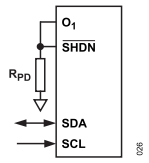

Figure 35. Shutdown by Internal Logic Output, O_1

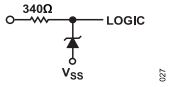

Figure 36. ESD Protection of Digital Pins

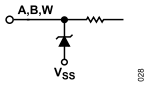

Figure 37. ESD Protection of Resistor Terminals

OUTLINE DIMENSIONS

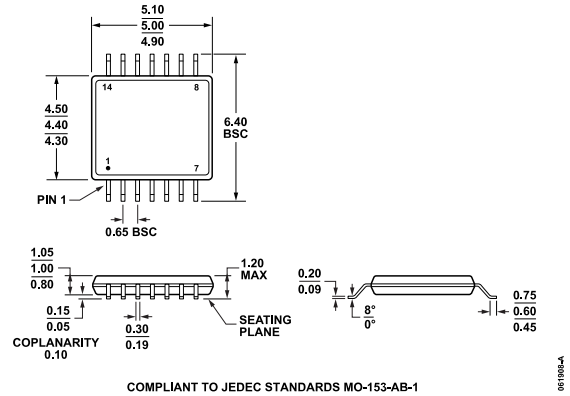

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

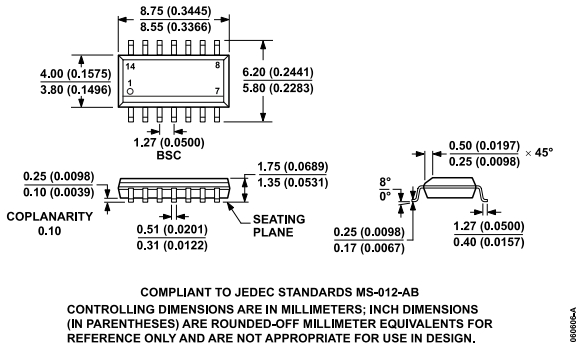

Figure 39. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in milimeters and inches

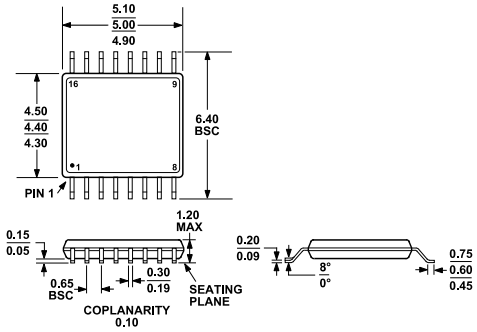

Figure 40. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters