

# Nonvolatile, I<sup>2</sup>C-Compatible 256-Position, Digital Potentiometer

## FEATURES

- ▶ Nonvolatile memory maintains wiper settings
- ▶ 256-position
- ▶ Thin LFCSP-10 (3 mm × 3 mm × 0.8 mm) package
- ▶ Compact MSOP-10 (3 mm × 4.9 mm × 1.1 mm) package
- ▶ I<sup>2</sup>C-compatible interface
- ▶ V<sub>LOGIC</sub> pin provides increased interface flexibility
- ▶ End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- ▶ Resistance tolerance stored in EEPROM (0.1% accuracy)
- ▶ Power-on EEPROM refresh time < 1ms
- ▶ Software write protect command
- ▶ Address Decode Pin AD0 and Pin AD1 allow 4 packages per bus
- ▶ 100-year typical data retention at 55°C
- ▶ Wide operating temperature -40°C to +125°C
- ▶ 3 V to 5 V single supply

## APPLICATIONS

- ▶ LCD panel V<sub>COM</sub> adjustment
- ▶ LCD panel brightness and contrast control
- ▶ Mechanical potentiometer replacement in new designs
- ▶ Programmable power supplies
- ▶ RF amplifier biasing
- ▶ Automotive electronics adjustment
- ▶ Gain control and offset adjustment
- ▶ Fiber to the home systems
- ▶ Electronics level settings

## GENERAL DESCRIPTION

The AD5259 provides a compact, nonvolatile LFCSP-10 (3 mm × 3 mm) or MSOP-10 (3 mm × 4.9 mm) packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors, but with enhanced resolution and solid-state reliability. The terms digital potentiometer, VR (variable resistor), and RDAC are used interchangeably.

## FUNCTIONAL BLOCK DIAGRAMS

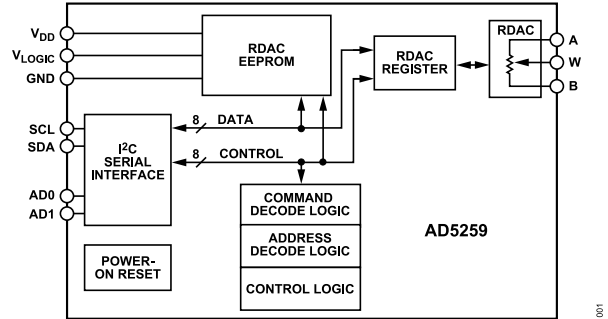


Figure 1. Block Diagram

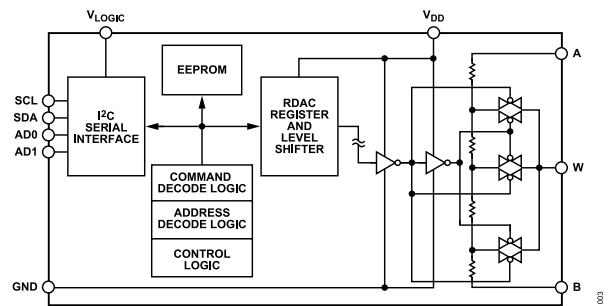
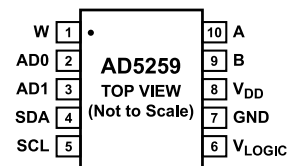


Figure 2. Block Diagram Showing Level Shifters

## CONNECTION DIAGRAM



NOTES  
1. THE EXPOSED PAD SHOULD BE CONNECTED TO GND OR LEFT FLOATING.

Figure 3. Pinout

The wiper settings are controllable through an I<sup>2</sup>C-compatible digital interface that is also used to read back the wiper register and EEPROM content. Resistor tolerance is also stored within EEPROM, providing an end-to-end tolerance accuracy of 0.1%.

A separate V<sub>LOGIC</sub> pin delivers increased interface flexibility. For users who need multiple parts on one bus, Address Bit AD0 and Address Bit AD1 allow up to four devices on the same bus.

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**REVISION HISTORY****10/2022—Rev. D to Rev. E**

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**5/2022—Rev. C to Rev. D**

Updated Outline Dimensions.....	21
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## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ;  $V_A = V_{DD}$ ;  $V_B = 0\text{ V}$ ;  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS: RHEOSTAT MODE						
Resistor Differential Nonlinearity	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$				LSB
5 k $\Omega$			-1	$\pm 0.2$	+1	
10 k $\Omega$			-1	$\pm 0.1$	+1	
50 k $\Omega$ /100 k $\Omega$			-0.5	$\pm 0.1$	+0.5	
Resistor Integral Nonlinearity	R-INL	$R_{WB}$ , $V_A = \text{no connect}$				LSB
5 k $\Omega$			-4	$\pm 0.3$	+4	
10 k $\Omega$			-2	$\pm 0.2$	+2	
50 k $\Omega$ /100 k $\Omega$			-1	$\pm 0.4$	+1	
Nominal Resistor Tolerance	$\Delta R_{AB}$	$T_A = 25^\circ\text{C}$ , $V_{DD} = 5.5\text{ V}$	-30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB} \times 10^6)/(R_{AB} \times \Delta T)$	Code = 0x00/0x80		500/15		ppm/ $^\circ\text{C}$
Total Wiper Resistance	$R_{WB}$	Code = 0x00		75	350	$\Omega$
DC CHARACTERISTICS: POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity	DNL					LSB
5 k $\Omega$			-1	$\pm 0.2$	+1	
10 k $\Omega$			-0.5	$\pm 0.1$	+0.5	
50 k $\Omega$ /100 k $\Omega$			-0.5	$\pm 0.2$	+0.5	
Integral Nonlinearity	INL					LSB
5 k $\Omega$			-1	$\pm 0.2$	+1	
10 k $\Omega$			-0.5	$\pm 0.1$	+0.5	
50 k $\Omega$ /100 k $\Omega$			-0.5	$\pm 0.1$	+0.5	
Full-Scale Error	$V_{WFSE}$	Code = 0xFF				LSB
5 k $\Omega$			-7	-3	0	
10 k $\Omega$			-4	-1.5	0	
50 k $\Omega$ /100 k $\Omega$			-1	-0.4	0	
Zero-Scale Error	$V_{WZSE}$	Code = 0x00				LSB
5 k $\Omega$		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	0	2.5	4	LSB
		$+85^\circ\text{C} < T_A < +125^\circ\text{C}$			6	LSB
10 k $\Omega$		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	0	1	3	LSB
		$+85^\circ\text{C} < T_A < +125^\circ\text{C}$			4	LSB
50 k $\Omega$ /100 k $\Omega$			0	0.2	0.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W \times 10^6)/(V_W \times \Delta T)$	Code = 0x00/0x80		60/5		ppm/ $^\circ\text{C}$
RESISTOR TERMINALS						
Voltage Range	$V_{A, B, W}$		GND		$V_{DD}$	V
Capacitance A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W	$C_W$	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		10		nA

## SPECIFICATIONS

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High	$V_{IH}$		$0.7 \times V_L$		$V_L + 0.5$	V
Input Logic Low	$V_{IL}$		-0.5		$0.3 \times V_L$	V
Leakage Current	$I_{IL}$					$\mu$ A
SDA, AD0, AD1		$V_{IN} = 0$ V or 5 V		0.01	$\pm 1$	
SCL – Logic High		$V_{IN} = 0$ V	-2.5	-1.3	+1	
SCL – Logic Low		$V_{IN} = 5$ V		0.01	$\pm 1$	
Input Capacitance	$C_{IL}$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD}$		2.7		5.5	V
Positive Supply Current	$I_{DD}$			0.1	2	$\mu$ A
Logic Supply	$V_{LOGIC}$		2.7		5.5	V
Logic Supply Current	$I_{LOGIC}$	$V_{IH} = 5$ V or $V_{IL} = 0$ V $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $+85^\circ\text{C} < T_A < +125^\circ\text{C}$		3	6	$\mu$ A
Programming Mode Current (EEPROM)	$I_{LOGIC(PROG)}$	$V_{IH} = 5$ V or $V_{IL} = 0$ V		35		mA
Power Dissipation	$P_{DISS}$	$V_{IH} = 5$ V or $V_{IL} = 0$ V, $V_{DD} = 5$ V		15	40	$\mu$ W
Power Supply Rejection Ratio	PSRR	$V_{DD} = +5$ V $\pm 10\%$ , code = 0x80		$\pm 0.005$	$\pm 0.06$	%/%
<b>DYNAMIC CHARACTERISTICS</b>						
Bandwidth -3 dB	BW	Code = 0x80 $R_{AB} = 5$ k $\Omega$ $R_{AB} = 10$ k $\Omega$ $R_{AB} = 50$ k $\Omega$ $R_{AB} = 100$ k $\Omega$		2000 800 160 80		kHz
Total Harmonic Distortion	$THD_W$	$R_{AB} = 10$ k $\Omega$ , $V_A = 1$ V rms, $V_B = 0$ , $f = 1$ kHz		0.01		%
$V_W$ Settling Time	$t_S$	$R_{AB} = 10$ k $\Omega$ , $V_{AB} = 5$ V, $\pm 1$ LSB error band		500		ns
Resistor Noise Voltage Density	$e_{N\_WB}$	$R_{WB} = 5$ k $\Omega$ , $f = 1$ kHz		9		nV/ $\sqrt{\text{Hz}}$

<sup>1</sup> Typical values represent average readings at 25°C and  $V_{DD} = 5$  V.

## TIMING CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5$  V  $\pm 10\%$  or 3 V  $\pm 10\%$ ;  $V_A = V_{DD}$ ;  $V_B = 0$  V;  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>I<sup>2</sup>C INTERFACE TIMING CHARACTERISTICS<sup>1</sup></b>						
SCL Clock Frequency	$f_{SCL}$		0		400	kHz
$t_{BUF}$ Bus Free Time Between Stop and Start	$t_1$		1.3			$\mu$ s
$t_{HD,STA}$ Hold Time (Repeated Start)	$t_2$	After this period, the first clock pulse is generated.	0.6			$\mu$ s
$t_{LOW}$ Low Period of SCL Clock	$t_3$		1.3			$\mu$ s
$t_{HIGH}$ High Period of SCL Clock	$t_4$		0.6			$\mu$ s
$t_{SU,STA}$ Setup Time for Repeated Start Condition	$t_5$		0.6			$\mu$ s
$t_{HD,DAT}$ Data Hold Time	$t_6$		0		0.9	$\mu$ s

## SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$t_{\text{SU,DAT}}$ Data Setup Time	$t_7$		100			ns
$t_{\text{F}}$ Fall Time of Both SDA and SCL Signals	$t_8$				300	ns
$t_{\text{R}}$ Rise Time of Both SDA and SCL Signals	$t_9$				300	ns
$t_{\text{SU,STO}}$ Setup Time for Stop Condition	$t_{10}$		0.6			$\mu\text{s}$
EEPROM Data Storing Time <sup>2</sup>	$t_{\text{EEMEM\_STORE}}$			26		ms
EEPROM Data Restoring Time at Power-On <sup>3</sup>	$t_{\text{EEMEM\_RESTORE1}}$	$V_{\text{DD}}$ rise time dependent. Measure without decoupling capacitors at $V_{\text{DD}}$ and GND.		300		$\mu\text{s}$
EEPROM Data Restoring Time upon Restore Command <sup>3</sup>	$t_{\text{EEMEM\_RESTORE2}}$	$V_{\text{DD}} = 5 \text{ V}$ .		300		$\mu\text{s}$
EEPROM Data Rewritable Time <sup>4</sup>	$t_{\text{EEMEM\_REWRITE}}$			540		$\mu\text{s}$
FLASH/EE MEMORY RELIABILITY						
Endurance <sup>5</sup>			100	700		kCycles
Data Retention <sup>6</sup>				100		Years

<sup>1</sup> Standard I<sup>2</sup>C mode operation guaranteed by design.

<sup>2</sup> No I<sup>2</sup>C transaction must take place during the EEPROM data storing time to guarantee that every I<sup>2</sup>C transaction is executed.

<sup>3</sup> During power-up, the output is momentarily preset to midscale before restoring EEPROM content.

<sup>4</sup> Delay time after power-on PRESET prior to writing new EEPROM data.

<sup>5</sup> Endurance is qualified to 100,000 cycles per JEDEC Std. 22 method A117, and is measured at  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+125^{\circ}\text{C}$ ; typical endurance at  $+25^{\circ}\text{C}$  is 700,000 cycles.

<sup>6</sup> Retention lifetime equivalent at junction temperature ( $T_{\text{J}}$ ) =  $55^{\circ}\text{C}$  per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.

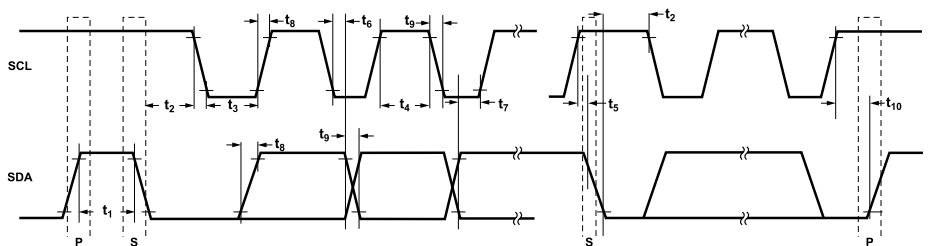


Figure 4. I<sup>2</sup>C Interface Timing Diagram

**ABSOLUTE MAXIMUM RATINGS**

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Value
$V_{DD}$ , $V_{\text{LOGIC}}$ to GND	-0.3 V to +7 V
$V_A$ , $V_B$ , $V_W$ to GND	GND - 0.3 V, $V_{DD} + 0.3$ V
$I_{\text{MAX}}$	
Pulsed <sup>1</sup>	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature ( $T_{\text{JMAX}}$ )	150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance <sup>2</sup> $\theta_{\text{JA}}$ : MSOP-10	200°C/W

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Package power dissipation =  $(T_{\text{JMAX}} - T_A)/\theta_{\text{JA}}$ .

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

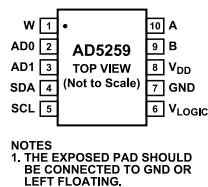


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin	Mnemonic	Description
1	W	W Terminal, $GND \leq V_W \leq V_{DD}$ .
2	AD0	Programmable Pin 0 for Multiple Package Decoding. State is registered on power-up.
3	AD1	Programmable Pin 1 for Multiple Package Decoding. State is registered on power-up.
4	SDA	Serial Data Input/Output.
5	SCL	Serial Clock Input. Positive edge triggered.
6	$V_{LOGIC}$	Logic Power Supply.
7	GND	Digital Ground.
8	$V_{DD}$	Positive Power Supply.
9	B	B Terminal, $GND \leq V_B \leq V_{DD}$ .
10	A	A Terminal, $GND \leq V_A \leq V_{DD}$ .
11	EPAD	Exposed Pad. The exposed pad should be connected to GND or left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5.5\text{ V}$ ,  $R_{AB} = 10\text{ k}\Omega$ ,  $T_A = +25^\circ\text{C}$ ; unless otherwise noted.

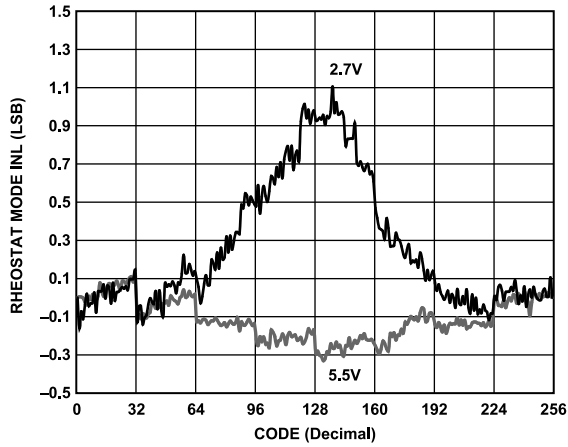


Figure 6. R-INL vs. Code vs. Supply Voltage

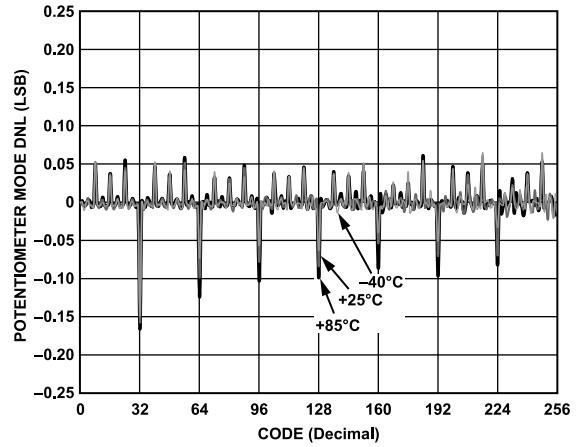


Figure 9. DNL vs. Code vs. Temperature

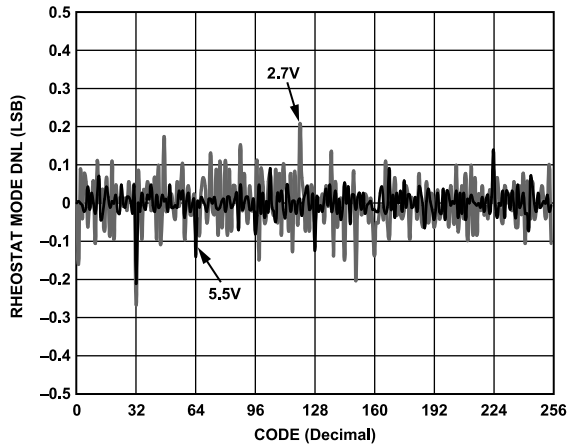


Figure 7. R-DNL vs. Code vs. Supply Voltage

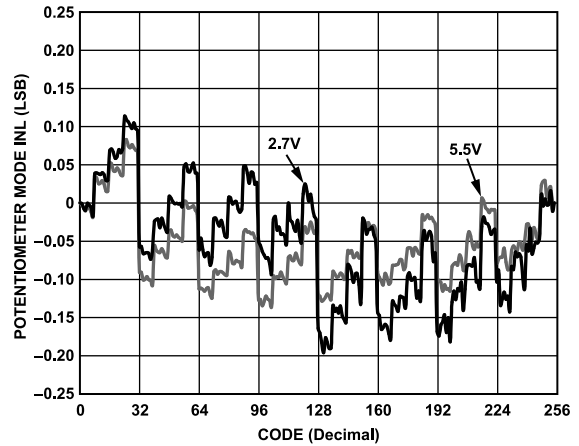


Figure 10. INL vs. Supply Voltages

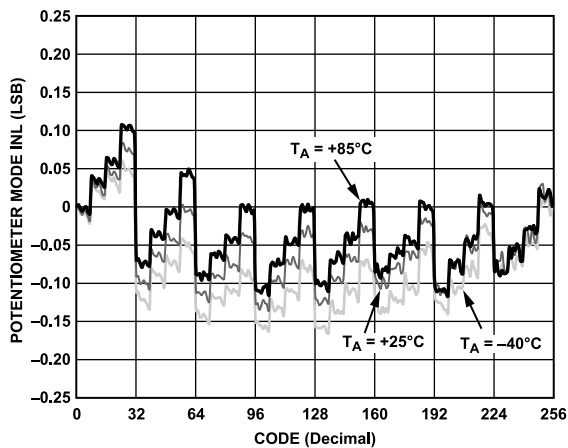


Figure 8. INL vs. Code vs. Temperature

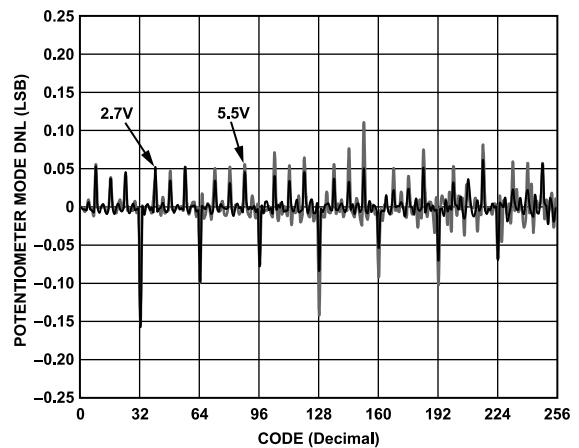


Figure 11. DNL vs. Code vs. Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

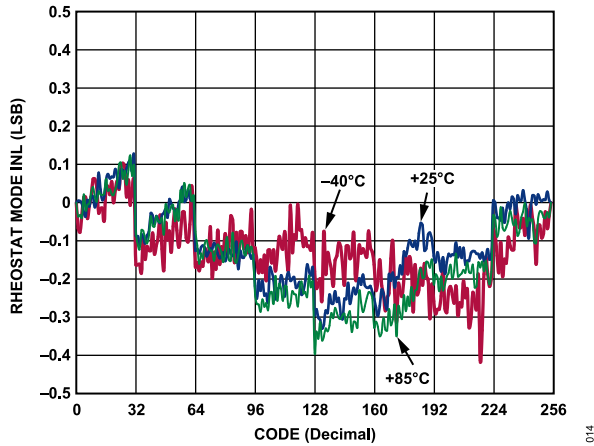


Figure 12. R-INL vs. Code vs. Temperature

014

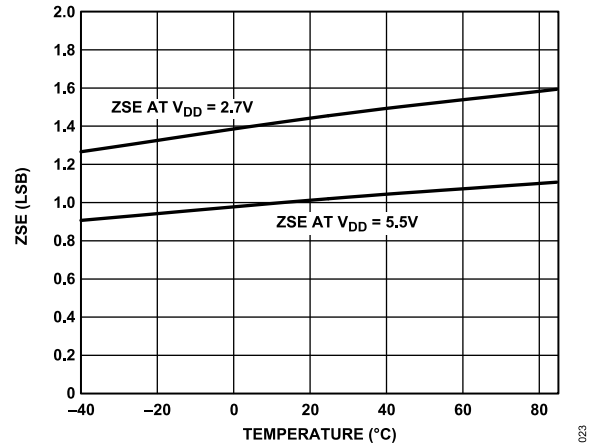


Figure 15. Zero-Scale Error vs. Temperature

023

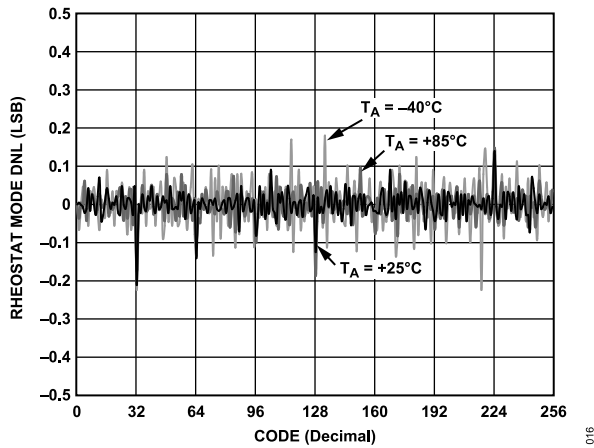


Figure 13. R-DNL vs. Code vs. Temperature

016

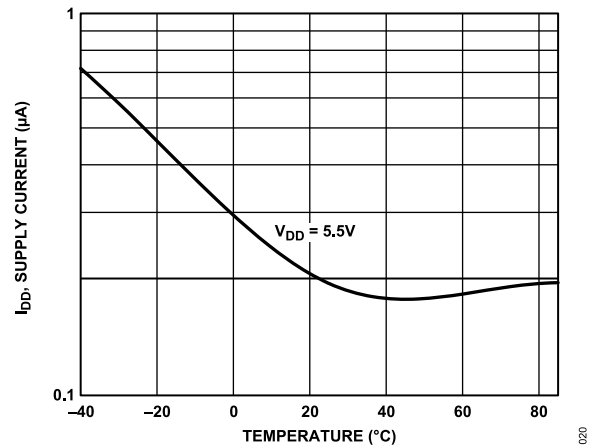


Figure 16. Supply Current vs. Temperature

020

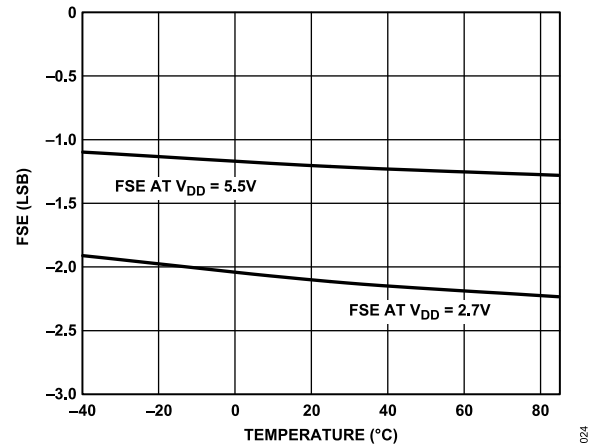


Figure 14. Full-Scale Error vs. Temperature

024

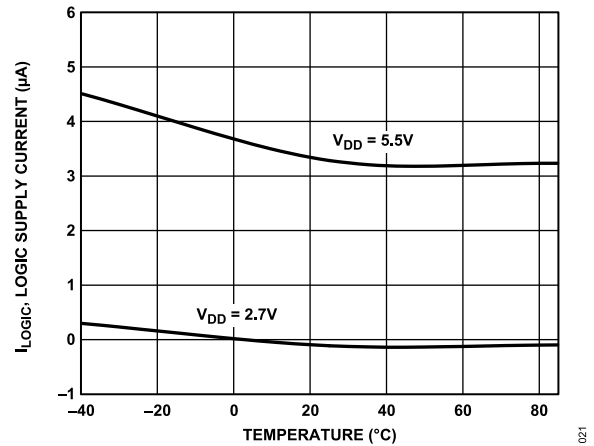


Figure 17. Logic Supply Current vs. Temperature vs. VDD

021

TYPICAL PERFORMANCE CHARACTERISTICS

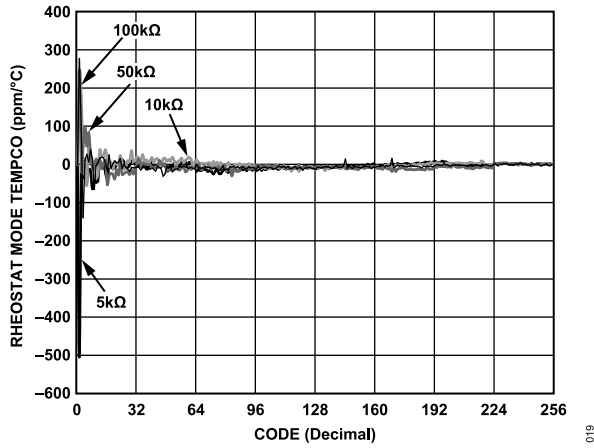


Figure 18. Rheostat Mode Tempco  $(\Delta R_{AB} \times 10^6)/(R_{AB} \times \Delta T)$  vs. Code

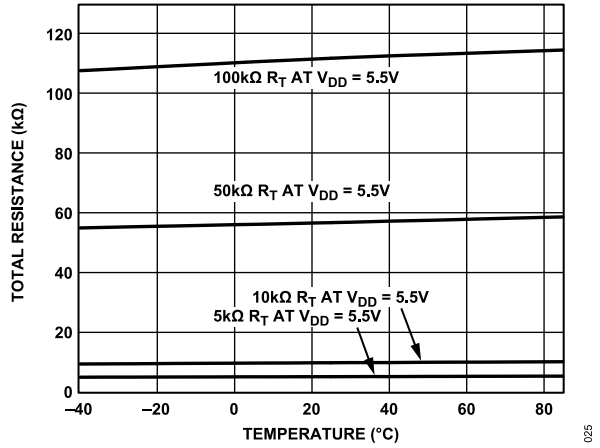


Figure 21. Total Resistance vs. Temperature

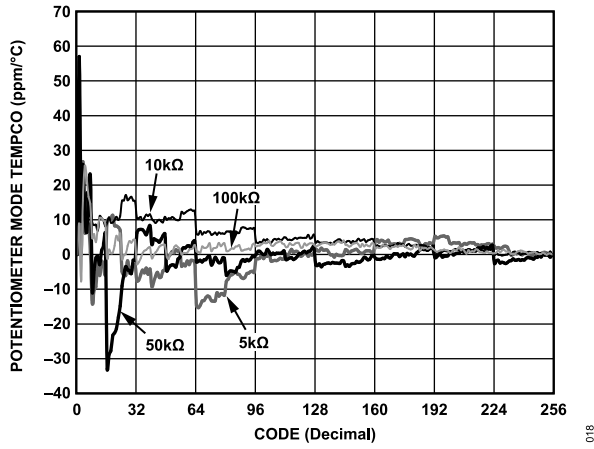


Figure 19. Potentiometer Mode Tempco  $(\Delta V_W \times 10^6)/(V_W \times \Delta T)$  vs. Code

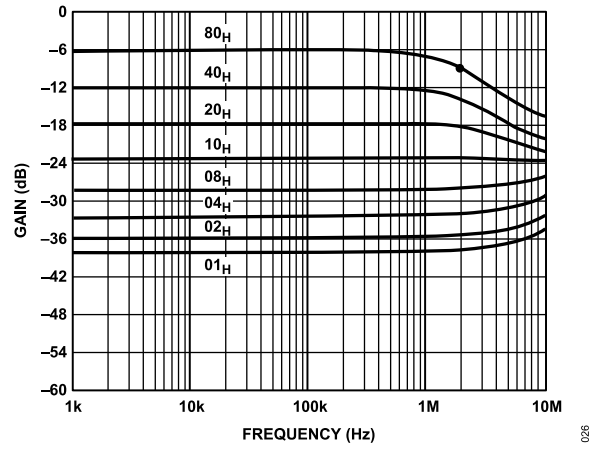


Figure 22. Gain vs. Frequency vs. Code, R<sub>AB</sub> = 5 kΩ

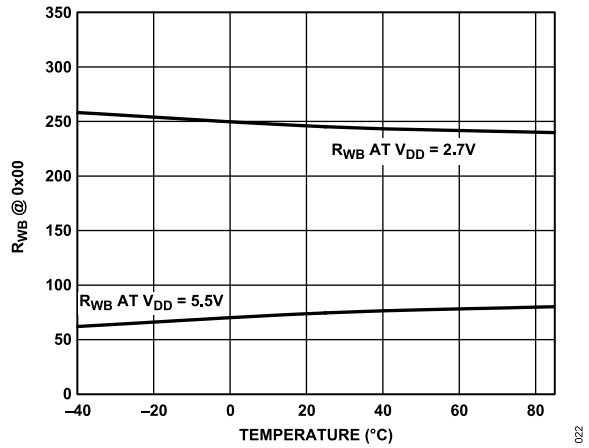


Figure 20. R<sub>WB</sub> vs. Temperature

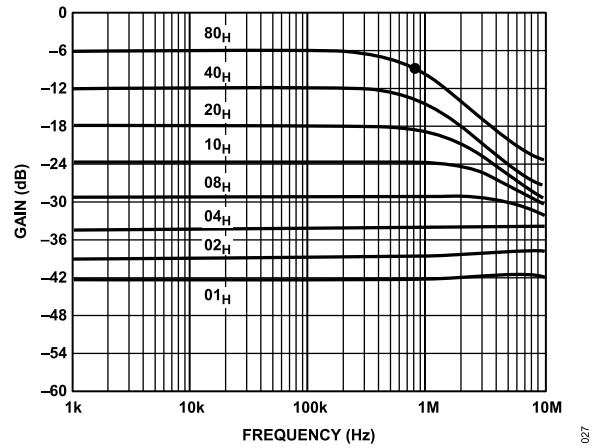


Figure 23. Gain vs. Frequency vs. Code, R<sub>AB</sub> = 10 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

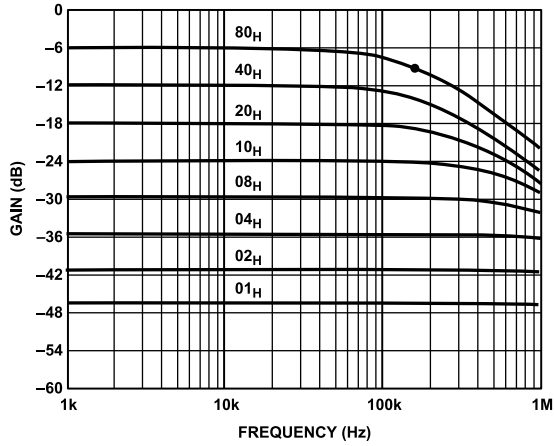


Figure 24. Gain vs. Frequency vs. Code,  $R_{AB} = 50\text{ k}\Omega$

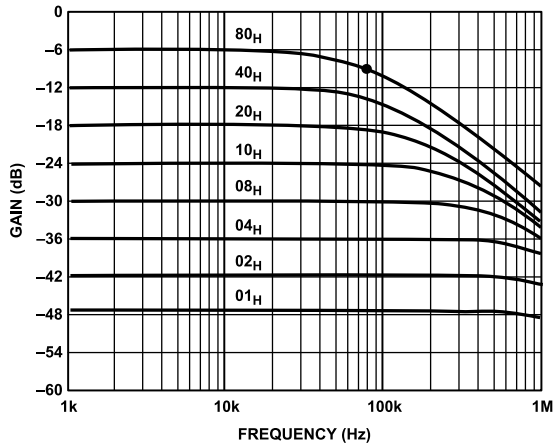


Figure 25. Gain vs. Frequency vs. Code,  $R_{AB} = 100\text{ k}\Omega$

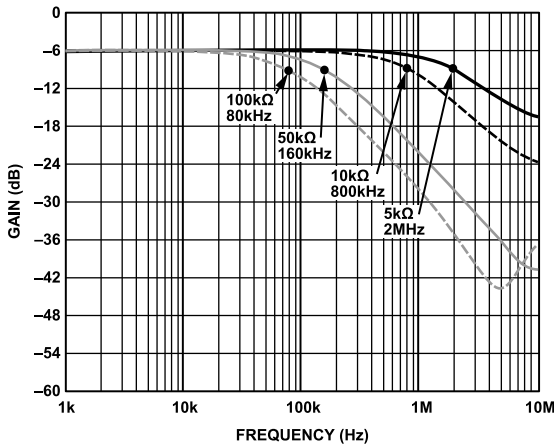


Figure 26. -3 dB Bandwidth @ Code = 0x80

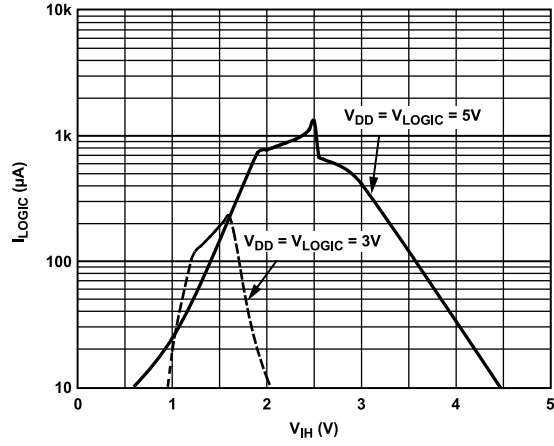


Figure 27. Logic Supply Current vs. Input Voltage

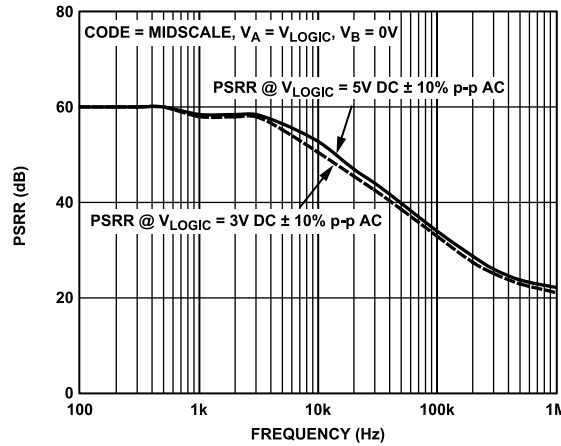


Figure 28. PSRR vs. Frequency

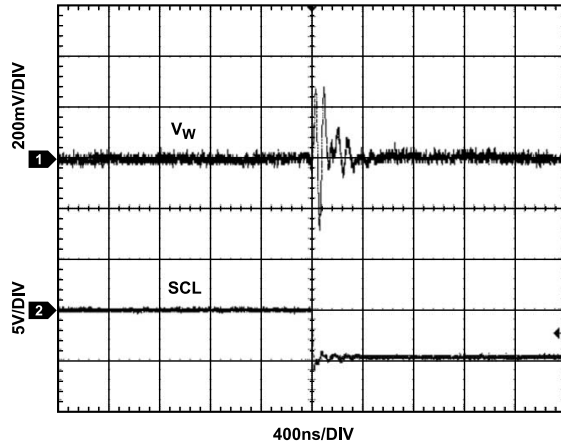


Figure 29. Digital Feedthrough

TYPICAL PERFORMANCE CHARACTERISTICS

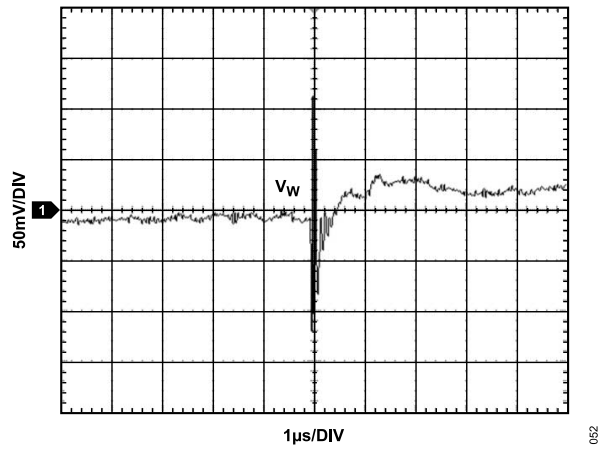


Figure 30. Midscale Glitch, Code 0x7F to 0x80

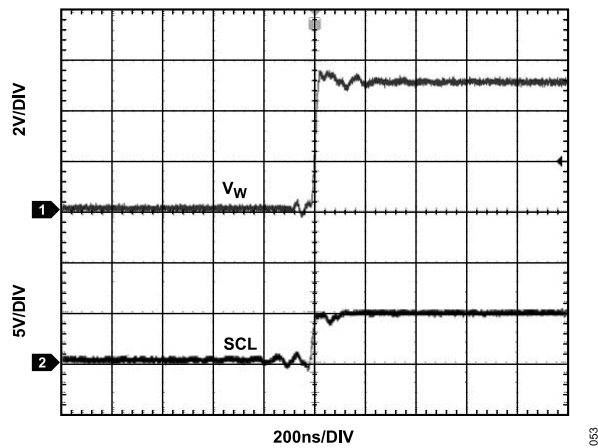


Figure 31. Large Signal Settling Time

TEST CIRCUITS

Figure 32 through Figure 37 illustrate the test circuits that define the test conditions used in the product Specifications tables.

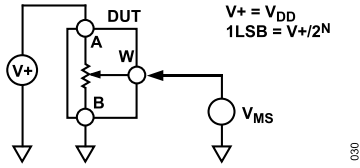


Figure 32. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

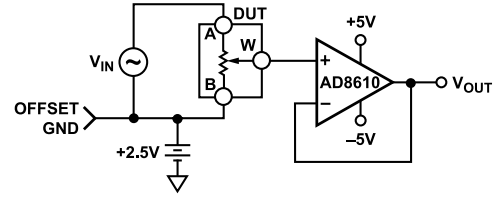


Figure 36. Test Circuit for Gain vs. Frequency

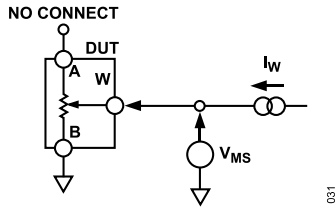


Figure 33. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

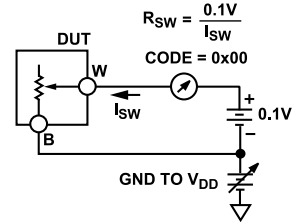


Figure 37. Test Circuit for Common-Mode Leakage Current

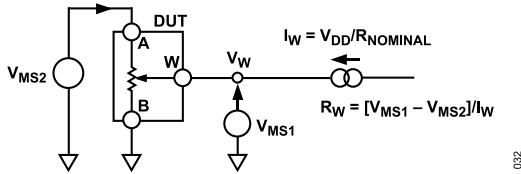


Figure 34. Test Circuit for Wiper Resistance

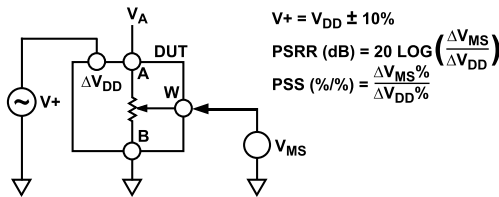


Figure 35. Test Circuit for Power Supply Sensitivity (PSS, PSRR)

## THEORY OF OPERATION

The AD5259 is a 256-position digitally-controlled variable resistor (VR) device. EEPROM is pre-loaded at midscale from the factory, and initial power-up is, accordingly, at midscale.

### PROGRAMMING THE VARIABLE RESISTOR

#### Rheostat Operation

The nominal resistance ( $R_{AB}$ ) of the RDAC between Terminal A and Terminal B is available in 5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ . The nominal resistance of the VR has 256 contact points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of 256 possible settings.

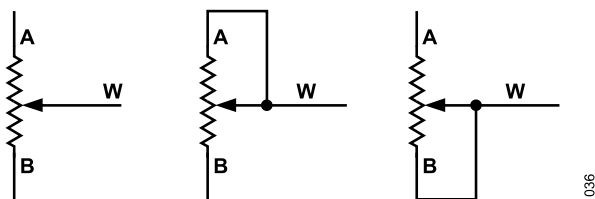


Figure 38. Rheostat Mode Configuration

The general equation determining the digitally programmed output resistance between Wiper W and Terminal B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

$D$  is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.

$R_{AB}$  is the end-to-end resistance.

$R_W$  is the wiper resistance contributed by the ON resistance of each internal switch.

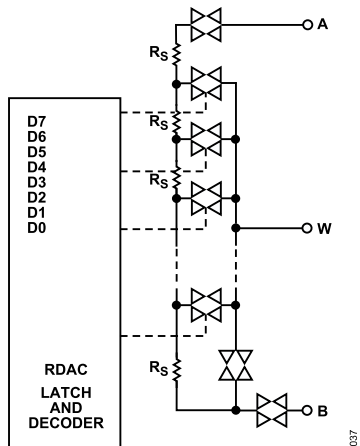


Figure 39. AD5259 Equivalent RDAC Circuit

In the zero-scale condition, there is a relatively low value finite wiper resistance. Care should be taken to limit the current flow between Wiper W and Terminal B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A produces a digitally controlled complementary resistance,  $R_{WA}$ . The resistance value setting for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value.

The general equation for this operation is

$$R_{WA}(D) = \frac{256-D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

Typical device-to-device matching is process lot dependent and may vary by up to  $\pm 30\%$ . For this reason, resistance tolerance is stored in the EEPROM, enabling the user to know the actual  $R_{AB}$  within 0.1%.

### PROGRAMMING THE POTENTIOMETER DIVIDER

#### Voltage Output Operation

The digital potentiometer easily generates a voltage divider at Wiper W to Terminal B and Wiper W to Terminal A proportional to the input voltage at Terminal A to Terminal B. Unlike the polarity of  $V_{DD}$  to GND, which must be positive, voltage across Terminal A to Terminal B, Wiper W to Terminal A, and Wiper W to Terminal B can be at either polarity.

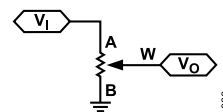


Figure 40. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at Wiper W to Terminal B starting at 0 V up to 1 LSB less than 5 V. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256-D}{256} V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance,  $V_W$ , is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the Internal Resistors  $R_{WA}$  and  $R_{WB}$  and not the absolute values.

## I<sup>2</sup>C-COMPATIBLE INTERFACE

The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see [Figure 4](#)). The next byte is the slave address byte, which consists of the slave address (first 7 bits) followed by an R/W bit (see [Table 6](#)). When the R/W bit is high, the master reads from the slave device. When the R/W bit is low, the master writes to the slave device.

The slave address of the part is determined by two configurable address pins, Pin AD0 and Pin AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I<sup>2</sup>C 7-bit address (see [Table 5](#)). The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is termed the slave acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register.

### WRITING

In the write mode, the last bit (R/W) of the slave address byte is logic low. The second byte is the instruction byte. The first three bits of the instruction byte are the command bits (see [Table 6](#)). The user must choose whether to write to the RDAC register, EEPROM register, or activate the software write protect (see [Table 7](#) to [Table 10](#)). The final five bits are all zeros (see [Table 13](#) to [Table 14](#)). The slave again responds by pulling the SDA line low during the ninth clock pulse.

The final byte is the data byte MSB first. With the write protect mode, data is not stored; rather, a logic high in the LSB enables write protect. Likewise, a logic low disables write protect. The slave again responds by pulling the SDA line low during the ninth clock pulse.

### STORING/RESTORING

In this mode, only the address and instruction bytes are necessary. The last bit (R/W) of the address byte is logic low. The first three bits of the instruction byte are the command bits (see [Table 6](#)). The two choices are transfer data from RDAC to EEPROM (store), or from EEPROM to RDAC (restore). The final five bits are all zeros

(see [Table 13](#) to [Table 14](#)). In addition, users should issue an NOP command immediately after restoring the EEMEM setting to RDAC, thereby minimizing supply current dissipation.

### READING

Assuming the register of interest was not just written to, it is necessary to write a dummy address and instruction byte. The instruction byte will vary depending on whether the data that is wanted is the RDAC register, EEPROM register, or tolerance register (see [Table 11](#) and [Table 17](#)).

After the dummy address and instruction bytes are sent, a repeat start is necessary. After the repeat start, another address byte is needed, except this time the R/W bit is logic high. Following this address byte is the readback byte containing the information requested in the instruction byte. Read bits appear on the negative edges of the clock.

The tolerance register can be read back individually (see [Table 15](#)) or consecutively (see [Table 17](#)). Refer to the [Read Modes](#) section for detailed information on the interpretation of the tolerance bytes.

After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition (see [Figure 46](#)). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then raises SDA high to establish a stop condition (see [Figure 47](#)).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output is updated on each successive byte until a stop condition is received. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

## I<sup>2</sup>C-COMPATIBLE FORMAT

The following generic, write, read, and store/restore control registers for the AD5259 all refer to the device addresses listed in [Table 5](#); the mode/condition reference key (S, P, SA, MA, NA,  $\bar{W}$ , R, and X) is listed below.

S = Start Condition

P = Stop Condition

SA = Slave Acknowledge

MA = Master Acknowledge

NA = No Acknowledge

$\bar{W}$  = Write

R = Read

X = Don't Care

AD1 and AD0 are two-state address pins.

**Table 5. Device Address Lookup**

AD1 Address Pin	AD0 Address Pin	I <sup>2</sup> C Device Address
0	0	0011000
1	0	0011010
0	1	1001100
1	1	1001110

## GENERIC INTERFACE

**Table 6. Generic Interface Format**

S	7-Bit Device Address (See <a href="#">Table 5</a> )	$R/\bar{W}$	SA	C2	C1	C0	A4	A3	A2	A1	A0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte								Data Byte										

**Table 7. RDAC-to-EEPROM Interface Command Descriptions**

C2	C1	C0	Command Description
0	0	0	Operation Between Interface and RDAC.
0	0	1	Operation Between Interface and EEPROM.
0	1	0	Operation Between Interface and Write Protection Register. See <a href="#">Table 10</a> .
1	0	0	NOP.
1	0	1	Restore EEPROM to RDAC. <sup>1</sup>
1	1	0	Store RDAC to EEPROM.

<sup>1</sup> This command leaves the device in the EEMEM read power state, which consumes power. Issue the NOP command to return the device to its idle state.

## WRITE MODES

**Table 8. Writing to RDAC Register**

S	7-Bit Device Address (See <a href="#">Table 5</a> )	0	SA	0	0	0	0	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte								Data Byte											

**Table 9. Writing to EEPROM Register**

S	7-Bit Device Address (See <a href="#">Table 5</a> )	0	SA	0	0	1	0	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte								Data Byte											

**Table 10. Activating/Deactivating Software Write Protect**

S	7-Bit Device Address (See <a href="#">Table 5</a> )	0	SA	0	1	0	0	0	0	0	0	0	SA	0	0	0	0	0	0	0	0	WP	SA	P
	Slave Address Byte			Instruction Byte								Data Byte												

In order to activate the write protection mode, the WP bit in [Table 10](#) must be logic high. To deactivate the write protection, the command must be sent again, except with the WP in logic zero state. WP is reset to the deactivated mode if power is cycled off and on.



**I<sup>2</sup>C-COMPATIBLE FORMAT****READ MODES**

Read modes are referred to as traditional because the first two bytes for all three cases are dummy bytes, which function to place the pointer towards the correct register; this is the reason for the repeat start. Theoretically, this step can be avoided if the user

reads a register previously written to. For example, if the EEPROM was just written to, the user can then skip the two dummy bytes and proceed directly to the slave address byte, followed by the EEPROM readback data.

**Table 11. Traditional Readback of RDAC Register Value**

S	7-Bit Device Address (See Table 5)	0	SA	0	0	0	0	0	0	0	0	0	0	SA	S <sup>1</sup>	7-Bit Device Address (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte											Slave Address Byte		Read Back Data											

<sup>1</sup> Repeated start.

**Table 12. Traditional Readback of Stored EEPROM Value**

S	7-Bit Device Address (See Table 5)	0	SA	0	0	1	0	0	0	0	0	0	0	SA	S <sup>1</sup>	7-Bit Device Address (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte											Slave Address Byte		Read Back Data											

<sup>1</sup> Repeated start.

**STORE/RESTORE MODES****Table 13. Storing RDAC Value to EEPROM**

S	7-Bit Device Address (See Table 5)	0	SA	1	1	0	0	0	0	0	0	0	0	SA	P
	Slave Address Byte			Instruction Byte											

**Table 14. Restoring EEPROM to RDAC<sup>1</sup>**

S	7-Bit Device Address (See Table 5)	0	SA	1	0	1	0	0	0	0	0	0	0	SA	P
	Slave Address Byte			Instruction Byte											

**TOLERANCE READBACK MODES****Table 15. Traditional Readback of Tolerance (Individually)**

S	7-Bit Device Address (See Table 5)	0	SA	0	0	1	1	1	1	1	0	0	SA	S <sup>1</sup>	7-Bit Device Address (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte											Slave Address Byte		Sign + Integer Byte										

<sup>1</sup> Repeated start.

**Table 16.**

S	7-Bit Device Address (See Table 5)	0	SA	0	0	1	1	1	1	1	1	1	SA	S <sup>1</sup>	7-Bit Device Address (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte											Slave Address Byte		Decimal Byte										

<sup>1</sup> Repeated start.

I<sup>2</sup>C-COMPATIBLE FORMAT

Table 17. Traditional Readback of Tolerance (Consecutively)

7-Bit Device Address (See Table 5)		S	0	A	0	0	1	1	1	1	1	S <sup>1</sup>	7-Bit Device Address (See Table 5)		1	S	D	D	D	D	D	D	D	M	D	D	D	D	D	D	N	P
Slave Address Byte		Instruction Byte				Slave Address Byte		Sign + Integer Byte							Decimal Byte																	

<sup>1</sup> Repeated start.

Calculating R<sub>AB</sub> Tolerance Stored in Read-Only Memory

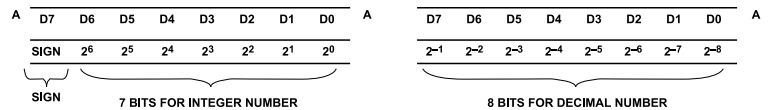


Figure 41. Format of Stored Tolerance in Sign Magnitude Format with Bit Position Descriptions. (Unit is Percent. Only Data Bytes are Shown.)

The AD5259 features a patented R<sub>AB</sub> tolerance storage in the nonvolatile memory. The tolerance is stored in the memory during factory production and can be read by users at any time. The knowledge of stored tolerance allows users to accurately calculate R<sub>AB</sub>. This feature is valuable for precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

The stored tolerance resides in the read-only memory and is expressed as a percentage. The tolerance is stored in two memory location bytes in sign magnitude binary form (see Figure 41).

The two EEPROM address bytes are 11110 (sign + integer) and 11111 (decimal number). The two bytes can be individually accessed with two separate commands (see Table 15). Alternatively, readback of the first byte followed by the second byte can be done in one command (see Table 17). In the latter case, the memory pointer will automatically increment from the first to the second EEPROM location (increments from 11110 to 11111) if read consecutively. In the first memory location, the MSB is designated for the sign (0 = + and 1 = -) and the seven LSBs are designated for the integer portion of the tolerance. In the second memory location, all eight data bits are designated for the decimal portion of tolerance. Note the decimal portion has a limited accuracy of only 0.1%. For example, if the rated R<sub>AB</sub> = 10 kΩ and the data readback from Address 11110 shows 0001 1100, and Address 11111 shows 0000 1111, then the tolerance can be calculated as

MSB: 0 = +  
 Next 7 MSB: 001 1100 = 28  
 8 LSB: 0000 1111 = 15 × 2<sup>-8</sup> = 0.06  
 Tolerance = +28.06%  
 Rounded Tolerance = +28.1% and therefore,  
 R<sub>AB\_ACTUAL</sub> = 12.810 kΩ

ESD PROTECTION OF DIGITAL PINS AND RESISTOR TERMINALS

The AD5259 V<sub>DD</sub>, V<sub>LOGIC</sub>, and GND power supplies define the boundary conditions for proper 3-terminal and digital input operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V<sub>DD</sub> or GND are clamped by the internal forward biased ESD protection diodes (see Figure 42). Digital Input SCL and Digital Input SDA are clamped by ESD protection diodes with respect to V<sub>LOGIC</sub> and GND as shown in Figure 43.

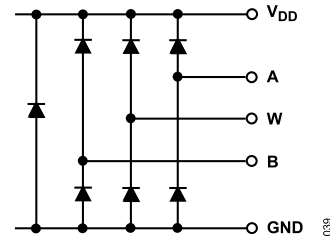


Figure 42. Maximum Terminal Voltages Set by V<sub>DD</sub> and GND

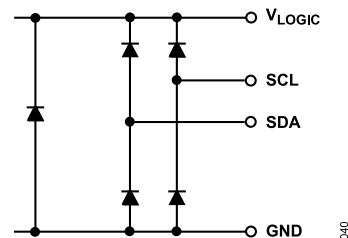


Figure 43. Maximum Terminal Voltages Set by V<sub>LOGIC</sub> and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 42), it is important to power GND/V<sub>DD</sub>/V<sub>LOGIC</sub> before applying any voltage to Terminal A, Terminal B, and Terminal W; otherwise, the diode is forward biased, so the V<sub>DD</sub> and V<sub>LOGIC</sub> are powered unintentionally

## I<sup>2</sup>C-COMPATIBLE FORMAT

and may affect the user's circuit. The ideal power-up sequence is in the following order: GND,  $V_{DD}$ ,  $V_{LOGIC}$ , digital inputs, and then  $V_A$ ,  $V_B$ ,  $V_W$ . The relative order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and the digital inputs is not important as long as they are powered after  $GND/V_{DD}/V_{LOGIC}$ .

## LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to use compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ . Low ESR 1  $\mu\text{F}$  to 10  $\mu\text{F}$  tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 44). The digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

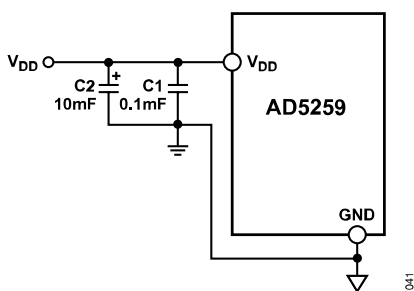


Figure 44. Power Supply Bypassing

## MULTIPLE DEVICES ON ONE BUS

The AD5259 has two configurable address pins, Pin AD0 and Pin AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I<sup>2</sup>C-compatible 7-bit address (see Table 5). This allows up to four devices on the bus to be written to or read from independently.

## EVALUATION BOARD

An evaluation board, with all necessary software, is available to program the AD5259 from any PC running Windows<sup>®</sup> 98/ 2000/ XP. The graphical user interface, as shown in Figure 45, is straightforward and easy to use. More detailed information is available in the board's user manual.

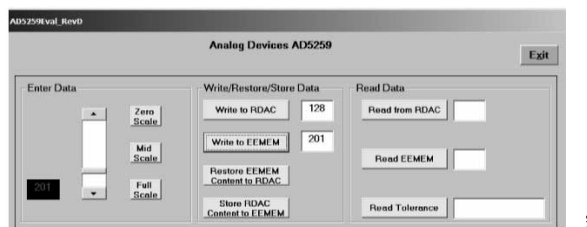


Figure 45. AD5259 Evaluation Board Software

## DISPLAY APPLICATIONS

## CIRCUITRY

A special feature of the AD5259 is its unique separation of the  $V_{LOGIC}$  and  $V_{DD}$  supply pins. The separation provides greater flexibility in applications that do not always provide needed supply voltages.

In particular, LCD panels often require a  $V_{COM}$  voltage in the range of 3 V to 5 V. The circuit in Figure 46 is the rare exception in which a 5 V supply is available to power the digital potentiometer.

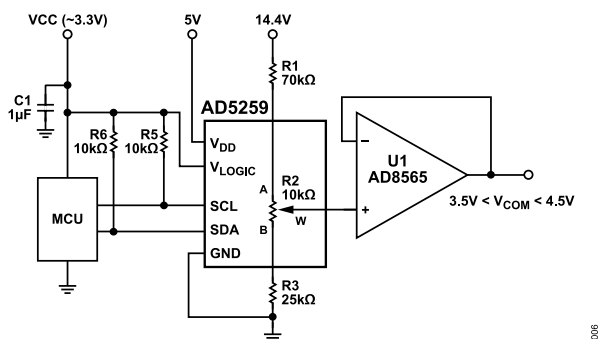


Figure 46.  $V_{COM}$  Adjustment Application

In the more common case shown in Figure 47, only analog 14.4 V and digital logic 3.3 V supplies are available. By placing discrete resistors above and below the digital potentiometer,  $V_{DD}$  can now be tapped off the resistor string itself. Based on the chosen resistor values, the voltage at  $V_{DD}$  in this case equals 4.8 V, allowing the wiper to be safely operated all the way up to 4.8 V. The current

draw of  $V_{DD}$  will not affect that node's bias because it is only on the order of microamps.  $V_{LOGIC}$  is tied to the MCU's 3.3 V digital supply because  $V_{LOGIC}$  will draw the 35 mA that is needed when writing to the EEPROM. It would be impractical to try and source 35 mA through the 70 k $\Omega$  resistor. Therefore,  $V_{LOGIC}$  is not connected to the same node as  $V_{DD}$ .

For this reason,  $V_{LOGIC}$  and  $V_{DD}$  are provided as two separate supply pins that can either be tied together or treated independently;  $V_{LOGIC}$  supplying the logic/EEPROM with power, and  $V_{DD}$  biasing up the A, B, and W terminals for added flexibility.

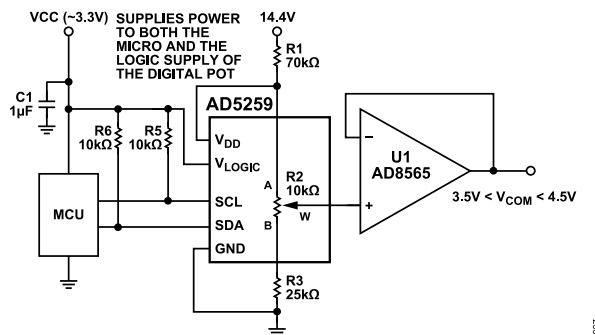


Figure 47. Circuitry When a Separate Supply is Not Available for  $V_{DD}$

For a more detailed look at this application, refer to the article, "Simple  $V_{COM}$  Adjustment uses any Logic Supply Voltage" in the September 30, 2004 issue of *EDN* magazine.

