Ultralow Input Bias Current Operational Amplifier

Data Sheet

AD549

FEATURES

- **Ultralow input bias current**
  - **60 fA maximum (AD549L)**
  - **100 fA maximum (AD549K)**
  - **250 fA maximum (AD549J)**
- **Input bias current guaranteed over the common-mode voltage range**
- **Low offset voltage**
  - **0.50 mV maximum (AD549K)**
  - **1.00 mV maximum (AD549J)**
- **Low offset drift**
  - **15 µV/°C maximum (AD549K)**
  - **20 µV/°C maximum (AD549J)**
- **Low power**
  - **700 µA maximum supply current**
  - **Low input voltage noise**
- **4 µV (typ) p-p over 0.1 Hz to 10 Hz**
- **MIL-STD-883B parts available**

APPLICATIONS

- **Electrometer amplifier**
- **Photodiode preamp**
- **pH electrode buffer**

CONNECTION DIAGRAM

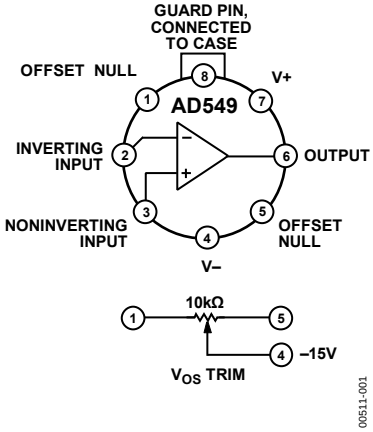

Figure 1.

GENERAL DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The ultralow input current of the part is achieved with Topgate™ JFET technology, a process development exclusive to Analog Devices, Inc. This technology allows fabrication of extremely low input current JFETs compatible with a standard junction isolated bipolar process. The 10^{15} Ω common-mode impedance, which results from the bootstrapped input stage, ensures that the input current is essentially independent of the common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers, such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample-and-hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8, thus, the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case. The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range of 0°C to +70°C. The S grade is specified over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C. Extended reliability plus screening is also available. Plus screening includes 168 hour burn-in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev. C.

PRODUCT HIGHLIGHTS

1. The AD549 input currents are specified, 100% tested, and guaranteed after the device is warmed up. They are guaranteed over the entire common-mode input voltage range.
2. The AD549 input offset voltage and drift are laser trimmed to 0.50 mV and 15 µV/°C (AD549K), and to 1 mV and 20 µV/°C (AD549J).
3. A maximum quiescent supply current of 700 µA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1 MHz unity-gain bandwidth and 3 V/µs slew rate. Settling time for a 10 V input step is 5 µs to 0.01%.

Rev. K **Document Feedback**

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SPECIFICATIONS

At 25°C and V_S = ±15 V dc, unless otherwise noted; all minimum and maximum specifications are guaranteed; specifications in **boldface** are tested on all production units at final electrical test, and results from those tests are used to calculate outgoing quality levels.

Table 1.

	AD549J			AD549K			AD549L			AD549S			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT BIAS CURRENT[1]													
Either Input, V_{CM} = 0 V		150	**250**		75	**100**		40	**60**		75	**100**	fA
Either Input, V_{CM} = ±10 V		150	250		75	100		40	60		75	100	fA
Either Input at T_{MAX}, V_{CM} = 0 V		11			4.2			2.8			420		pA
Offset Current		50			30			20			30		fA
Offset Current at T_{MAX}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE[2]													
Initial Offset		0.5	**1.0**		0.15	**0. 5**		0.3	**0.5**		0.3	**0.5**	mV
Offset at T_{MAX}			**1.9**			**0.9**			**0.9**			**2.0**	mV
vs. Temperature		10	**20**		10	**15**		5	**10**		10	**15**	µV/°C
vs. Supply		32	**100**		10	**32**		10	**32**		10	**32**	µV/V
vs. Supply, T_{MIN} to T_{MAX}		32	**100**		10	**32**		10	**32**		32	**50**	µV/V
Long-Term Offset Stability		15			15			15			15		µV/month
INPUT VOLTAGE NOISE													
f = 0.1 Hz to 10 Hz		4			4	**6**		4			4		µV p-p
f = 10 Hz		90			90			90			90		nV/√Hz
f = 100 Hz		60			60			60			60		nV/√Hz
f = 1 kHz		35			35			35			35		nV/√Hz
f = 10 kHz		35			35			35			35		nV/√Hz
INPUT CURRENT NOISE													
f = 0.1 Hz to 10 Hz		0.7			0.5			0.36			0.5		fA rms
f = 1 kHz		0.22			0.16			0.11			0.16		fA/√Hz
INPUT IMPEDANCE													
Differential													
V_{DIFF} = ±1		10^{13}||1			10^{13}||1			10^{13}||1			10^{13}||1		Ω||pF
Common Mode													
V_{CM} = ±10 V		10^{15}||0.8			10^{15}||0.8			10^{15}||0.8			10^{15}||0.8		Ω||pF
OPEN-LOOP GAIN													
V_{OUT} at ±10 V, R_L = 10 kΩ	**300**	1000		**300**	1000		**300**	1000		**300**	1000		V/mV
V_{OUT} at ±10 V, R_L = 10 kΩ, T_{MIN} to T_{MAX}	**300**	800		**300**	800		**300**	800		**300**	800		V/mV
V_{OUT} = ±10 V, R_L = 2 kΩ	**100**	250		**100**	250		**100**	250		**100**	250		V/mV
V_{OUT} = ±10 V, R_L = 2 kΩ, T_{MIN} to T_{MAX}	**80**	200		**80**	200		**80**	200		**25**	150		V/mV
INPUT VOLTAGE RANGE													
Differential[3]			±20			±20			±20			±20	V
Common-Mode Voltage	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Common-Mode Rejection Ratio													
−10 V ≤ V_{CM} ≤ +10 V	**80**	90		**90**	100		**90**	100		**90**	100		dB
T_{MIN} to T_{MAX}	**76**	80		**80**	90		**80**	90		**80**	90		dB
OUTPUT CHARACTERISTICS													
V_{OUT} at R_L = 10 kΩ, T_{MIN} to T_{MAX}	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	V
V_{OUT} at R_L = 2 kΩ, T_{MIN} to T_{MAX}	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Short-Circuit Current	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	mA
T_{MIN} to T_{MAX}	**9**			**9**			**9**			**6**			mA
Load Capacitance Stability, G = +1		4000			4000			4000			4000		pF

Parameter	AD549J			AD549K			AD549L			AD549S			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/µs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		µs
Settling Time, 0.01%		5			5			5			5		µs
Overload Recovery, 50% Overdrive, G = −1		2			2			2			2		µs
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		70	0		70	0		70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C

[1] Bias current specifications are guaranteed after five minutes of operation at T_A = 25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2] Input offset voltage specifications are guaranteed after five minutes of operation at T_A = 25°C.
[3] Defined as maximum continuous voltage between the inputs, such that neither input exceeds ±10 V from ground.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Input Voltage[1]	±18 V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	
AD549J, AD549K, AD549L	0°C to +70°C
AD549S	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

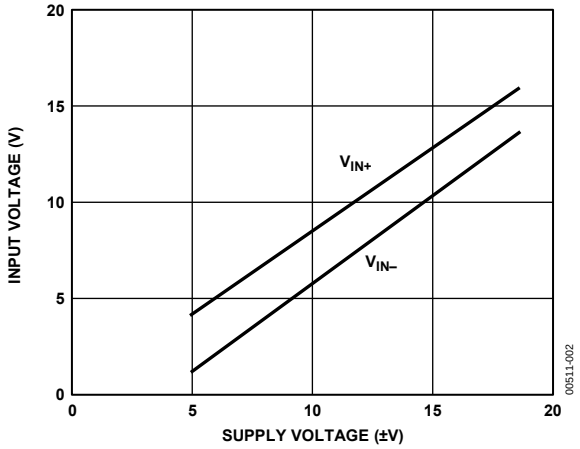

Figure 2. Input Voltage Range vs. Supply Voltage

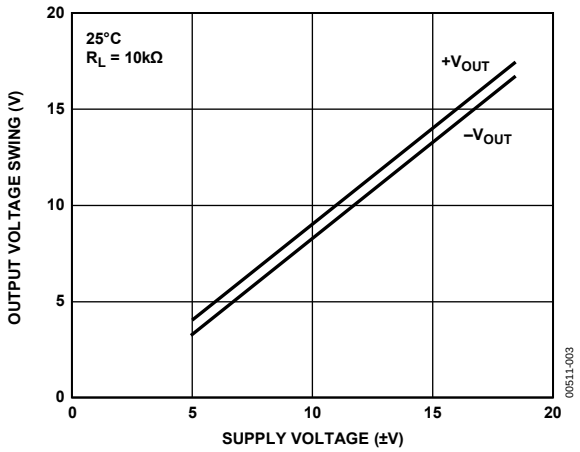

Figure 3. Output Voltage Swing vs. Supply Voltage

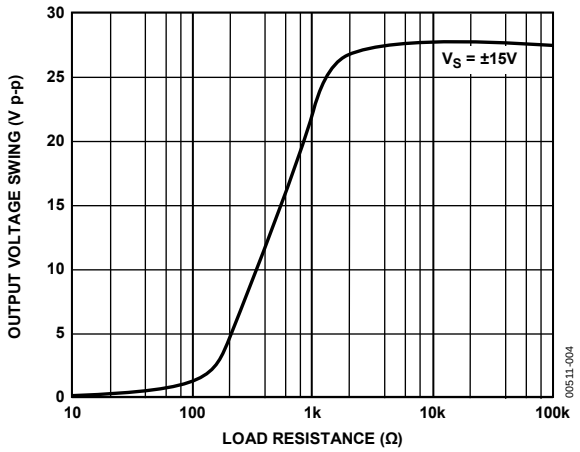

Figure 4. Output Voltage Swing vs. Load Resistance

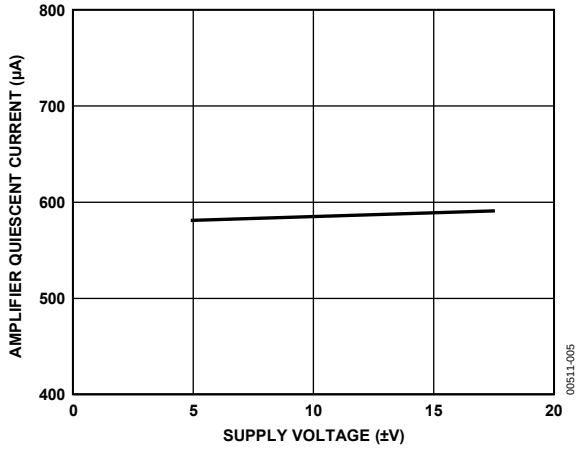

Figure 5. Quiescent Current vs. Supply Voltage

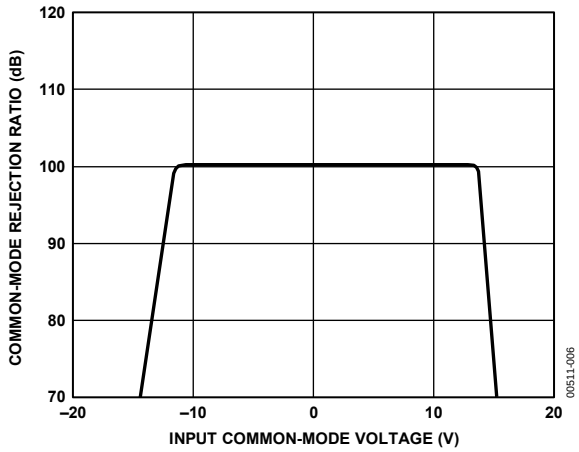

Figure 6. CMRR vs. Input Common-Mode Voltage

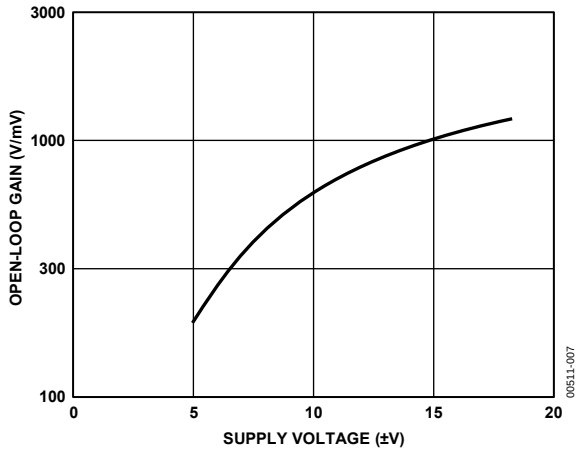

Figure 7. Open-Loop Gain vs. Supply Voltage

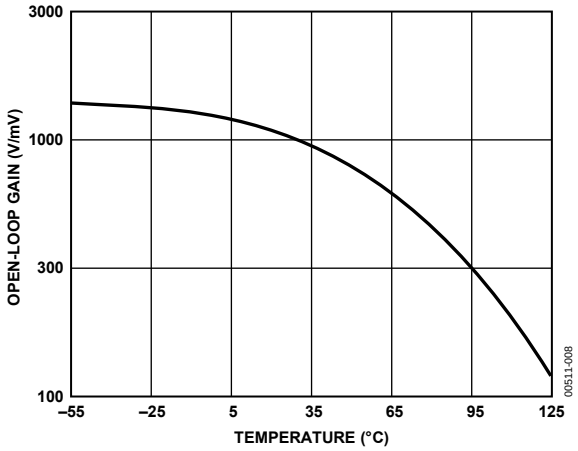

Figure 8. Open-Loop Gain vs. Temperature

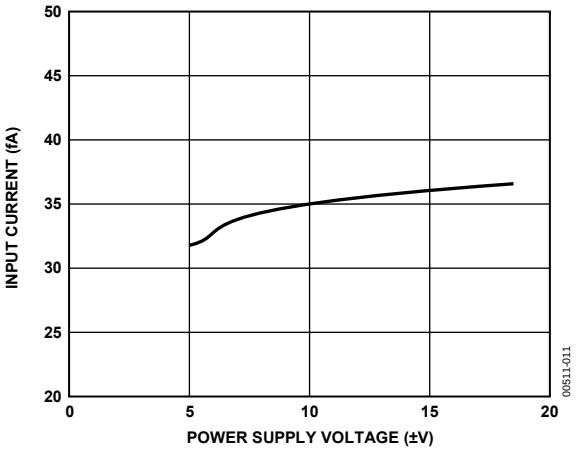

Figure 11. Input Bias Current vs. Power Supply Voltage

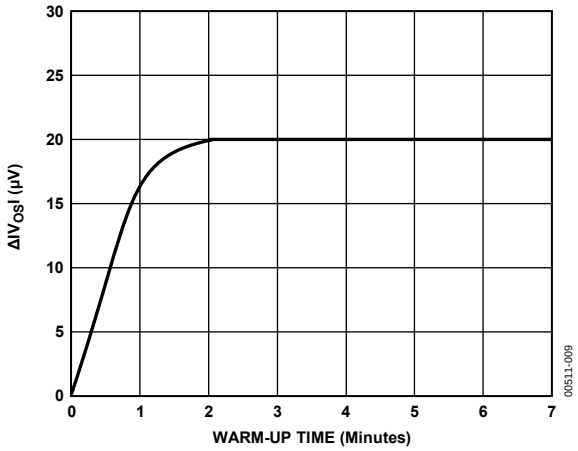

Figure 9. Change in Offset Voltage vs. Warm-Up Time

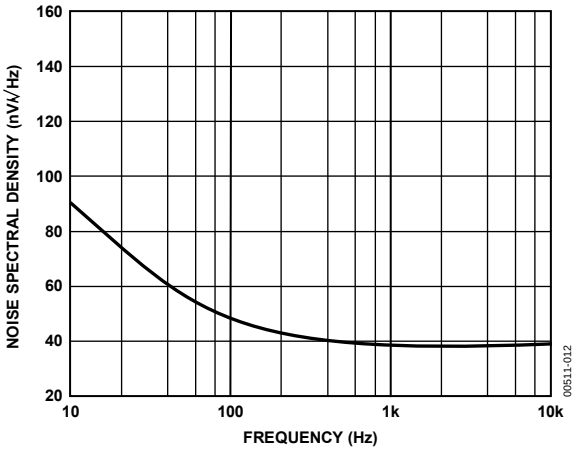

Figure 12. Input Voltage Noise Spectral Density

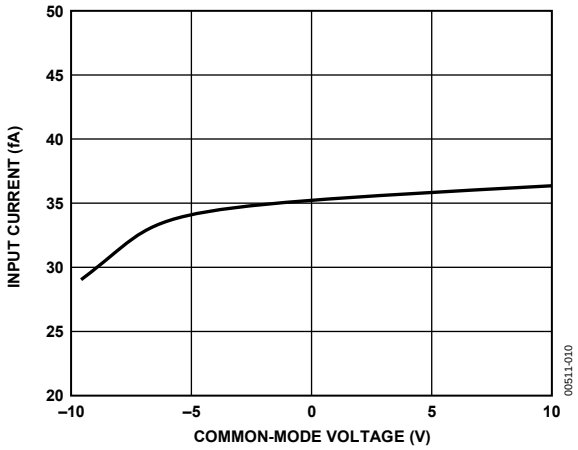

Figure 10. Input Bias Current vs. Common-Mode Voltage

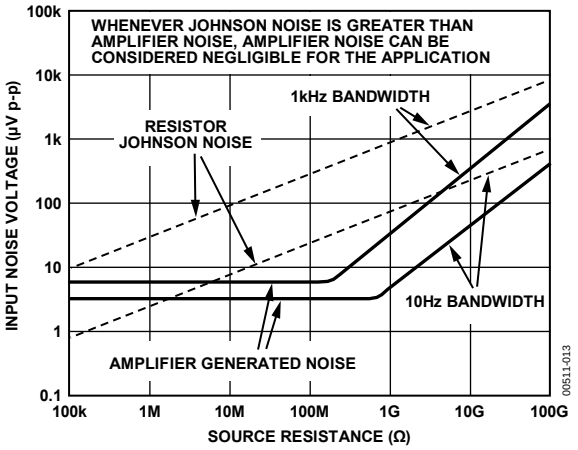

Figure 13. Noise vs. Source Resistance

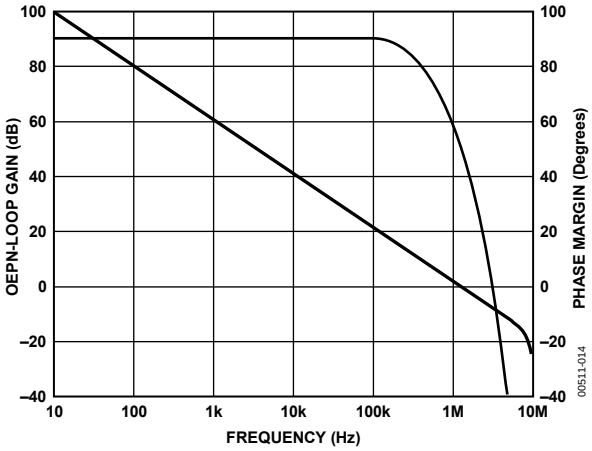

Figure 14. Open-Loop Frequency Response

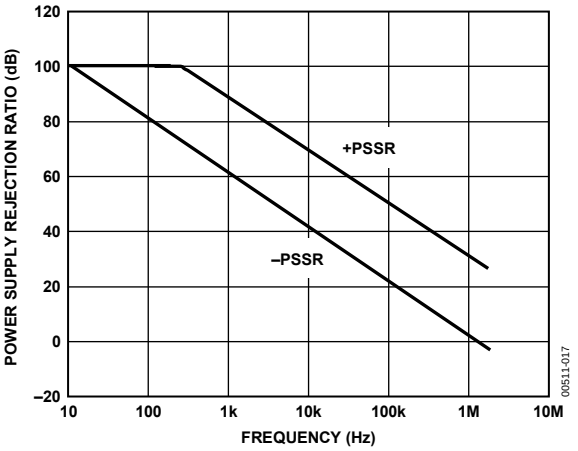

Figure 17. PSRR vs. Frequency Response

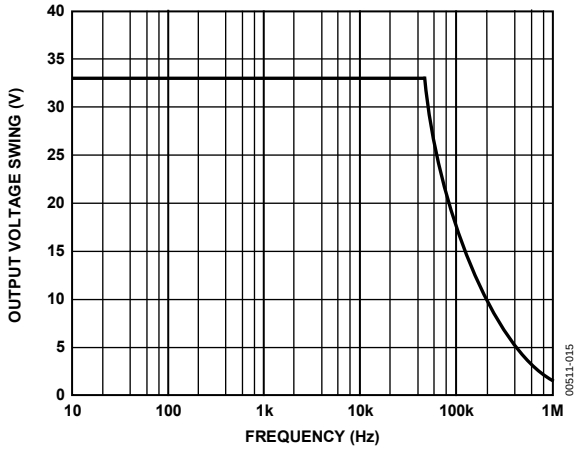

Figure 15. Large Signal Frequency Response

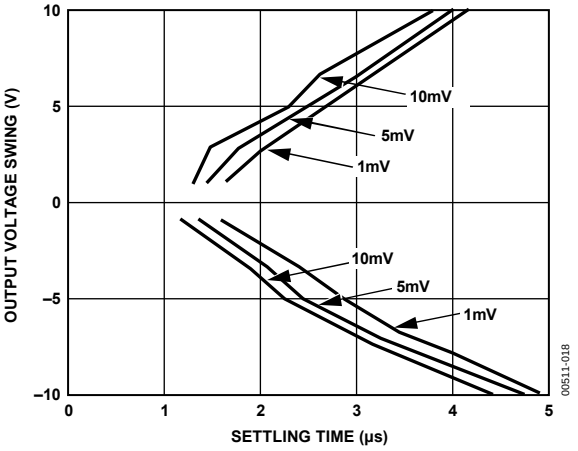

Figure 18. Output Voltage Swing and Error vs. Settling Time

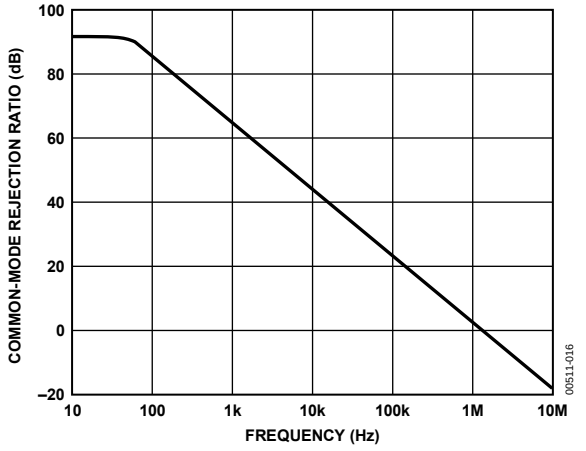

Figure 16. CMRR vs. Frequency

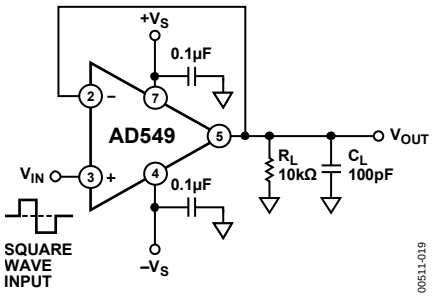

Figure 19. Unity-Gain Follower

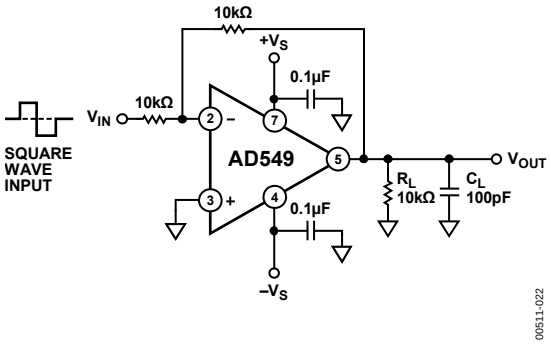

Figure 22. Unity-Gain Inverter

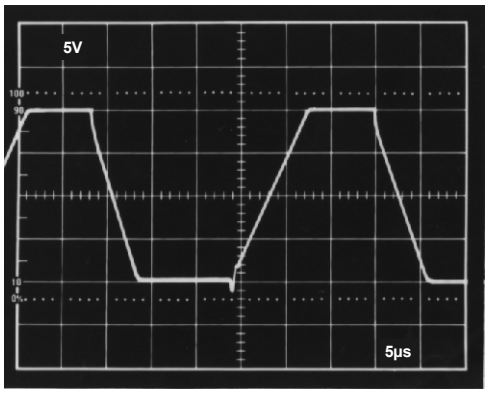

Figure 20. Unity-Gain Follower Large Signal Pulse Response

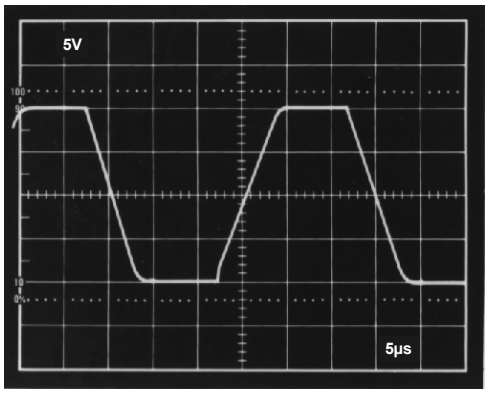

Figure 23. Unity-Gain Inverter Large Signal Pulse Response

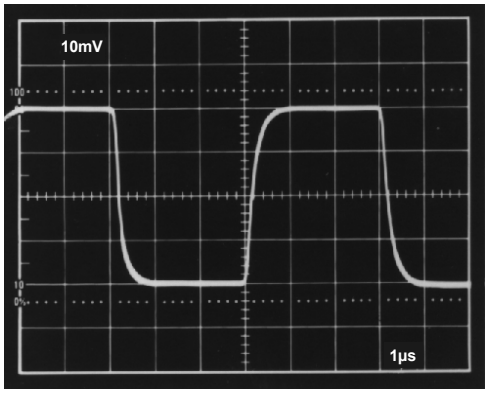

Figure 21. Unity-Gain Follower Small Signal Pulse Response

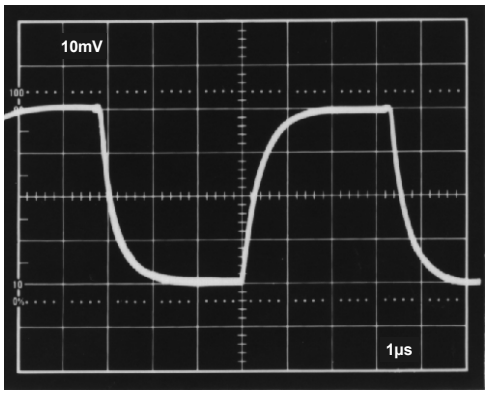

Figure 24. Unity-Gain Inverter Small Signal Pulse Response

FUNCTIONAL DESCRIPTION

MINIMIZING INPUT CURRENT

The AD549 is optimized for low input current and offset voltage. Careful attention to how the amplifier is used reduces input currents in actual applications.

Keep the amplifier operating temperature as low as possible to minimize input current. Like other JFET input amplifiers, the AD549 input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C. Figure 25 is a plot of the AD549 input current vs. ambient temperature.

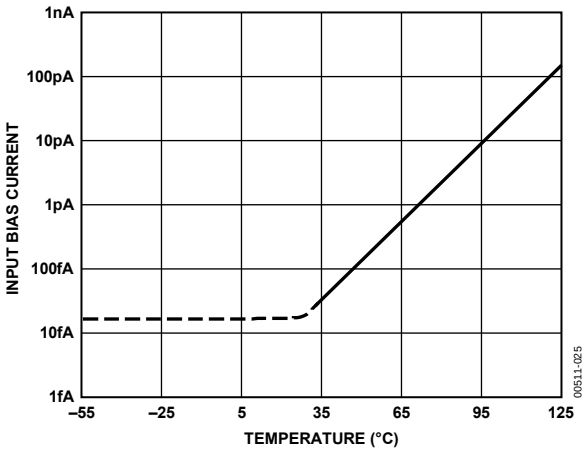

Figure 25. Input Bias Current vs. Ambient Temperature

On-chip power dissipation raises the chip operating temperature, causing an increase in input bias current. Due to the low quiescent supply current of the AD549, the chip temperature is less than 3°C higher than its ambient temperature when the (unloaded) amplifier is operating with 15 V supplies. The difference in the input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in the input current. Maintaining a minimum load resistance of 10 Ω is recommended. Input current vs. additional power dissipation due to output drive current is plotted in Figure 26.

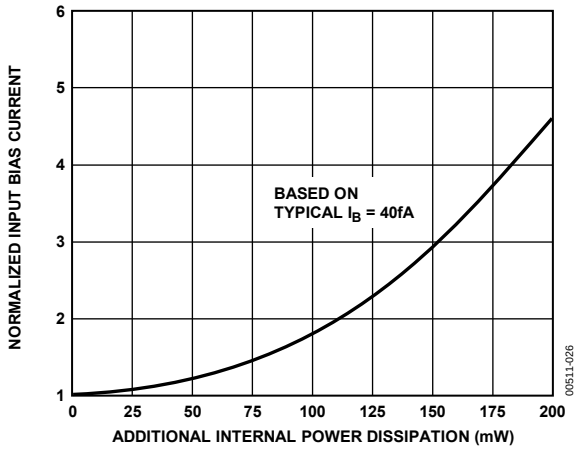

Figure 26. Input Bias Current vs. Additional Power Dissipation

CIRCUIT BOARD NOTES

A number of physical phenomena generate spurious currents that degrade the accuracy of low current measurements. Figure 27 is a schematic of a current to voltage (I-to-V) converter with these parasitic currents modeled.

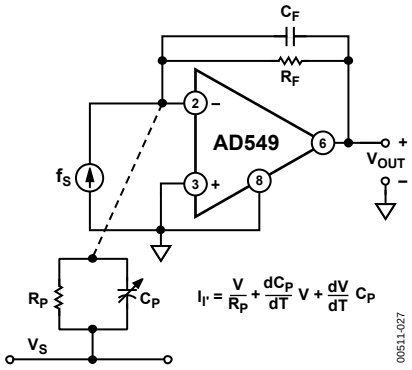

Figure 27. Sources of Parasitic Leakage Currents

Finite resistance from input lines to voltages on the board, modeled by Resistor R_P, results in parasitic leakage. Insulation resistance of more than 10^{15} Ω must be maintained between the amplifier signal and supply lines to capitalize on the low input currents of the AD549. Standard PCB material does not have high enough insulation resistance; therefore, connect the input leads of the AD549 to standoffs made of insulating material with adequate volume resistivity (that is, Teflon®). The surface of the insulator must be kept clean to preserve surface resistivity. For Teflon, an effective cleaning procedure consists of swabbing the surface with high grade isopropyl alcohol, rinsing with deionized water, and baking the board at 80°C for 10 minutes.

In addition to high volume and surface resistivity, other properties are desirable in the insulating material chosen. Resistance to water absorption is important because surface water films drastically reduce surface resistivity. The insulator chosen should also exhibit minimal piezoelectric effects (charge emission due to mechanical stress) and triboelectric effects (charge generated by friction). Charge imbalances generated by these mechanisms can appear as parasitic leakage currents. These effects are modeled by Variable Capacitor C_P in Figure 27. Table 3 lists various insulators and their properties.[2]

Guarding the input lines by completely surrounding them with a metal conductor biased near the potential of the input lines has two major benefits. First, parasitic leakage from the signal line is reduced because the voltage between the input line and the guard is very low. Second, stray capacitance at the input node is minimized. Input capacitance can substantially degrade signal bandwidth and the stability of the I-to-V converter.

[2] *Electronic Measurements*, pp. 15–17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.

The case of the AD549 is connected to Pin 8 so that it can be bootstrapped near the input potential. This minimizes pin leakage and input common-mode capacitance due to the case. Guard schemes for inverting and noninverting amplifier topologies are illustrated in Figure 28 and Figure 29.

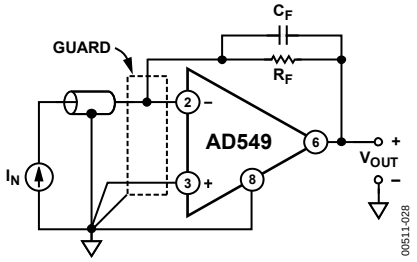

Figure 28. Inverting Amplifier with Guard

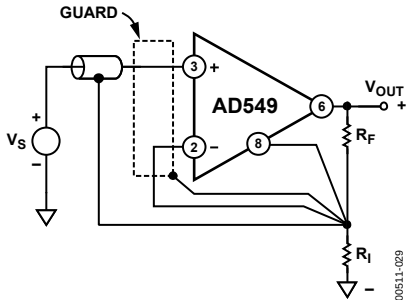

Figure 29. Noninverting Amplifier with Guard

Other guidelines include keeping the circuit layout as compact as possible and keeping the input lines short. Keeping the assembly rigid and minimizing sources of vibration reduces triboelectric and piezoelectric effects. All precision, high impedance circuitry requires shielding against interference noise. Use low noise coaxial or triaxial cables for remote connections to the input signal lines.

OFFSET NULLING

The AD549 input offset voltage can be nulled by using balance Pin 1 and Pin 5, as shown in Figure 30. Nulling the input offset voltage in this fashion introduces an added input offset voltage drift component of 2.4 µV/°C per mV of nulled offset (a maximum additional drift of 1.2 µV/°C for the AD549K and AD549L, and 2.4 µV/°C for the AD549J).

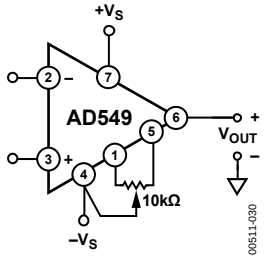

Figure 30. Standard Offset Null Circuit

The approach in Figure 31 can be used when the amplifier is used as an inverter. This method introduces a small voltage referenced to the power supplies in series with the positive input terminal of the amplifier. The amplifier input offset voltage drift with temperature is not affected. However, variation of the power supply voltages causes offset shifts.

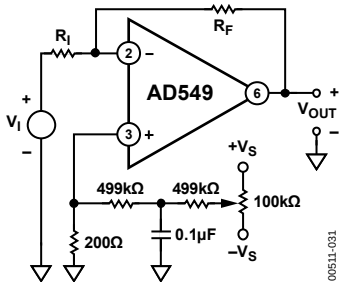

Figure 31. Alternate Offset Null Circuit for Inverter

Table 3. Insulating Materials and Characteristics

Material	Volume Resistivity (V to CM)	Minimal Triboelectric Effect[1]	Minimal Piezoelectric Effect[1]	Resistance to Water Absorption[1]
Teflon	10^{17} to 10^{18}	W	W	G
Kel-F®	10^{17} to 10^{18}	W	M	G
Sapphire	10^{16} to 10^{18}	M	G	G
Polyethylene	10^{14} to 10^{18}	M	G	M
Polystyrene	10^{12} to 10^{18}	W	M	M
Ceramic	10^{12} to 10^{14}	W	M	W
Glass Epoxy	10^{10} to 10^{17}	W	M	W
PVC	10^{10} to 10^{15}	G	M	G
Phenolic	10^{5} to 10^{12}	W	G	W

[1] G: good with regard to property; M: moderate with regard to property; W: weak with regard to property.

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ magnify the effect of the input capacitances (stray and inherent to the AD549) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account because the circuit bandwidth and stability can be adversely affected.

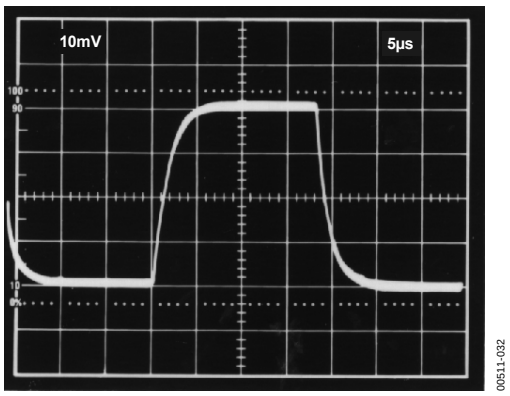

Figure 32. Follower Pulse Response from 1 MΩ Source Resistance, Case Not Bootstrapped

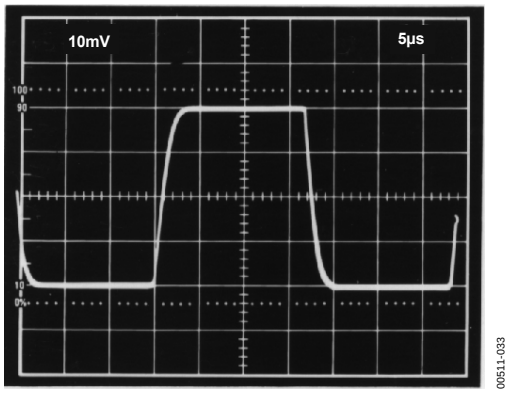

Figure 33. Follower Pulse Response from 1 MΩ Source Resistance, Case Bootstrapped

In a follower, the source resistance and input common-mode capacitance form a pole that limits the bandwidth to $\frac{1}{2}\pi R_S C_S$. Bootstrapping the metal case by connecting Pin 8 to the output minimizes capacitance due to the package. Figure 32 and Figure 33 show the follower pulse response from a 1 MΩ source resistance with and without the package connected to the output. Typical common-mode input capacitance for the AD549 is 0.8 pF.

In an inverting configuration, the differential input capacitance forms a pole in the loop transmission of the circuit. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ appears in Figure 34. Figure 35 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD549 is 1 pF.

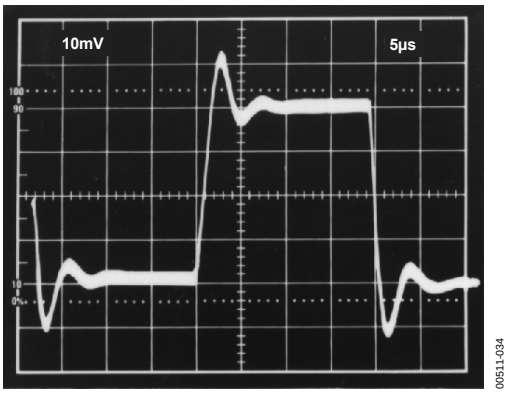

Figure 34. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

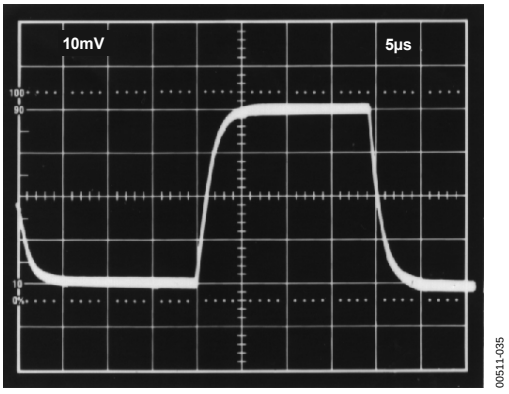

Figure 35. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

COMMON-MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD549 is from 3 V less than the positive supply voltage to 5 V greater than the negative supply voltage. Exceeding this range degrades the CMRR of the amplifier. Driving the common-mode voltage above the positive supply causes the amplifier output to saturate at the upper limit of the output voltage. Recovery time is typically 2 µs after the input has been returned to within the normal operating range. Driving the input common-mode voltage within 1 V of the negative supply causes phase reversal of the output signal. In this case, normal operation typically resumes within 0.5 µs of the input voltage returning within range.

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD549 input currents vs. differential input voltage (defined as $V_{IN+} - V_{IN-}$) appears in Figure 36. The input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 V to 1.5 V above the other terminal. Under these conditions, the input current limits at 30 µA.

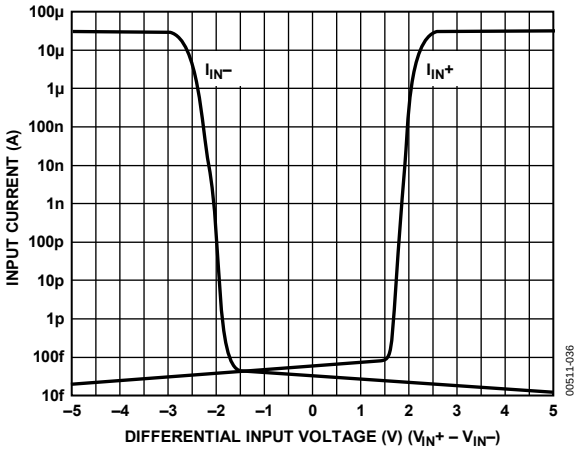

Figure 36. Input Current vs. Differential Input Voltage

INPUT PROTECTION

The AD549 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 37. R_P is chosen to limit the current through the inverting input to 1 mA for expected transient (less than 1 sec) overvoltage conditions, or to 100 µA for a continuous overload. Because R_P is inside the feedback loop and is much lower in value than the amplifier input resistance, it does not affect the dc gain of the inverter. However, the Johnson noise of the resistor adds root sum of squares to the amplifier input noise.

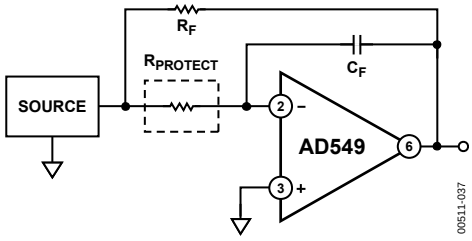

Figure 37. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 38, R_P and the capacitance at the positive input terminal produce a pole in the signal frequency response at a $f = \frac{1}{2}\pi RC$. Again, the Johnson noise, R_P, adds to the input voltage noise of the amplifier.

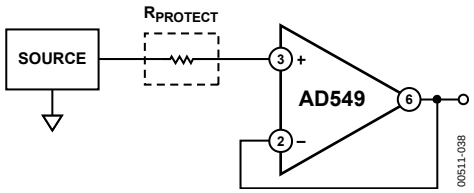

Figure 38. Follower with Input Current Limit

Figure 39 is a schematic of the AD549 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Use low leakage diodes, such as the FD333s, and shield them from light to prevent photocurrents from being generated. Even with these precautions, the diodes measurably increase input current and capacitance.

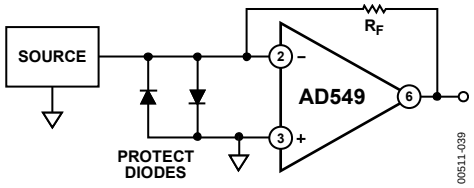

Figure 39. Input Voltage Clamp with Diodes

SAMPLE-AND-DIFFERENCE CIRCUIT TO MEASURE ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct I-to-V conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques, and care in physical layout are essential to making accurate leakage measurements.

Figure 40 is a schematic of the sample-and-difference circuit. It uses two AD549 electrometer amplifiers (A and B) as I-to-V converters with high value (10^{10} Ω) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10 fA/mV (10 pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low leakage polystyrene capacitor. An ultralow leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The use of rigid coaxial cable affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

The test apparatus is calibrated without a device under test present. After power is turned on, a 5 minute stabilization period is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by the offset voltages and leakage currents of the I-to-V converters.

$$V_{ERR1} = 10\ (V_{OS}A - I_BA \times RSa)$$

$$V_{ERR2} = 10\ (V_{OS}B - I_BB \times RSb)$$

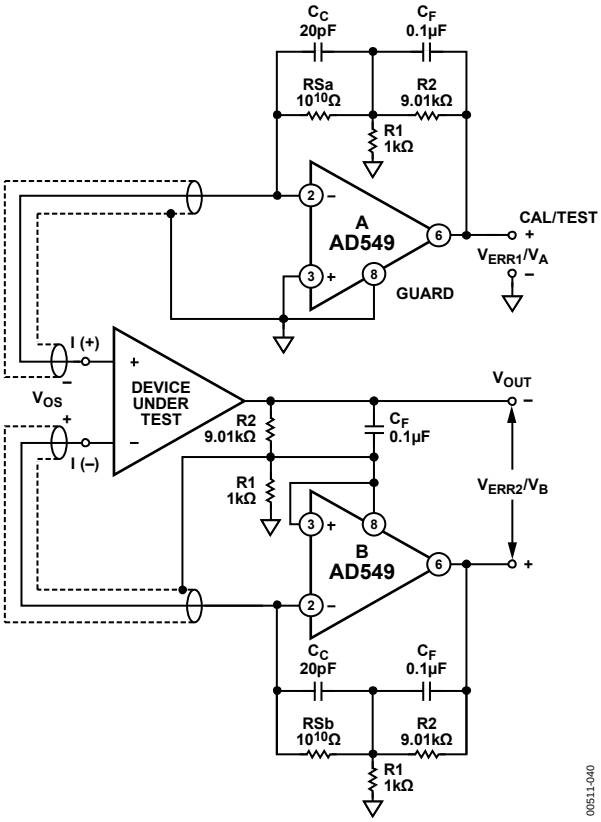

Figure 40. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under testing in addition to providing the I-to-V conversion. The offset error of the device under testing appears as a common-mode signal and does not affect the test measurement. As a result, only the leakage current of the device under testing is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$

$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the I-to-V converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10 fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The low input current and low input offset voltage of the AD549 make it an excellent choice for very sensitive photodiode preamps (see Figure 41). The photodiode develops a signal current, I_S, equal to

$$I_S = R \times P$$

where P is light power incident on the diode surface, in watts, and R is the photodiode responsivity in amps/watt. R_F converts the signal current to an output voltage

$$V_{OUT} = R_F \times I_S$$

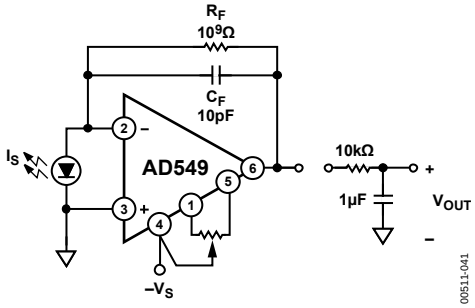

Figure 41. Photodiode Preamp

The dc error sources and an equivalent circuit for a small area (0.2 mm square) photodiode are indicated in Figure 42.

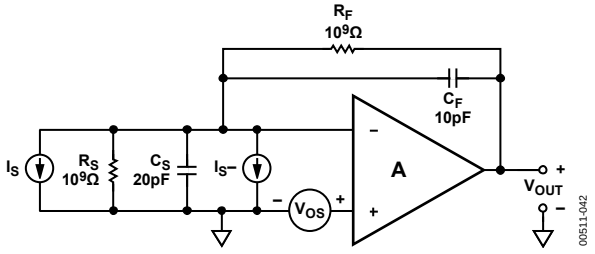

Figure 42. Photodiode Preamp DC Error Sources

Input current, I_B, contributes an output voltage error, V_{E1}, proportional to the feedback resistance

$$V_{E1} = I_B \times R_F$$

The input voltage offset of the op amp causes an error current through the photodiode shunt resistance, R_S

$$I = V_{OS}/R_S$$

The error current results in an error voltage (V_{E2}) at the amplifier output equal to

$$V_{E2} = (1 + R_F/R_S)V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of 10^9 Ω), R_F/R_S can easily be greater than 1, especially if a large feedback resistance is used. Also, R_F/R_S increases with temperature because photodiode shunt resistance typically drops by a factor of 2 for every 10°C rise in temperature. An op amp with low offset voltage and low drift must be used to maintain accuracy. The AD549K offers a guaranteed maximum 0.50 mV offset voltage and 15 mV/°C drift for very sensitive applications.

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that is detectable by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 43; Figure 44 is the spectral density vs. frequency plot of the contribution of each of the noise sources to the output voltage noise (circuit parameters in Figure 42 are assumed). The rms contribution of each noise source to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves optimizes the resolution of the preamplifier for a given bandwidth.

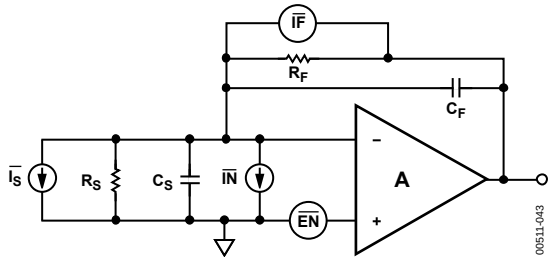

Figure 43. Photodiode Preamp Noise Sources

The photodiode preamp in Figure 41 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which, assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the peak in the noise gain that multiplies the op amp input voltage noise contribution. A single-pole filter at the output of the amplifier limits the op amp output voltage noise bandwidth to 26 Hz, comparable to the signal bandwidth. This greatly improves the signal-to-noise ratio of the preamplifier (in this case, by a factor of 3).

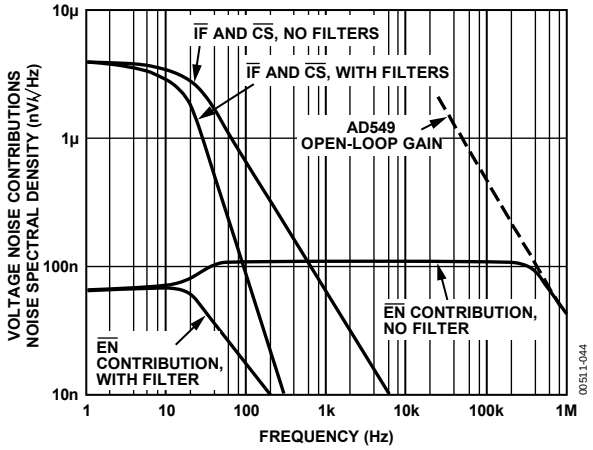

Figure 44. Spectral Density of the Photodiode Preamp Noise Sources vs. Frequency

LOG RATIO AMPLIFIER

Logarithmic ratio circuits are useful for processing signals with wide dynamic range. The 60 fA maximum input current of the AD549L makes it possible to build a log ratio amplifier with 1% log conformance for input currents ranging from 10 pA to 1 mA, a dynamic range of 160 dB.

The log ratio amplifier in Figure 45 provides an output voltage proportional to the log base 10 of the ratio of Input Current I_1 and Input Current I_2. Resistor R1 and Resistor R2 are provided for voltage inputs. Because NPN devices are used in the feedback loop of the front-end amplifiers that provide the log transfer function, the output is valid only for positive input voltages and input currents. The input currents set the Collector Current IC1 and Collector Current IC2 of a matched pair of log transistors, Q1 and Q2, to develop Voltage V_A and Voltage V_B

$$V_A, V_B = -(kT/q)\ln IC/IES$$

where *IES* is the saturation current of the transistor.

The difference of V_A and V_B is taken by the subtractor section to obtain

$$V_C = (kT/q)\ln(IC2/IC1)$$

V_C is scaled up by the ratio of (R9 + R10)/R8, which is equal to approximately 16 at room temperature, resulting in the output voltage

$$V_{OUT} = 1\text{ V} \times \log(IC2/IC1)$$

R8 is a resistor with a positive 3500 ppm/°C temperature coefficient to provide the necessary temperature compensation. The parallel combination of R15 and R7 is provided to keep the gain of the subtractor section for positive and negative inputs matched over temperature.

Frequency compensation is provided by R11, R12, C1, and C2. The bandwidth of the circuit is 300 kHz at input signals greater than 50 µA; bandwidth decreases smoothly with decreasing signal levels.

To trim the circuit, set the input currents to 10 µA and trim the A3 offset using the trim potentiometer of the amplifier for the output to equal 0. Next, set I_1 to 1 µA and adjust the output to equal 1 V by trimming R10. Additional offset trims on Amplifier A1 and Amplifier A2 can be used to increase the voltage input accuracy and dynamic range.

The very low input current of the AD549 makes this circuit useful over a very wide range of signal currents. The total input current (which determines the low level accuracy of the circuit) is the sum of the amplifier input current, the leakage across the compensating capacitor (negligible if a polystyrene or Teflon capacitor is used), and the collector-to-collector and collector-to-base leakages of one side of the dual log transistors. The magnitudes of these last two leakages depend on the amplifier input offset voltage and are typically less than 10 fA with 1 mV offsets. The low level accuracy is limited primarily by the amplifier input current, only 60 fA maximum when the AD549L is used.

The effects of the emitter resistance of Q1 and Q2 can degrade circuit accuracy at input currents above 100 µA. The networks composed of R13, D1, R16, R14, D2, and R17 compensate for these errors, so that this circuit has less than a 1% log conformance error at 1 mA input currents. The correct value for R13 and R14 depends on the type of log transistors used. The 49.9 kΩ resistors were chosen for use with LM394 transistors. Smaller resistance values are needed for smaller log transistors.

TEMPERATURE COMPENSATED pH PROBE AMPLIFIER

A pH probe can be modeled as an mV-level voltage source with a series source resistance dependent on the electrode composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 Ω and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 46 illustrates the use of the AD549 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, and Teflon standoffs is necessary to capitalize on the AD549 low input current. If an AD549L (60 fA maximum input current) is used, the error contributed by the input current is held below 60 µV for pH electrode source impedances up to 10^9 Ω. Input offset voltages (which can be trimmed) are below 0.5 mV.

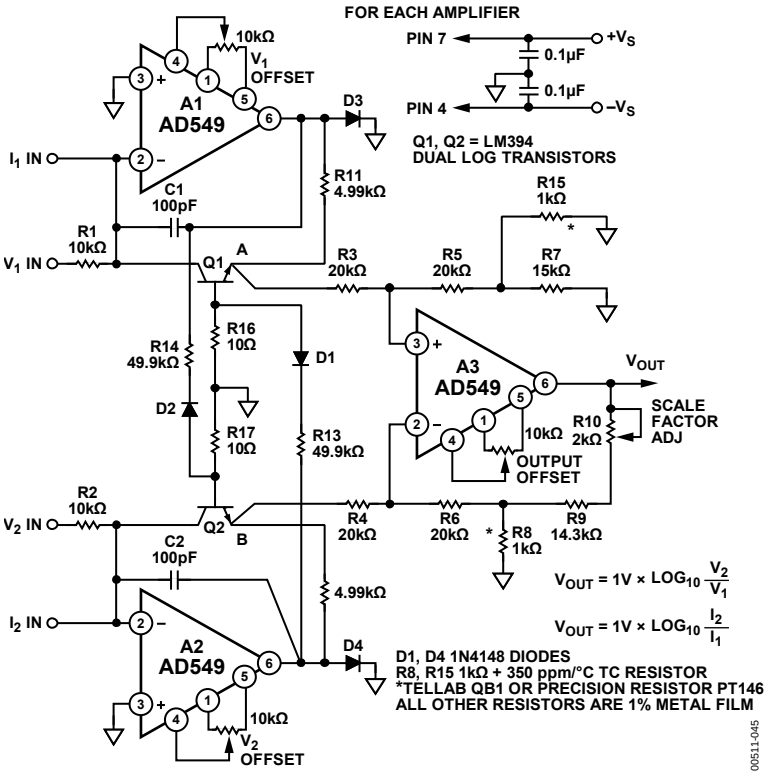

Figure 45. Log Ratio Amplifier

The pH probe output is ideally 0 V at a pH of 7, independent of temperature. The slope of the transfer function of the probe, though predictable, is temperature dependent (−54.2 mV/pH at 0°C and −74.04 mV/pH at 100°C). By using an AD590 temperature sensor and an AD534 analog divider, an accurate temperature compensation network can be added to the basic pH probe amplifier. Table 4 shows voltages at various points, thereby illustrating the compensation. The AD549 is set for a noninverting gain of 13.51. The output of the AD590 circuitry (Point C) is equal to 10 V at 100°C and decreases by 26.8 mV/°C. The output of the AD534 analog divider (Point D) is a temperature-compensated output voltage centered at 0 V for a pH of 7 and has a transfer function of –1.00 V/pH unit. The output range spans from −7.00 V (pH = 14) to +7.00 V (pH = 0).

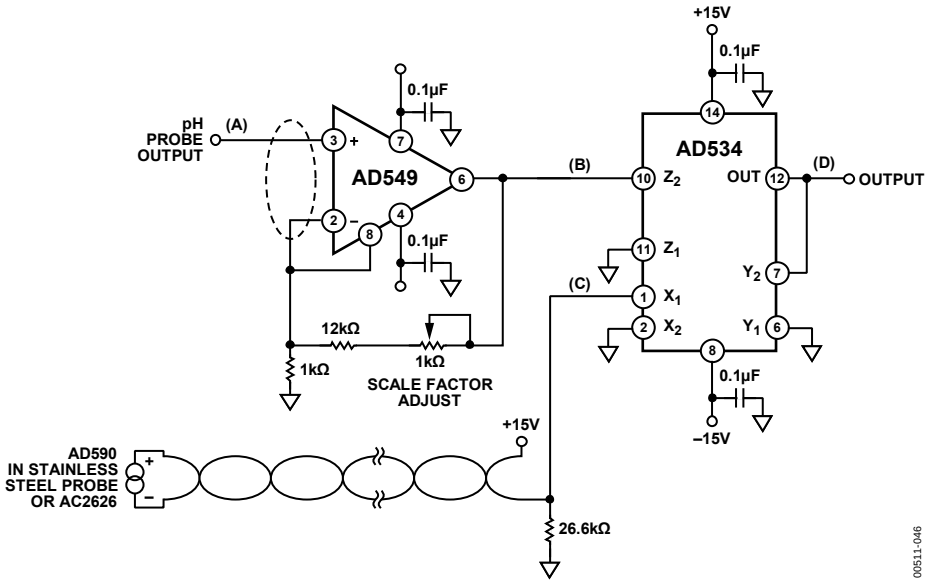

Figure 46. Temperature Compensated pH Amplifier

Table 4. Illustration of Temperature Compensation

	Point			
Probe Temperature (°C)	**A (Probe Output) (mV)**	**B (A × 13.51) (V)**	**C (AD590 Output) (V)**	**D (10 × (B ÷ C)) (V)**
0	54.20	0.732	7.32	1.00
25	59.16	0.799	7.99	1.00
37	61.54	0.831	8.31	1.00
60	66.10	0.893	8.93	1.00
100	74.04	1.000	10.00	1.00