Low Cost Instrumentation Amplifier

Data Sheet **AD622**

FEATURES

Easy to use
Low cost solution
Higher performance than two or three op amp design
Unity gain with no external resistor
Optional gains with one external resistor
  (Gain range: 2 to 1000)
Wide power supply range: ±2.6 V to ±15 V
Available in 8-lead PDIP and 8-lead SOIC_N packages
Low power, 1.5 mA maximum supply current
DC performance
  0.15% gain accuracy: G = 1
  125 µV maximum input offset voltage
  1.0 µV/°C maximum input offset drift
  5 nA maximum input bias current
  66 dB minimum common-mode rejection ratio: G = 1
Noise
  12 nV/√Hz @ 1 kHz input voltage noise
  0.60 µV p-p noise: 0.1 Hz to 10 Hz, G = 10
AC characteristics
  800 kHz bandwidth: G = 10
  10 µs settling time to 0.1% @ G = 1 to 100
  1.2 V/µs slew rate

APPLICATIONS

Transducer interface
Low cost thermocouple amplifier
Industrial process controls
Difference amplifier
Low cost data acquisition

PIN CONFIGURATION

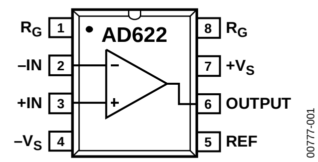

Figure 1. 8-Lead PDIP and 8-Lead SOIC_N (N and R Suffixes)

GENERAL DESCRIPTION

The AD622 is a low cost, moderately accurate instrumentation amplifier in the traditional pin configuration that requires only one external resistor to set any gain between 2 and 1000. For a gain of 1, no external resistor is required. The AD622 is a complete difference or subtractor amplifier system that also provides superior linearity and common-mode rejection by incorporating precision laser-trimmed resistors.

The AD622 replaces low cost, discrete, two or three op amp instrumentation amplifier designs and offers good common-mode rejection, superior linearity, temperature stability, reliability, power, and board area consumption. The low cost of the AD622 eliminates the need to design discrete instrumentation amplifiers to meet stringent cost targets. While providing a lower cost solution, it also provides performance and space improvements.

Table 1. Next Generation Upgrades for AD622

Part	Comment
AD8221	Better specs at lower price
AD8222	Dual channel or differential out
AD8226	Low power, wide input range
AD8220	JFET input
AD8228	Best gain accuracy
AD8295	+2 precision op amps or differential out
AD8421	Low noise, better specs

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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8/07—Rev. C to Rev. D

Updated Format ... Universal
Added Thermal Resistance Section ... 5
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Added Large Input Voltages at Large Gains Section ... 11
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4/99—Rev. B to Rev. C

8/98—Rev. A to Rev. B

2/97—Rev. 0 to Rev. A

1/96—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ typical, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
GAIN	G = 1 + (50.5 k/R_G)				
Gain Range		1		1000	
Gain Error[1]	V_{OUT} = ±10 V				
G = 1			0.05	0.15	%
G = 10			0.2	0.50	%
G = 100			0.2	0.50	%
G = 1000			0.2	0.50	%
Nonlinearity	V_{OUT} = ±10 V				
G = 1 to 1000	R_L = 10 kΩ		10		ppm
G = 1 to 100	R_L = 2 kΩ		10		ppm
Gain vs. Temperature	Gain = 1			10	ppm/°C
	Gain > 1[1]			−50	ppm/°C
VOLTAGE OFFSET	Total RTI Error = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		60	125	µV
Average Temperature Coefficient	V_S = ±5 V to ±15 V			1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V		600	1500	µV
Average Temperature Coefficient	V_S = ±5 V to ±15 V			15	µV/°C
Offset Referred to Input vs. Supply (PSR)	V_S = ±5 V to ±15 V				
G = 1		80	100		dB
G = 10		95	120		dB
G = 100		110	140		dB
G = 1000		110	140		dB
INPUT CURRENT					
Input Bias Current			2.0	5.0	nA
Average Temperature Coefficient			3.0		pA/°C
Input Offset Current			0.7	2.5	nA
Average Temperature Coefficient			2.0		pA/°C
INPUT					
Input Impedance					
Differential			10‖2		G Ω‖pF
Common Mode			10‖2		GΩ‖pF
Input Voltage Range[2]	V_S = ±2.6 V to ±5 V	$-V_S + 1.9$		$+V_S - 1.2$	V
Over Temperature		$-V_S + 2.1$		$+V_S - 1.3$	V
	V_S = ±5 V to ±18 V	$-V_S + 1.9$		$+V_S - 1.4$	V
Over Temperature		$-V_S + 2.1$		$+V_S - 1.4$	V
Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V				
G = 1		66	78		dB
G = 10		86	98		dB
G = 100		103	118		dB
G = 1000		103	118		dB
OUTPUT					
Output Swing	R_L = 10 kΩ				
	V_S = ±2.6 V to ±5 V	$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature		$-V_S + 1.4$		$+V_S - 1.3$	V
	V_S = ±5 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature		$-V_S + 1.6$		$+V_S - 1.5$	V
Short Current Circuit			±18		mA

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC RESPONSE					
Small Signal −3 dB Bandwidth					
G = 1			1000		kHz
G = 10			800		kHz
G = 100			120		kHz
G = 1000			12		kHz
Slew Rate			1.2		V/µs
Settling Time to 0.1%	10 V step				
G = 1 to 100			10		µs
NOISE					
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{(e^2_{ni}) + (e_{no}/G)2}$				
Input Voltage Noise, e_{ni}			12		nV/√Hz
Output Voltage Noise, e_{no}			72		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1			4.0		µV p-p
G = 10			0.6		µV p-p
G = 100			0.3		µV p-p
Current Noise	f = 1 kHz		100		fA/√Hz
0.1 Hz to 10 Hz			10		pA p-p
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		50	60	µA
Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	V
Gain to Output			1 ± 0.0015		
POWER SUPPLY					
Operating Range[3]		±2.6		±18	V
Quiescent Current	V_S = ±2.6 V to ±18 V		0.9	1.3	mA
Over Temperature			1.1	1.5	mA
TEMPERATURE RANGE					
For Specified Performance			−40 to +85		°C

[1] Does not include effects of External Resistor R_G.
[2] One input grounded, G = 1.
[3] Defined as the same supply range that is used to specify PSR.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	650 mW
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage[2]	±25 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air; see Table 4.
[2] May be further restricted for gains greater than 14. See the Input Protection section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

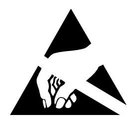
THERMAL RESISTANCE

θ_{JA} is specified for the device in free air.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead PDIP (N-8)	95	°C/W
8-Lead SOIC_N (R-8)	155	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted.

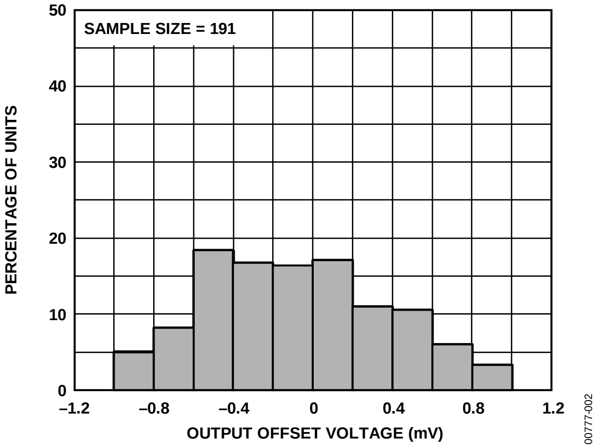


Figure 2. Typical Distribution of Output Offset Voltage

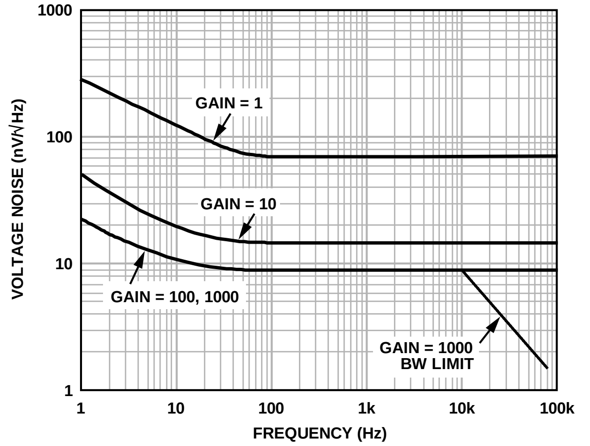


Figure 5. Voltage Noise Spectral Density vs. Frequency (G = 1 to 1000)

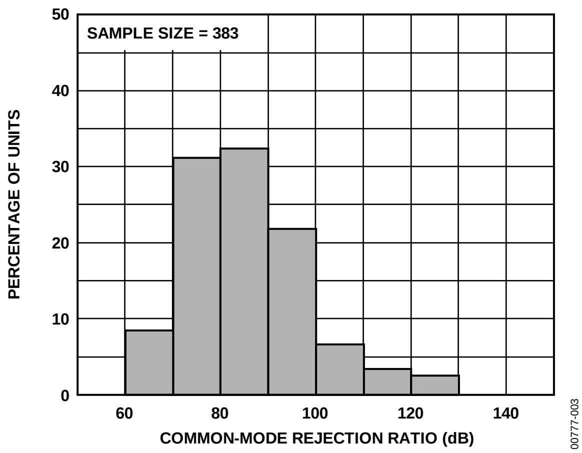


Figure 3. Typical Distribution of Common-Mode Rejection

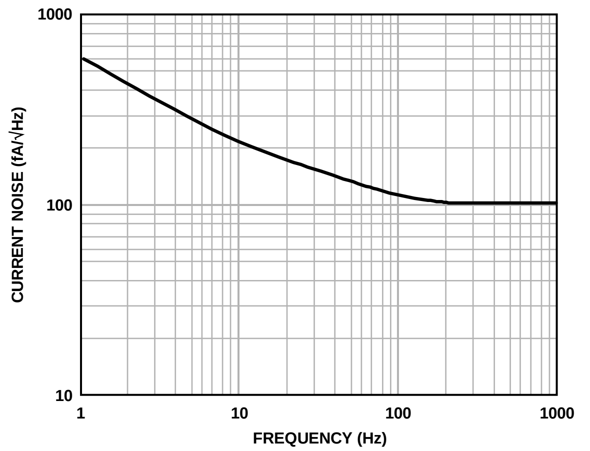


Figure 6. Current Noise Spectral Density vs. Frequency

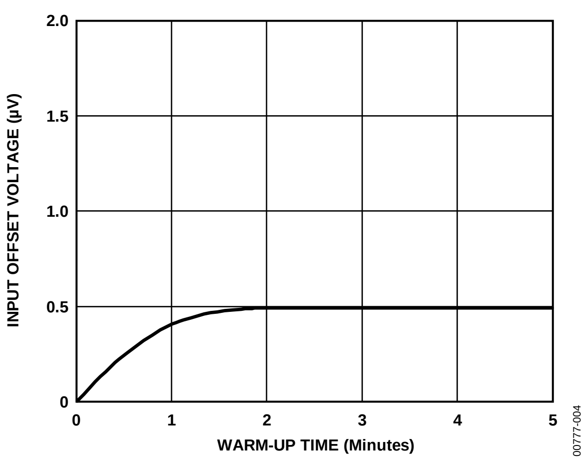


Figure 4. Change in Input Offset Voltage vs. Warm-Up Time

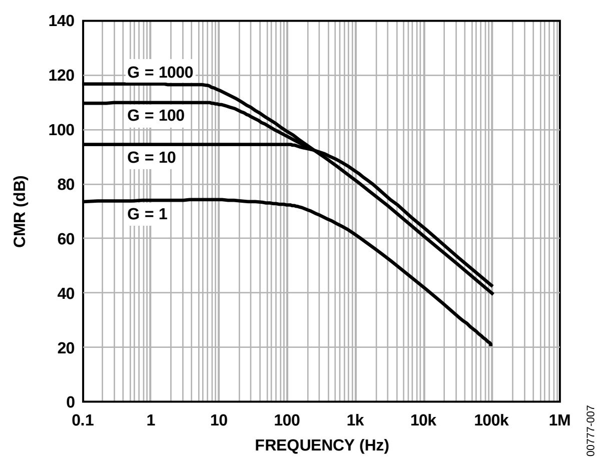


Figure 7. CMR vs. Frequency, RTI, 0 kΩ to 1 kΩ Source Imbalance

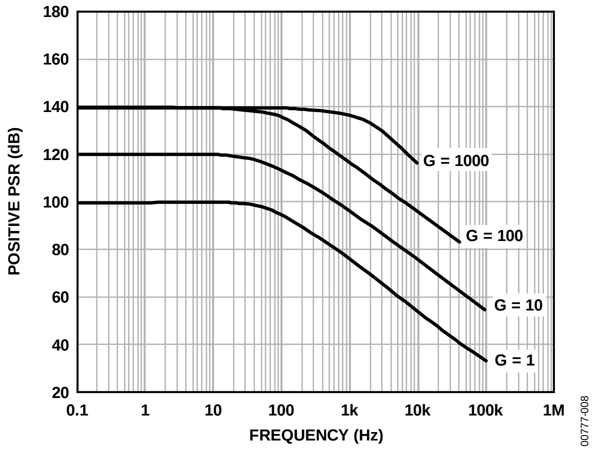


Figure 8. Positive PSR vs. Frequency, RTI (G = 1 to 1000)

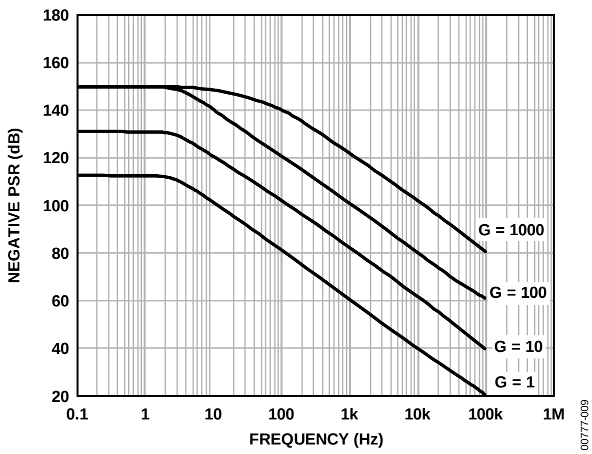


Figure 9. Negative PSR vs. Frequency, RTI (G = 1 to 1000)

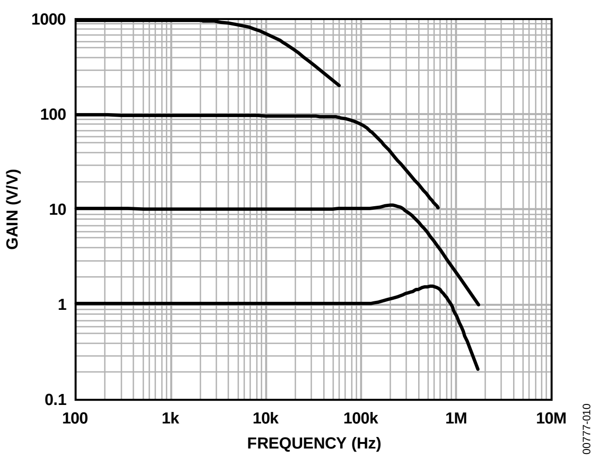


Figure 10. Gain vs. Frequency

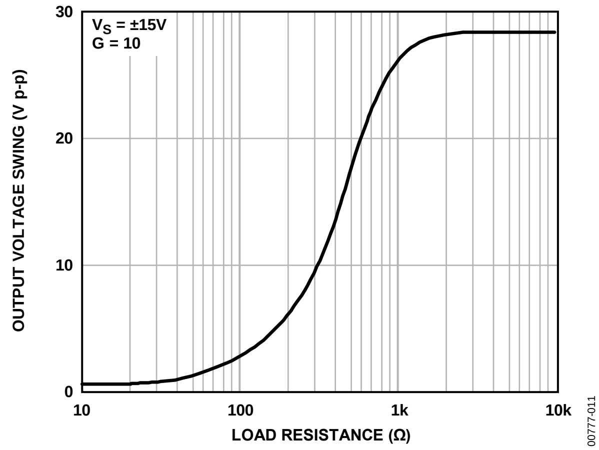


Figure 11. Output Voltage Swing vs. Load Resistance

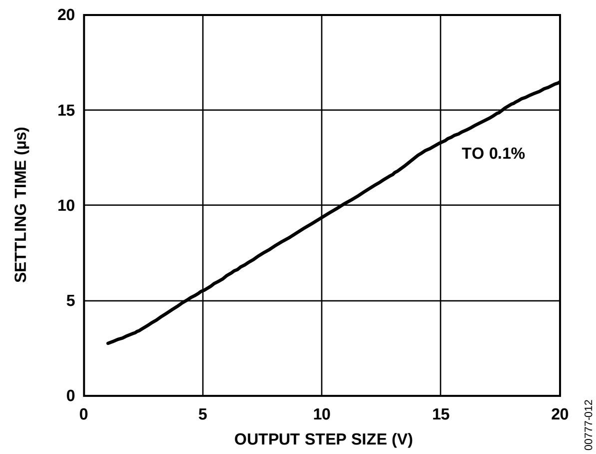


Figure 12. Settling Time vs. Step Size (G = 1)

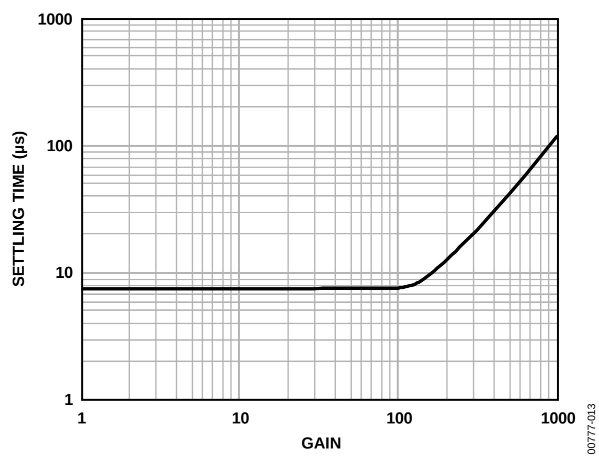


Figure 13. Settling Time to 0.1% vs. Gain, for a 10 V Step

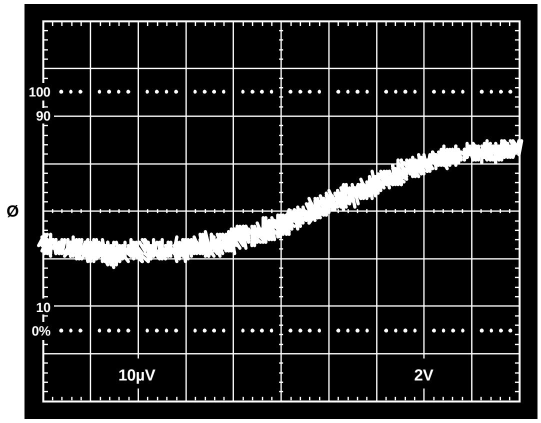


Figure 14. Gain Nonlinearity, G = 1, R_L = 10 kΩ (20 µV = 2 ppm)

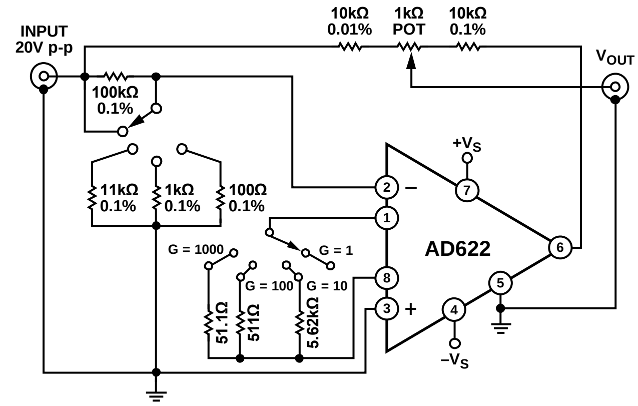


Figure 15. Settling Time Test Circuit

THEORY OF OPERATION

The AD622 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain accurately (to 0.5% at G = 1000) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus insuring AD622 performance.

Input Transistor Q1 and Input Transistor Q2 provide a single differential-pair bipolar input for high precision (see Figure 16). Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the Q1 and Q2 input devices, thereby impressing the input voltage across External Gain-Setting Resistor R_G. This creates a differential gain from the inputs to the A1 and A2 outputs given by $G = (R1 + R2)/R_G + 1$. Unity-Gain Subtractor A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

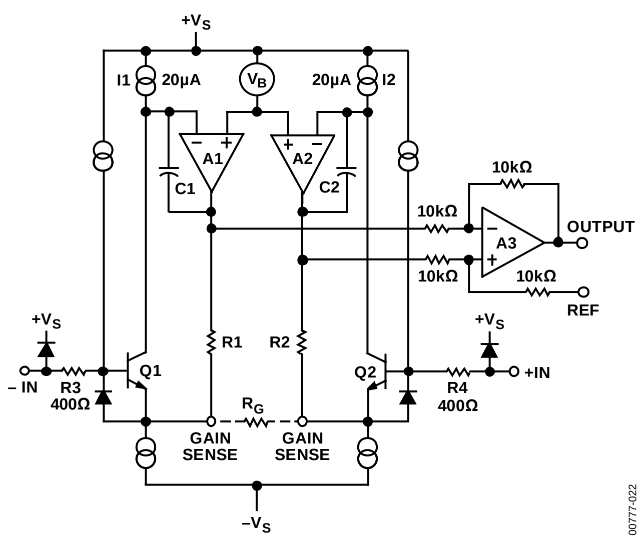


Figure 16. Simplified Schematic of the AD622

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has the following three important advantages:

- Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors.
- The gain-bandwidth product (determined by C1, C2, and the preamp transconductance) increases with programmed gain, thus optimizing frequency response.
- The input voltage noise is reduced to a value of 12 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 25.25 kΩ, allowing the gain to be programmed accurately with a single external resistor.

MAKE vs. BUY: A TYPICAL APPLICATION ERROR BUDGET

The AD622 offers cost and performance advantages over discrete two op amp instrumentation amplifier designs along with smaller size and fewer components. In a typical application shown in Figure 17, a gain of 10 is required to receive and amplify a 0 to 20 mA signal from the AD694 current transmitter. The current is converted to a voltage in a 50 Ω shunt. In applications where transmission is over long distances, line impedance can be significant so that differential voltage measurement is essential. Where there is no connection between the ground returns of transmitter and receiver, there must be a dc path from each input to ground, implemented in this case using two 1 kΩ resistors. The error budget detailed in Table 5 shows how to calculate the effect of various error sources on circuit accuracy.

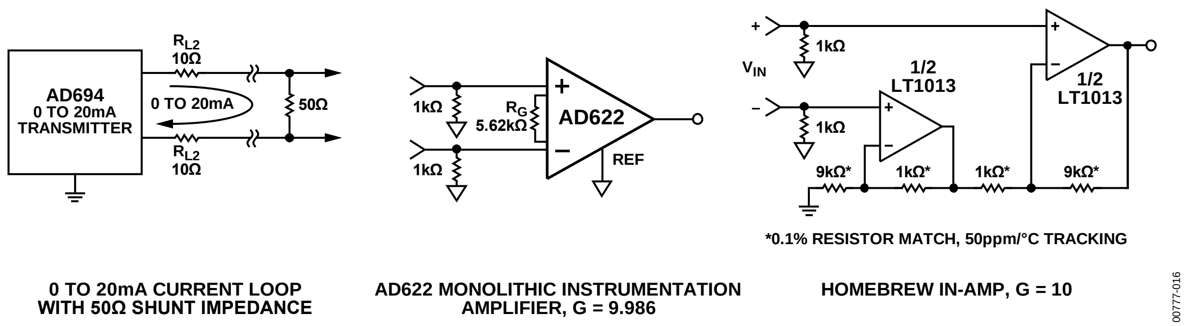


Figure 17. Make vs. Buy

The AD622 provides greater accuracy at lower cost. The higher cost of the homebrew circuit is dominated in this case by the matched resistor network. One could also realize a homebrew design using cheaper discrete resistors that are either trimmed or hand selected to give high common-mode rejection. This level of common-mode rejection, however, degrades significantly over temperature due to the drift mismatch of the discrete resistors.

Note that for the homebrew circuit, the LT1013 specification for noise has been multiplied by √2. This is because a two op amp type instrumentation amplifier has two op amps at its inputs, both contributing to the overall noise.

Table 5. Make vs. Buy Error Budget

			Total Error in ppm Relative to 1 V FS	
Error Source	**AD622 Circuit Calculation**	**Homebrew Circuit Calculation**	**AD622**	**Homebrew**
ABSOLUTE ACCURACY at T_A = 25°C				
Total RTI Offset Voltage, µV	125 µV + 1500 µV/10	800 µV × 2	275	1600
Input Offset Current, nA	2.5 nA × 1 kΩ	15 nA × 1 kΩ	2.5	15
CMR, dB	86 dB→50 ppm × 0.5 V	(0.1% Match × 0.5 V)/10 V	25	50
		Total Absolute Error	302.5	1665
DRIFT TO 85°C				
Gain Drift, ppm/°C	(50 ppm + 5 ppm) × 60°C	(50 ppm)/°C × 60°C	3300	3000
Total RTI Offset Voltage, µV/°C	(1 µV/°C + 15 µV/°C /10) × 60°C	9 µV/°C × 2 × 60°C	150	1080
Input Offset Current, pA/°C	2 pA/°C × 1 kΩ × 60°C	155 pA/°C × 1 kΩ × 60°C	0.12	9.3
		Total Drift Error	3450.12	4089.3
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	10 ppm	20 ppm	10	20
Typ 0.1 Hz to 10 Hz Voltage Noise, µV p-p	0.6 µV p-p	0.55 µV p-p × √2	0.6	0.778
		Total Resolution Error	10.6	20.778
		Grand Total Error	3763	5775

GAIN SELECTION

The AD622 gain is resistor programmed by R_G or, more precisely, by whatever impedance appears between Pin 1 and Pin 8. The AD622 is designed to offer gains as close as possible to popular integer values using standard 1% resistors. Table 6 shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula

$$R_G = \frac{50.5\ \text{k}\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G. To minimize gain drift, R_G should have a low temperature coefficient less than 10 ppm/°C for the best performance.

Table 6. Required Values of Gain Resistors

Desired Gain	1% Std Table Value of R_G, Ω	Calculated Gain
2	51.1 k	1.988
5	12.7 k	4.976
10	5.62 k	9.986
20	2.67 k	19.91
33	1.58 k	32.96
40	1.3 k	39.85
50	1.02 k	50.50
65	787	65.17
100	511	99.83
200	255	199.0
500	102	496.1
1000	51.1	989.3

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD622 are attributable to two sources: input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as follows:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. The reference terminal provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD622 safely withstands an input current of ±60 mA for several hours at room temperature. This is true for all gains and power on and off, which is useful if the signal source and amplifier are powered separately. For longer time periods, the input current should not exceed 6 mA.

For input voltages beyond the supplies, a protection resistor should be placed in series with each input to limit the current to 6 mA. These can be the same resistors as those used in the RFI filter. High values of resistance can impact the noise and AC CMRR performance of the system. Low leakage diodes (such as the BAV199) can be placed at the inputs to reduce the required protection resistance.

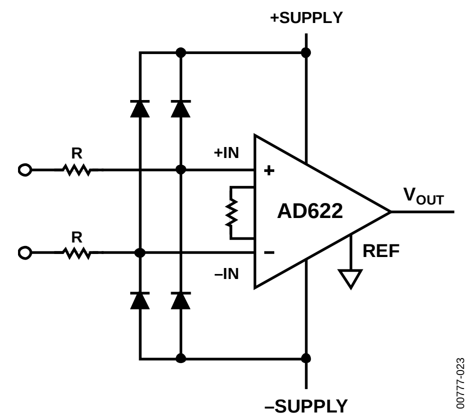


Figure 18. Diode Protection for Voltages Beyond Supply

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance may appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass, RC network placed at the input of the instrumentation amplifier, as shown in Figure 19. In addition, this RC input network also provides additional input overload protection (see the Input Protection section).

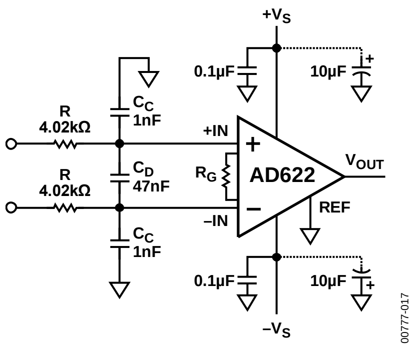


Figure 19. RFI Suppression Circuit for AD622 Series In-Amps

The filter limits the input signal bandwidth to the following cutoff frequencies:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

Figure 19 shows an example where the differential filter frequency is approximately 400 Hz, and the common-mode filter frequency is approximately 40 kHz. With this differential filter in place and operating at gain of 1000, the typical dc offset shift over a frequency range of 1 Hz to 20 MHz is less than 1.5 µV RTI, and the RF signal rejection of the circuit is better than 71 dB. At a gain of 100, the dc offset shift is well below 1 mV RTI, and RF rejection is greater than 70 dB.

The input resistors should be selected to be high enough to isolate the sensor from the C_C and C_D capacitors but low enough not to influence system noise. Mismatch between $R \times C_C$ at the positive input and $R \times C_C$ at the negative input degrades the CMRR of the AD622. Therefore, the C_C capacitors should be high precision types such as NPO/COG ceramics. The tolerance of the C_D capacitor is less critical.

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore, when amplifying floating input sources such as transformers or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 20, Figure 21, and Figure 22. Refer to the *Designer's Guide to Instrumentation Amplifiers* (free from Analog Devices, Inc.) for more information regarding in-amp applications.

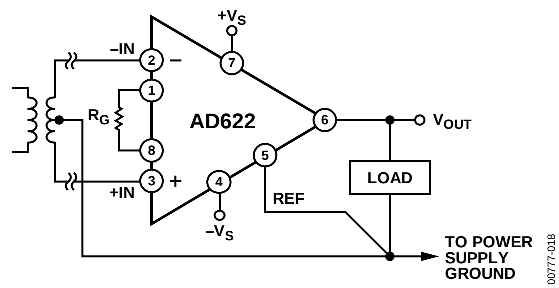


Figure 20. Ground Returns for Bias Currents with Transformer Coupled Inputs

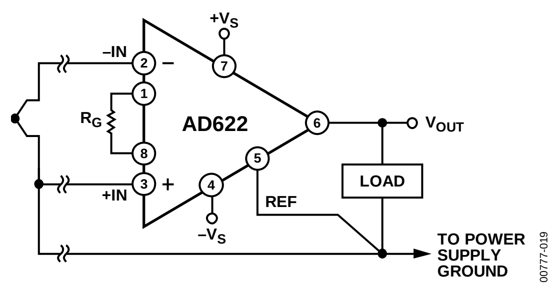


Figure 21. Ground Returns for Bias Currents with Thermocouple Inputs

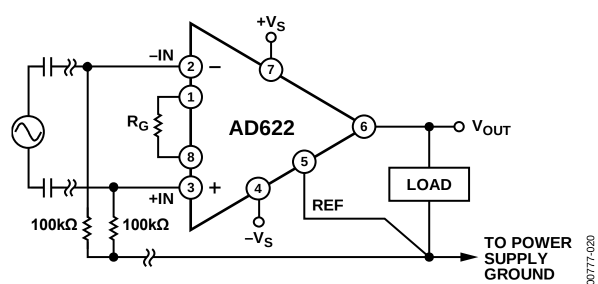


Figure 22. Ground Returns for Bias Currents with AC-Coupled Inputs

OUTLINE DIMENSIONS

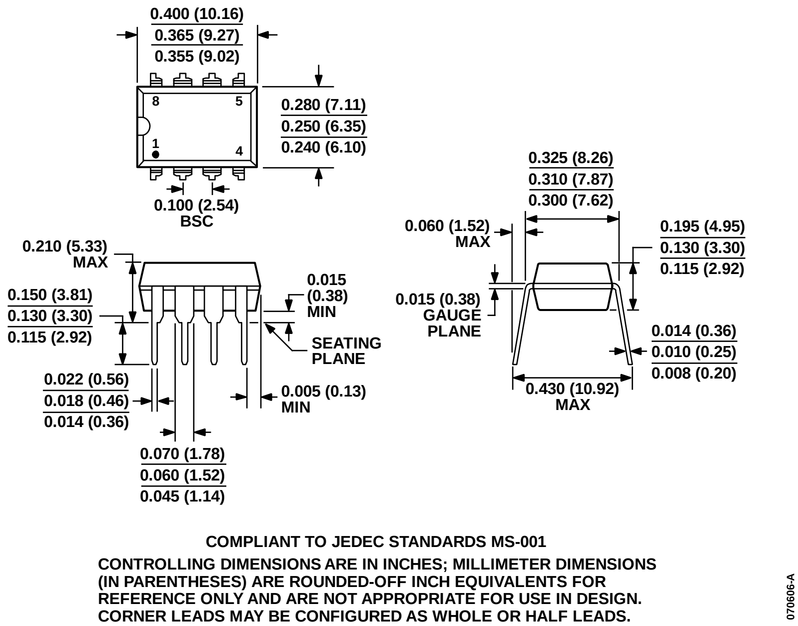


Figure 23. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)

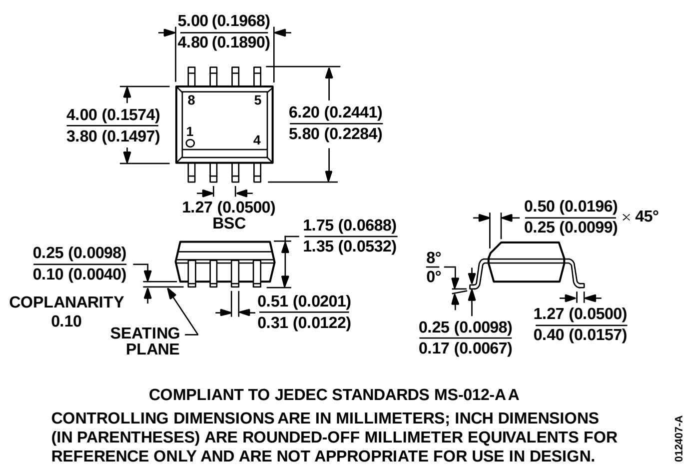


Figure 24. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD622ANZ	−40°C to +85°C	8-Lead PDIP	N-8
AD622AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD622AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD622AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD622ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD622ARZ-RL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD622ARZ-R7	−40°C to +85°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

NOTES