Low Cost Analog Multiplier

Data Sheet

AD633

FEATURES

4-quadrant multiplication
Low cost, 8-lead SOIC and PDIP packages
Complete—no external components required
Laser-trimmed accuracy and stability
Total error within 2% of full scale
Differential high impedance X and Y inputs
High impedance unity-gain summing input
Laser-trimmed 10 V scaling reference

APPLICATIONS

Multiplication, division, squaring
Modulation/demodulation, phase detection
Voltage-controlled amplifiers/attenuators/filters

FUNCTIONAL BLOCK DIAGRAM

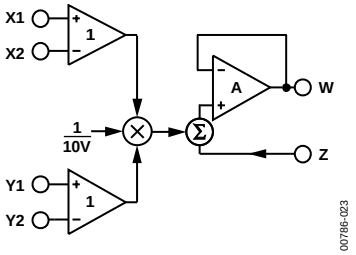

Figure 1.

GENERAL DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs, and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead PDIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The versatility of the AD633 is not compromised by its simplicity. The Z input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications. For further information, see the Multiplier Application Guide.

The AD633 is available in 8-lead PDIP and SOIC packages. It is specified to operate over the 0°C to 70°C commercial temperature range (J Grade) or the −40°C to +85°C industrial temperature range (A Grade).

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-lead SOIC and PDIP packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

Rev. K **Document Feedback**

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SPECIFICATIONS

T_A = 25°C, V_S = ±15 V, $R_L \geq 2$ kΩ.

Table 1.

Parameter	Conditions	AD633J, AD633A Min	Typ	Max	Unit
TRANSFER FUNCTION			$W = \frac{(X1 - X2)(Y1 - Y2)}{10\ \text{V}} + Z$		
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	±2[1]	% full scale
T_{MIN} to T_{MAX}			±3		% full scale
Scale Voltage Error	SF = 10.00 V nominal		±0.25%		% full scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% full scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	±1[1]	% full scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	±0.4[1]	% full scale
X Feedthrough	Y nulled, X = ±10 V		±0.3	±1[1]	% full scale
Y Feedthrough	X nulled, Y = ±10 V		±0.1	±0.4[1]	% full scale
Output Offset Voltage[2]			±5	±50[1]	mV
DYNAMICS					
Small Signal Bandwidth	V_O = 0.1 V rms		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/µs
Settling Time to 1%	ΔV_O = 20 V		2		µs
OUTPUT NOISE					
Spectral Density			0.8		µV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		µV rms
OUTPUT					
Output Voltage Swing		±11[1]			V
Short Circuit Current	R_L = 0 Ω		30	40[1]	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	±10[1]			V
	Common mode	±10[1]			V
Offset Voltage (X, Y)			±5	±30[1]	mV
CMRR (X, Y)	V_{CM} = ±10 V, f = 50 Hz	60[1]	80		dB
Bias Current (X, Y, Z)			0.8	2.0[1]	µA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		±8[1]		±18[1]	V
Supply Current	Quiescent		4	6[1]	mA

[1] This specification was tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All minimum and maximum specifications are guaranteed; however, only this specification was tested on all production units.

[2] Allow approximately 0.5 ms for settling following power on.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Input Voltages[1]	±18 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AD633J	0°C to 70°C
AD633A	−40°C to +85°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Rating	1000 V

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	Unit
8-Lead PDIP	90	°C/W
8-Lead SOIC	155	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

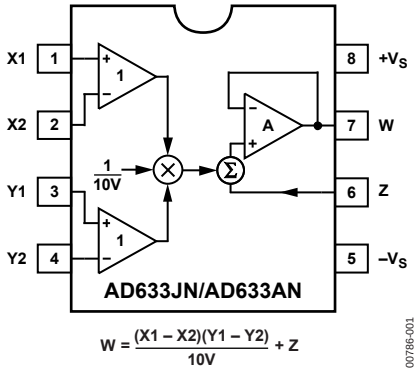


Figure 2. 8-Lead PDIP

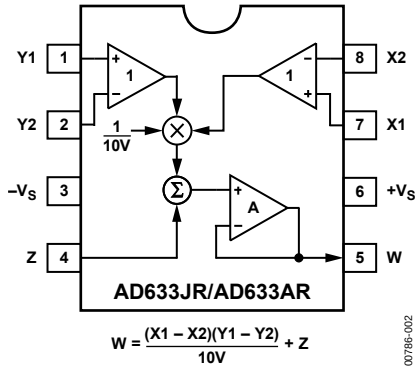


Figure 3. 8-Lead SOIC

Table 4. 8-Lead PDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	X Multiplicand Noninverting Input
2	X2	X Multiplicand Inverting Input
3	Y1	Y Multiplicand Noninverting Input
4	Y2	Y Multiplicand Inverting Input
5	$-V_S$	Negative Supply Rail
6	Z	Summing Input
7	W	Product Output
8	$+V_S$	Positive Supply Rail

Table 5. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y1	Y Multiplicand Noninverting Input
2	Y2	Y Multiplicand Inverting Input
3	$-V_S$	Negative Supply Rail
4	Z	Summing Input
5	W	Product Output
6	$+V_S$	Positive Supply Rail
7	X1	X Multiplicand Noninverting Input
8	X2	X Multiplicand Inverting Input

TYPICAL PERFORMANCE CHARACTERISTICS

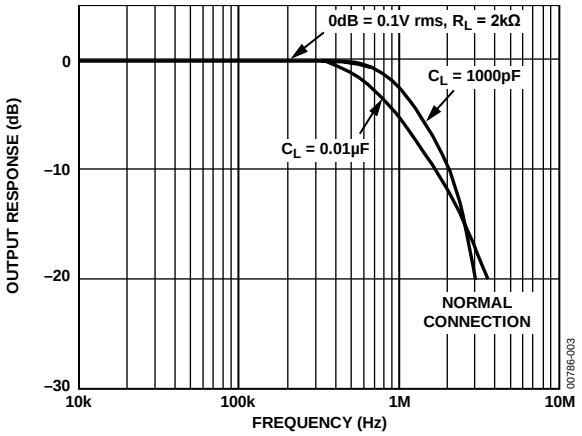


Figure 4. Frequency Response

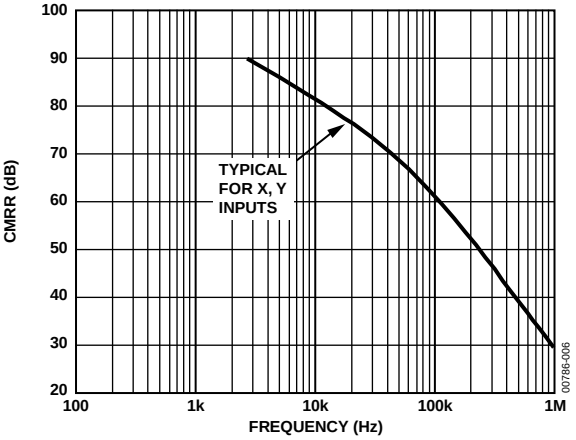


Figure 7. CMRR vs. Frequency

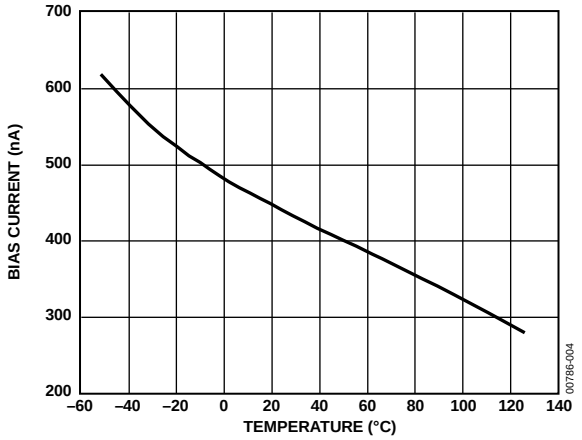


Figure 5. Input Bias Current vs. Temperature (X, Y, or Z Inputs)

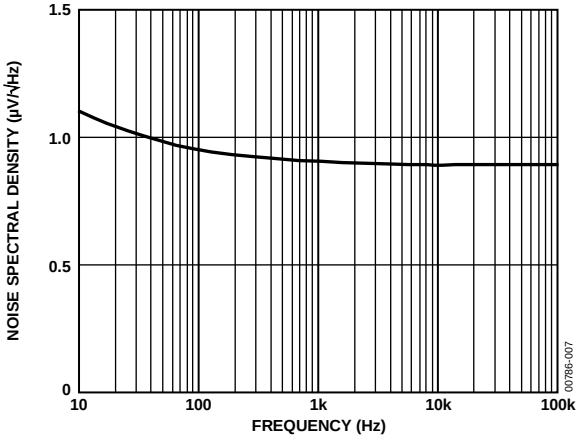


Figure 8. Noise Spectral Density vs. Frequency

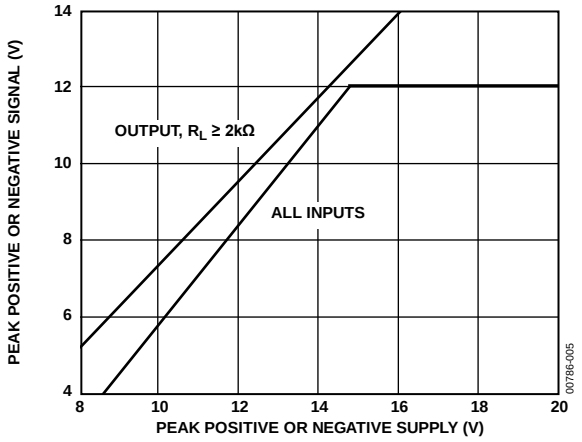


Figure 6. Input and Output Signal Ranges vs. Supply Voltages

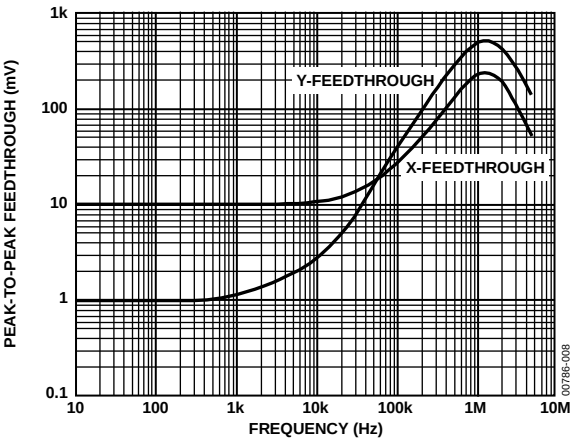


Figure 9. AC Feedthrough vs. Frequency

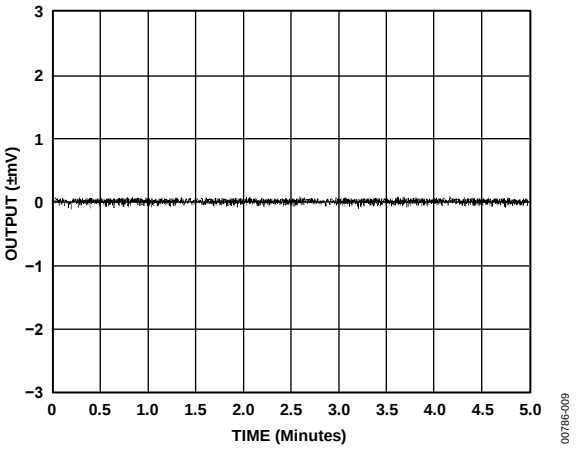


Figure 10. Typical V_{OS} vs. Time, For Five Minutes Following Power Up

FUNCTIONAL DESCRIPTION

The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity-gain connected output amplifier with an accessible summing node. Figure 1 shows the functional block diagram. The differential X and Y inputs are converted to differential currents by voltage-to-current converters. The product of these currents is generated by the multiplying core. A buried Zener reference provides an overall scale factor of 10 V. The sum of (X × Y)/10 + Z is then applied to the output amplifier. The amplifier summing Node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computational functions.

Inspection of the block diagram shows the overall transfer function is

$$W = \frac{(X1 - X2)(Y1 - Y2)}{10\ \text{V}} + Z \quad (1)$$

ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor error, and nonlinearity in the multiplying core. The input and output offsets can be eliminated by using the optional trim of Figure 11. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.4% and 0.1% of full scale, respectively. Scale factor error is typically 0.25% of full scale. The high impedance Z input should always reference the ground point of the driven system, particularly if it is remote. Likewise, the differential X and Y inputs should reference their respective grounds to realize the full accuracy of the AD633.

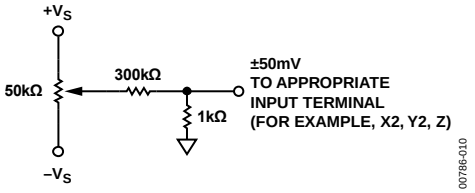


Figure 11. Optional Offset Trim Configuration

APPLICATIONS INFORMATION

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage-controlled amplifiers, and frequency doublers. These applications show the pin connections for the AD633JN (8-lead PDIP), which differs from the AD633JR (8-lead SOIC).

MULTIPLIER CONNECTIONS

Figure 12 shows the basic connections for multiplication. The X and Y inputs normally have their negative nodes grounded, but they are fully differential, and in many applications, the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity while achieving some desired output polarity), or both may be driven.

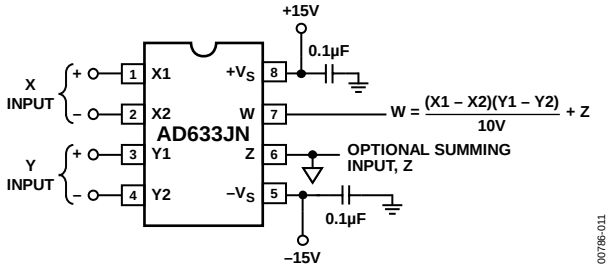


Figure 12. Basic Multiplier Connections (See the Model Results Section)

SQUARING AND FREQUENCY DOUBLING

As is shown in Figure 13, squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input can have either polarity, but the output is positive. However, the output polarity can be reversed by interchanging the X or Y inputs. The Z input can be used to add a further signal to the output.

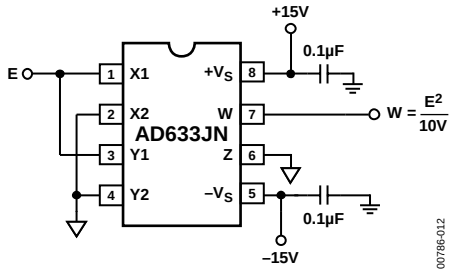


Figure 13. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, because

$$\frac{(E\sin\omega t)^2}{10\text{ V}} = \frac{E^2}{20\text{ V}}(1-\cos 2\omega t) \quad (2)$$

Equation 2 shows a dc term at the output that varies strongly with the amplitude of the input, E. This can be avoided using the connections shown in Figure 14, where an RC network is used to generate two signals whose product has no dc term. It uses the identity

$$\cos\theta\sin\theta = \frac{1}{2}(\sin 2\theta) \quad (3)$$

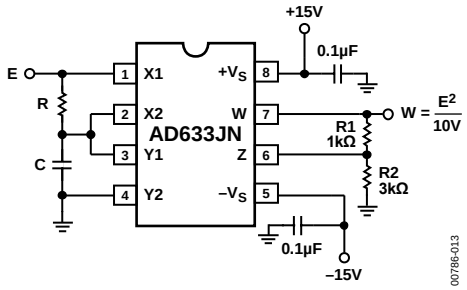


Figure 14. Bounceless Frequency Doubler (See the Model Results Section)

At $\omega_o = 1/CR$, the X input leads the input signal by 45° (and is attenuated by √2), and the Y input lags the X input by 45° (and is also attenuated by √2). Because the X and Y inputs are 90° out of phase, the response of the circuit is (satisfying Equation 3)

$$W = \frac{1}{(10\text{ V})}\frac{E}{\sqrt{2}}(\sin\omega_0 t + 45°)\frac{E}{\sqrt{2}}(\sin\omega_0 t + 45°)$$

$$= \frac{E^2}{(40\text{ V})}(\sin 2\,\omega_0 t) \quad (4)$$

which has no dc component. Resistor R1 and Resistor R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.

The amplitude of the output is only a weak function of frequency; the output amplitude is 0.5% too low at $\omega = 0.9\,\omega_0$ and $\omega_0 = 1.1\,\omega_0$.

GENERATING INVERSE FUNCTIONS

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 15 shows how to implement square rooting with the transfer function for the condition E < 0.

The 1N4148 diode is required to prevent latchup, which can occur in such applications if the input were to change polarity, even momentarily.

$$W = \sqrt{-(10E)\text{V}} \quad (5)$$

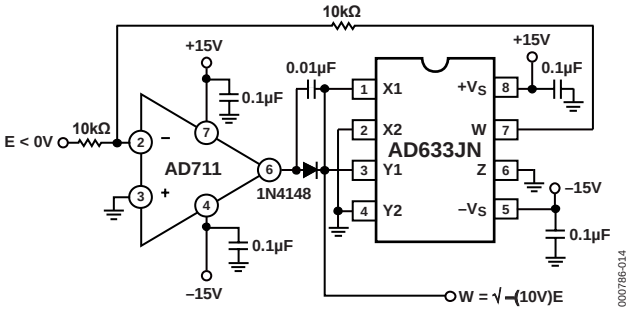


Figure 15. Connections for Square Rooting

Likewise, Figure 16 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W = -(10\text{ V})\frac{E}{E_X} \quad (6)$$

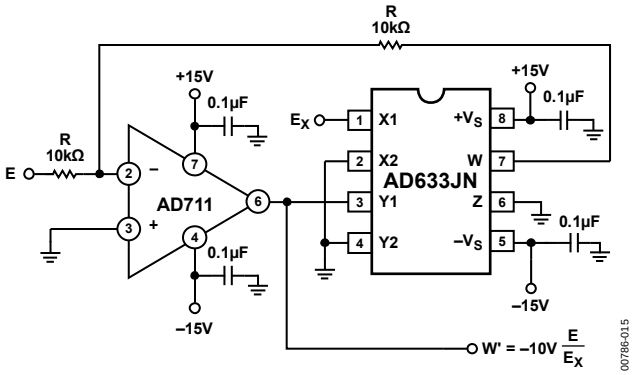


Figure 16. Connections for Division

VARIABLE SCALE FACTOR

In some instances, it may be desirable to use a scaling voltage other than 10 V. The connections shown in Figure 17 increase the gain of the system by the ratio (R1 + R2)/R1. This ratio is limited to 100 in practical applications. The summing input, S, can be used to add an additional signal to the output, or it can be grounded.

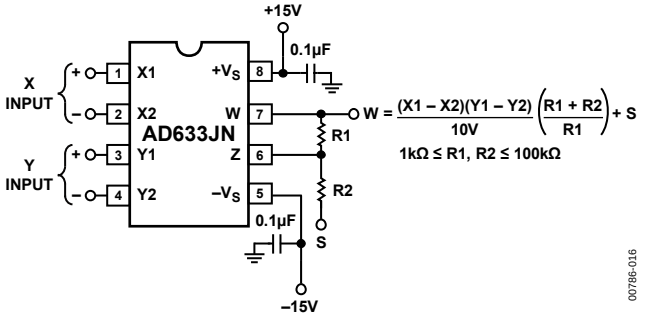


Figure 17. Connections for Variable Scale Factor

CURRENT OUTPUT

The voltage output of the AD633 can be converted to a current output by the addition of a resistor, R, between the W and Z pins of the AD633 as shown in Figure 18.

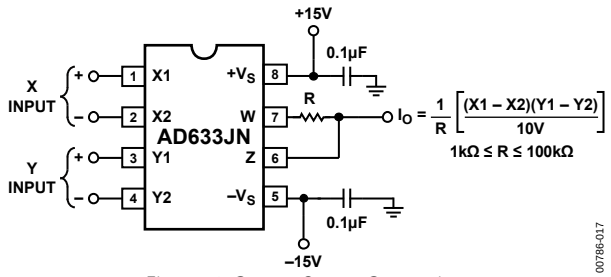


Figure 18. Current Output Connections

This arrangement forms the basis of voltage-controlled integrators and oscillators as is shown later in this section. The transfer function of this circuit has the form

$$I_O = \frac{1}{R}\frac{(X1-X2)(Y1-Y2)}{10\text{ V}} \quad (7)$$

LINEAR AMPLITUDE MODULATOR

The AD633 can be used as a linear amplitude modulator with no external components. Figure 19 shows the circuit. The carrier and modulation inputs to the AD633 are multiplied to produce a double sideband signal. The carrier signal is fed forward to the Z input of the AD633 where it is summed with the double sideband signal to produce a double sideband with the carrier output.

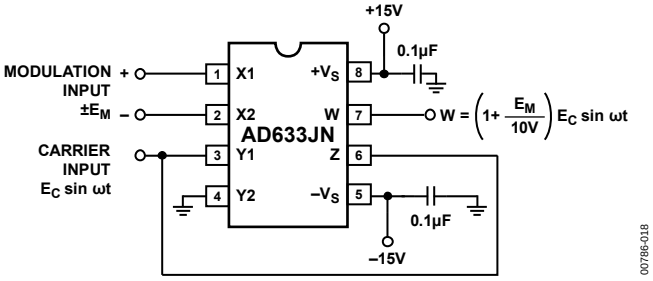


Figure 19. Linear Amplitude Modulator

VOLTAGE-CONTROLLED, LOW-PASS AND HIGH-PASS FILTERS

Figure 20 shows a single multiplier used to build a voltage-controlled, low-pass filter. The voltage at Output A is a result of filtering E_S. The break frequency is modulated by E_C, the control input. The break frequency, f_2, equals

$$f_2 = \frac{E_C}{10(2\pi RC)} \quad (8)$$

and the roll-off is 6 dB per octave. This output, which is at a high impedance point, may need to be buffered.

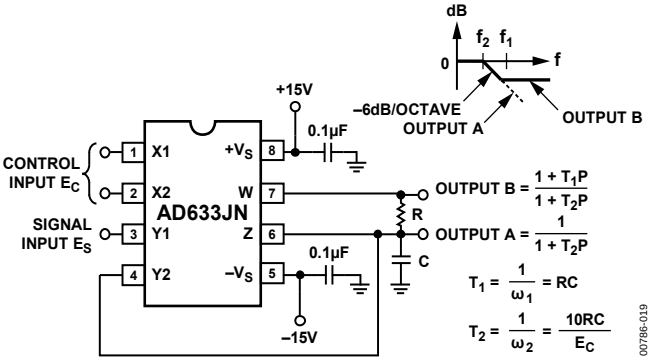


Figure 20. Voltage-Controlled, Low-Pass Filter

The voltage at Output B, the direct output of the AD633, has the same response up to frequency f_1, the natural breakpoint of RC filter, and then levels off to a constant attenuation of $f_1/f_2 = 10/E_C$

$$f_1 = \frac{1}{2\pi RC} \quad (9)$$

For example, if R = 8 kΩ and C = 0.002 µF, then Output A has a pole at frequencies from 100 Hz to 10 kHz for E_C ranging from 100 mV to 10 V. Output B has an additional 0 at 10 kHz (and can be loaded because it is the low impedance output of the multiplier). The circuit can be changed to a high-pass filter Z interchanging the resistor and capacitor as shown in Figure 21.

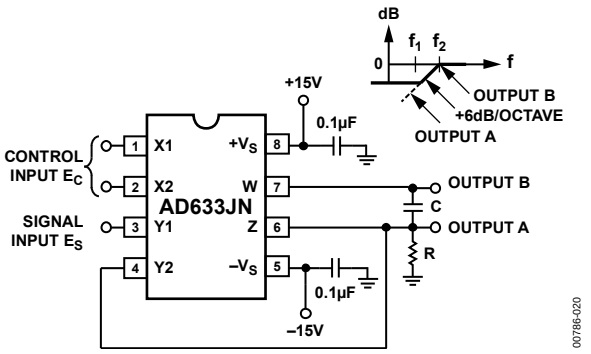


Figure 21. Voltage-Controlled, High-Pass Filter

VOLTAGE-CONTROLLED QUADRATURE OSCILLATOR

Figure 22 shows two multipliers being used to form integrators with controllable time constants in second-order differential equation feedback loop. R2 and R5 provide controlled current output operation. The currents are integrated in capacitors C1 and C2, and the resulting voltages at high impedance are applied to the X inputs of the next AD633. The frequency control input, E_C, connected to the Y inputs, varies the integrator gains with a calibration of 100 Hz/V. The accuracy is limited by the Y input offsets. The practical tuning range of this circuit is 100:1. C2 (proportional to C1 and C3), R3, and R4 provide regenerative feedback to start and maintain oscillation. The diode bridge, D1 through D4 (1N914s), and Zener diode D5 provide economical temperature stabilization and amplitude stabilization at ±8.5 V by degenerative damping. The output from the second integrator (10 V sin ωt) has the lowest distortion.

AUTOMATIC GAIN CONTROL (AGC) AMPLIFIERS

Figure 23 shows an AGC circuit that uses an rms-to-dc converter to measure the amplitude of the output waveform. The AD633 and A1, half of an AD712 dual op amp, form a voltage-controlled amplifier. The rms-to-dc converter, an AD736, measures the rms value of the output signal. Its output drives A2, an integrator/comparator whose output controls the gain of the voltage-controlled amplifier. The 1N4148 diode prevents the output of A2 from going negative. R8, a 50 kΩ variable resistor, sets the output level of the circuit. Feedback around the loop forces the voltages at the inverting and noninverting inputs of A2 to be equal, thus the AGC.

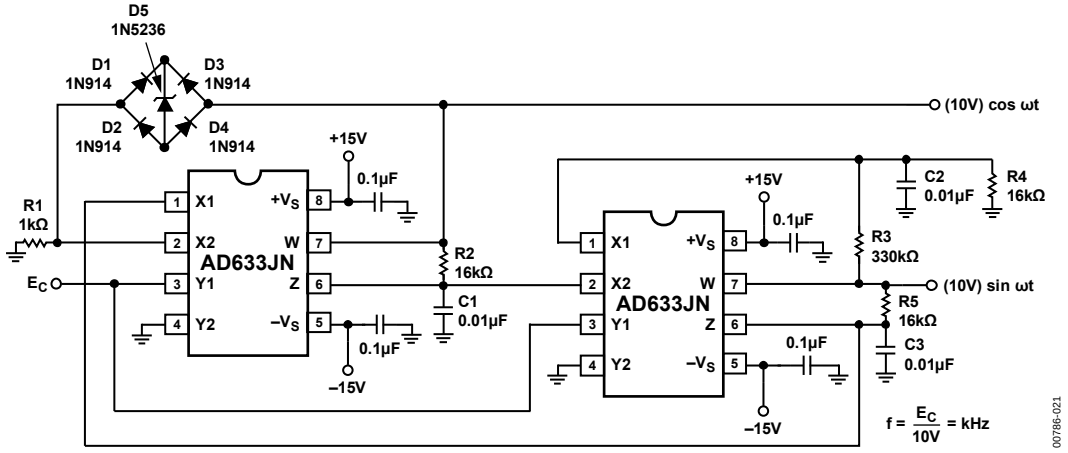


Figure 22. Voltage-Controlled Quadrature Oscillator

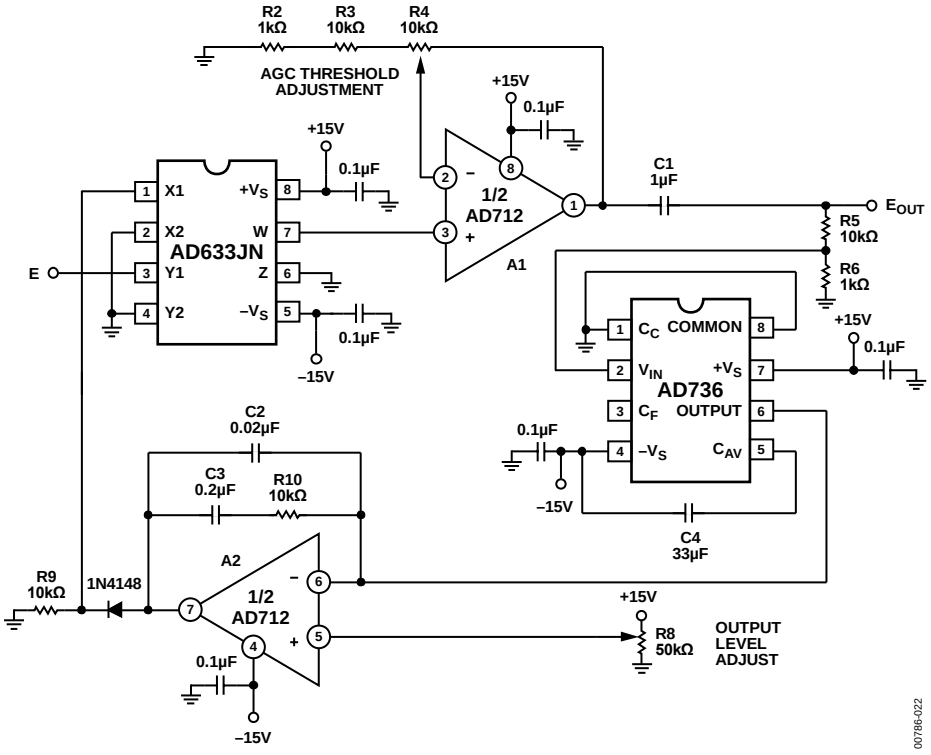


Figure 23. Connections for Use in Automatic Gain Control Circuit

MODEL RESULTS

Circuit simulation using SPICE models embedded in various application formats such as PSPICE, Multisim, and SIMetrix is a popular and efficient method of assessing the integrity of a circuit before creating the printed circuit board in which the circuits are ultimately used. Although impossible to demonstrate all of the multiplier functions in every available program, Figure 24 through Figure 41 demonstrate how the schematic and graph for simple dc, sin(x), and pulse applications appear in three popular SPICE programs. If a simulator is not shown here, a good way to progress is to start with a basic dc circuit to verify that the circuit converges and then continue with waveforms that are more complex. When analyzing nonlinear devices such as multipliers, the most common simulation issue is convergence, the iterative process by which SPICE seeks the initial dc bias condition before completely solving the circuit and displaying a graph.

Figure 24 through Figure 41 are arranged schematic first, followed by the graphic result. If the user has a problem with a simulator, the most efficient fix is to contact applications support for the program in use.

EXAMPLES OF DC, SIN, AND PULSE SOLUTIONS USING MULTISIM

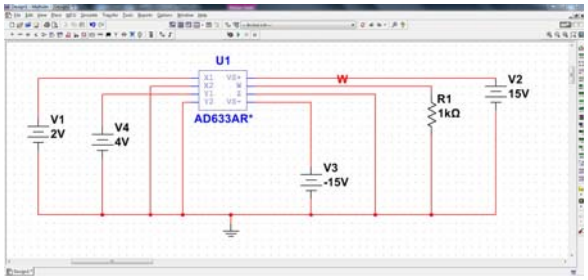


Figure 24. Circuit to Multiply Two Integers Schematic Created in Multisim

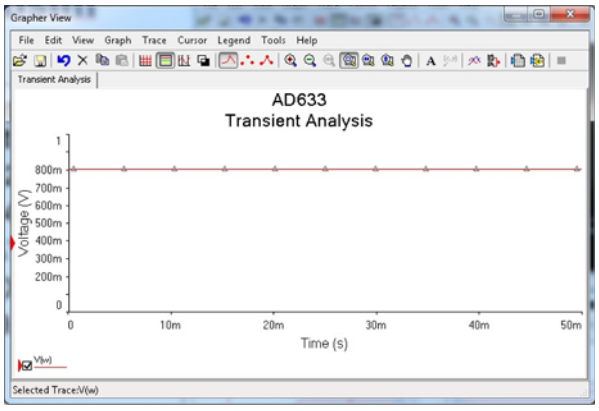


Figure 25. Circuit to Multiply Two Integers Response Graph Displayed in Multisim (2 V × 4 V)/10 V = 0.8 V

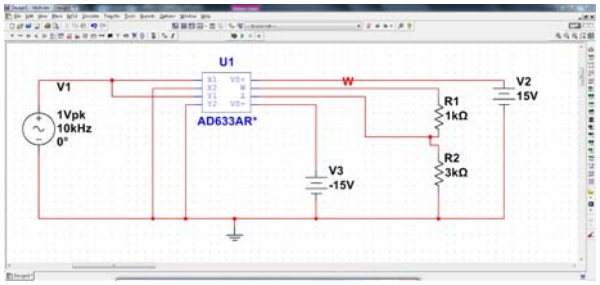


Figure 26. Frequency Doubler Circuit Schematic Created in Multisim

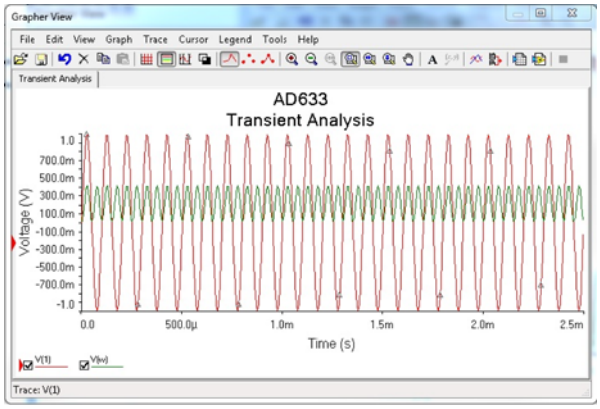


Figure 27. Frequency Doubler Response Graph Displayed in Multisim

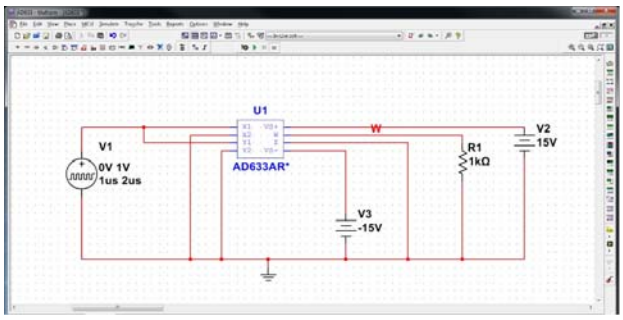


Figure 28. Pulse Circuit Schematic Created in Multisim

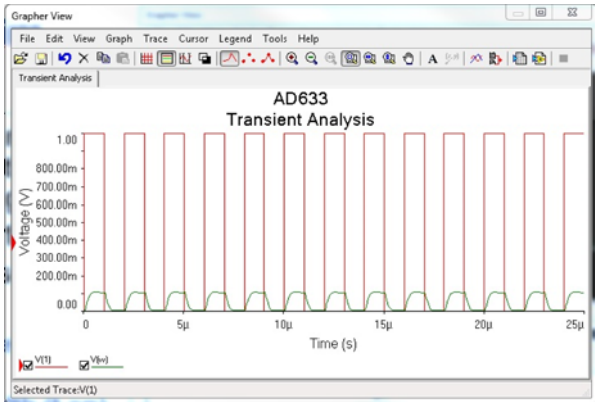


Figure 29. Pulse Circuit Response Graph Displayed in Multisim

EXAMPLES OF DC, SIN, AND PULSE SOLUTIONS USING PSPICE

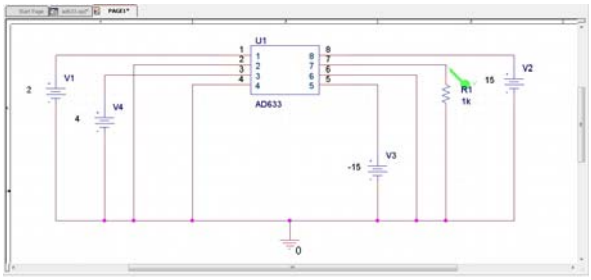


Figure 30. Simple Circuit Schematic Created in PSPICE

Figure 31. Simple Circuit Response Graph Displayed in PSPICE
(2 V × 4 V)/10 V = 0.8 V

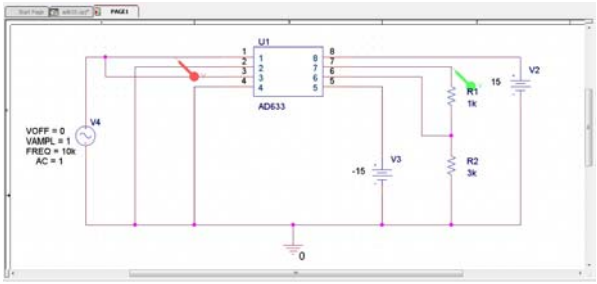


Figure 32. Frequency Doubler Circuit Schematic Created in PSPICE

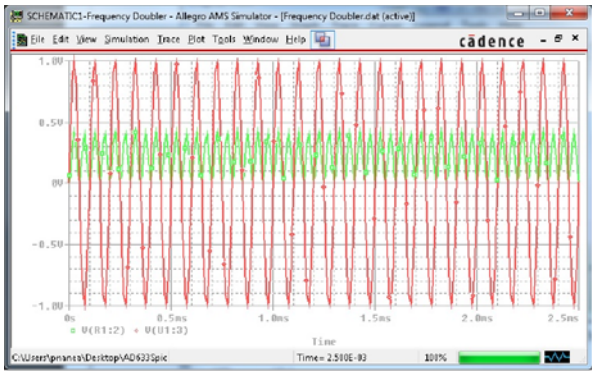


Figure 33. Frequency Doubler Response Graph Displayed in PSPICE

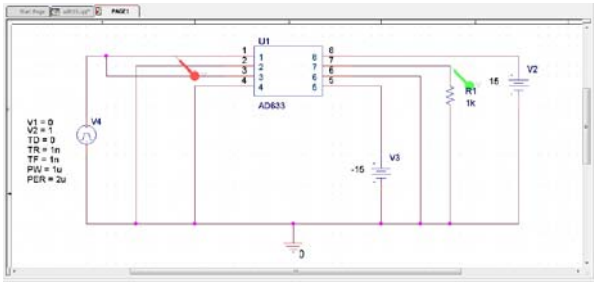


Figure 34. Pulse Circuit Schematic Created in PSPICE

Figure 35. Pulse Circuit Response Graph Displayed in PSPICE

EXAMPLES OF DC, SIN, AND PULSE SOLUTIONS USING SIMETRIX

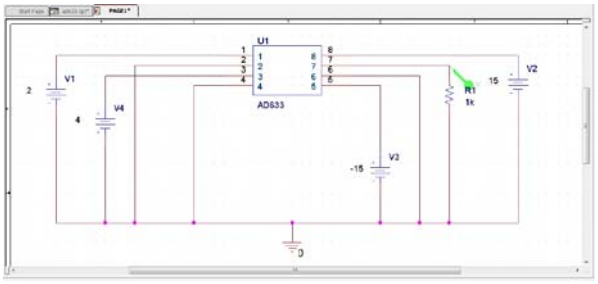


Figure 36. Simple Circuit Schematic Created in SIMetrix

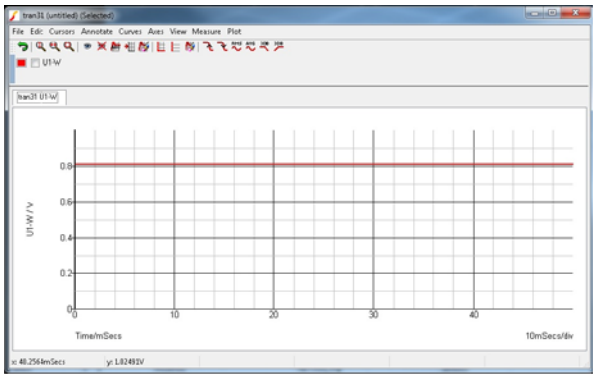


Figure 37.Simple Circuit Response Graph Displayed in SIMetrix
(2 V × 4 V)/10 V = 0.8 V

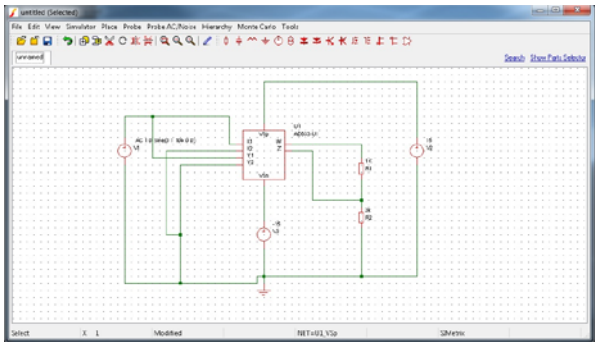


Figure 38. Frequency Doubler Circuit Schematic Created in SIMetrix

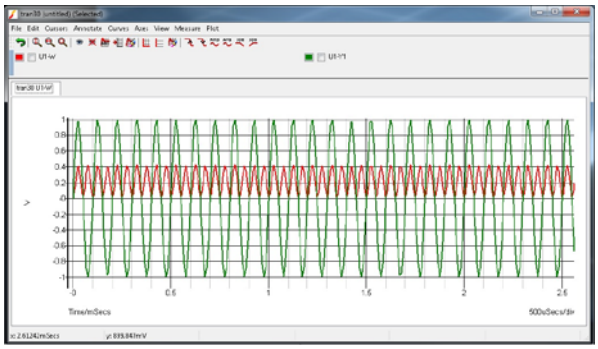


Figure 39. Frequency Doubler Response Graph Displayed in SIMetrix

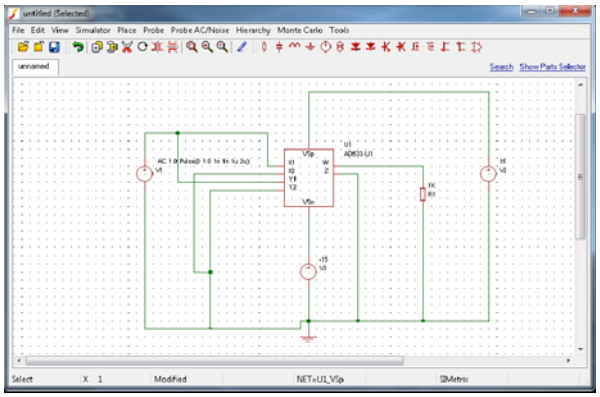


Figure 40. Pulse Circuit Schematic Created in SIMetrix

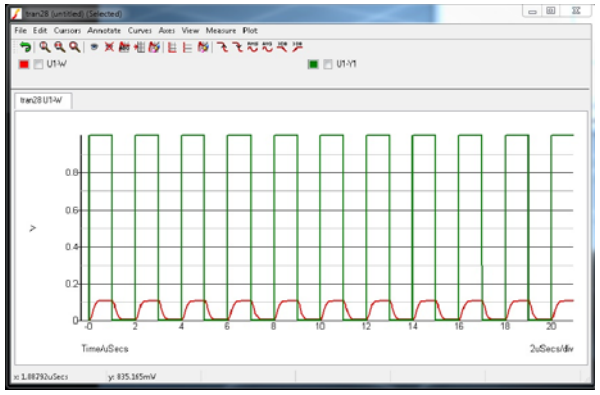


Figure 41. Pulse Circuit Response Displayed in SIMetrix

EVALUATION BOARD

The evaluation board of the AD633 enables simple bench-top experimenting to be performed with easy control of the AD633. Built-in flexibility allows convenient configuration to accommodate most operating configurations. Figure 42 is a photograph of the AD633 evaluation board.

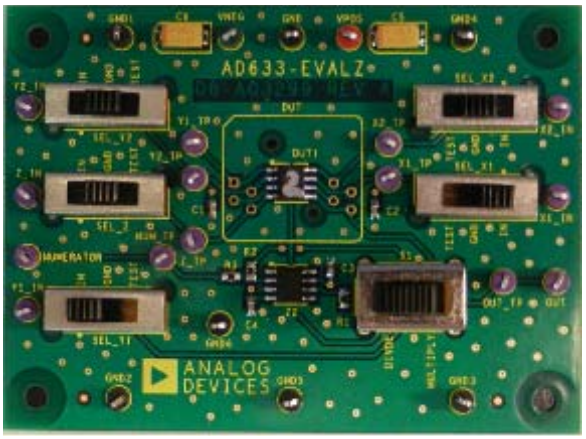


Figure 42. AD633 Evaluation Board

Any dual-polarity power supply capable of providing 10 mA or greater is all that is required to perform the intended tests, in addition to whatever test equipment the user wants.

Referring to the schematic in Figure 49, inputs to the multiplier are differential and dc-coupled. Three-position slide switches enhance flexibility by enabling the multiplier inputs to be connected to an active signal source, to ground, or to a test loop connected directly to the device pin for direct measurements, such as bias current. Inputs may be connected single ended or differentially, but must have a dc path to ground for bias current. If the impedance of an input source is non-zero, an equal value impedance must be connected to the opposite polarity input to avoid introducing additional offset voltage.

The AD633-EVALZ can be configured for multiplier or divider operation by switch S1. Refer to Figure 16 for divider circuit connections.

Figure 43 through Figure 46 are the signal, power, and ground-plane artworks, and Figure 47 shows the component and circuit side silkscreen. Figure 48 shows the assembly.

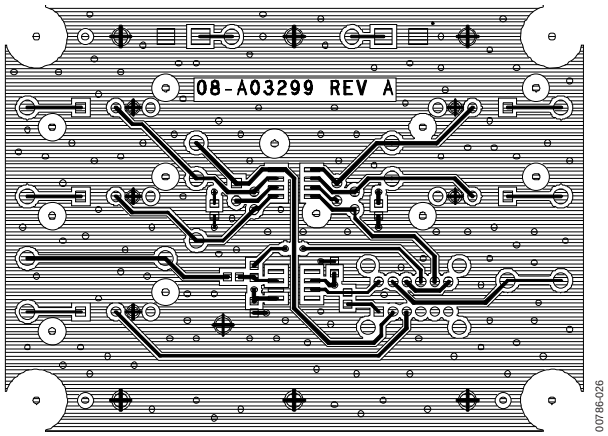


Figure 43. Component Side Copper

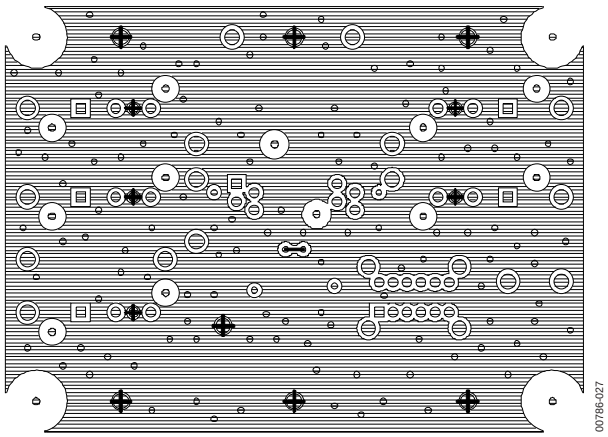


Figure 44. Circuit Side Copper

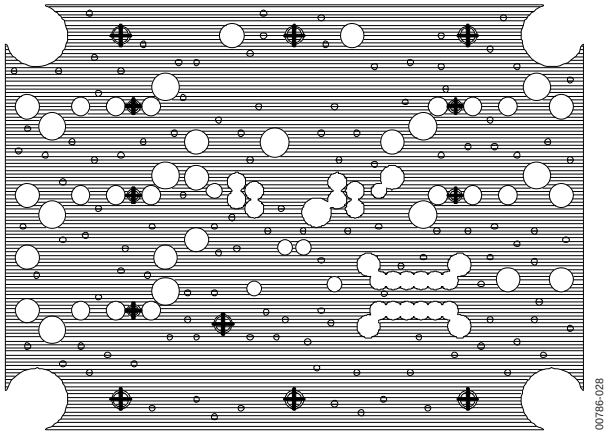


Figure 45. Inner Layer Ground Plane

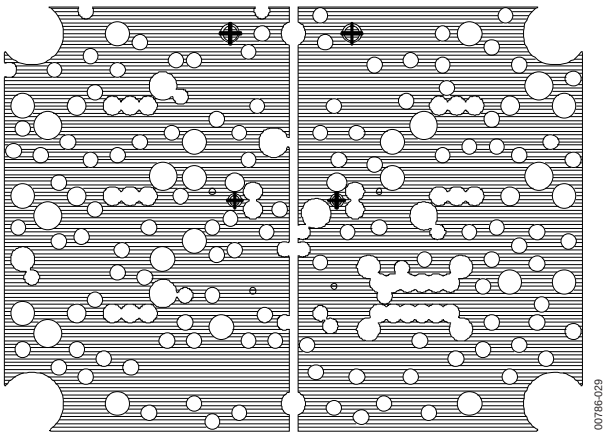


Figure 46. Inner Layer Power Plane

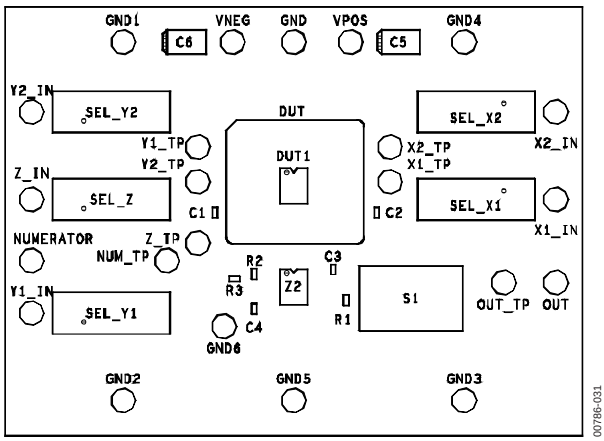


Figure 48. AD633-EVALZ Assembly

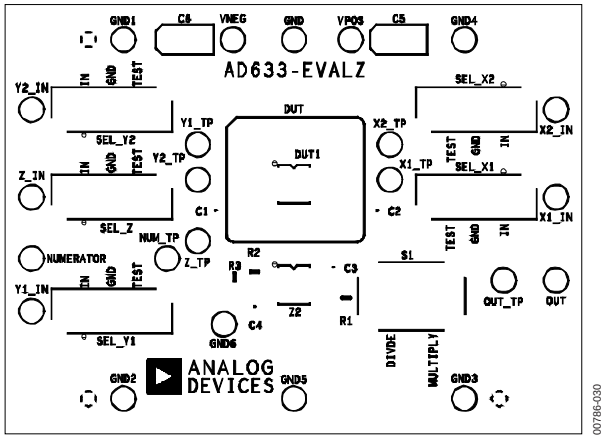


Figure 47. Component Side Silk Screen

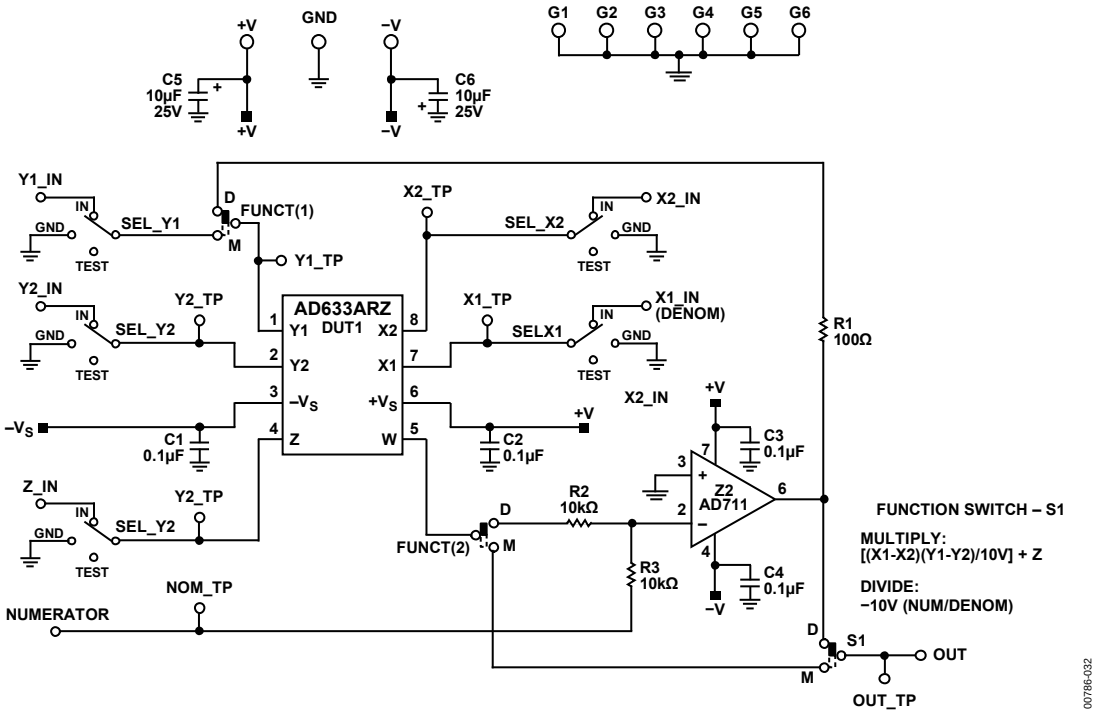


Figure 49. Schematic of the AD633 Evaluation Board

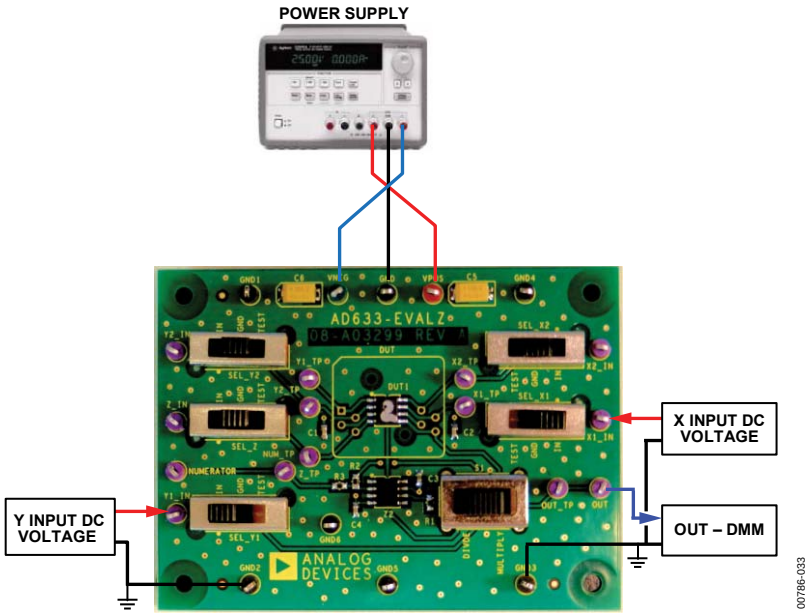
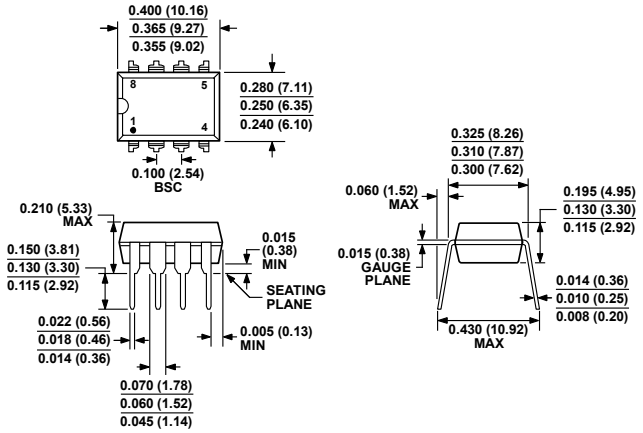


Figure 50. AD633-EVALZ Configured for Bench Experiments

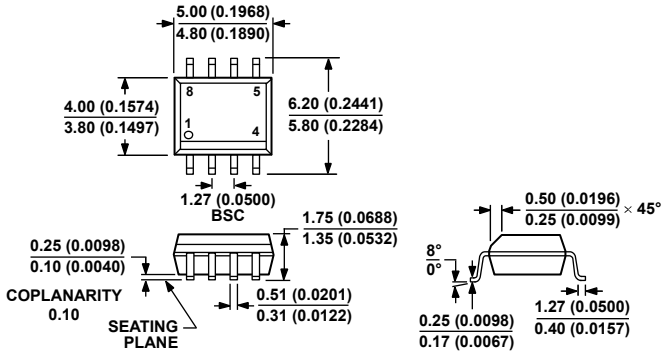
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 51. 8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)