385 MHz BW IF Diversity Receiver

Data Sheet **AD6674**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- In band SFDR = 83 dBFS at 340 MHz (750 MSPS)
- In band SNR = 66.7 dBFS at 340 MHz (750 MSPS)
- 1.4 W total power per channel at 750 MSPS (default settings)
- Noise density = −153 dBFS/Hz at 750 MSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- Flexible input range
  - AD6674-750 and AD6674-1000
    - 1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
  - AD6674-500
    - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient automatic gain control (AGC) implementation
- Noise shaping requantizer (NSR) option for main receiver function
- Variable dynamic range (VDR) option for digital predistortion (DPD) function
- 2 integrated wideband digital processors per channel
  - 12-bit numerically controlled oscillator (NCO), up to
    - 4 cascaded half-band filters
- Differential clock inputs
- Integer clock divide by 1, 2, 4, or 8
- Energy saving power-down modes
- Flexible JESD204B lane configurations
- Small signal dither

APPLICATIONS

- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE, LTE-A
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

GENERAL DESCRIPTION

The AD6674 is a 385 MHz bandwidth mixed-signal intermediate frequency (IF) receiver. It consists of two, 14-bit 1.0 GSPS/750 MSPS/500 MSPS analog-to-digital converters (ADC) and various digital signal processing blocks consisting of four wideband DDCs, an NSR, and VDR monitoring. It has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of sampling wide bandwidth analog signals of up to 2 GHz. The AD6674 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

FUNCTIONAL BLOCK DIAGRAM

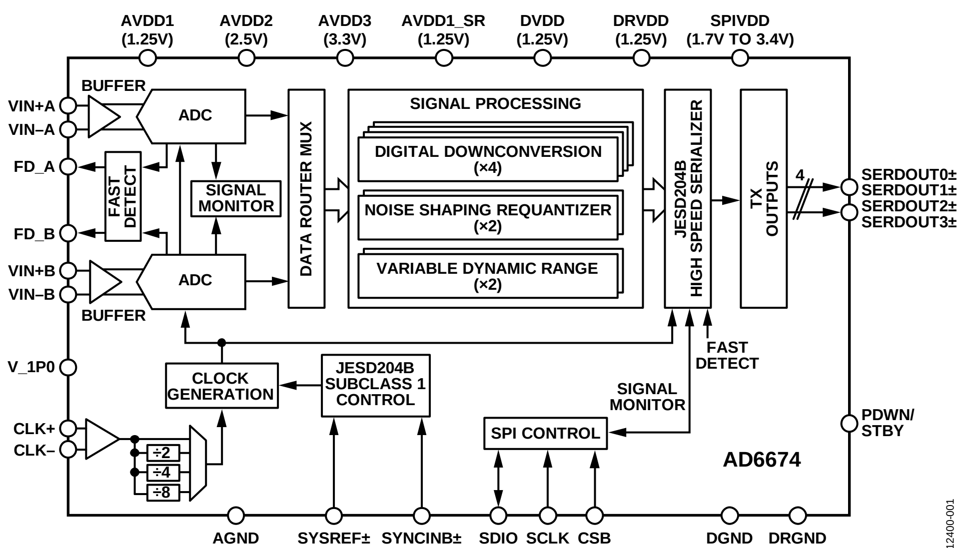

Figure 1.

Rev. D Document Feedback

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REVISION HISTORY

The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO), and up to four half-band decimation filters.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the SPI. With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6674 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining a 9-bit output resolution. NSR is enabled by default on the AD6674.

Each ADC output is also connected internally to a VDR block. This optional mode allows full dynamic range for defined input signals. Inputs that are within a defined mask (based on DPD applications) are passed unaltered. Inputs that violate this defined mask result in the reduction of the output resolution.

With VDR, the dynamic range of the observation receiver is determined by a defined input frequency mask. For signals falling within the mask, the outputs are presented at the maximum resolution allowed. For signals exceeding defined power levels within this frequency mask, the output resolution is truncated. This mask is based on DPD applications and supports tunable real IF sampling, and zero IF or complex IF receive architectures.

Operation of the AD6674 between the DDC, NSR, and VDR modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD6674 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. Besides the fast detect outputs, the AD6674 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

Users can configure the Subclasss 1 JESD204B-based high speed serialized output in a variety of two-lane and four-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD6674 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V capable 3-wire serial port interface (SPI).

The AD6674 is available in a Pb-free, 64-lead LFCSP, specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination eases filter design and implementation.
3. Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. Programmable fast overrange detection.
7. 9 mm × 9 mm 64-lead LFCSP.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

		AD6674-1000			AD6674-750			AD6674-500			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		14						14			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full	−0.31	0	+0.31	−0.51	0	+0.42	−0.3	0	+0.3	% FSR
Offset Matching	Full		0	+0.23		0	+0.41		0	+0.3	% FSR
Gain Error	Full	−6	0	+6	−6	0	+6	−6	0	+6	% FSR
Gain Matching	Full		1	+4.5		1	+5.2		1	+5.1	% FSR
Differential Nonlinearity (DNL)	Full	−0.7	±0.5	+0.8	−0.6	±0.5	+0.8	−0.6	±0.5	+0.7	LSB
Integral Nonlinearity (INL)	Full	−5.7	±2.5	+6.9	−3.4	±2.5	+5.0	−4.5	±2.5	+5.0	LSB
TEMPERATURE DRIFT											
Offset Error	Full		−14			−9			−3		ppm/°C
Gain Error	Full		±13.8			−57			±25		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Voltage	Full		1.0			1.0			1.0		V
INPUT REFERRED NOISE											
V_{REF} = 1.0 V	25°C		2.63			2.48			2.06		LSB rms
ANALOG INPUTS											
Differential Input Voltage Range (Internal V_{REF} = 1.0 V)	Full	1.46	1.70	1.94	1.46	1.70	1.94	1.46	2.06	2.06	V p-p
Common-Mode Voltage (V_{CM})	Full		2.05			2.05			2.05		V
Differential Input Capacitance[1]	Full		1.5			1.5			1.5		pF
Analog Full Power Bandwidth	Full		2			2			2		GHz
POWER SUPPLY											
AVDD1	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	2.44	2.50	2.56	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	3.2	3.3	3.4	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	1.7	1.8	3.4	1.7	1.8	3.4	V
I_{AVDD1}[2]	Full		685	721		545	623		427	466	mA
I_{AVDD2}[2]	Full		595	677		460	572		398	463	mA
I_{AVDD3}[2]	Full		125	142		125	142		89	100	mA
I_{AVDD1_SR}[2]	Full		16	18		10	17		10	18	mA
I_{DVDD}[2]	Full		263	292		165	217		139	183	mA
I_{DRVDD}[2, 3]	Full		200	225		190	258		182	237	mA
L = 2 Mode[4]	25°C		N/A[5]			N/A[5]			140		mA
I_{SPIVDD}	Full		5	6		5	7.0		5	7	mA

Parameter	Temp	AD6674-1000			AD6674-750			AD6674-500			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER CONSUMPTION											
Total Power Dissipation[2]	Full		3.3	3.6		2.8	3.1		2.24	2.5	W
Power-Down Dissipation	Full		835			835			710		mW
Standby[6]	Full		1.4			1.4			1.2		W

[1] Differential capacitance is measured between the VIN+x and VIN−x pins (x = A, B).
[2] Measured with a low input frequency, full-scale sine wave.
[3] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[4] L is the number of lanes per converter device (lanes per link).
[5] N/A means not applicable. At the maximum sample rate, it is not applicable to use L = 2 mode on the JESD204B output interface because this exceeds the maximum lane rate of 12.5 Gbps. L = 2 mode is supported when the equation ((M × N′ × (10/8) × f_{OUT})/L) results in a lane rate that is ≤12.5 Gbps. f_{OUT} is the output sample rate and is denoted by f_S/DCM, where DCM = decimation ratio.
[6] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD6674-1000			AD6674-750			AD6674-500			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ANALOG INPUT FULL SCALE	Full		1.7			1.7			2.06		V p-p
NOISE DENSITY[2]	Full		−154			−153			−153		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		67.2			67.3			69.2		dBFS
f_{IN} = 170 MHz	Full	65.1	66.6		65.8	67.1		67.8	69.0		dBFS
f_{IN} = 340 MHz	25°C		65.3			66.7			68.6		dBFS
f_{IN} = 450 MHz	25°C		64.0			66.2			68.0		dBFS
f_{IN} = 765 MHz	25°C		62.4			64.3			64.4		dBFS
f_{IN} = 985 MHz	25°C		61.4			63.6			63.8		dBFS
f_{IN} = 1950 MHz	25°C		57.0			59.9			60.5		dBFS
NSR Enabled (21% BW Mode)[4]											
f_{IN} = 10 MHz	25°C		73.8			74.0			75.2		dBFS
f_{IN} = 170 MHz	25°C		73.6			73.8			75.2		dBFS
f_{IN} = 340 MHz	25°C		73.5			73.7			74.8		dBFS
f_{IN} = 450 MHz	25°C		71.9			72.2			74.2		dBFS
f_{IN} = 765 MHz	25°C		69.0			71.4			70.3		dBFS
f_{IN} = 985 MHz	25°C		68.2			71.0			69.3		dBFS
f_{IN} = 1950 MHz	25°C		63.6			66.6			65.3		dBFS
NSR Enabled (28% BW Mode)[4]											
f_{IN} = 10 MHz	25°C		72.4			72.8			72.4		dBFS
f_{IN} = 170 MHz	25°C		72.2			72.6			72.4		dBFS
f_{IN} = 340 MHz	25°C		72.1			72.5			72.1		dBFS
f_{IN} = 450 MHz	25°C		70.5			71.0			71.9		dBFS
f_{IN} = 765 MHz	25°C		67.0			70.0			68.3		dBFS
f_{IN} = 985 MHz	25°C		66.3			68.9			67.7		dBFS
f_{IN} = 1950 MHz	25°C		61.9			65.1			64.1		dBFS

		AD6674-1000			AD6674-750			AD6674-500			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		67.1			67.1			69.0		dBFS
f_{IN} = 170 MHz	Full	65.0	66.4		65.6	67.0		67.6	68.8		dBFS
f_{IN} = 340 MHz	25°C		65.2			66.5			68.4		dBFS
f_{IN} = 450 MHz	25°C		63.8			66.1			67.9		dBFS
f_{IN} = 765 MHz	25°C		62.1			64.1			64.2		dBFS
f_{IN} = 985 MHz	25°C		61.1			63.1			63.6		dBFS
f_{IN} = 1950 MHz	25°C		56.0			59.0			60.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		10.8			10.8			11.2		Bits
f_{IN} = 170 MHz	Full	10.5	10.7		10.4	10.8		10.8	11.1		Bits
f_{IN} = 340 MHz	25°C		10.5			10.7			11.1		Bits
f_{IN} = 450 MHz	25°C		10.3			10.5			11.0		Bits
f_{IN} = 765 MHz	25°C		10.0			10.4			10.4		Bits
f_{IN} = 985 MHz	25°C		9.8			10.2			10.3		Bits
f_{IN} = 1950 MHz	25°C		9.0			9.5			9.7		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		88			85			83		dBFS
f_{IN} = 170 MHz	Full	75	85		75	86		80	88		dBFS
f_{IN} = 340 MHz	25°C		85			83			83		dBFS
f_{IN} = 450 MHz	25°C		82			82			81		dBFS
f_{IN} = 765 MHz	25°C		82			80			80		dBFS
f_{IN} = 985 MHz	25°C		80			76			75		dBFS
f_{IN} = 1950 MHz	25°C		68			68			70		dBFS
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)[3]											
VDR Mode (Input Mask Not Triggered)											
f_{IN} = 10 MHz	25°C		−95			−95			−95		dBFS
f_{IN} = 170 MHz	Full	−81	−94		−81	−89		−82	−95		dBFS
f_{IN} = 340 MHz	25°C		−88			−83			−93		dBFS
f_{IN} = 450 MHz	25°C		−86			−82			−93		dBFS
f_{IN} = 765 MHz	25°C		−81			−85			−88		dBFS
f_{IN} = 985 MHz	25°C		−82			−83			−89		dBFS
f_{IN} = 1950 MHz	25°C		−75			−80			−84		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD)[3] A_{IN1} AND A_{IN2} = −7.0 dBFS											
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−87			−85			−88		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−88			−83			−88		dBFS
CROSSTALK[5]	25°C		95			95			95		dB
FULL POWER BANDWIDTH	25°C		2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at low analog input frequency (30 MHz).
[3] See Table 10 for recommended device settings to achieve stated typical performance.
[4] When NSR is activated on the AD6674-750 and AD6674-1000, the decimating half-band filter is also enabled.
[5] Crosstalk is measured at 185 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0			V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 μA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 μA)	Full	0			V
SYNC INPUTS (SYNCINB+, SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0			V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss is measured from 100 MHz to 0.75 × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

		AD6674-1000			AD6674-750			AD6674-500			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK											
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	0.3		4	0.3		4	GHz
Maximum Sample Rate[1]	Full	1000			750			500			MSPS
Minimum Sample Rate[2]	Full	300			300			300			MSPS
Clock Pulse Width High	Full	500			666.67			1000			ps
Clock Pulse Width Low	Full	500			666.67			1000			ps
OUTPUT PARAMETERS											
Unit Interval (UI)[3]	Full		100			133.33			200		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C		32			32			32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C		32			32			32		ps
PLL Lock Time	25°C		2			2			2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	10	12.5	3.125	7.5	12.5	3.125	5	12.5	Gbps
LATENCY											
Pipeline Latency	Full		75			75			75		Clock cycles
Fast Detect Latency	Full			28			28			28	Clock cycles
Wake-Up Time (Standby)[5]	25°C		1			1			1		ms
Wake-Up Time (Power-Down)[5]	25°C			4			4			4	ms
APERTURE											
Aperture Delay (t_A)	Full		530			530			530		ps
Aperture Uncertainty (Jitter, t_J)	Full		55			55			55		fs rms
Out-of-Range Recovery Time	Full		1			1			1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] At full baud rate (12.5 Gbps), each ADC outputs data on two differential pair lanes.
[5] Wake-up time is defined as the time required to return to normal operation from power-down mode or standby mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK± to SYSREF± TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYSREF± setup time		117		ps
t_{H_SR}	Device clock to SYSREF± hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK is in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK is in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between the falling edge of SCLK and the output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

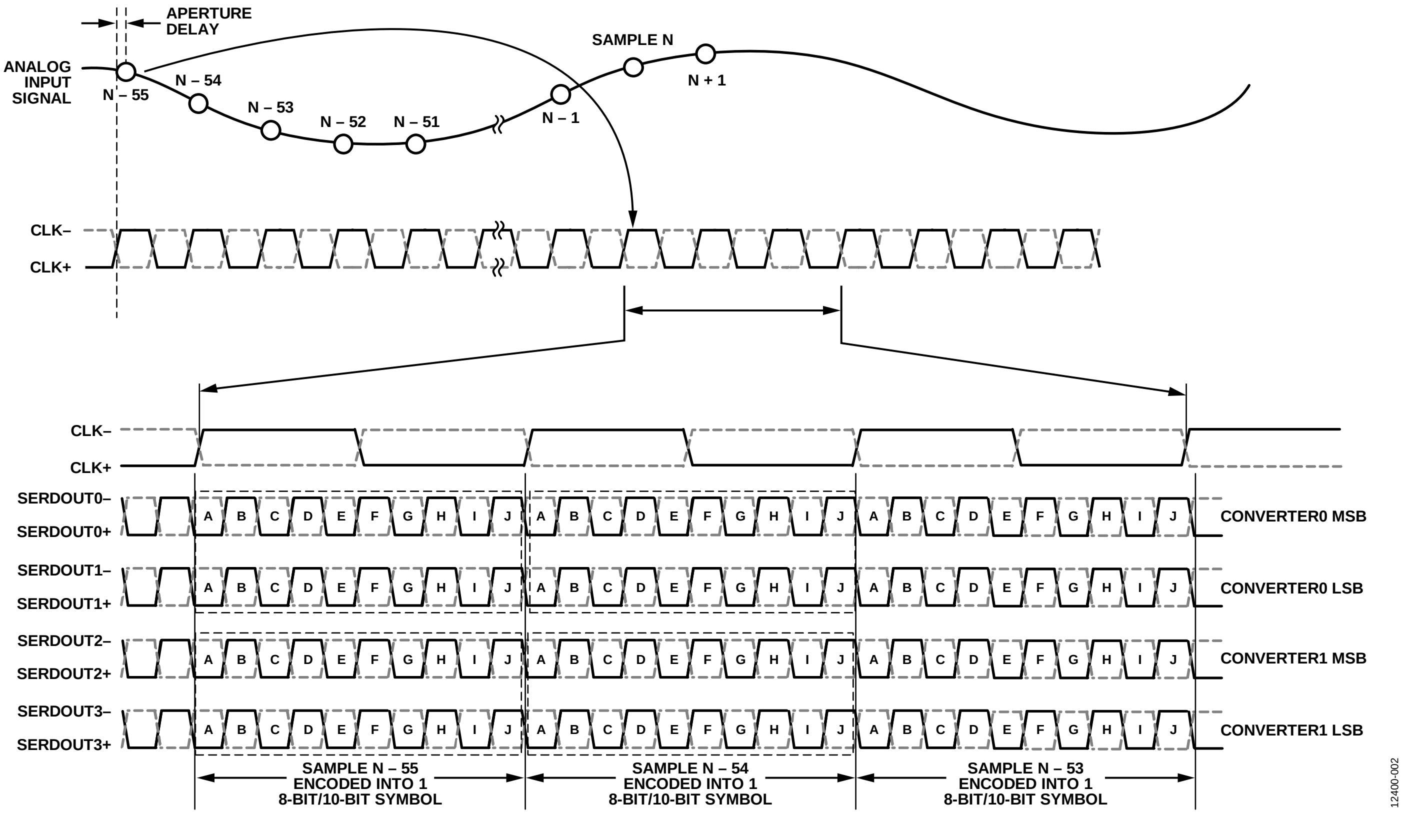


Figure 2. Data Output Timing (VDR Mode; L = 4; M = 2; F = 1)

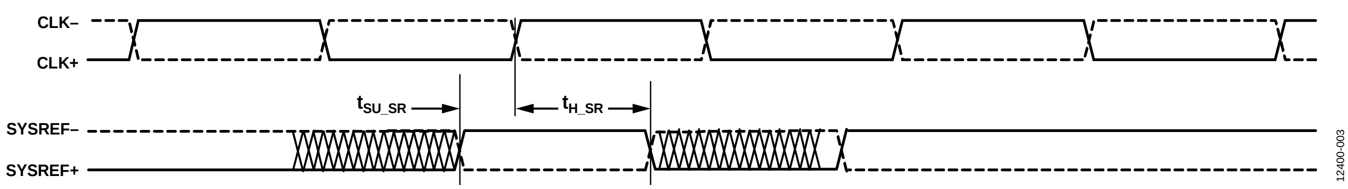


Figure 3. SYSREF± Setup and Hold Timing

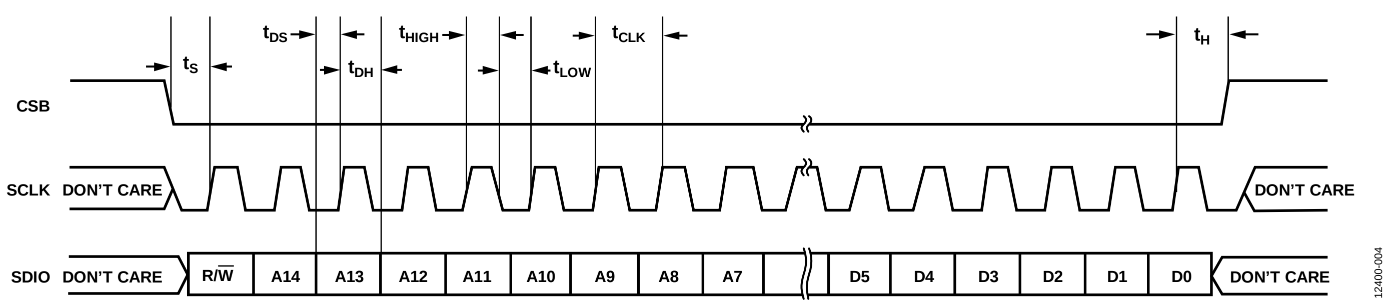


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−40°C to +115°C
Storage Temperature Range (Ambient)	−60°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

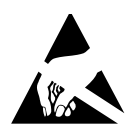
Typical θ_{JA}, Ψ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation, effectively reducing θ_{JA} and Ψ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance Values

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1, 2]	6.3[1, 3]	4.7[1, 5]	1.2[1, 5]	°C/W
	1.0	15.6[1, 2]	5.9[1, 3]	N/A[4]		°C/W
	2.5	15.0[1, 2]	5.7[1, 3]	N/A[4]		°C/W

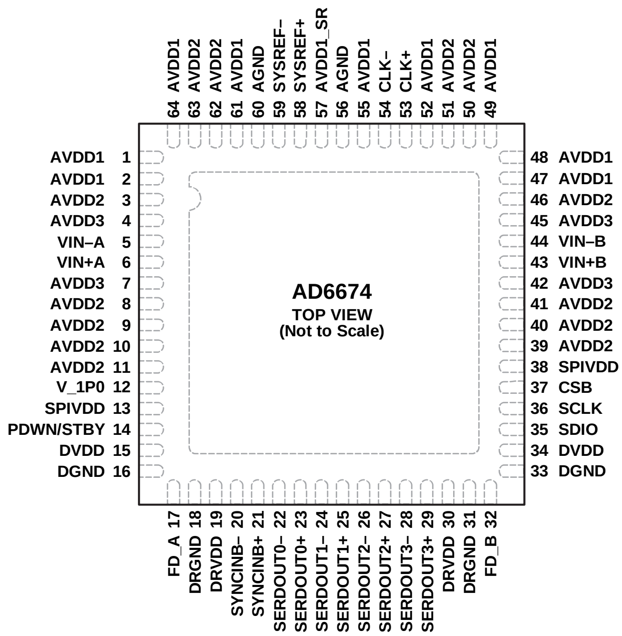
[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] N/A means not applicable.
[5] Per MIL-STD 883, Method 1012.1.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFENCE FOR AVDDx. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

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Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation. See the Applications Information section for more details.
1, 2, 47, 48, 49, 52, 55, 61, 64	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63	AVDD2	Supply	Analog Power Supply (2.5 V Nominal).
4, 7, 42, 45	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 38	SPIVDD	Supply	Digital Power Supply for SPI (1.7 V to 3.4 V).
15, 34	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 33	DGND	Ground	Ground Reference for DVDD.
18, 31	DRGND	Ground	Ground Reference for DRVDD.
19, 30	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
56, 60	AGND[1]	Ground	Ground Reference for SYSREF±.
57	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
43, 44	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
53, 54	CLK+, CLK−	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
17, 32	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
20, 21	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input True/Complement.
58, 59	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement.
Data Outputs			
22, 23	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. This pin requires an external 10 kΩ pull-down resistor.
35	SDIO	Input/Output	SPI Serial Data Input/Output.
36	SCLK	Input	SPI Serial Clock.
37	CSB	Input	SPI Chip Select (Active Low).

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, see the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

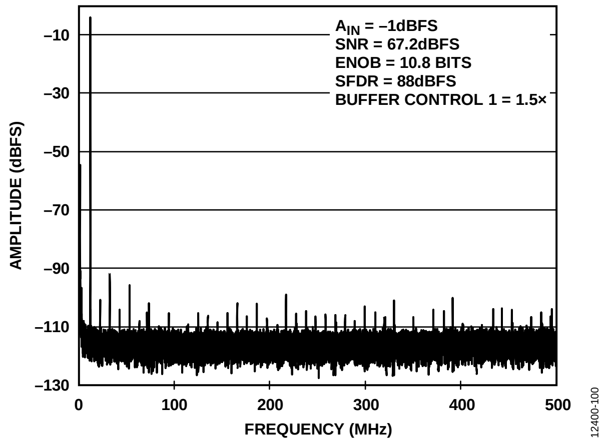

Figure 6. Single Tone FFT with f_{IN} = 10.3 MHz

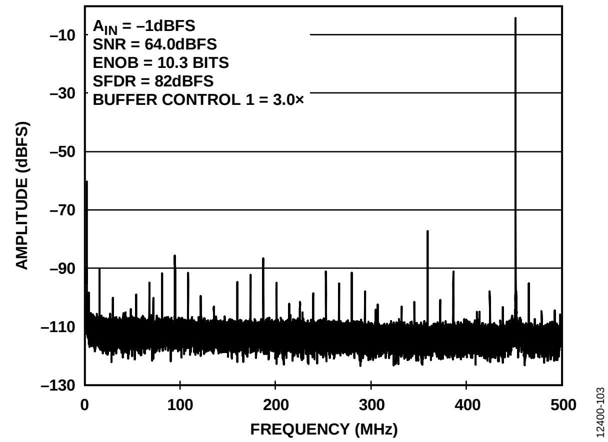

Figure 9. Single Tone FFT with f_{IN} = 450.3 MHz

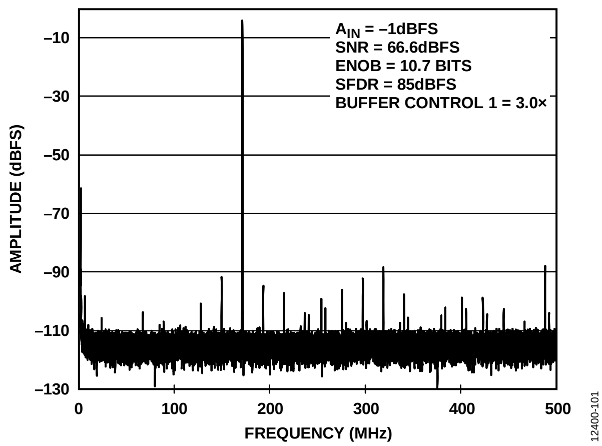

Figure 7. Single Tone FFT with f_{IN} = 170.3 MHz

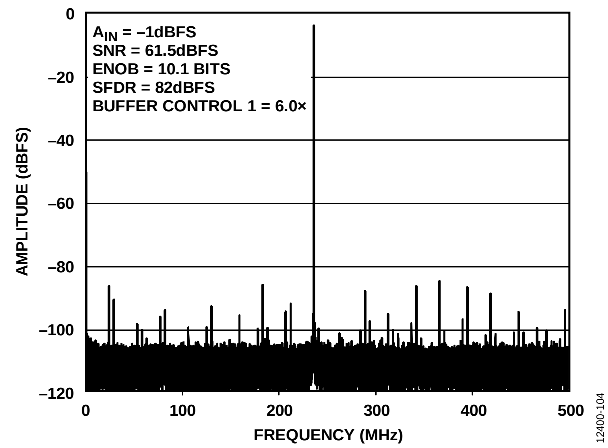

Figure 10. Single Tone FFT with f_{IN} = 765.3 MHz

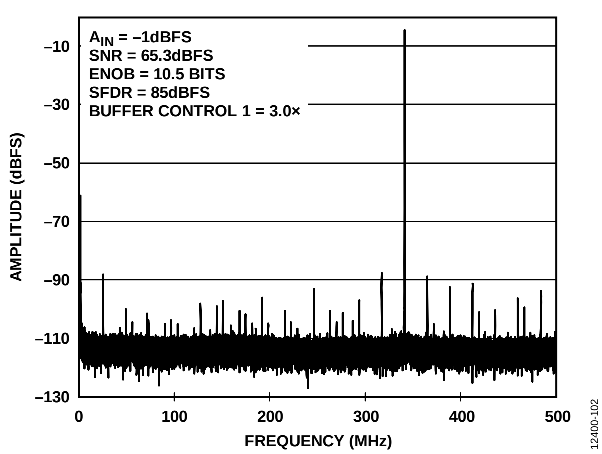

Figure 8. Single Tone FFT with f_{IN} = 340.3 MHz

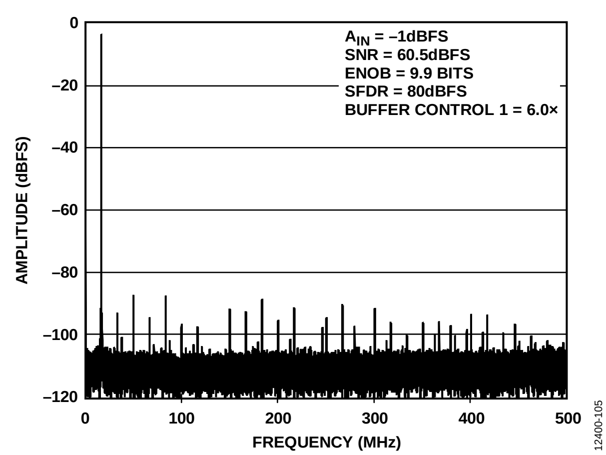

Figure 11. Single Tone FFT with f_{IN} = 985.3 MHz

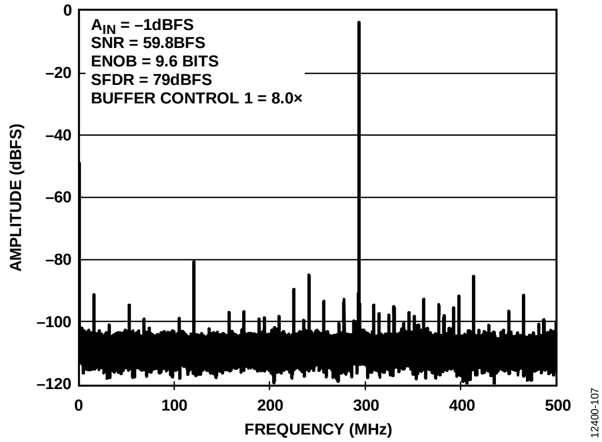

Figure 12. Single Tone FFT with f_{IN} = 1293.3 MHz

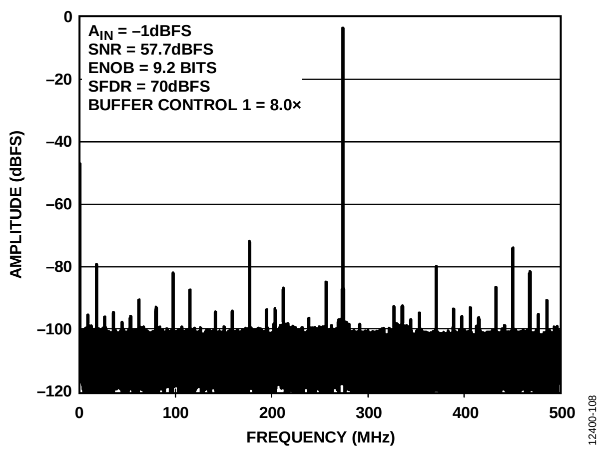

Figure 13. Single Tone FFT with f_{IN} = 1725.3 MHz

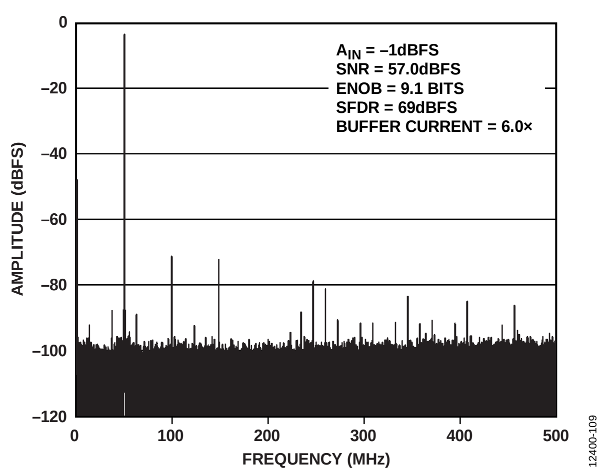

Figure 14. Single Tone FFT with f_{IN} = 1950.3 MHz

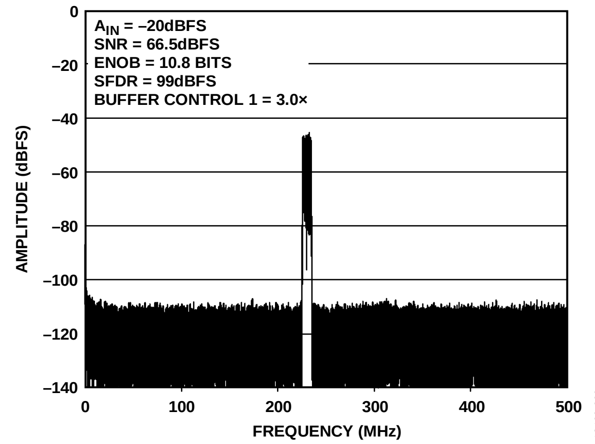

Figure 15. LTE-FDD 10 MHz Channel FFT with f_{IN} = 230 MHz

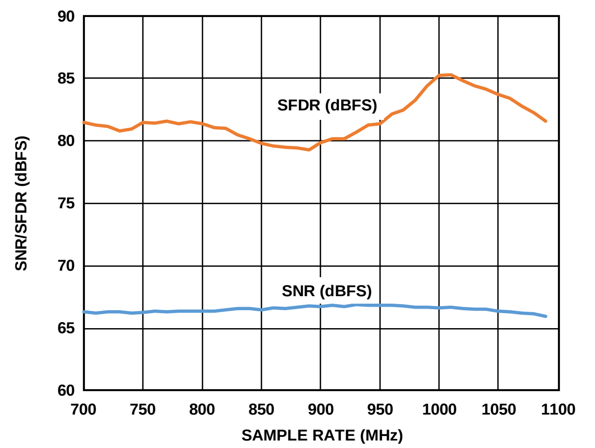

Figure 16. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz; Buffer Control 1 = 3.0×

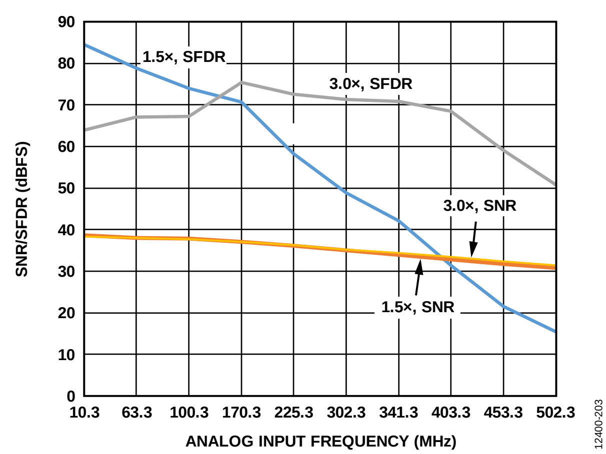

Figure 17. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 = 1.5× and 3.0×

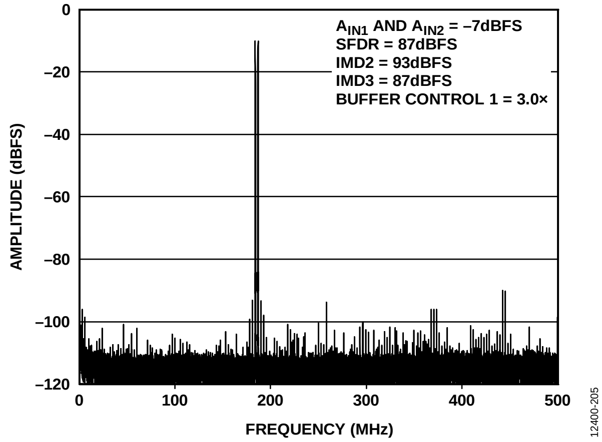

Figure 18. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

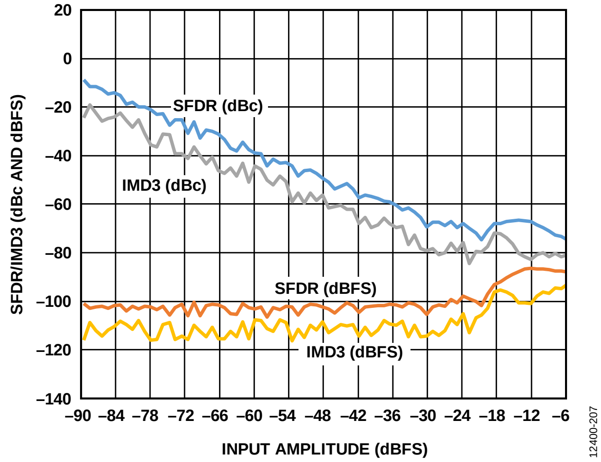

Figure 20. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

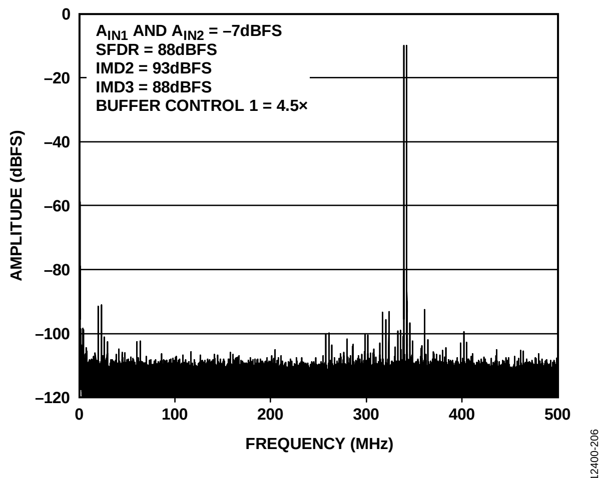

Figure 19. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

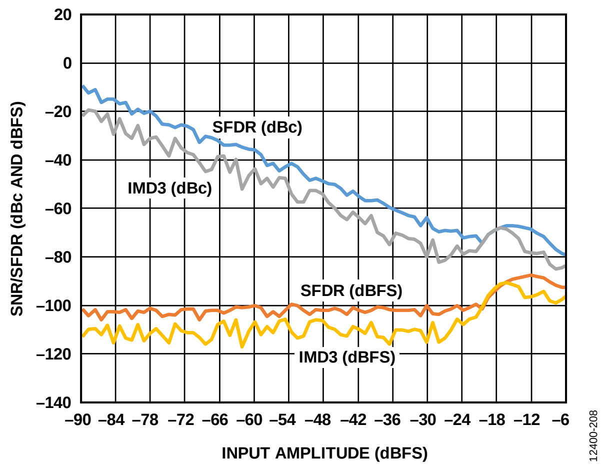

Figure 21. Two-Tone IMD3/SFDR vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

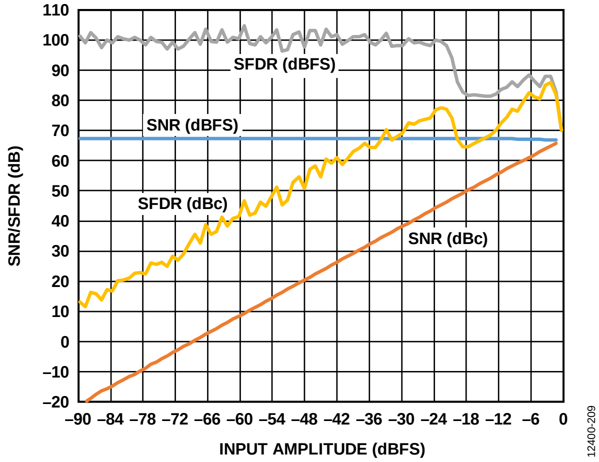

Figure 22. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 170.3 MHz

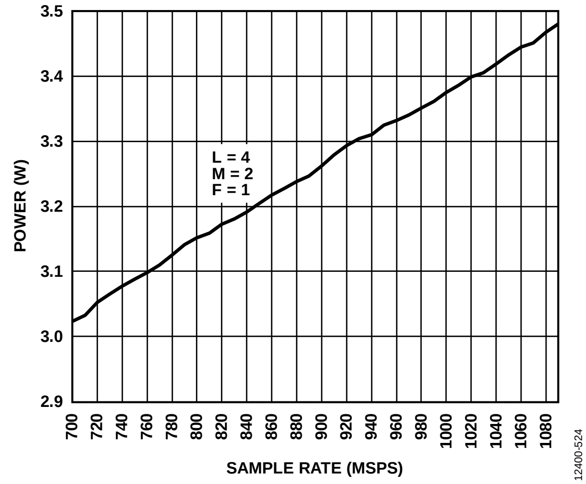

Figure 24. Power Dissipation vs. Sampel Rate (f_S) (Default SPI)

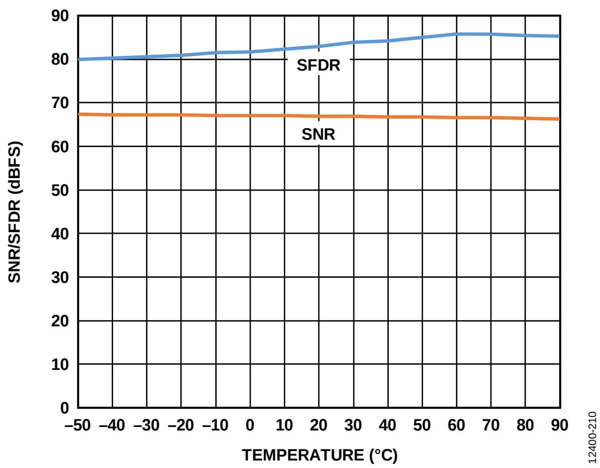

Figure 23. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

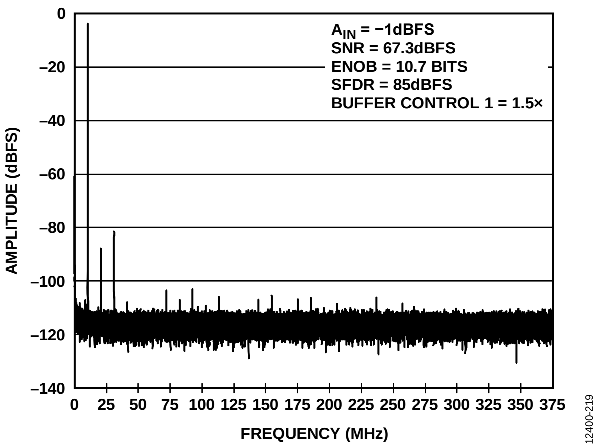

Figure 25. Single Tone FFT with f_{IN} = 10.3 MHz

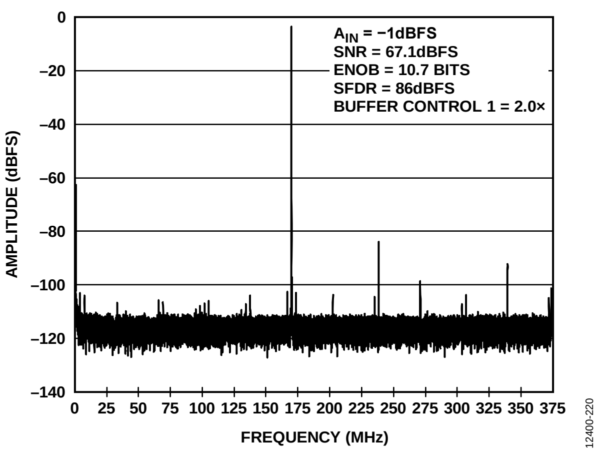

Figure 26. Single Tone FFT with f_{IN} = 170.3 MHz

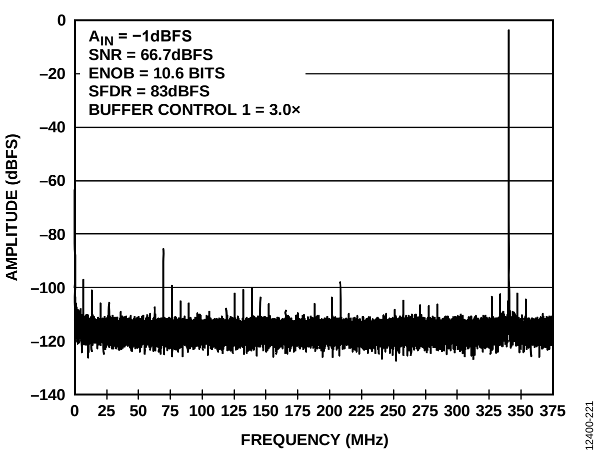

Figure 27. Single Tone FFT with f_{IN} = 340.3 MHz

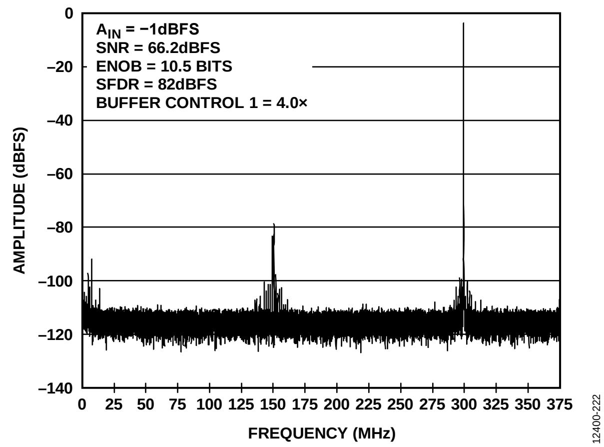

Figure 28. Single Tone FFT with f_{IN} = 450.3 MHz

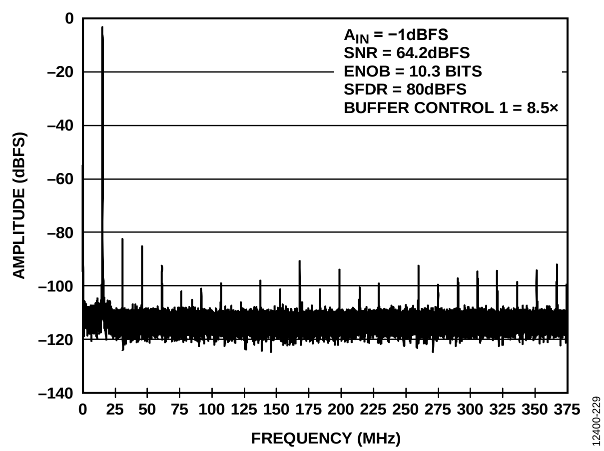

Figure 29. Single Tone FFT with f_{IN} = 765.3 MHz

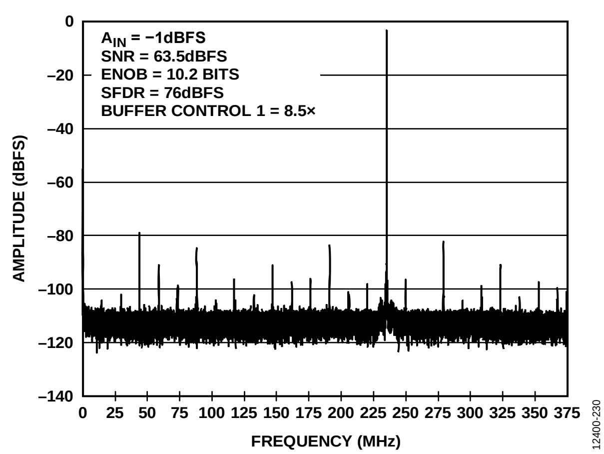

Figure 30. Single Tone FFT with f_{IN} = 985.3 MHz

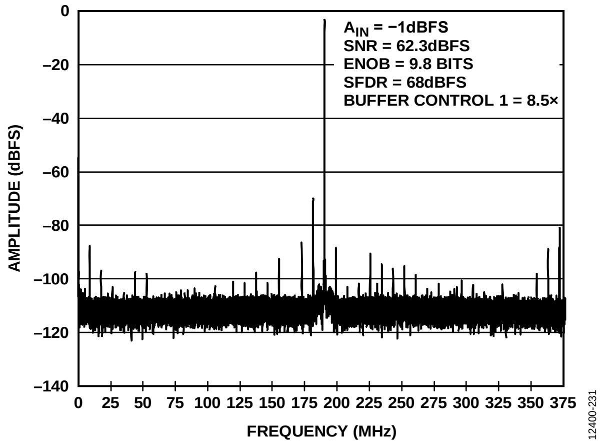

Figure 31. Single Tone FFT with f_{IN} = 1310.3 MHz

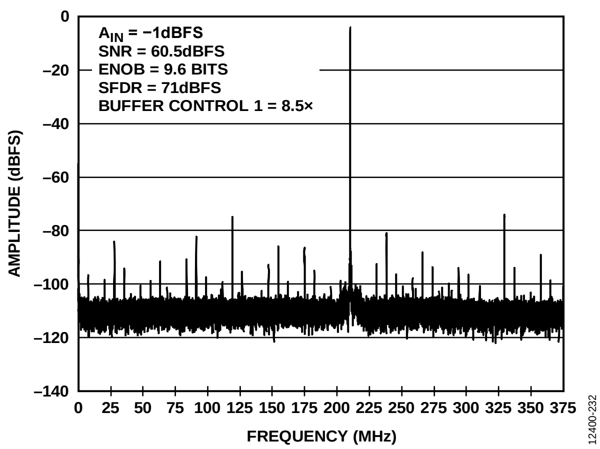

Figure 32. Single Tone FFT with f_{IN} = 1710.3 MHz

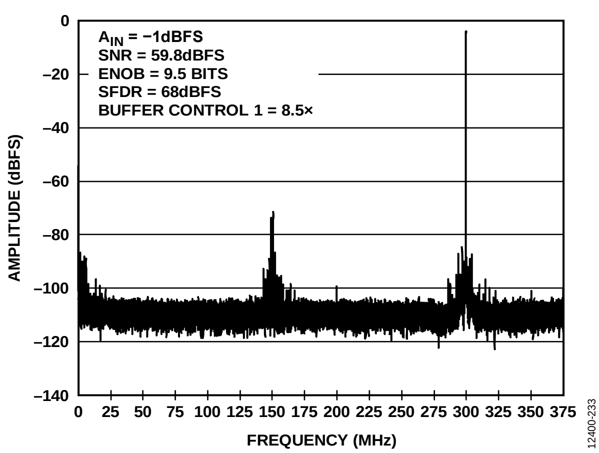

Figure 33. Single Tone FFT with f_{IN} = 1950.3 MHz

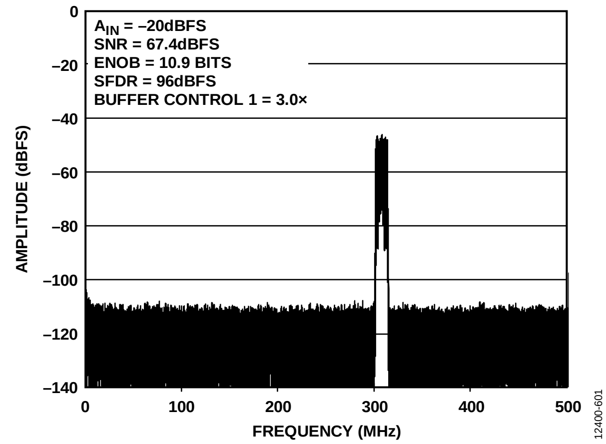

Figure 34. LTE-FDD 10 MHz Channel FFT with f_{IN} = 230 MHz

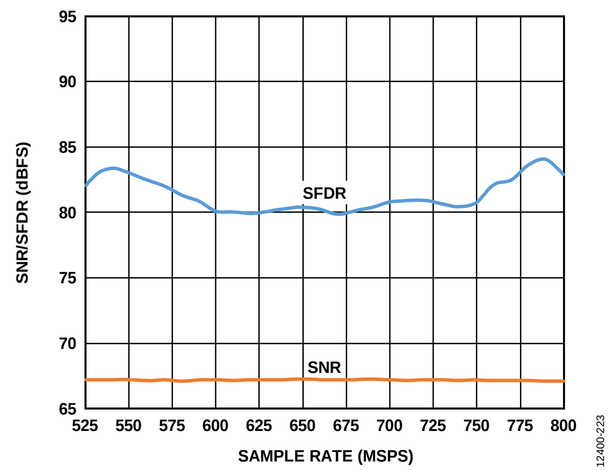

Figure 35. SNR/SFDR vs. Sample Rate (f_S); f_{IN} = 170.3 MHz, Buffer Control 1 = 3.0×

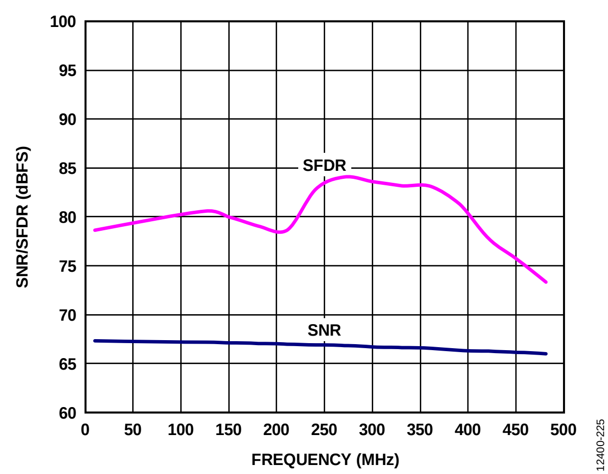

Figure 36. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 = 3.0×

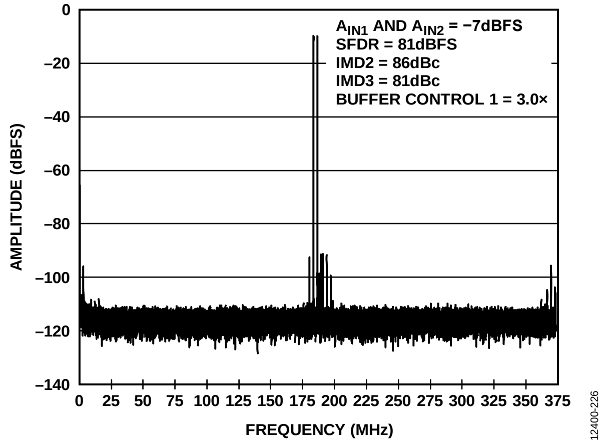

Figure 37. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

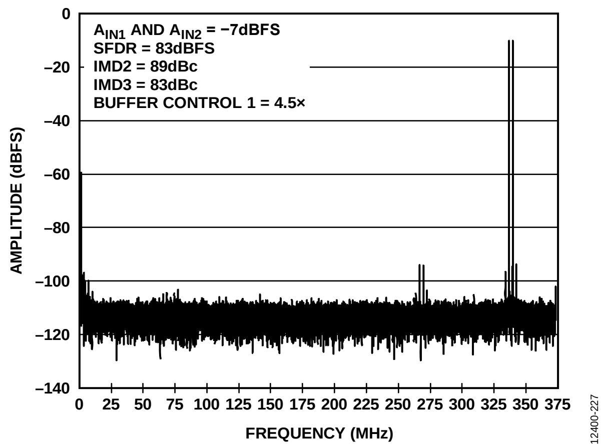

Figure 38. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

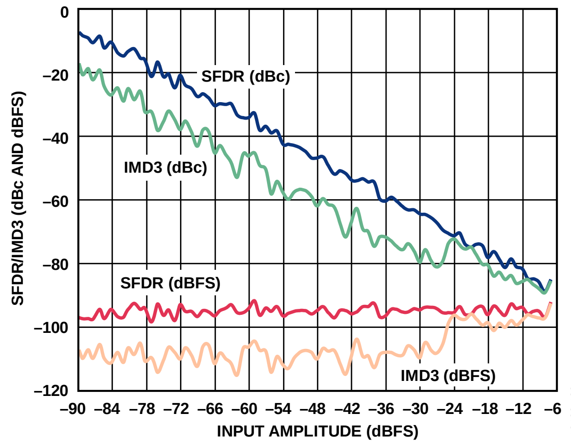

Figure 39. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

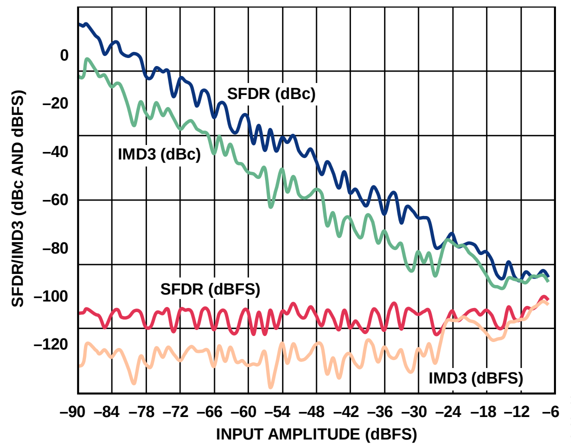

Figure 40. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

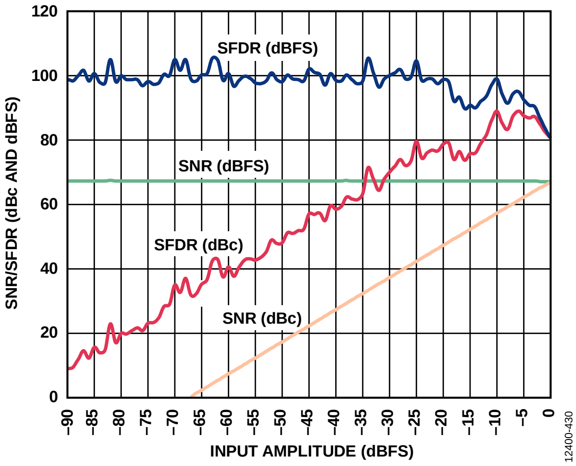

Figure 41. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 170.3 MHz

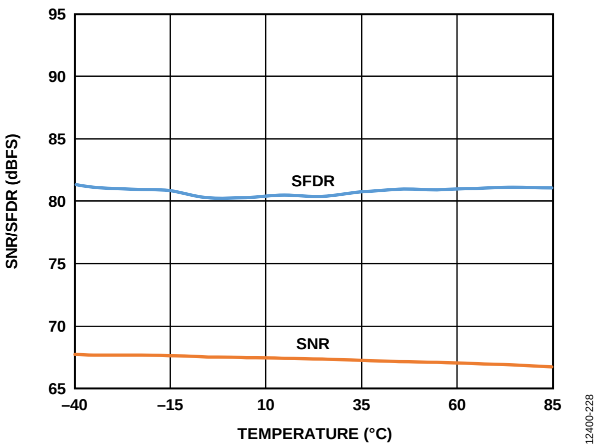

Figure 42. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

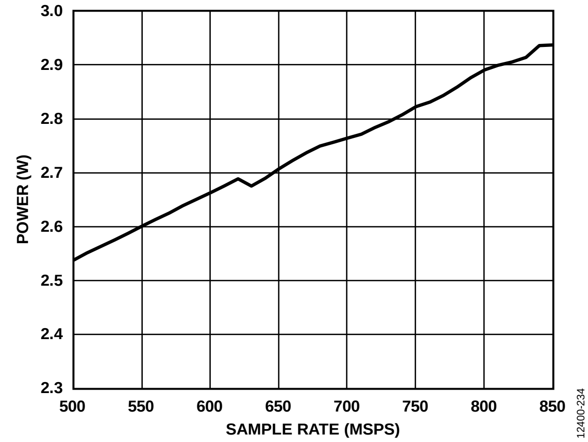

Figure 43. Power Dissipation vs. Sample Rate (f_S); L = 4, M = 2, F = 1 for $f_S \geq$ 625 MSPS and L= 2, M = 2, F = 2 for f_S < 625 MSPS (Default SPI)

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted. See Table 10 for recommended settings.

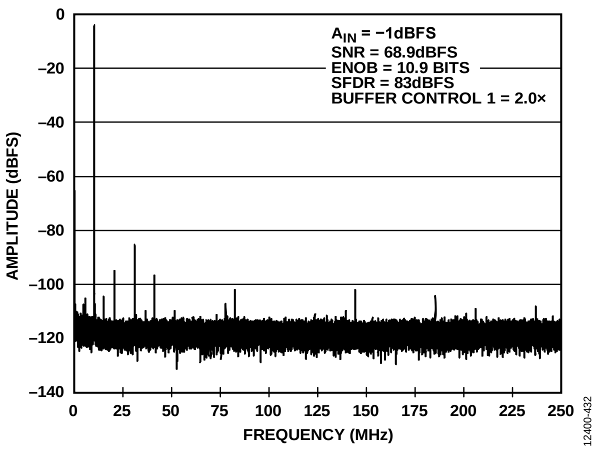

Figure 44. Single Tone FFT with f_{IN} = 10.3 MHz

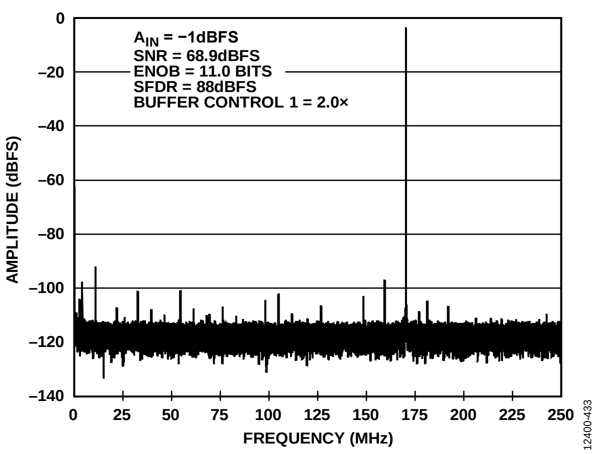

Figure 45. Single Tone FFT with f_{IN} = 170.3 MHz

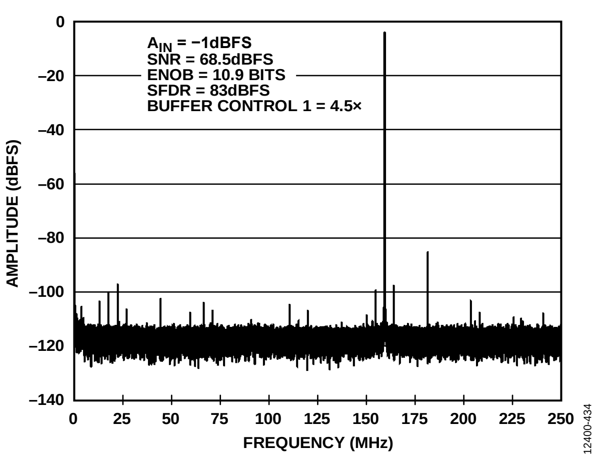

Figure 46. Single Tone FFT with f_{IN} = 340.3 MHz

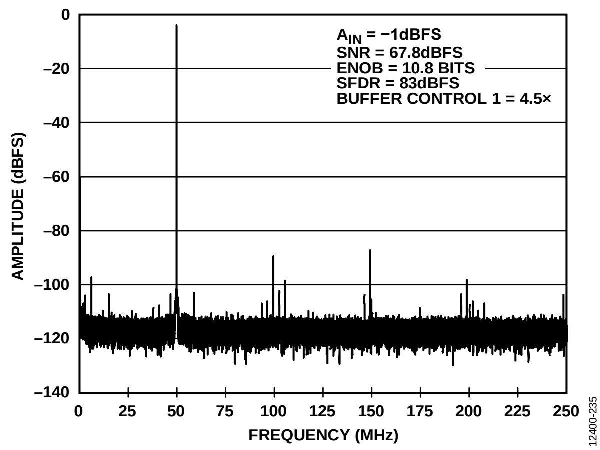

Figure 47. Single Tone FFT with f_{IN} = 450.3 MHz

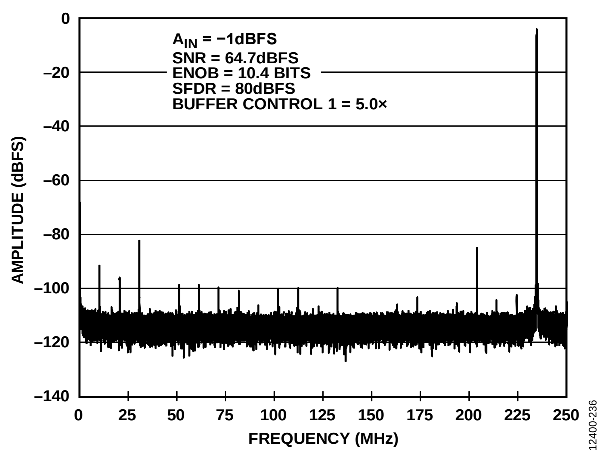

Figure 48. Single Tone FFT with f_{IN} = 765.3 MHz

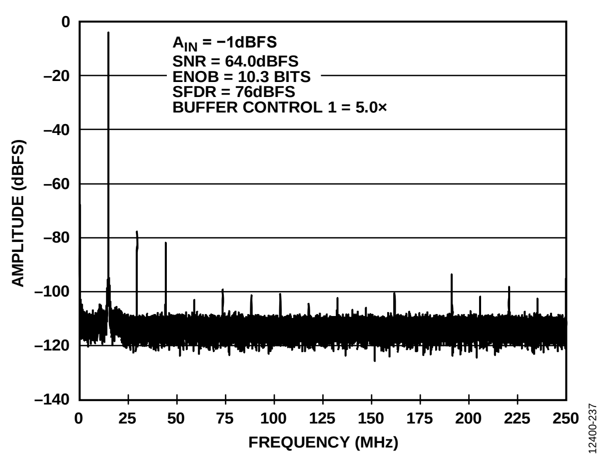

Figure 49. Single Tone FFT with f_{IN} = 985.3 MHz

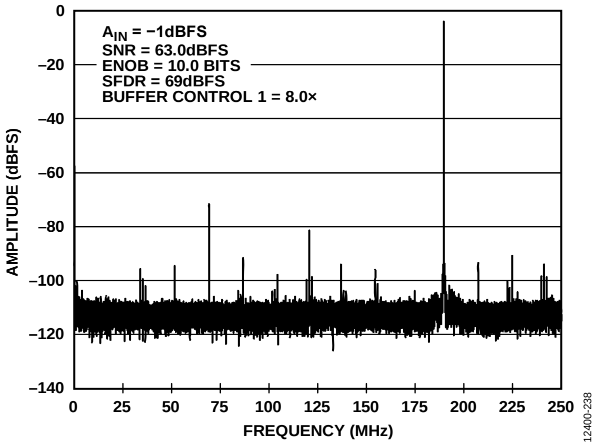

Figure 50. Single Tone FFT with f_{IN} = 1310.3 MHz

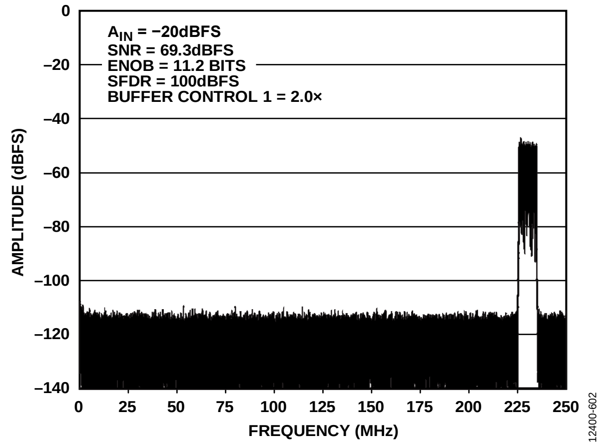

Figure 53. LTE-TDD 10 MHz Channel FFT with f_{IN} = 230 MHz

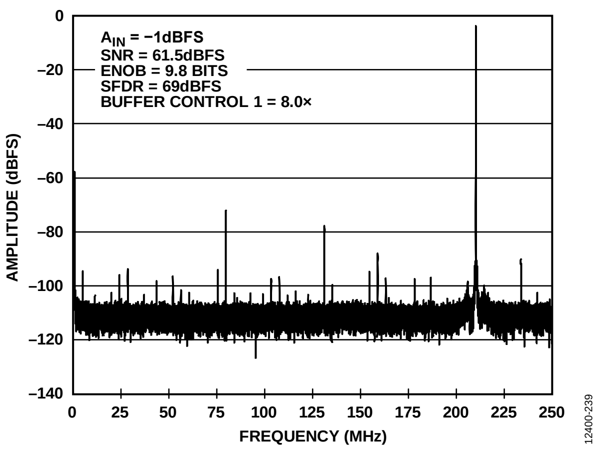

Figure 51. Single Tone FFT with f_{IN} = 1710.3 MHz

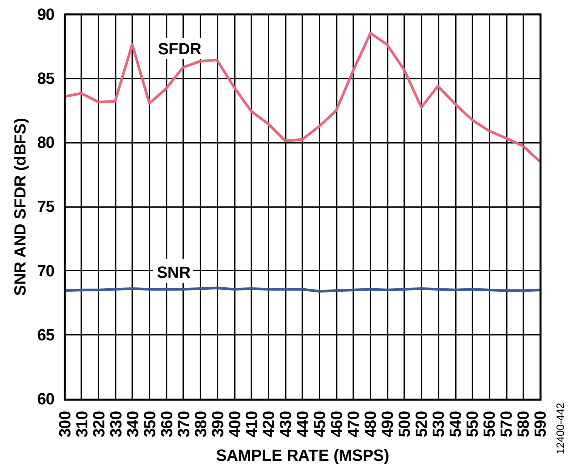

Figure 54. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz; Buffer Control 1 = 2.0×

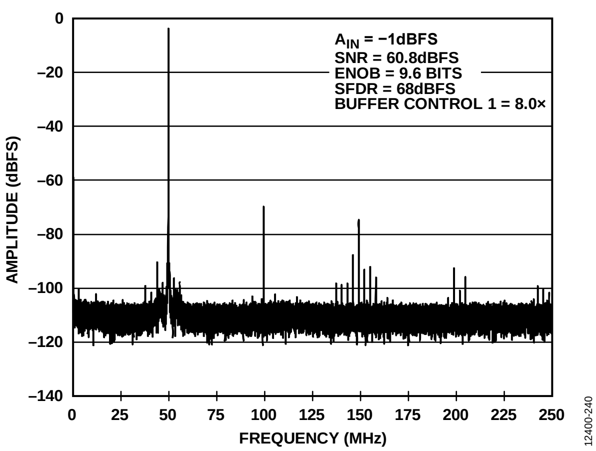

Figure 52. Single Tone FFT with f_{IN} = 1950.3 MHz

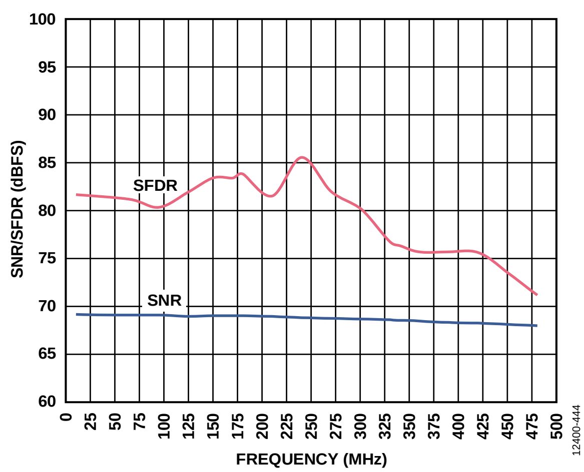

Figure 55. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 = 3.0×

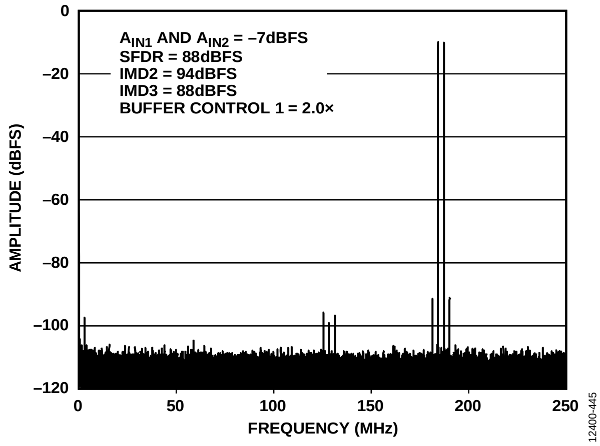

Figure 56. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

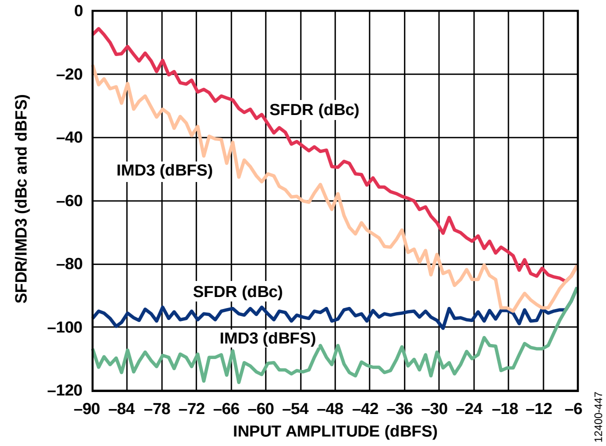

Figure 58. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

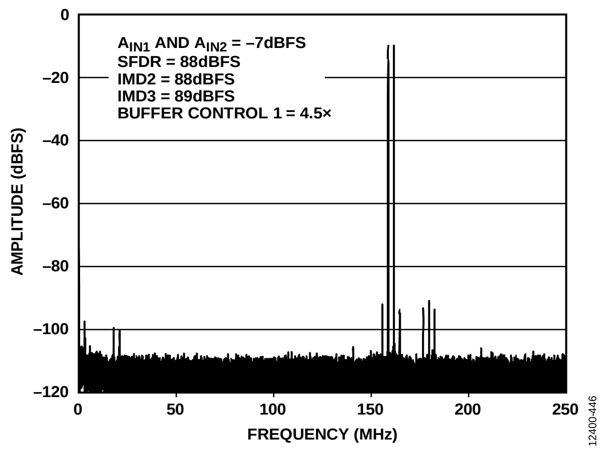

Figure 57. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

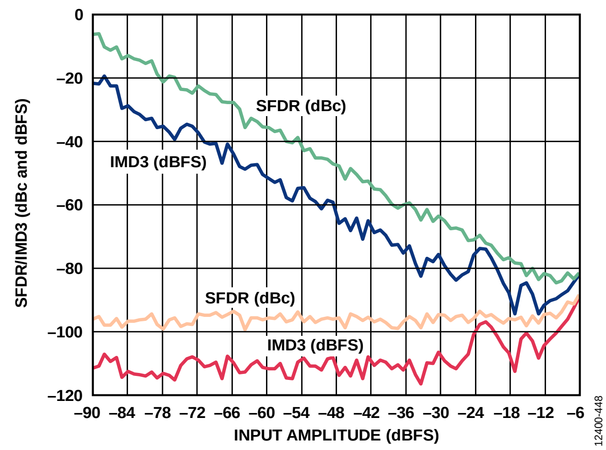

Figure 59. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

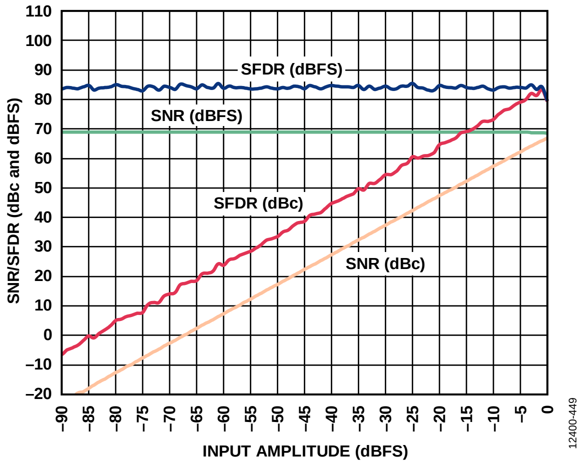

Figure 60. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 170.3 MHz

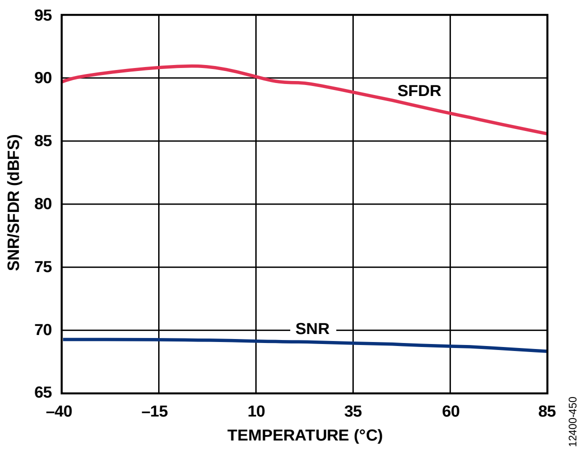

Figure 61. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

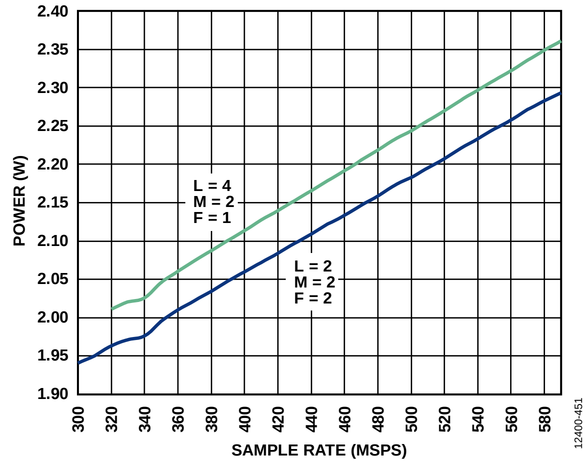

Figure 62. Power Dissipation vs. Sample Rate (f_S) (Default SPI)

EQUIVALENT CIRCUITS

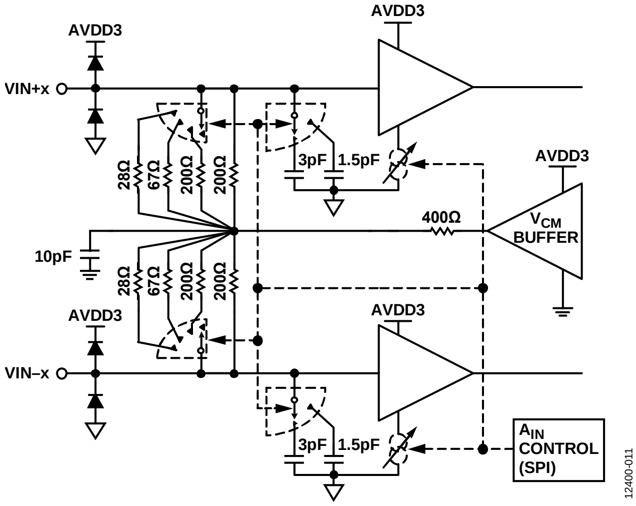

Figure 63. Analog Inputs

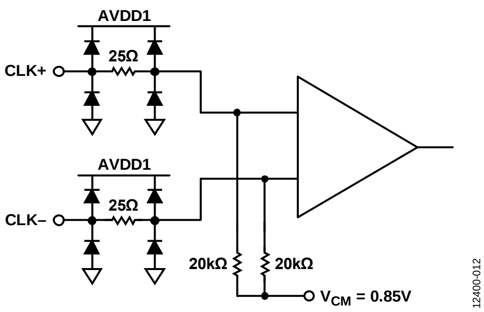

Figure 64. Clock Inputs

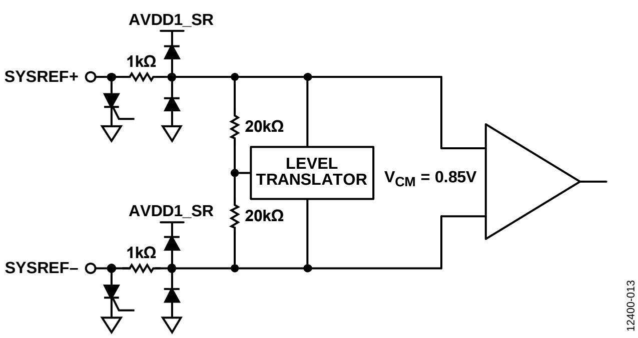

Figure 65. SYSREF± Inputs

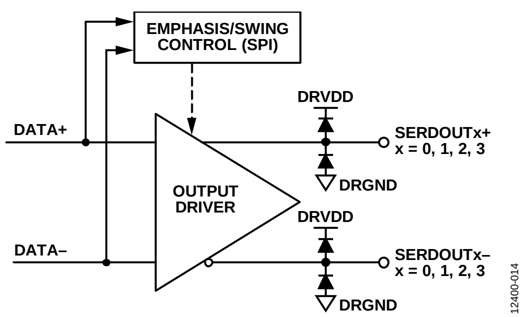

Figure 66. Digital Outputs

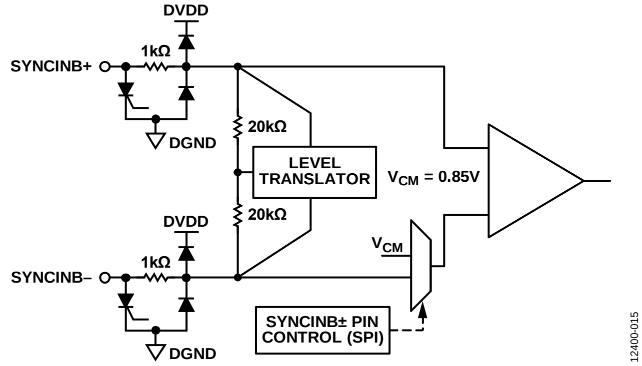

Figure 67. SYNCINB± Inputs

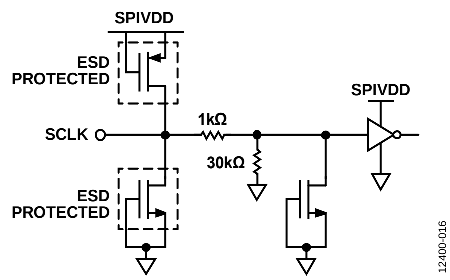

Figure 68. SCLK Inputs

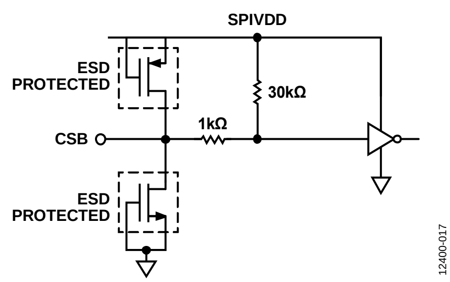

Figure 69. CSB Input

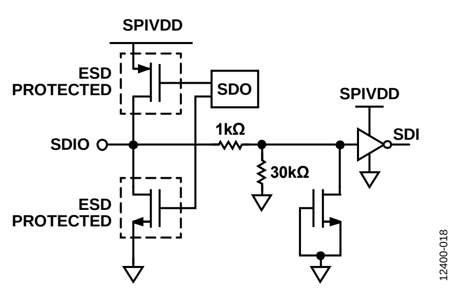

Figure 70. SDIO

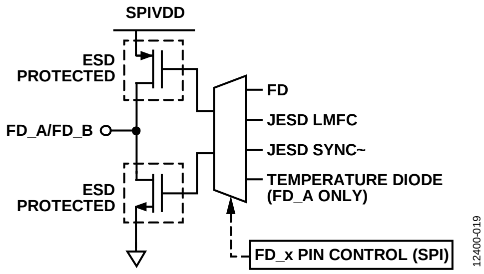

Figure 71. FD_A/FD_B Outputs

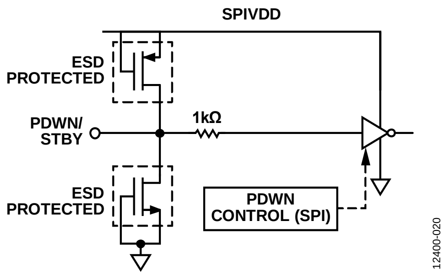

Figure 72. PDWN/STBY Input

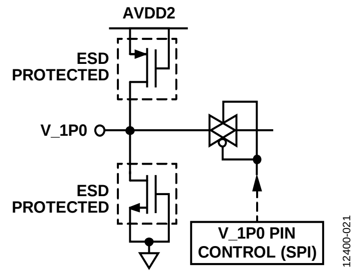

Figure 73. V_1P0 Input/Output

THEORY OF OPERATION

The AD6674 has two analog input channels and two JESD204B output lane pairs. The AD6674 is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD6674 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD6674 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect bits of the ADC output data stream, which are enabled and programmed via Register 0x245 through Register 0x24C. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly lower the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data rate can be configured in one-lane (L = 1) and two-lane (L = 2) configurations depending upon the sample rate and the decimation ratio. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

ADC ARCHITECTURE

The architecture consists of an input buffered pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 63. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces the kickback from the ADC. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6674 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, can help reduce the peak transient current inserted from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each section of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, refer to the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) at www.analog.com. In general, the precise values depend on the application.

For best dynamic performance, match the source impedances driving VIN+x and VIN−x such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD6674, the available span is programmable through the SPI port from 1.46 V p-p to 2.06 V p-p differential, with 1.70 V p-p differential being the default for the AD6674-1000 and AD6674-750, whereas the default for the AD6674-500 is 2.06 V p-p.

Differential Input Configurations

There are several ways to drive the AD6674, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 74 and Table 9) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD6674.

For low to midrange frequencies, it is recommended to use a double balun or double transformer network (see Figure 74) for optimum performance from the AD6674. For higher frequencies in the second or third Nyquist zone, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 74 and Table 9).

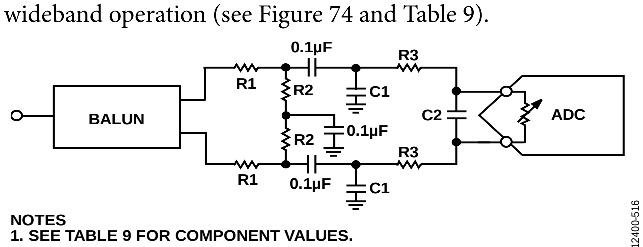

Figure 74. Differential Transformer Coupled Configuration for AD6674

Table 9. Differential Transformer Coupled Input Configuration Component Values

Device	Frequency Range	Transformer	R1 (Ω)	R2 (Ω)	R3 (Ω)	C1 (pF)	C2 (pF)
AD6674-500	DC to 250 MHz	ETC1-1-13	10	50	10	4	2
	250 MHz to 2 GHz	BAL0006/BAL0006SMG	10	50	10	4	2
AD6674-750	DC to 375 MHz	ETC1-1-13	10	50	10	4	2
	375 MHz to 2 GHz	BAL0006/BAL0006SMG	10	50	10	4	2
AD6674-1000	DC to 500 MHz	ECT1-1-13/BAL0006SMG	25	25	10	4	2
	500 MHz to 2 GHz	BAL0006/BAL0006SMG	25	25	0	Open	Open

Input Common Mode

The analog inputs of the AD6674 are internally biased to the common mode, as shown in Figure 75. The common-mode buffer has limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V ± 100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD6674 offers flexible controls for the analog inputs such as input termination, input capacitance, buffer current, and input full-scale adjustment. All of the available controls are shown in Figure 75.

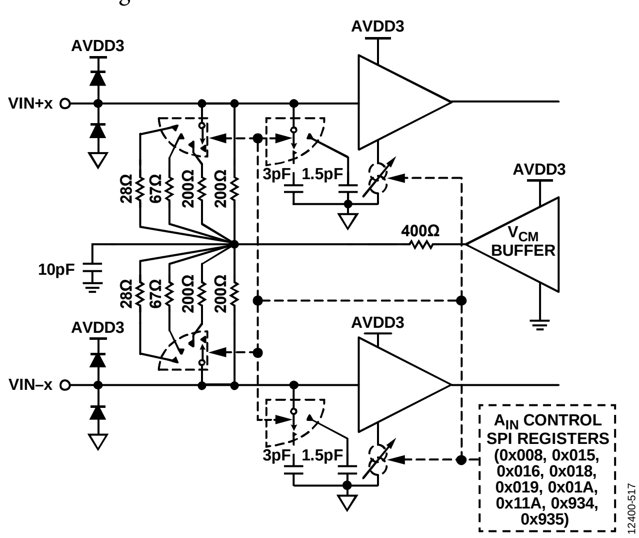

Figure 75. Analog Input Controls

Use Register 0x018, Register 0x019, Register 0x01A, Register 0x11A, Register 0x934, and Register 0x935 to adjust the buffer behavior on each channel to optimize the SFDR over various input frequencies and bandwidths of interest.

Input Buffer Control Registers (Register 0x018, Register 0x019, Register 0x01A, Register 0x934, Register 0x935, Register 0x11A)

The input buffer has many registers that set the bias currents and other settings for operation at different frequencies. These bias currents and settings can be changed to suit the input frequency range of operation. Register 0x018 controls the buffer bias current to reduce the effects of charge kickback from the ADC core. This setting can be scaled from a low setting of 1.0× to a high setting of 8.5×. The default setting in Register 0x018 is 3.0× for the AD6674-750 and AD6674-1000, whereas the default for the AD6674-500 is 2.0×. These settings are sufficient for operation in the first Nyquist zone. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 76. For a complete list of buffer current settings, see Table 45 for more details.

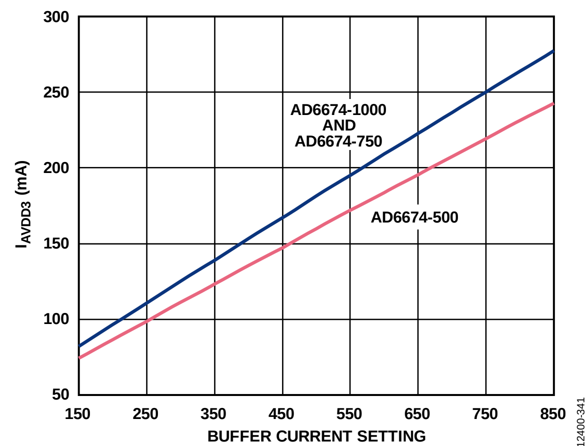

Figure 76. I_{AVDD3} vs. Buffer Current Setting in Register 0x018

Register 0x019, Register 0x01A, Register 0x11A, and Register 0x935 offer secondary bias controls for the input buffer for frequencies >500 MHz. Register 0x934 can be used to reduce input capacitance to achieve wider signal bandwidth but doing so may result in slightly lower linearity and noise performance. These register settings do not affect the AVDD3 power as much as Register 0x018 does. For frequencies <500 MHz, it is recommended to use the default settings for these registers. Table 10 shows the recommended values for the buffer current control registers for various speed grades.

Use Register 0x11A when sampling in higher Nyquist zones (>500 MHz for the AD6674-1000). This setting enables the ADC sampling network to optimize the sampling and settling times internal to the ADC for high frequency operation. For frequencies greater than 500 MHz, it is recommended to operate the ADC core at a 1.46 V full-scale setting irrespective of the speed grade. This setting offers better SFDR without any significant decrease in SNR.

Figure 77, Figure 78, and Figure 79 show the SFDR vs. analog input frequency for various buffer settings (I_{BUFF}) for the AD6674-1000.

The recommended settings shown in Table 10 were used to collect the data while changing only the contents of Register 0x018.

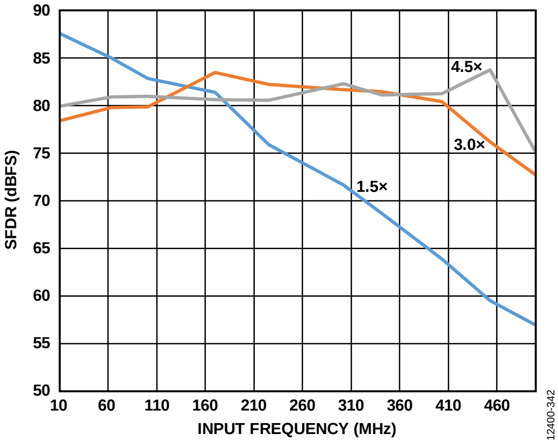

Figure 77. Buffer Current Sweeps, AD6674-1000 (SFDR vs. Input Frequency and I_{BUFF}); 10 MHz < f_{IN} < 500 MHz; Front-End Network Shown in Figure 74

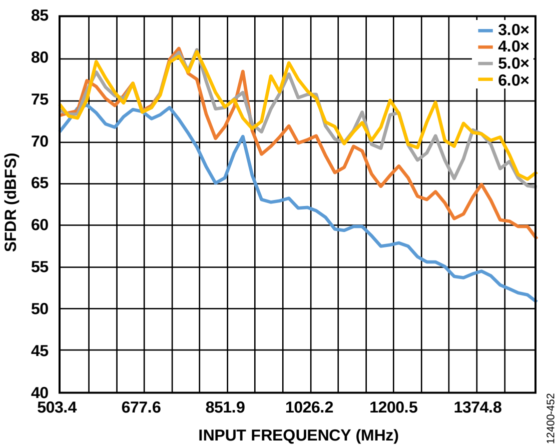

Figure 78. Buffer Current Sweeps, AD6674-1000 (SFDR vs. Input Frequency and I_{BUFF}); 500 MHz < f_{IN} < 1500 MHz; Front-End Network Shown in Figure 74

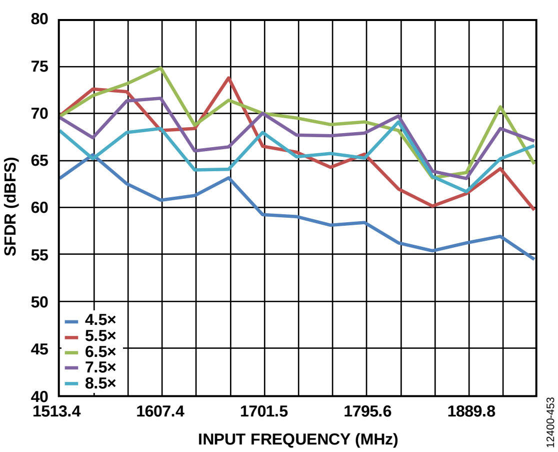

Figure 79. Buffer Current Sweeps, AD6674-1000 (SFDR vs. Input Frequency and I_{BUFF}); 1500 MHz < f_{IN} < 2 GHz; Front-End Network Shown in Figure 74

In certain high frequency applications, the SFDR can be improved by reducing the full-scale setting, as shown in Table 10. At high frequencies, the performance of the ADC core is limited by jitter. The SFDR can be improved by reducing the full-scale level.

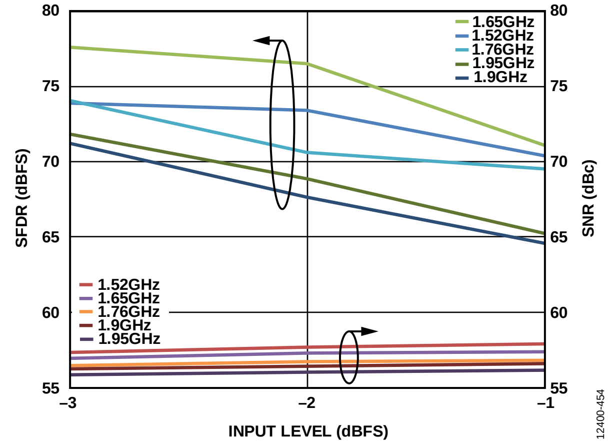

Figure 80. SNR/SFDR vs. Input Level and Input Frequencies, AD6674-1000

Figure 81, Figure 82, and Figure 83 show the SFDR vs. analog input frequency for various buffer settings for the AD6674-500. The recommended settings shown in Table 10 were used to take the data while changing the contents of register 0x018 only.

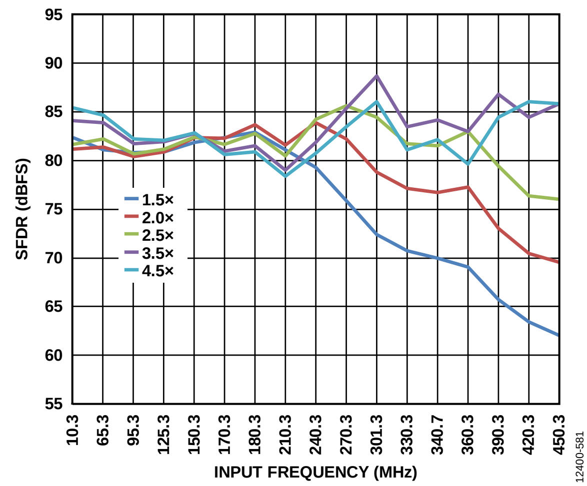

Figure 81. Buffer Current Sweeps, AD6674-750 (SFDR vs. Input Frequency and I_{BUFF}); 10 MHz < f_{IN} < 450 MHz; Front-End Network Shown in Figure 74

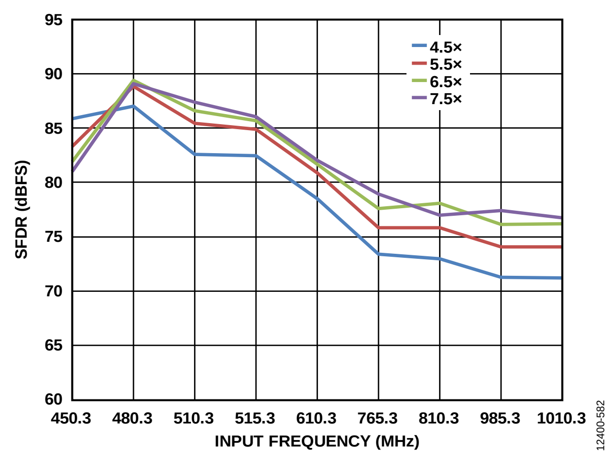

Figure 82. Buffer Current Sweeps, AD6674-750 (SFDR vs. Input Frequency and I_{BUFF}); 450 MHz < f_{IN} < 800 MHz; Front-End Network Shown in Figure 74

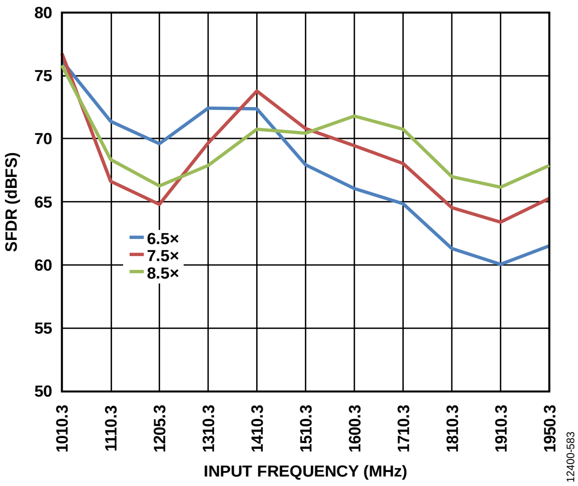

Figure 83. Buffer Current Sweeps, AD6674-750 (SFDR vs. Input Frequency and I_{BUFF}); 800 MHz < f_{IN} < 2 GHz; Front-End Network Shown in Figure 74

Figure 84, Figure 85, and Figure 86 show the SFDR vs. analog input frequency for various buffer settings for the AD6674-500. The recommended settings shown in Table 10 were used to take the data while changing the contents of register 0x018 only.

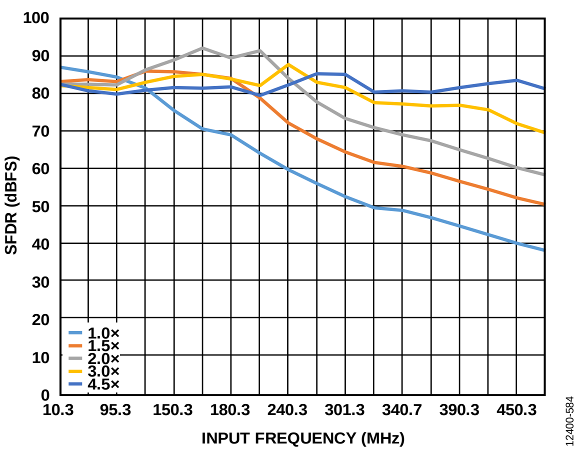

Figure 84. Buffer Current Sweeps, AD6674-500 (SFDR vs. Input Frequency and I_{BUFF}); 10 MHz < f_{IN} < 450 MHz; Front-End Network Shown in Figure 74

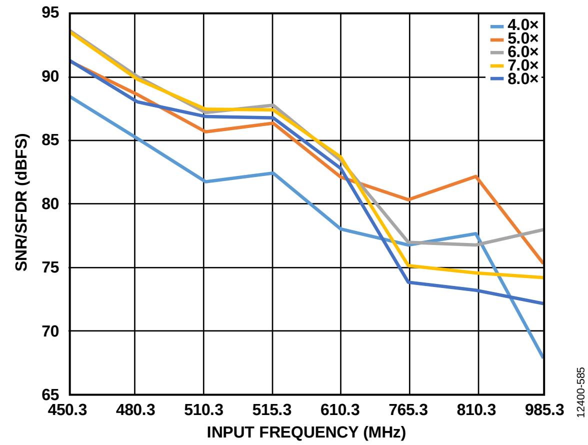

Figure 85. Buffer Current Sweeps, AD6674-500 (SFDR vs. Input Frequency and I_{BUFF}); 450 MHz < f_{IN} < 1000 MHz; Front-End Network Shown in Figure 74

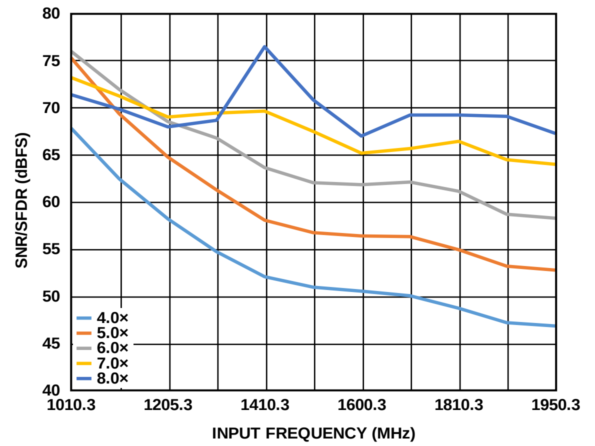

Figure 86. Buffer Current Sweeps, AD6674-500 (SFDR vs. Input Frequency and I_{BUFF}); 1 GHz < f_{IN} < 2 GHz; Front-End Network Shown in Figure 74

Table 10. AD6674 Performance Optimization for Input Frequencies

Product	Frequency (MHz)	Buffer Control 1 (0x018)	Buffer Control 2 (0x019)	Buffer Control 3 (0x01A)	Buffer Control 4 (0x11A)	Buffer Control 5 (0x935)	Input Full-Scale Control (0x030)	Input Full-Scale Range (0x025)	Input Capacitance (0x934)	Input Termination (0x016)[1]
AD6674-500	DC to 250	0x20 (2.0×)	0x60 (Setting 3)	0x0A (Setting 3)	0x00 (off)	0x04 (on)	0x04	0x0C (2.06 V p-p)	0x1F	0x0C/0x1C/ 0x2C/0x6C
	250 to 500	0x70 (4.5×)	0x60 (Setting 3)	0x0A (Setting 3)	0x00 (off)	0x04 (on)	0x04	0x0C (2.06 V p-p)	0x1F	0x0C/0x1C/ 0x2C/0x6C
	500 to 1000	0x80 (5.0×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F/0x00[2]	0x0C/0x1C/ 0x2C/0x6C
	1000 to 2000	0xF0 (8.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F/0x00[2]	0x0C/0x1C/ 0x2C/0x6C
AD6674-750	DC to 200	0x20 (2.0×)	0x40 (Setting 1)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x14	0x0A (1.70 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	DC to 375	0x40 (3.0×)	0x40 (Setting 1)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x14	0x0A (1.70 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	200 to 500	0x70 (4.5×)	0x40 (Setting 1)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x14	0x0A (1.70 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	375 to 750	0xA0 (6.0×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	500 to 750	0xD0 (7.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	750 to 1000	0xF0 (8.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F/0x00[2]	0x0E/0x1E/ 0x2E/0x6E
	1000 to 2000	0xF0 (8.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F/0x00[2]	0x0E/0x1E/ 0x2E/0x6E
AD6674-1000	DC to 150	0x10 (1.5×)	0x50 (Setting 2)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x18	0x0A (1.70 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	DC to 500	0x40 (3.0×)	0x50 (Setting 2)	0x09 (Setting 2)	0x00 (off)	0x04 (on)	0x18	0x0A (1.70 V p-p)	0x1F	0x0E/0x1E/ 0x2E/0x6E
	500 to 1000	0xA0 (6.0×)	0x60 (Setting 3)	0x09 (Setting 2)	0x20 (on)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F/0x00[2]	0x0E/0x1E/ 0x2E/0x6E
	1000 to 2000	0xD0 (7.5×)	0x70 (Setting 4)	0x09 (Setting 2)	0x20 (on)	0x00 (off)	0x18	0x08 (1.46 V p-p)	0x1F/0x00[2]	0x0E/0x1E/ 0x2E/0x6E

[1] The input termination can be changed to accommodate the application with little or no impact to ac performance.
[2] The input capacitance can be set to 1.5 pF to achieve wider input bandwidth but results in slightly lower linearity and noise performance.

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD6674 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD6674. This internal 1.0 V reference sets the full-scale input range of the ADC. The full-scale input range can be adjusted via Register 0x025. For more information on adjusting the input swing, see Table 45. Figure 87 shows the block diagram of the internal 1.0 V reference controls.

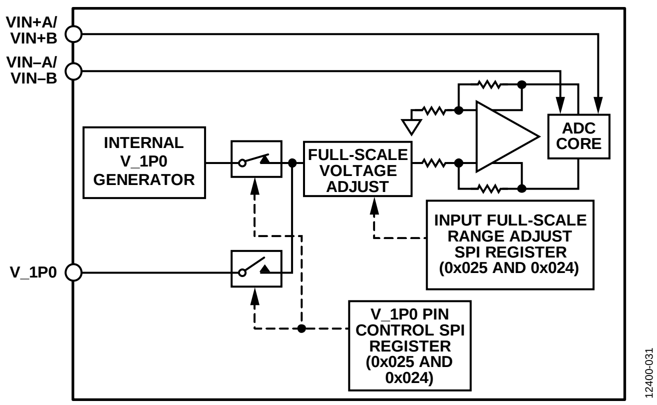

Figure 87. Internal Reference Configuration and Controls

Register 0x024 enables the user to either use this internal 1.0 V reference or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD6674, refer to the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 88 shows the typical drift characteristics of the internal 1.0 V reference.

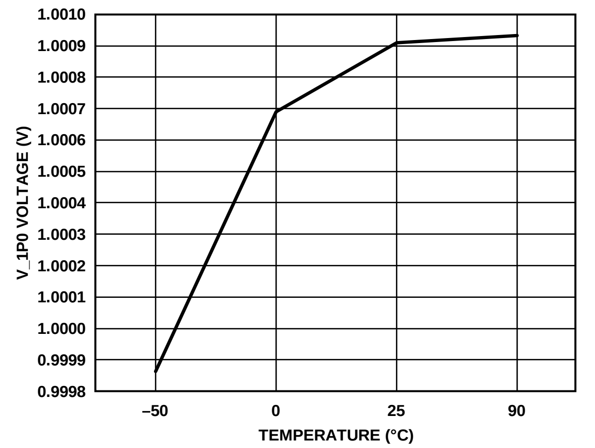

Figure 88. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 89 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD6674. The grayed out areas show unused blocks within the AD6674 while the ADR130 provides the external reference.

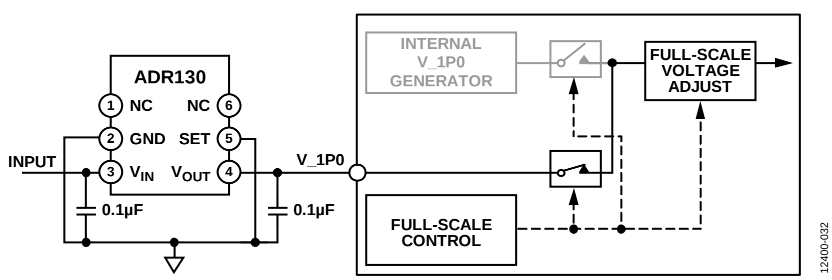

Figure 89. External Reference Using the ADR130

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD6674 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 90 shows one preferred method for clocking the AD6674. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

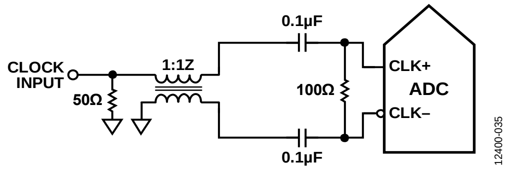

Figure 90. Transformer Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins as shown in Figure 91 and Figure 92.

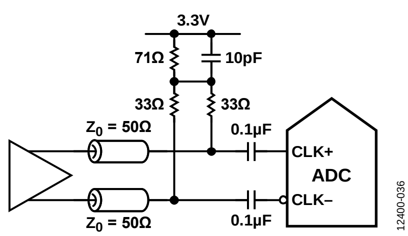

Figure 91. Differential CML Sample Clock

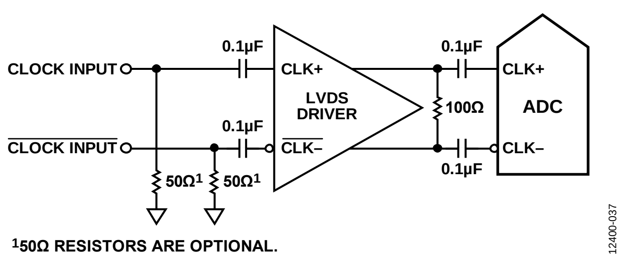

Figure 92. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the AD6674. For example, the AD6674-1000 can be clocked at 2 GHz with the internal clock divider set to 2. This ensures a 50% duty cycle, high slew rate internal clock for the ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider

The AD6674 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, or 8. The divide ratios can be selected using Register 0x10B. This is shown in Figure 93. The maximum frequency at the output of the divider is 1.0 GHz.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, take care to program the appropriate divider ratio into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

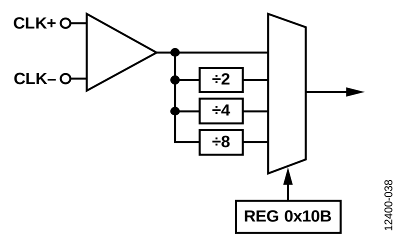

Figure 93. Clock Divider Circuit

The AD6674 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This feature is enabled by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling.

After programming the desired clock divider settings, changing the input clock frequency, or glitching the input clock, a datapath soft reset is recommended by writing 0x02 to Register 0x001. This reset function restarts all the datapath and clock generation circuitry in the device. The reset occurs on the first clock cycle after the register is programmed, and the device requires 5 ms to recover. This reset does not affect the contents of the memory map registers.

Input Clock Divider ½ Period Delay Adjustment

The input clock divider inside the AD6674 provides phase delay in increments of ½ the input clock cycle. Program Register 0x10C to enable this delay independently for each channel. Changing the register does not affect the stability of the JESD204B link.

Clock Fine Delay Adjustment

Adjust the AD6674 sampling edge instant by writing to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the feature, and Register 0x118, Bits[7:0], set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in ~1.7 ps increments. The clock delay adjustment takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjustment in Register 0x117 causes a datapath reset. However, the contents of Register 0x118 can be changed without affecting the stability of the JESD204B link.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) is calculated by

$$SNR = 20 \times \log 10(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 94).

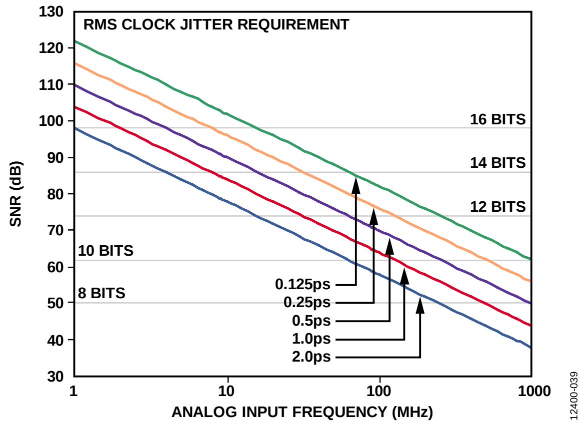

Figure 94. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD6674. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime it using the original clock at the last step. See the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

Figure 95 shows the estimated SNR of the AD6674-1000 across input frequency for different clock induced jitter values. The SNR can be estimated by using the following equation:

$$SNR(\text{dBFS}) = 10\log\left[10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right]$$

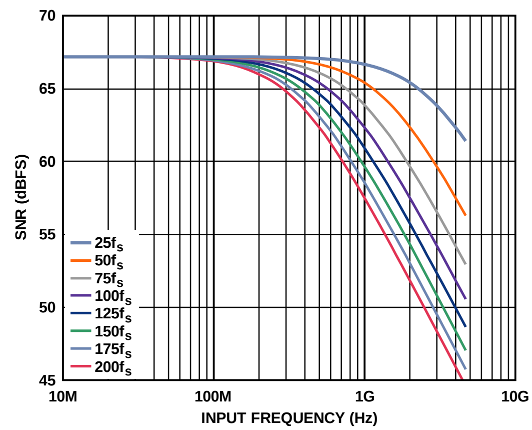

Figure 95. Estimated SNR Degradation for the AD6674-1000 vs. Input Frequency and Jitter

POWER-DOWN/STANDBY MODE

The AD6674 has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode. The default operation is the PDWN function. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. This can be changed using Register 0x571[7] to select /K/ characters.

TEMPERATURE DIODE

The AD6674 contains a diode-based temperature sensor for measuring the temperature of the die. This diode outputs a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028[0] to enable or disable the diode. Register 0x028 is a local register. Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040[2:0]. See Table 45 for more information.

The voltage response of the temperature diode (with SPIVDD = 1.8 V) is shown in Figure 96.

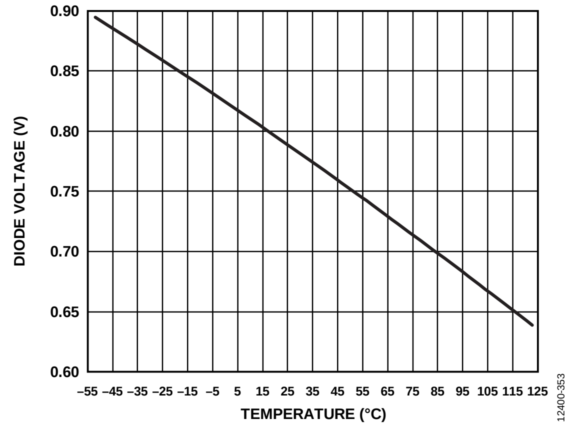

Figure 96. Temperature Diode Voltage vs. Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD6674 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD6674 constantly monitors the analog input level and records any overrange condition in any of the eight virtual converters. For more information on the virtual converters, refer to Figure 102. The overrange status of each virtual converter is registered as a sticky bit (that is, it is set until cleared) in Register 0x563. Clear the contents of Register 0x563 using Register 0x562 by toggling the bits corresponding to the virtual converter to set and reset the position.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The fast detect (FD) bit (enabled in the control bits via Register 0x559 and Register 0x55A) is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 97.

The FD_x indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located in Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28. The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Threshold Magnitude}/2^{13})$$

The FD_x indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located in Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0x0FFF to Register 0x247 and Register 0x248; and to set a lower threshold of −10 dBFS, write 0x0A1D to Register 0x249 and Register 0x24A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located in Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x245 to Register 0x24C in Table 45) for more details.

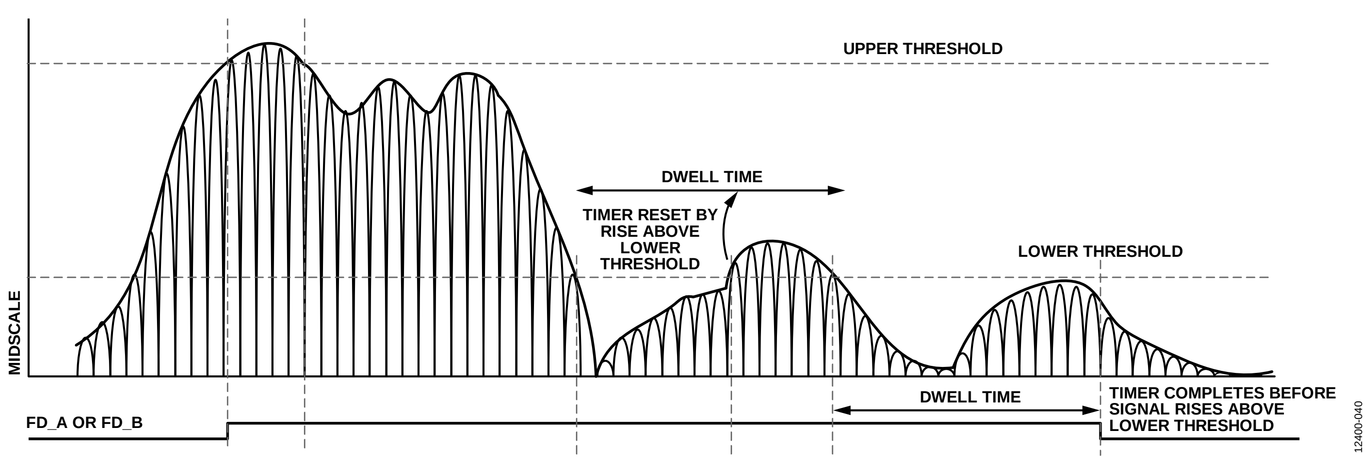

Figure 97. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 98 shows the simplified block diagram of the signal monitor block.

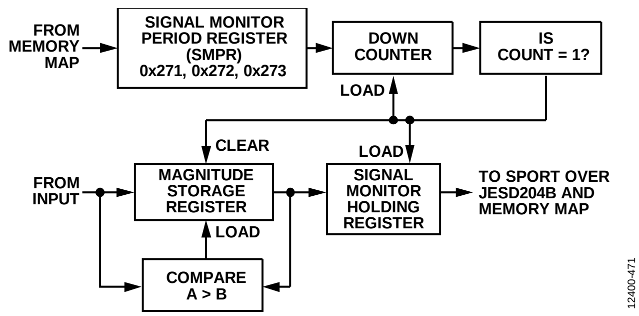

Figure 98. Signal Monitor Block

The peak detector captures the largest signal within the observation period. This period observes only the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude is derived by using the following equation:

$$\textit{Peak Magnitude}\ (\text{dBFS}) = 20 \log(\textit{Peak Detector Value}/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period that is determined by the signal monitor period registers (SMPRs). Only even values of the SMPR are supported. The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer that decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the serial port (SPORT) over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the internal magnitude storage register, and the comparison and update procedure, as explained previously, continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. This signal control monitor function is enabled by setting Bits[1:0] of Register 0x279 and Bit 1 of Register 0x27A.

Figure 99 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. There are a maximum of three control bits that can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Configuration 1 and Configuration 2 in Figure 99). To select the SPORT over JESD204B option, program Register 0x559, Register 0x55A, and Register 0x58F. See the Memory Map Register Table section for more information on setting these bits.

Figure 100 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 101 shows the SPORT over the JESD204B signal monitor frame data with a monitor period timer set to 80 samples.

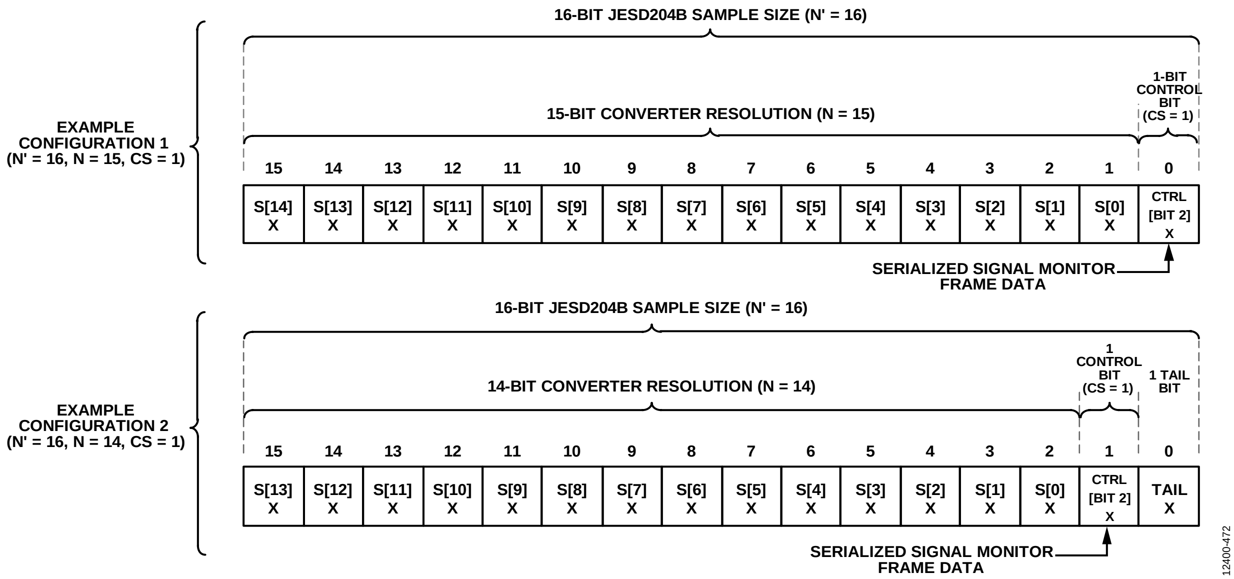

Figure 99. Signal Monitor Control Bit Example Configurations

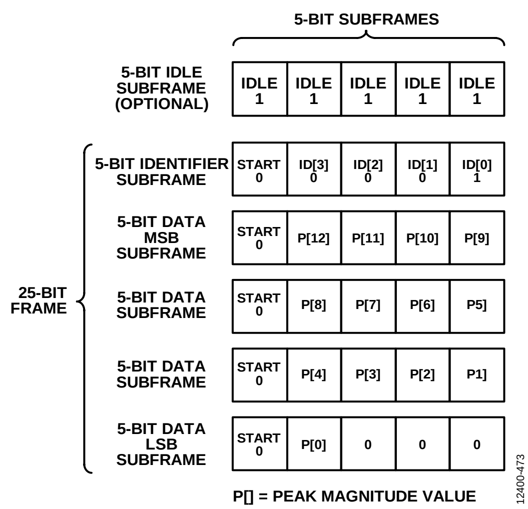

Figure 100. SPORT over JESD204B Signal Monitor Frame Data

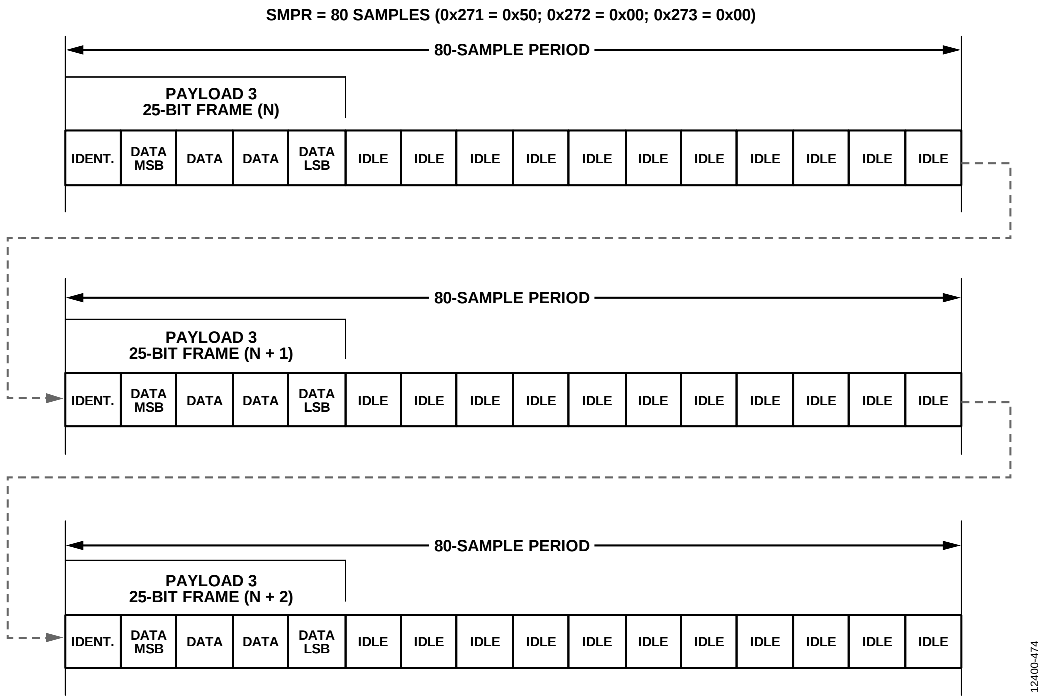

Figure 101. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

DIGITAL DOWNCONVERTER (DDC)

The AD6674 includes four digital downconverters (DDCs) that provide filtering and reduce the output data rate. This digital processing section includes an NCO, a half-band decimating filter, an FIR filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverter can be configured to output either real data or complex output data.

The DDCs output a 16-bit stream. To enable this operation, the converter number of bits, N, is set to a default value of 16, even though the analog core only outputs 14 bits. In full bandwidth operation, the ADC outputs are the 14-bit word followed by two zeros, unless the tail bits are enabled.

DDC I/Q INPUT SELECTION

The AD6674 has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real and complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x311, Register 0x331, Register 0x351, and Register 0x371). See Table 45 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real and complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit, Bit 3, in the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

The Chip Q ignore bit in the chip mode register (Register 0x200[5]) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 110.

DDC GENERAL DESCRIPTION

The four DDC blocks are used to extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a 12-bit complex NCO and quadrature mixers that can be used for frequency translation of both real and complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using a chain of up to four half-band low-pass filters for rate conversion. The decimation process lowers the output data rate, which in turn reduces the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, this stage compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real by performing an $f_S/4$ mixing operation plus a filter to remove the complex component of the signal.

Figure 102 shows the detailed block diagram of the DDCs implemented in the AD6674.

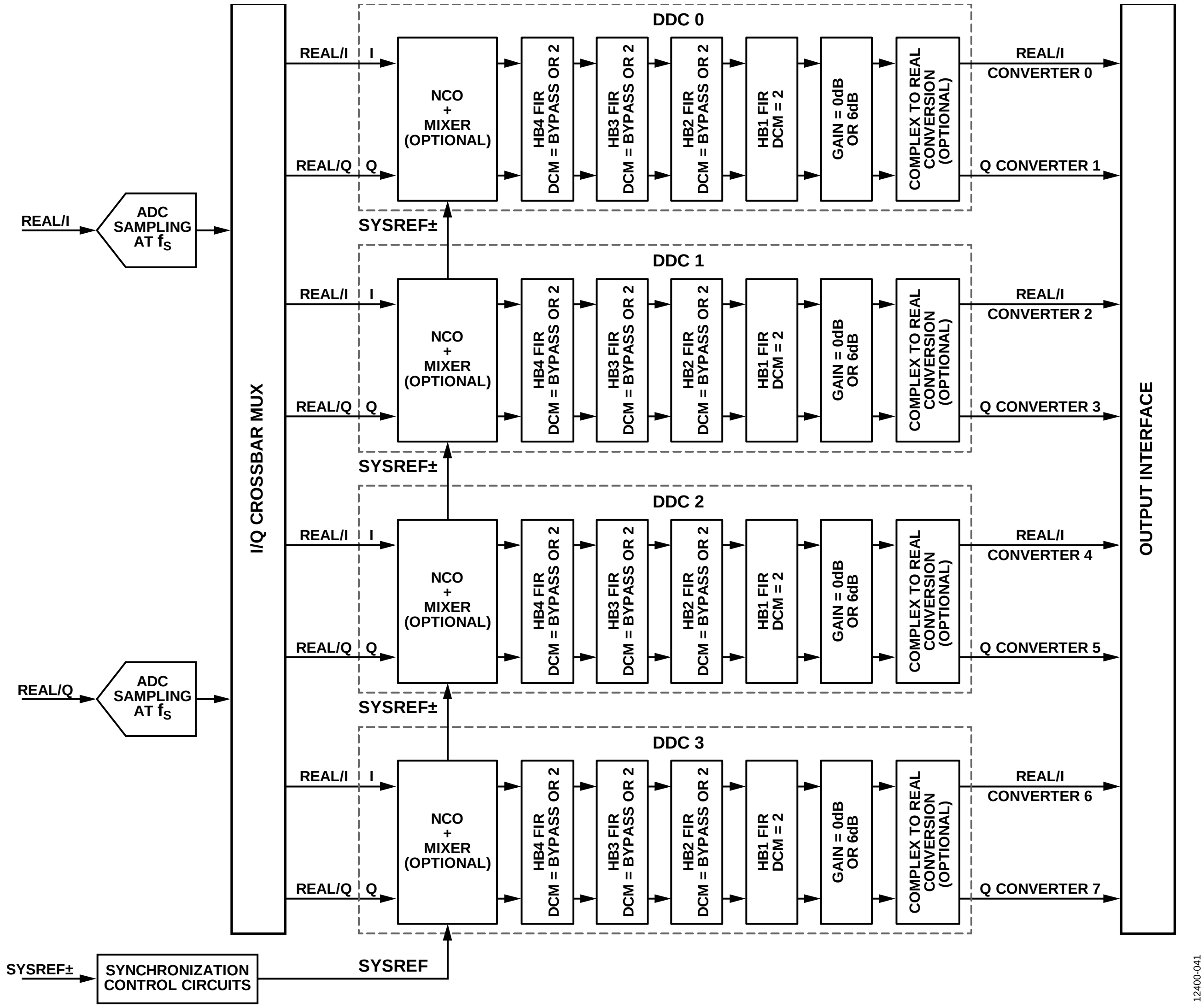

Figure 102. DDC Detailed Block Diagram

Figure 103 shows an example usage of one of the four DDC blocks with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1). It shows both complex (decimate by 16) and real (decimate by 8) output options.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio of all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

Table 11, Table 12, Table 13, Table 14, and Table 15 show the DDC samples when the chip decimation ratio is set to 1, 2, 4, 8, or 16, respectively. When DDCs have different decimation ratios, the chip decimation ratio must be set to the lowest decimation ratio of all the DDC channels. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate.

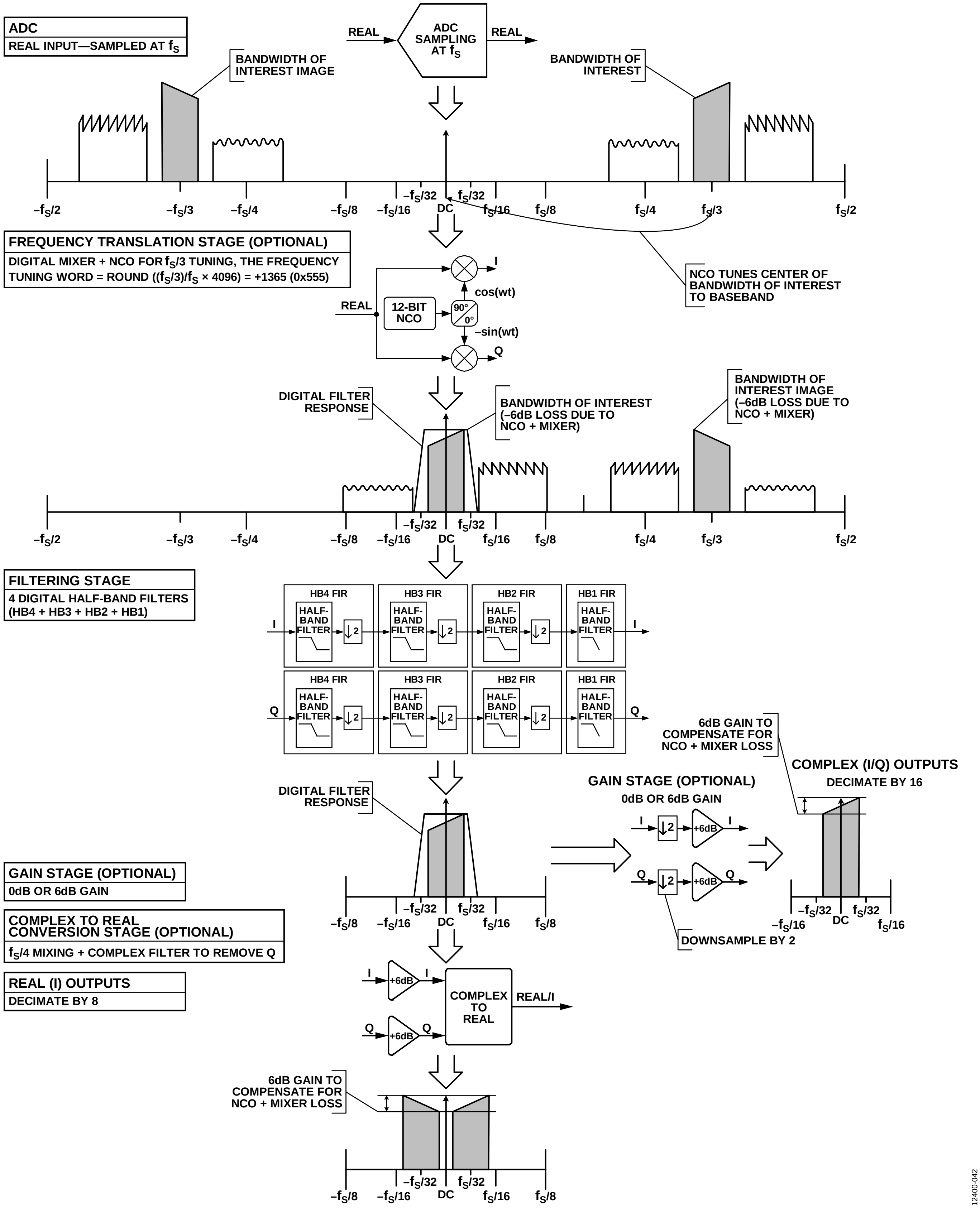

Figure 103. DDC Theory of Operation Example (Real Input, Decimate by 16)

Table 11. DDC Samples When Chip Decimation Ratio = 1

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N	N	N	N	N
N + 3	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 4	N + 2	N	N	N + 2	N	N	N
N + 5	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 6	N + 2	N	N	N + 2	N	N	N
N + 7	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 8	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 9	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 10	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 11	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 12	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 13	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 14	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 15	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 16	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 17	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 18	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 19	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 20	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 21	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 22	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 23	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 24	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 25	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 26	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 27	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 28	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 29	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1
N + 30	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 31	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM = decimation.

Table 12. DDC Samples When Chip Decimation Ratio = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N + 2	N	N	N
N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 4	N + 2	N	N + 4	N + 2	N	N
N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 6	N + 2	N	N + 6	N + 2	N	N
N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM = decimation.

Table 13. DDC Samples When Chip Decimation Ratio = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N + 2	N	N
N + 3	N + 1	N + 3	N + 1	N + 1
N + 4	N + 2	N + 4	N + 2	N
N + 5	N + 3	N + 5	N + 3	N + 1
N + 6	N + 2	N + 6	N + 2	N
N + 7	N + 3	N + 7	N + 3	N + 1

[1] DCM = decimation.

Table 14. DDC Samples When Chip Decimation Ratio = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N
N + 1	N + 1	N + 1
N + 2	N + 2	N
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2
N + 5	N + 5	N + 3
N + 6	N + 6	N + 2
N + 7	N + 7	N + 3

[1] DCM = decimation.

Table 15. DDC Samples When Chip Decimation Ratio = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

[1] DCM -= decimation.

For example, if the chip decimation ratio is set to decimate by 4, DDC 0 is set to use HB2 + HB1 filters (complex outputs, decimate by 4) and DDC 1 is set to use HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8). DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 16.

Table 16. DDC Output Samples When Chip DCM[1] = 4, DDC 0 DCM[1] = 4 (Complex), and DDC 1 DCM[1] = 8 (Real)

	DDC 0		DDC 1	
DDC Input Samples	**Output Port I**	**Output Port Q**	**Output Port I**	**Output Port Q**
N	I0 (N)	Q0 (N)	I1 (N)	Not applicable
N + 1				
N + 2				
N + 3				
N + 4	I0 (N + 1)	Q0 (N + 1)		
N + 5				
N + 6				
N + 7				
N + 8	I0 (N + 2)	Q0 (N + 2)	I1 (N + 1)	Not applicable
N + 9				
N + 10				
N + 11				
N + 12	I0 (N + 3)	Q0 (N + 3)		
N + 13				
N + 14				
N + 15				

[1] DCM = decimation.

FREQUENCY TRANSLATION

GENERAL DESCRIPTION

Frequency translation is accomplished by using a 12-bit complex NCO with a digital quadrature mixer. This stage translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370). These IF modes are

- Variable IF mode
- 0 Hz IF or zero IF (ZIF) mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

NCO and mixers are enabled. NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

The mixers are bypassed, and the NCO is disabled.

$f_S/4$ Hz IF Mode

The mixers and the NCO are enabled in special downmixing by $f_S/4$ mode to save power.

Test Mode

Input samples are forced to 0.999 to positive full scale. The NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters.

Figure 104 and Figure 105 show examples of the frequency translation stage for both real and complex inputs.

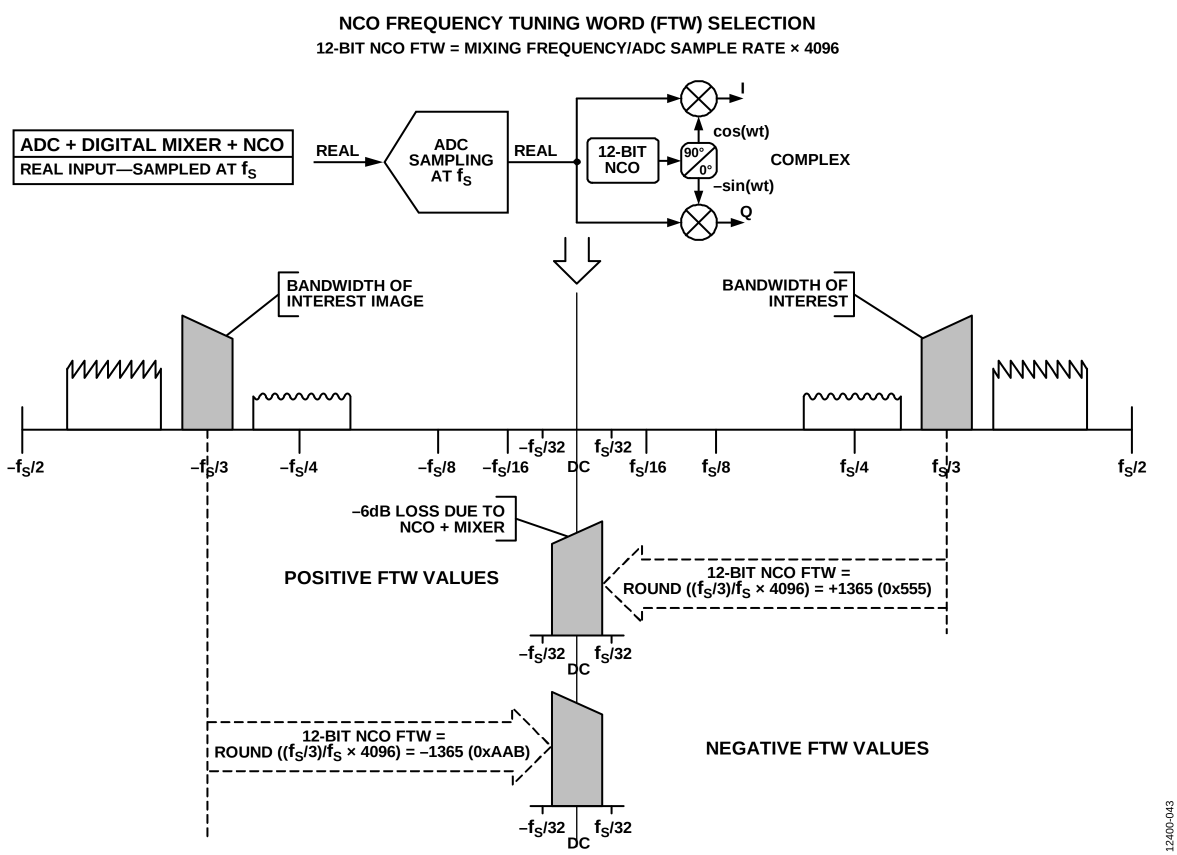

Figure 104. DDC NCO Frequency Tuning Word Selection—Real Inputs

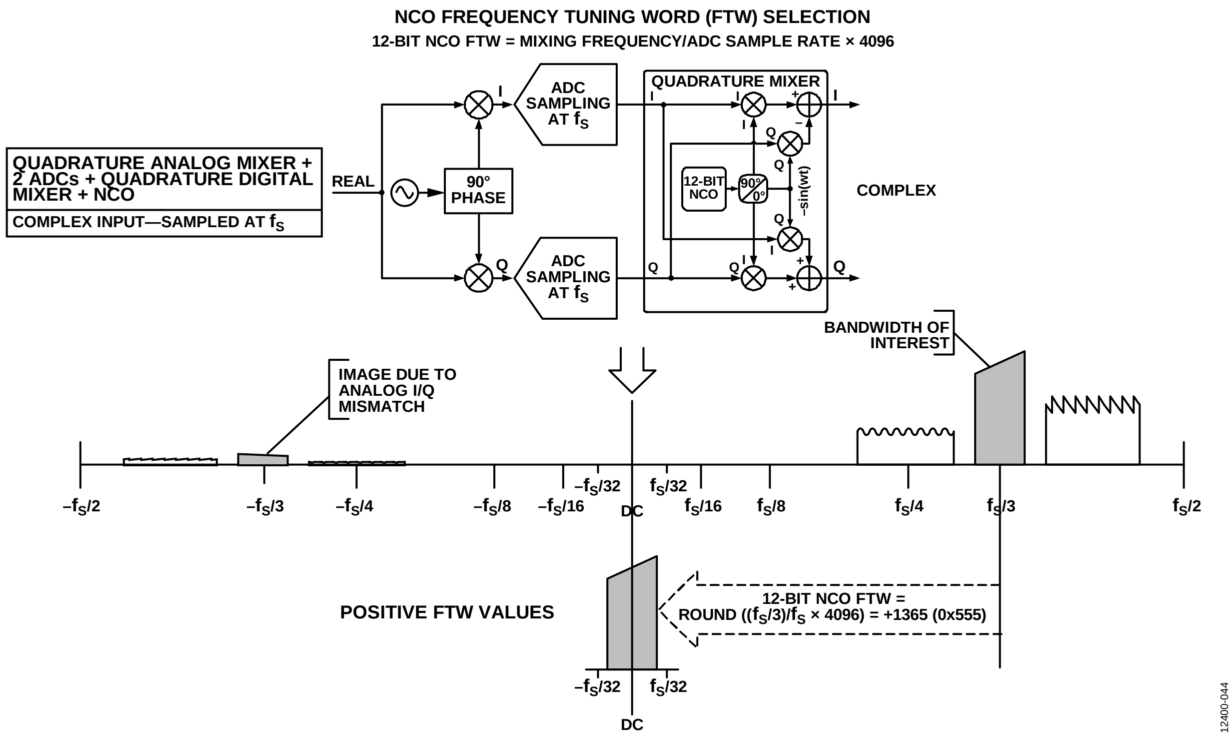

Figure 105. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO + MIXER LOSS AND SFDR

When mixing a real input signal down to baseband, 6 dB of loss is introduced in the signal due to filtering of the negative image. An additional 0.05 dB of loss is introduced by the NCO. The total loss of a real input signal mixed down to baseband is 6.05 dB. For this reason, it is recommended that the user compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the maximum value each I/Q sample can reach is 1.414 × full scale after it passes through the complex mixer. To avoid overrange of the I/Q samples and to keep the data bit-widths aligned with real mixing, 3.06 dB of loss is introduced in the mixer for complex signals. An additional 0.05 dB of loss is introduced by the NCO. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

NUMERICALLY CONTROLLED OSCILLATOR

The AD6674 has a 12-bit NCO for each DDC that enables the frequency translation process. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The NCO can be set up by providing a frequency tuning word (FTW) and a phase offset word (POW).

Setting Up the NCO FTW and POW

The NCO frequency value is given by the 12-bit twos complement number entered in the NCO FTW. Frequencies between $-f_S/2$ and $+f_S/2$ ($f_S/2$ excluded) are represented using the following frequency words:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents dc (frequency is 0 Hz).
- 0x7FF represents a frequency of $+f_S/2 - f_S/2^{12}$.

The NCO frequency tuning word can be calculated using the following equation:

$$NCO\_FTW = \text{round}\left(2^{12}\frac{\text{mod}(f_C, f_S)}{f_S}\right)$$

where:
NCO_FTW is a 12-bit twos complement number representing the NCO FTW.
f_C is the desired carrier frequency in Hz.
f_S is the AD6674 sampling frequency (clock rate) in Hz.
mod( ) is a remainder function. For example, mod(110,100) = 10 and for negative numbers, mod(−32,10) = −2.
round( ) is a rounding function. For example, round(3.6) = 4 and for negative numbers, round(−3.4) = −3.

Note that this equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

For example, if the ADC sampling frequency (f_S) is 500 MSPS and the carrier frequency (f_C) is 140.312 MHz, then

$$NCO\_FTW =$$

$$\text{round}\left(2^{12}\frac{\text{mod}(140.312,500)}{500}\right) = 1149 \text{ MHz}$$

This, in turn, converts to 0x47D in the 12-bit twos complement representation for NCO_FTW. The actual carrier frequency, f_{C_ACTUAL}, is calculated based on the following equation:

$$f_{C\_ACTUAL} = \frac{NCO\_FTW \times f_S}{2^{12}} = 140.26 \text{ MHz}$$

A 12-bit POW is available for each NCO to create a known phase relationship between multiple AD6674 chips or individual DDC channels inside one AD6674 chip.

The following procedure must be followed to update the FTW and/or POW registers to ensure proper operation of the NCO:

1. Write to the FTW registers for all the DDCs.
2. Write to the POW registers for all the DDCs.
3. Synchronize the NCOs either through the DDC NCO soft reset bit (Register 0x300[4]) accessible through the SPI or through the assertion of the SYSREF± pin.

It is important to note that the NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers have completed. This is necessary to ensure the proper operation of the NCO.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW. The phase increment value of each PAW is determined by the FTW See the Setting Up the NCO FTW and POW section for more information.

Use the following two methods to synchronize multiple PAWs within the chip.

- Using the SPI. Use the DDC NCO soft reset bit in the DDC synchronization control register (Register 0x300[4]) to reset all the PAWs in the chip. This is accomplished by setting the DDC NCO soft reset bit high and then setting this bit low. Note that this method can only be used to synchronize DDC channels within the same AD6674 chip.
- Using the SYSREF± pin. When the SYSREF± pin is enabled in the SYSREF± control registers (Register 0x120 and Register 0x121) and the DDC synchronization is enabled in the DDC synchronization control register (Register 0x300[1:0]), any subsequent SYSREF± event resets all the PAWs in the chip. Note that this method can be used to synchronize DDC channels within the same AD6674 chip or DDC channels within separate AD6674 chips.

Mixer

The NCO is accompanied by a mixer. Its operation is similar to an analog quadrature mixer. It performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, this mixer performs a real mixer operation (with two multipliers). For complex input signals, the mixer performs a complex mixer operation (with four multipliers and two adders). The mixer adjusts its operation based on the input signal (real or complex) provided to each individual channel. The selection of real or complex inputs can be controlled individually for each DDC block using Bit 7 of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

FIR FILTERS

GENERAL DESCRIPTION

There are four sets of decimate by 2, low-pass, half-band, finite impulse response (FIR) filters (labeled HB1 FIR, HB2 FIR, HB3 FIR, and HB4 FIR in Figure 102) following the frequency translation stage. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate, while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

HB1 FIR is always enabled and cannot be bypassed. The HB2, HB3, and HB4 FIR filters are optional and can be bypassed for higher output sample rates.

Table 17 shows the different bandwidths selectable by including different half-band filters. In all cases, the DDC filtering stage on the AD6674 provides <−0.001 dB of pass-band ripple and >100 dB of stop-band alias rejection.

Table 18 shows the amount of stop-band alias rejection for multiple pass-band ripple/cutoff points. The decimation ratio of the filtering stage of each DDC can be controlled individually through Bits[1:0] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

Table 17. DDC Filter Characteristics

ADC Sample Rate (MSPS)	Half Band Filter Selection	Real Output: Decimation Ratio	Real Output: Output Sample Rate (MSPS)	Complex (I/Q) Output: Decimation Ratio	Complex (I/Q) Output: Output Sample Rate (MSPS)	Alias Protected Bandwidth (MHz)	Ideal SNR Improvement[1] (dB)	Pass-Band Ripple (dB)	Alias Rejection (dB)
1000	HB1	1	1000	2	500 (I) + 500 (Q)	385.0	1	<−0.001	>100
	HB1 + HB2	2	500	4	250 (I) + 250 (Q)	192.5	4		
	HB1 + HB2 + HB3	4	250	8	125 (I) + 125 (Q)	96.3	7		
	HB1 + HB2 + HB3 + HB4	8	125	16	62.5 (I) + 62.5 (Q)	48.1	10		
750	HB1	1	750	2	375 (I) + 375 (Q)	288.8	1		
	HB1 + HB2	2	375	4	187.5 (I) + 187.5 (Q)	144.4	4		
	HB1 + HB2 + HB3	4	187.5	8	93.75 (I) + 93.75 (Q)	72.2	7		
	HB1 + HB2 + HB3 + HB4	8	93.75	16	46.875 (I) + 46.875 (Q)	36.1	10		
500	HB1	1	500	2	250 (I) + 250 (Q)	192.5	1		
	HB1 + HB2	2	250	4	125 (I) + 125 (Q)	96.3	4		
	HB1 + HB2 + HB3	4	125	8	62.5 (I) + 62.5 (Q)	48.1	7		
	HB1 + HB2 + HB3 + HB4	8	62.5	16	31.25 (I) + 31.25 (Q)	24.1	10		

[1] Ideal SNR improvement due to oversampling and filtering = 10log(bandwidth/(f_S/2)).

Table 18. DDC Filter Alias Rejection

Alias Rejection (dB)	Pass-Band Ripple/Cutoff Point (dB)	Alias Protected Bandwidth for Real (I) Outputs[1]	Alias Protected Bandwidth for Complex (I/Q) Outputs
>100	<−0.001	<38.5% × f_{OUT}	<77% × f_{OUT}
90	<−0.001	<38.7% × f_{OUT}	<77.4% × f_{OUT}
85	<−0.001	<38.9% × f_{OUT}	<77.8% × f_{OUT}
63.3	<−0.006	<40% × f_{OUT}	<80% × f_{OUT}
25	−0.5	44.4% × f_{OUT}	88.8% × f_{OUT}
19.3	−1.0	45.6% × f_{OUT}	91.2% × f_{OUT}
10.7	−3.0	48% × f_{OUT}	96% × f_{OUT}

[1] *f_{OUT} = ADC input sample rate ÷ DDC decimation.*

HALF-BAND FILTERS

The AD6674 offers four half-band filters to enable digital signal processing of the ADC converted data. These half-band filters are bypassable and can be individually selected.

HB4 Filter

The first decimate by 2, half-band, low-pass, FIR filter (HB4) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB4 filter is only used when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, it is bypassed. Table 19 and Figure 106 show the coefficients and response of the HB4 filter.

Table 19. HB4 Filter Coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	−0.049316	−808
C4, C8	0	0
C5, C7	0.293273	4805
C6	0.500000	8192

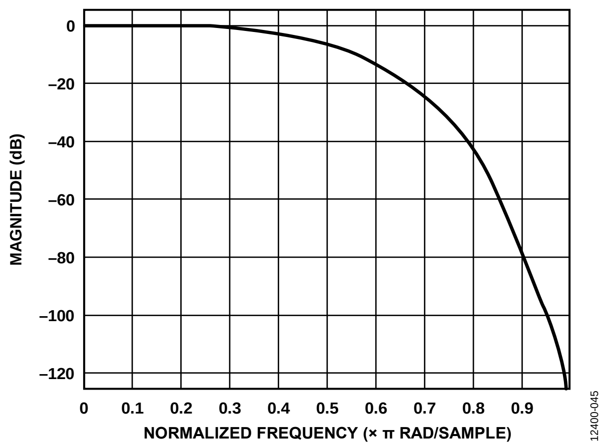

Figure 106. HB4 Filter Response

HB3 Filter

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, it is bypassed. Table 20 and Figure 107 show the coefficients and response of the HB3 filter.

Table 20. HB3 Filter Coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C11	0.006554	859
C2, C10	0	0
C3, C9	−0.050819	−6661
C4, C8	0	0
C5, C7	0.294266	38,570
C6	0.500000	65,536

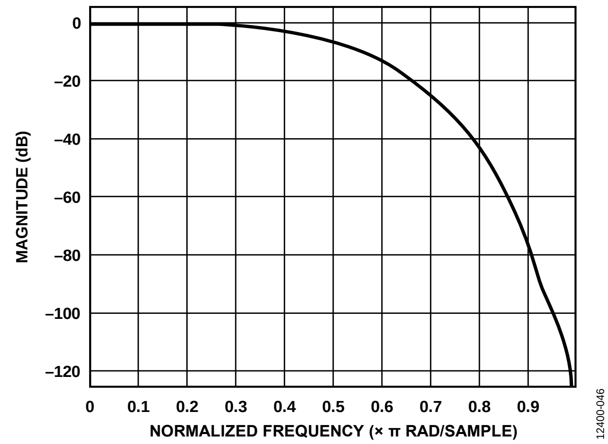

Figure 107. HB3 Filter Response

HB2 Filter

The third decimate by 2, half-band, low-pass, FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB2 filter is only used when complex or real outputs (decimate by 4, 8, or 16) is enabled; otherwise, it is bypassed.

Table 21 and Figure 108 show the coefficients and response of the HB2 filter.

Table 21. HB2 Filter Coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (19-Bit)
C1, C19	0.000614	161
C2, C18	0	0
C3, C17	−0.005066	−1328
C4, C16	0	0
C5, C15	0.022179	5814
C6, C14	0	0
C7, C13	−0.073517	−19,272
C8, C12	0	0
C9, C11	0.305786	80,160
C10	0.500000	131,072

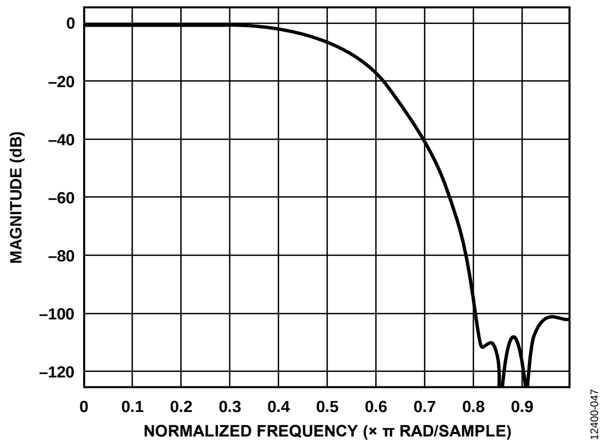

Figure 108. HB2 Filter Response

HB1 Filter

The fourth and final decimate by 2, half-band, low-pass, FIR filter (HB1) uses a 55-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 22 and Figure 109 show the coefficients and response of the HB1 filter.

Table 22. HB1 Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C1, C55	−0.000023	−24
C2, C54	0	0
C3, C53	0.000097	102
C4, C52	0	0
C5, C51	−0.000288	−302
C6, C50	0	0
C7, C49	0.000696	730
C8, C48	0	0
C9, C47	−0.0014725	−1544
C10, C46	0	0
C11, C45	0.002827	2964
C12, C44	0	0
C13, C43	−0.005039	−5284
C14, C42	0	0
C15, C41	0.008491	8903
C16, C40	0	0
C17, C39	−0.013717	−14,383
C18, C38	0	0
C19, C37	0.021591	22,640
C20, C36	0	0
C21, C35	−0.033833	−35,476
C22, C34	0	0
C23, C33	0.054806	57,468
C24, C32	0	0
C25, C31	−0.100557	−105,442
C26, C30	0	0
C27, C29	0.316421	331,792
C28	0.500000	524,288

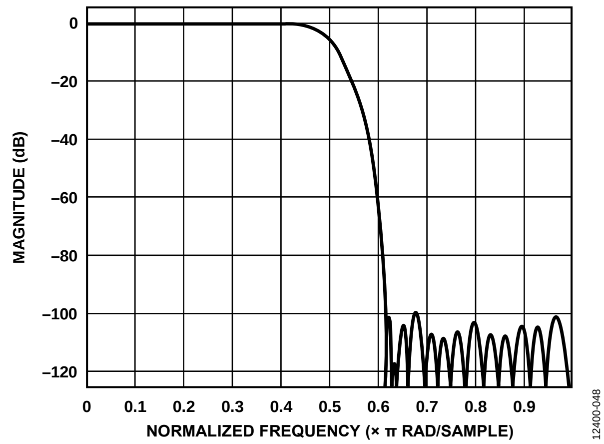

Figure 109. HB1 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits, and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage.

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage along with an $f_S/4$ complex mixer to upconvert the signal. After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 110 shows a simplified block diagram of the complex to real conversion.

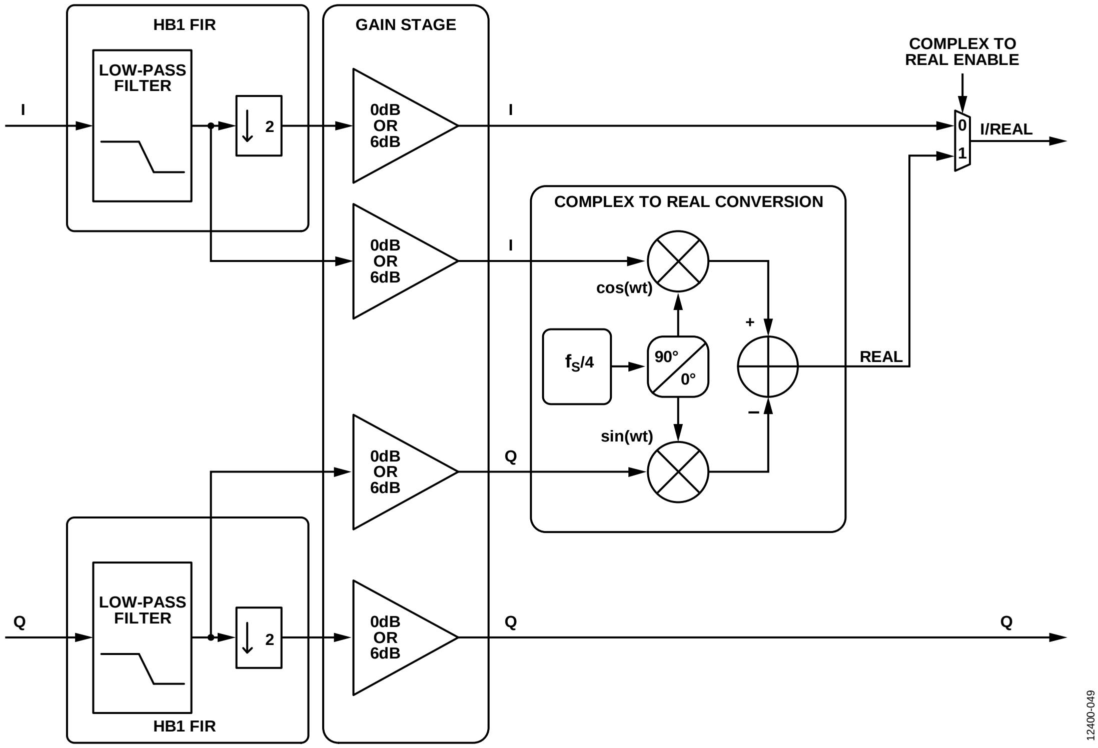

Figure 110. Complex to Real Conversion Block

DDC EXAMPLE CONFIGURATIONS

Table 23 describes the register settings for multiple DDC example configurations.

Table 23. DDC Example Configurations

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
One DDC	2	Complex	Complex	38.5% × f_S	2	0x200 = 0x01 (one DDC; I/Q selected) 0x201 = 0x01 (chip decimate by 2) 0x310 = 0x83 (complex mixer; 0 dB gain; variable IF; complex outputs; HB1 filter) 0x311 = 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0
One DDC	4	Complex	Complex	19.25% × f_S	2	0x200 = 0x01 (one DDC; I/Q selected) 0x201 = 0x02 (chip decimate by 4) 0x310= 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2 + HB1 filters) 0x311= 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) 0x314, 0x315= FTW and POW set as required by application for DDC 0

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Two DDCs	2	Real	Real	19.25%× f_S	2	0x200 = 0x22 (two DDCs; I only selected) 0x201 = 0x01 (chip decimate by 2) 0x310, 0x330 = 0x48 (real mixer; 6 dB gain; variable IF; real output; HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	2	Complex	Complex	38.5%× f_S	4	0x200 = 0x22 (two DDCs; I only selected) 0x201 = 0x01 (chip decimate by 2) 0x310, 0x330 = 0x4B (complex mixer; 6 dB gain; variable IF; complex output; HB1 filter) 0x311, 0x331 = 0x04 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Complex	19.25% × f_S	4	0x200 = 0x02 (two DDCs; I/Q selected) 0x201 = 0x02 (chip decimate by 4) 0x310, 0x330 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2 + HB1 filters) 0x311, 0x331 = 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Real	9.63% × f_S	2	0x200 = 0x22 (two DDCs; I only selected) 0x201 = 0x02 (chip decimate by 4) 0x310, 0x330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x311, 0x331 = 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Real	9.63% × f_S	2	0x200 = 0x22 (two DDCs; I only selected) 0x201 = 0x02 (chip decimate by 4) 0x310, 0x330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Two DDCs	4	Real	Complex	19.25% × f_S	4	0x200 = 0x02 (two DDCs; I/Q selected) 0x201 = 0x02 (chip decimate by 4) 0x310, 0x330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	8	Real	Real	4.81% × f_S	2	0x200 = 0x22 (two DDCs; I only selected) 0x201 = 0x03 (chip decimate by 8) 0x310, 0x330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x05 (DDC 1 I input = ADC Channel B; DDC 1 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1
Four DDCs	8	Real	Complex	9.63% × f_S	8	0x200 = 0x03 (four DDCs; I/Q selected) 0x201 = 0x03 (chip decimate by 8) 0x310, 0x330, 0x350, 0x370 = 0x41 (real mixer; 6 dB gain; variable IF; complex output; HB3 + HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) 0x351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) 0x371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1 0x354, 0x355, 0x360, 0x361 = FTW and POW set as required by application for DDC 2 0x374, 0x375, 0x380, 0x381 = FTW and POW set as required by application for DDC 3

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Four DDCs	8	Real	Real	4.81% × f_S	4	0x200 = 0x23 (four DDCs; I only selected) 0x201 = 0x03 (chip decimate by 8) 0x310, 0x330, 0x350, 0x370 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) 0x351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) 0x371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 0x334, 0x335, 0x340, 0x341 = FTW and POW set as required by application for DDC 1 0x354, 0x355, 0x360, 0x361 = FTW and POW set as required by application for DDC 2 0x374, 0x375, 0x380, 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	16	Real	Complex	4.81% × f_S	8	0x200 = 0x03 (four DDCs; I/Q selected) 0x201 = 0x04 (chip decimate by 16) 0x310, 0x330, 0x350, 0x370 = 0x42 (real mixer; 6 dB gain; variable IF; complex output; HB4 + HB3 + HB2 + HB1 filters) 0x311 = 0x00 (DDC 0 I input = ADC Channel A; DDC 0 Q input = ADC Channel A) 0x331 = 0x00 (DDC 1 I input = ADC Channel A; DDC 1 Q input = ADC Channel A) 0x351 = 0x05 (DDC 2 I input = ADC Channel B; DDC 2 Q input = ADC Channel B) 0x371 = 0x05 (DDC 3 I input = ADC Channel B; DDC 3 Q input = ADC Channel B) 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0. 0x334, 0x335, 0x040, 0x341 = FTW and POW set as required by application for DDC 1 0x354, 0x355, 0x360, 0x361 = FTW and POW set as required by application for DDC 2 0x374, 0x375, 0x380, 0x381 = FTW and POW set as required by application for DDC 3

[1] f_S is the ADC sample rate. Bandwidths listed are <−0.001 dB of pass-band ripple and >100 dB of stop-band alias rejection.
[2] The NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers have completed. This is necessary to ensure the proper operation of the NCO. See the NCO Synchronization section for more information.

NOISE SHAPING REQUANTIZER (NSR)

When operating the AD6674 with the NSR enabled, a decimating half-band filter that is optimized at certain input frequency bands can also be enabled. This filter offers the user the flexibility in signal bandwidth process and image rejection. Careful frequency planning can offer advantages in analog filtering preceding the ADC. The filter can function either in high-pass or low-pass mode. On the AD6674-750 and AD6674-1000, this filter is nonbypassable when the NSR is enabled. The filter can be optionally enabled on the AD6674-500 when the NSR is enabled. When operating with NSR enabled, the decimating half-band filter mode (low pass or high pass) is selected by setting Bit 7 in Register 0x41E.

DECIMATING HALF-BAND FILTER

The AD6674 decimating half-band filter reduces the input sample rate by a factor of 2 while rejecting aliases that fall into the band of interest. For an input sample clock of 1000 MHz, this reduces the output sample rate to 500 MSPS. This filter is designed to provide >40 dB of alias protection for 39.5% of the output sample rate (79% of the Nyquist band). For an ADC sample rate of 1000 MSPS, the filter provides a maximum usable bandwidth of 197.5 MHz.

Half-Band Filter Coefficients

The 19-tap, symmetrical, fixed coefficient half-band filter has low power consumption due to its polyphase implementation. Table 24 lists the coefficients of the half-band filter in low-pass mode. In high-pass mode, Coefficient C9 is multiplied by −1. The normalized coefficients used in the implementation and the decimal equivalent values of the coefficients are listed. Coefficients not listed in Table 24 are 0s.

Table 24. Fixed Coefficients for Half-Band Filter

Coefficient Number	Normalized Coefficient	Decimal Coefficient (12-Bit)
0	0.012207	25
C2, C16	−0.022949	−47
C4, C14	0.045410	93
C6, C12	−0.094726	−194
C8, C10	0.314453	644
C9	0.500000	1024

Half-Band Filter Features

The half-band decimating filter is designed to provide approximately 39.5% of the output sample rate in usable bandwidth (19.75% of the input sample clock). The filter provides >40 dB of rejection. The response of the half-band filter in low-pass mode is shown in Figure 111 for an input sample clock of 1000 MHz. In low-pass mode, operation is allowed in the first Nyquist zone, which includes frequencies of up to $f_S/2$, where f_S is the decimated sample rate. For example, with an input clock of 1000 MHz, the output sample rate is 500 MSPS and $f_S/2$ = 250 MHz.

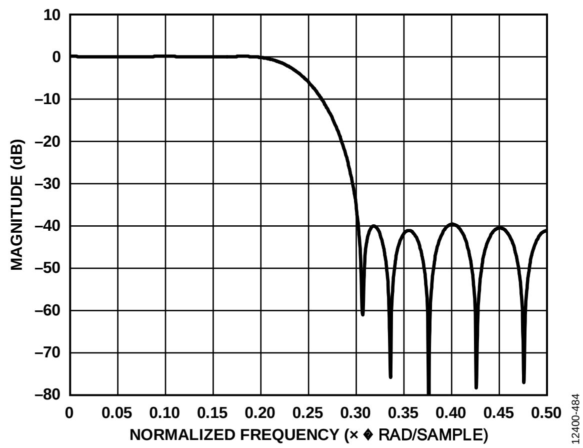

Figure 111. Low-Pass Half-Band Filter Response

The half-band filter can also be utilized in high-pass mode. The usable bandwidth remains at 39.5% of the output sample rate (19.75% of the input sample clock), which is the same as in low-pass mode). Figure 112 shows the response of the half-band filter in high-pass mode with an input sample clock of 1000 MHz. In high-pass mode, operation is allowed in the second and third Nyquist zones, which includes frequencies from $f_S/2$ to 3 $f_S/2$, where f_S is the decimated sample rate. For example, with an input clock of 1000 MHz, the output sample rate is 500 MSPS, $f_S/2$ = 250 MHz, and 3 $f_S/2$ = 750 MHz.

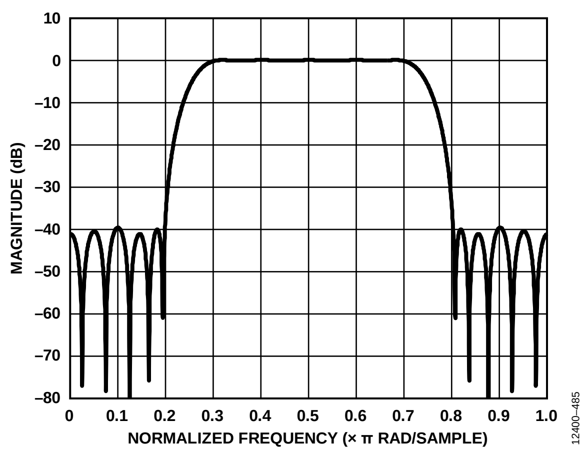

Figure 112. High-Pass Half-Band Filter Response

NSR OVERVIEW

The AD6674 features an NSR to allow higher than 9-bit SNR to be maintained in a subset of the Nyquist band. The harmonic performance of the receiver is unaffected by the NSR feature. When enabled, the NSR contributes an additional 3.0 dB of loss to the input signal, such that a 0 dBFS input is reduced to −3.0 dBFS at the output pins. This loss does not degrade the SNR performance of the AD6674.

The NSR feature can be independently controlled per channel via the SPI.

Two different bandwidth modes are provided; select the mode from the SPI port. In each of the two modes, the center frequency of the band can be tuned such that IFs can be placed anywhere in the Nyquist band. The NSR feature is enabled by default on the AD6674. The bandwidth and mode of the NSR operation are selected by setting the appropriate bits in Register 0x420 and Register 0x422. By selecting the appropriate profile and mode bits in these two registers, the NSR feature can be enabled for the desired mode of operation.

21% BW Mode (>75 MHz at 375 MSPS)

The first NSR mode offers excellent noise performance across a bandwidth that is 21% of the ADC output sample rate (42% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR mode register (Address 0x420) to 000. In this mode, set the useful frequency range using the 6-bit tuning word in the NSR tuning register (Address 0x422). There are 59 possible tuning words (TW), from 0 to 58; each step is 0.5% of the ADC sample rate.

$$f_0 = f_{ADC} \times 0.005 \times TW$$

where:
f_0 is the left band edge.
f_{ADC} is the ADC sample rate.
TW is the tuning word.

$$f_{CENTER} = f_0 + 0.105 \times f_{ADC}$$

where f_{CENTER} is the channel center.

$$f_1 = f_0 + 0.21 \times f_{ADC}$$

where f_1 is the right band edge.

Figure 113 to Figure 115 show the typical spectrum that can be expected from the AD6674 in the 21% BW mode for three different tuning words.

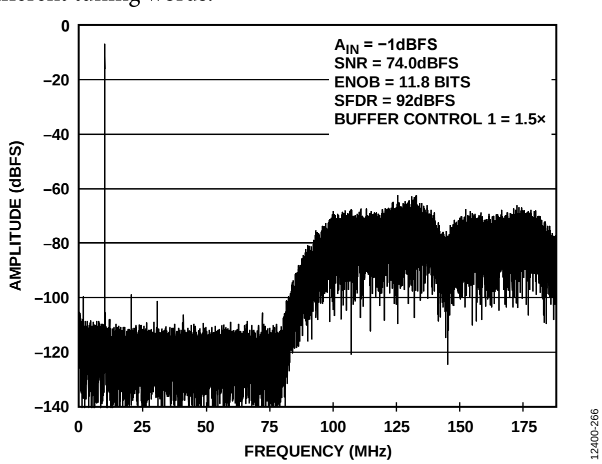

Figure 113. AD6674-750, f_{CLOCK} = 750 MHz, f_S = 375 MSPS, f_{IN} = 10.3 MHz, 21% BW Mode, Tuning Word = 0

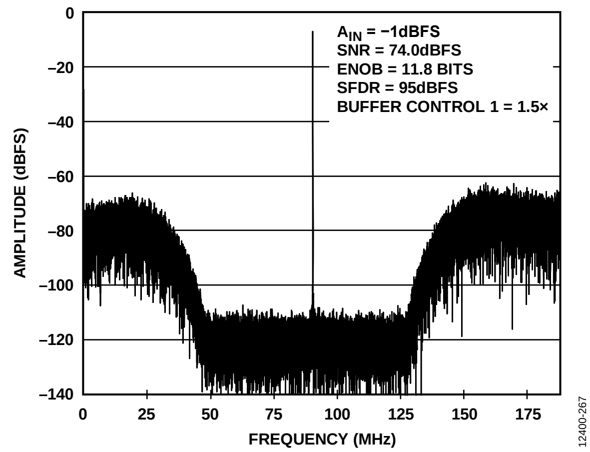

Figure 114. AD6674-750, f_{CLOCK} = 750 MHz, f_S = 375 MSPS, f_{IN} = 90.3 MHz, 21% BW Mode, Tuning Word = 26 (f_S/4 Tuning)

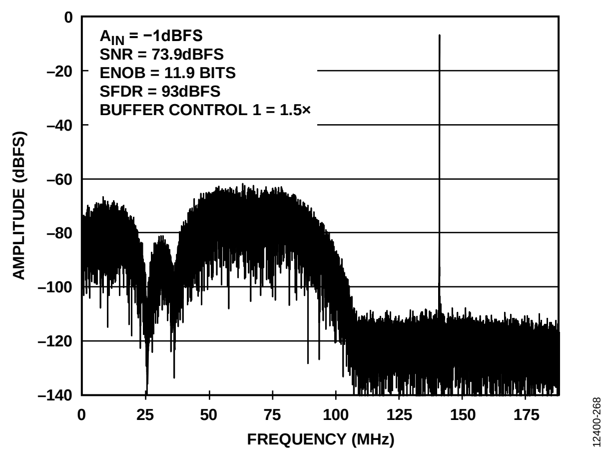

Figure 115. AD6674-750, f_{CLOCK} = 750 MHz, f_S = 375 MSPS, f_{IN} = 140.3 MHz, 21% BW Mode, Tuning Word = 58

28% BW Mode (>100 MHz at 375 MSPS)

The second NSR mode offers excellent noise performance across a bandwidth that is 28% of the ADC output sample rate (56% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR mode register (Address 0x420) to 001. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x422). There are 44 possible tuning words (TW, from 0 to 43); each step is 0.5% of the ADC sample rate.

$$f_0 = f_{ADC} \times 0.005 \times TW$$

where:
f_0 is the left band edge.
f_{ADC} is the ADC sample rate.
TW is the tuning word.

$$f_{CENTER} = f_0 + 0.14 \times f_{ADC}$$

where f_{CENTER} is the channel center.

$$f_1 = f_0 + 0.28 \times f_{ADC}$$

where f_1 is the right band edge.

Figure 116 to Figure 118 show the typical spectrum that can be expected from the AD6674 in the 28% BW mode for three different tuning words.

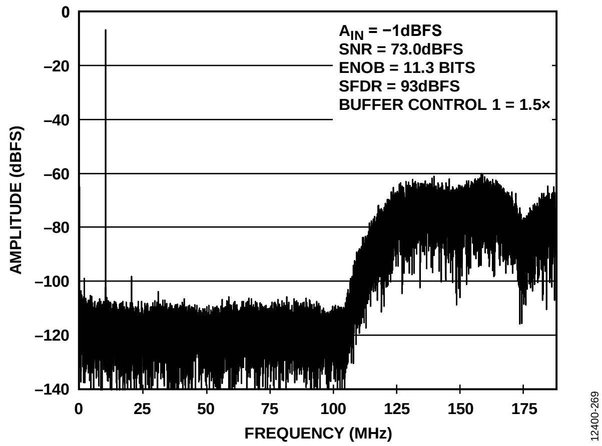

Figure 116. AD6674-750, f_{CLOCK} = 750 MHz, f_S = 375 MSPS, f_{IN} = 10.3 MHz, 28% BW Mode, Tuning Word = 0

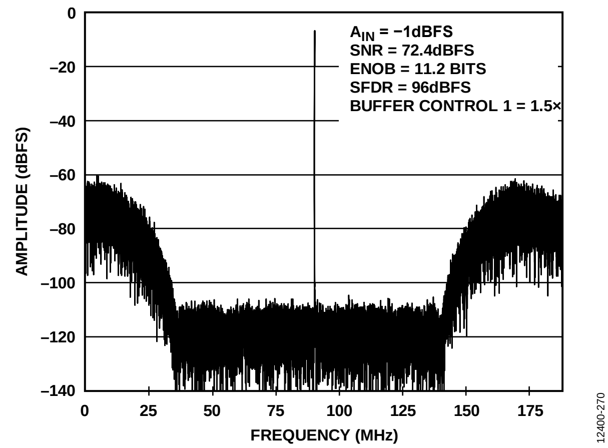

Figure 117. AD6674-750, f_{CLOCK} = 750 MHz, f_S = 375 MSPS, f_{IN} = 90.3 MHz, 28% BW Mode, Tuning Word = 19 (f_S/4 Tuning)

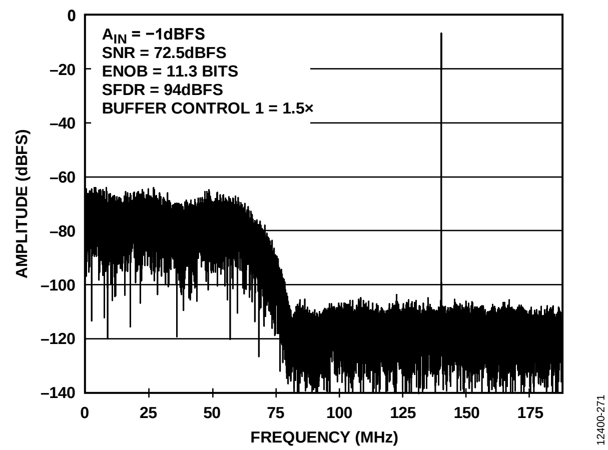

Figure 118. AD6674-750, f_{CLOCK} = 750 MHz, f_S = 375 MSPS, f_{IN} = 140.3 MHz, 28% BW Mode, Tuning Word = 43

VARIABLE DYNAMIC RANGE (VDR)

The AD6674 features a VDR digital processing block to allow up to a 14-bit dynamic range to be maintained in a subset of the Nyquist band. Across the full Nyquist band, a minimum 9-bit dynamic range is available at all times. This operation is suitable for applications such as DPD processing. The harmonic performance of the receiver is unaffected by this feature. When enabled, VDR does not contribute loss to the input signal but operates by effectively changing the output resolution at the output pins. This feature can be independently controlled per channel via the SPI.

The VDR block operates in either complex or real mode. In complex mode, VDR has selectable bandwidths of 25% and 43% of the output sample rate. In real mode, the bandwidth of operation is limited to 25% of the output sample rate. The bandwidth and mode of the VDR operation are selected by setting the appropriate bits in Register 0x430.

When the VDR block is enabled, input signals that violate a defined mask (signified by gray shaded areas in Figure 119) result in the reduction of the output resolution of the AD6674. The VDR block analyzes the peak value of the aggregate signal level in the disallowed zones to determine the reduction of the output resolution. To indicate that the AD6674 is reducing output, the resolution VDR punish bits and/or a VDR high/low resolution bit can optionally be inserted into the output data stream as control bits by programming the appropriate value into Register 0x559 and Register 0x55A. Up to two control bits can be used without the need to change the converter resolution parameter, N. Up to three control bits can be used, but if using three, the converter resolution parameter, N, must be changed to 13. The VDR high/low resolution bit can be programmed into either of the three available control bits and simply indicates if VDR is reducing output resolution (bit value is a 1), or if full resolution is available (bit value is a 0). Enable the two punish bits to give a clearer indication of the available resolution of the sample. To decode these two bits, see Table 25.

Table 25. VDR Reduced Output Resolution Values

VDR Punish Bits[1:0]	Output Resolution (Bits)
00	14
01	13
10	12 or 11
11	10 or 9

The frequency zones of the mask are defined by the bandwidth mode selected in Register 0x430. The upper amplitude limit for input signals located in these frequency zones is −30 dBFS. If the input signal level in the disallowed frequency zones goes above an amplitude level of −30 dBFS (into the gray shaded areas), the VDR block triggers a reduction in the output resolution, as shown in Figure 119. The VDR block engages and begins limiting output resolution gradually as the signal amplitudes increase in the mask regions. As the signal amplitude level increases into the mask regions, the output resolution is gradually lowered. For every 6 dB increase in signal level above −30 dBFS, one bit of output resolution is discarded from the output data by the VDR block, as shown in Table 26. These zones can be tuned within the Nyquist band by setting Bits[3:0] in Register 0x434 to determine the VDR center frequency (f_{VDR}). The VDR center frequency in complex mode can be adjusted from 1/16 f_S to 15/16 f_S in 1/16 f_S steps. In real mode, f_{VDR} can be adjusted from 1/8 f_S to 3/8 f_S in 1/16 f_S steps.

Table 26. VDR Reduced Output Resolution Values

Signal Amplitude Violating Defined VDR Mask	Output Resolution (Bits)
Amplitude ≤ −30 dBFS	14
−30 dBFS < amplitude ≤ −24 dBFS	13
−24 dBFS < amplitude ≤ −18 dBFS	12
−18 dBFS < amplitude ≤ −12 dBFS	11
−12 dBFS < amplitude ≤ −6 dBFS	10
−6 dBFS < amplitude ≤ 0 dBFS	9

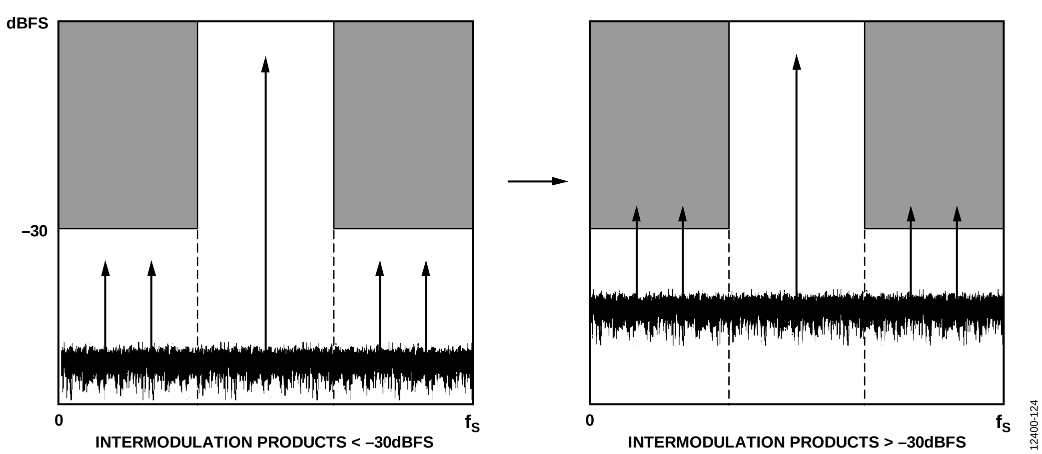

Figure 119. VDR Operation—Reduction in Output Resolution

VDR REAL MODE

The real mode of VDR works over a bandwidth of 25% of the sample rate (50% of the Nyquist band). The output bandwidth of the AD6674 can be 25% only when operating in real mode. Figure 120 shows the frequency zones for the 25% bandwidth real output VDR mode tuned to a center frequency (f_{VDR}) of f_S/4 (tuning word = 0x04). The frequency zones where the amplitude may not exceed −30 dBFS are the upper and lower portions of the Nyquist band signified by the red shaded areas.

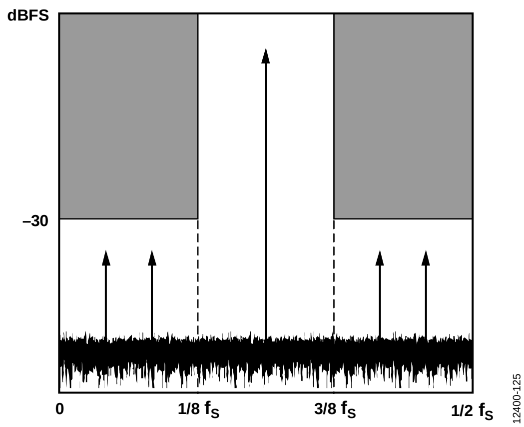

Figure 120. 25% VDR Bandwidth, Real Mode

The center frequency (f_{VDR}) of the VDR function can be tuned within the Nyquist band from 1/8 f_S to 3/8 f_S in 1/16 f_S steps. In real mode, Tuning Word 2 (0x02) through Tuning Word 6 (0x06) are valid. Table 27 shows the relative frequency values, and Table 28 shows the absolute frequency values based on a sample rate of 737.28 MSPS.

Table 27. VDR Tuning Words and Relative Frequency Values, 25% BW, Real Mode

Tuning Word	Lower Band Edge	Center Frequency	Upper Band Edge
2 (0x02)	0	1/8 f_S	1/4 f_S
3 (0x03)	1/16 f_S	3/16 f_S	5/16 f_S
4 (0x04)	1/8 f_S	1/4 f_S	3/8 f_S
5 (0x05)	3/16 f_S	5/16 f_S	7/16 f_S
6 (0x06)	1/4 f_S	3/8 f_S	1/2 f_S

Table 28. VDR Tuning Words and Absolute Frequency Values, 25% BW, Real Mode with f_S = 737.28 MSPS

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
2 (0x02)	0	92.16	184.32
3 (0x03)	46.08	138.24	230.40
4 (0x04)	92.16	184.32	276.48
5 (0x05)	138.24	230.40	322.56
6 (0x06)	184.32	276.48	368.64

VDR COMPLEX MODE

The complex mode of VDR works with selectable bandwidths of 25% of the sample rate (50% of the Nyquist band) and 43% of the sample rate (86% of the Nyquist band). Figure 121 and Figure 122 show the frequency zones for VDR in the complex mode. When operating VDR in complex mode, place I input signal data on Channel A and place Q input signal data on Channel B.

Figure 121 shows the frequency zones for the 25% bandwidth VDR mode with a center frequency of f_S/4 (tuning word = 0x04). The frequency zones where the amplitude may not exceed −30 dBFS are the upper and lower portions of the Nyquist band extending into the complex domain.

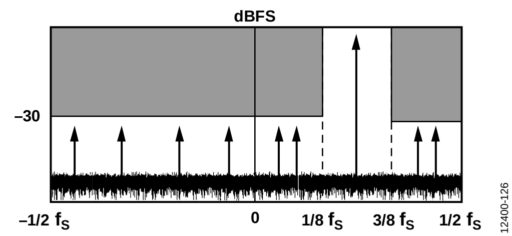

Figure 121. 25% VDR Bandwidth, Complex Mode

The center frequency (f_{VDR}) of the VDR function can be tuned within the Nyquist band from 0 to 15/16 f_S in 1/16 f_S steps. In complex mode, Tuning Word 0 (0x00) through Tuning Word 15 (0x0F) are valid. Table 29 and Table 30 show the tuning words and frequency values for the 25% complex mode. Table 29 shows the relative frequency values, and Table 30 shows the absolute frequency values based on a sample rate of 737.28 MSPS.

Table 29. VDR Tuning Words and Relative Frequency Values, 25% BW, Complex Mode

Tuning Word	Lower Band Edge	Center Frequency	Upper Band Edge
0 (0x00)	−1/8 f_S	0	1/8 f_S
1 (0x01)	−1/16 f_S	1/16 f_S	3/16 f_S
2 (0x02)	0	1/8 f_S	1/4 f_S
3 (0x03)	1/16 f_S	3/16 f_S	5/16 f_S
4 (0x04)	1/8 f_S	1/4 f_S	3/8 f_S
5 (0x05)	3/16 f_S	5/16 f_S	7/16 f_S
6 (0x06)	1/4 f_S	3/8 f_S	1/2 f_S
7 (0x07)	5/16 f_S	7/16 f_S	9/16 f_S
8 (0x08)	3/8 f_S	1/2 f_S	5/8 f_S
9 (0x09)	7/16 f_S	9/16 f_S	11/16 f_S
10 (0x0A)	1/2 f_S	5/8 f_S	3/4 f_S
11 (0x0B)	9/16 f_S	11/16 f_S	13/16 f_S
12 (0x0C)	5/8 f_S	3/4 f_S	7/8 f_S
13 (0x0D)	11/16 f_S	13/16 f_S	15/16 f_S
14 (0x0E)	3/4 f_S	7/8 f_S	f_S
15 (0x0F)	13/16 f_S	15/16 f_S	17/16 f_S

Table 30. VDR Tuning Words and Absolute Frequency Values, 25% BW, Complex Mode (f_S = 737.28 MSPS)

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
0 (0x00)	−92.16	0.00	92.16
1 (0x01)	−46.08	46.08	138.24
2 (0x02)	0.00	92.16	184.32
3 (0x03)	46.08	138.24	230.40
4 (0x04)	92.16	184.32	276.48
5 (0x05)	138.24	230.40	322.56
6 (0x06)	184.32	276.48	368.64
7 (0x07)	230.40	322.56	414.72
8 (0x08)	276.48	368.64	460.80
9 (0x09)	322.56	414.72	506.88
10 (0x0A)	368.64	460.80	552.96
11 (0x0B)	414.72	506.88	599.04
12 (0x0C)	460.80	552.96	645.12
13 (0x0D)	506.88	599.04	691.20
14 (0x0E)	552.96	645.12	737.28
15 (0x0F)	599.04	691.20	783.36

Table 31 and Table 32 show the tuning words and frequency values for the 43% complex mode. Table 31 shows the relative frequency values, and Table 32 shows the absolute frequency values based on a sample rate of 737.28 MSPS. Figure 122 shows the frequency zones for the 43% BW VDR mode with a center frequency (f_{VDR}) of f_S/4 (tuning word = 0x04). The frequency zones where the amplitude may not exceed −30 dBFS are the upper and lower portions of the Nyquist band extending into the complex domain.

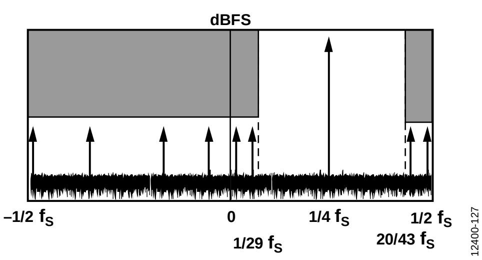

Figure 122. 43% VDR Bandwidth, Complex Mode

Table 31. VDR Tuning Words and Relative Frequency Values, 43% BW, Complex Mode

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
0 (0x00)	−14/65 f_S	0	14/65 f_S
1 (0x01)	−11/72 f_S	1/16 f_S	5/18 f_S
2 (0x02)	−1/11 f_S	1/8 f_S	16/47 f_S
3 (0x03)	−1/36 f_S	3/16 f_S	29/72 f_S
4 (0x04)	1/29 f_S	1/4 f_S	20/43 f_S
5 (0x05)	7/72 f_S	5/16 f_S	19/36 f_S
6 (0x06)	4/25 f_S	3/8 f_S	49/83 f_S
7 (0x07)	2/9 f_S	7/16 f_S	47/72 f_S
8 (0x08)	2/7 f_S	1/2 f_S	5/7 f_S
9 (0x09)	25/72 f_S	9/16 f_S	7/9 f_S
10 (0x0A)	34/83 f_S	5/8 f_S	21/25 f_S
11 (0x0B)	17/36 f_S	11/16 f_S	65/72 f_S
12 (0x0C)	23/43 f_S	3/4 f_S	28/29 f_S
13 (0x0D)	43/72 f_S	13/16 f_S	37/36 f_S
14 (0x0E)	31/47 f_S	7/8 f_S	12/11 f_S
15 (0x0F)	13/18 f_S	15/16 f_S	83/72 f_S

Table 32. VDR Tuning Words and Absolute Frequency Values, 43% BW, Complex Mode (f_S = 737.28 MSPS)

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
0 (0x00)	−158.80	0.00	158.80
1 (0x01)	−112.64	46.08	204.80
2 (0x02)	−67.03	92.16	250.99
3 (0x03)	−20.48	138.24	296.96
4 (0x04)	25.42	184.32	342.92
5 (0x05)	71.68	230.40	389.12
6 (0x06)	117.96	276.48	435.26
7 (0x07)	163.84	322.56	481.28
8 (0x08)	210.65	368.64	526.63
9 (0x09)	256.00	414.72	573.44
10 (0x0A)	302.02	460.80	619.32
11 (0x0B)	348.16	506.88	665.60
12 (0x0C)	394.36	552.96	711.86
13 (0x0D)	440.32	599.04	757.76
14 (0x0E)	486.29	645.12	804.31
15 (0x0F)	532.48	691.20	849.92

DIGITAL OUTPUTS

INTRODUCTION TO JESD204B INTERFACE

The AD6674 digital outputs are designed to the JEDEC Standard No. JESD204B serial interface for data converters. JESD204B is a protocol to link the AD6674 to a digital processing device over a serial interface with lane rates of up to 12.5 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and enabling smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8B/10B encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, users are encouraged to refer to the JESD204B standard.

The AD6674 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link and these parameters must match between the JESD204B transmitter (AD6674 output) and receiver (logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link) (AD6674 value = 1, 2, or 4)
- M is the number of converters per converter device (virtual converters per link) (AD6674 value = 1, 2, 4, or 8)
- F is the number of octets per frame (AD6674 value = 1, 2, 4, 8, or 16)
- N′ is the number of bits per sample (JESD204B word size) (AD6674 value = 8 or 16)
- N is the converter resolution (AD6674 value = 7 to 16)
- CS is the number of control bits per sample (AD6674 value = 0, 1, 2, or 3)
- K is the number of frames per multiframe (AD6674 value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S is the number of samples transmitted per single converter per frame cycle (AD6674 value = set automatically based on L, M, F, and N′)
- HD is high density mode (AD6674 = set automatically based on L, M, F, and N′)
- CF is the number of control words per frame clock cycle per converter device (AD6674 value = 0)

Figure 123 shows a simplified block diagram of the AD6674 JESD204B link. By default, the AD6674 is configured to use two converters and four lanes. Converter A data is output to SERDOUT0±/SERDOUT1±, and Converter B is output to SERDOUT2±/SERDOUT3±. The AD6674 allows other configurations such as combining the outputs of both converters onto a single lane or changing the mapping of the A and B digital output paths. These modes are set up through a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD6674, the 14-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number (PN) sequence. The tail bits can also be replaced with control bits indicating an overrange, SYSREF±, signal monitor output, VDR punish bits, or fast detect output. Control bits are filled and inserted MSB first, such that enabling CS = 1 activates Control Bit 2, enabling CS = 2 activates Control Bit 2 and Control Bit 1, and enabling CS = 3 activates Control Bit 2, Control Bit 1, and Control Bit 0.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver must be a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8B/10B encoder. The 8B/10B encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 124 shows how the 14-bit data is transferred from the ADC, the tail bits are added, the two octets are scrambled, and the octets are encoded into two 10-bit symbols. Figure 124 illustrates the default data format.

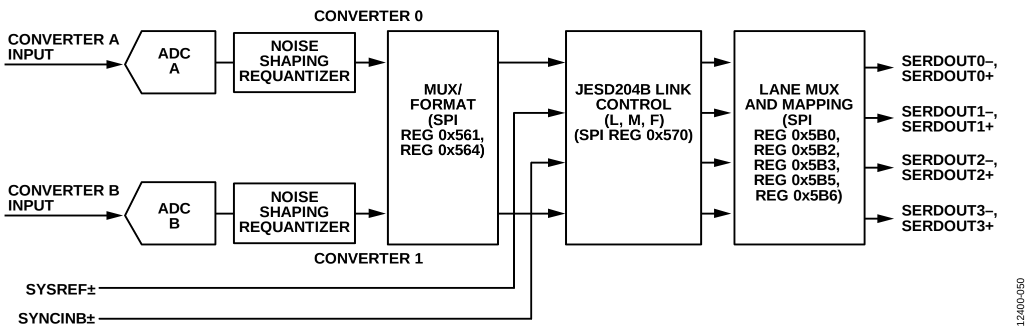

Figure 123. Transmit Link Simplified Block Diagram Showing NSR Mode (Register 0x200 = 0x07)

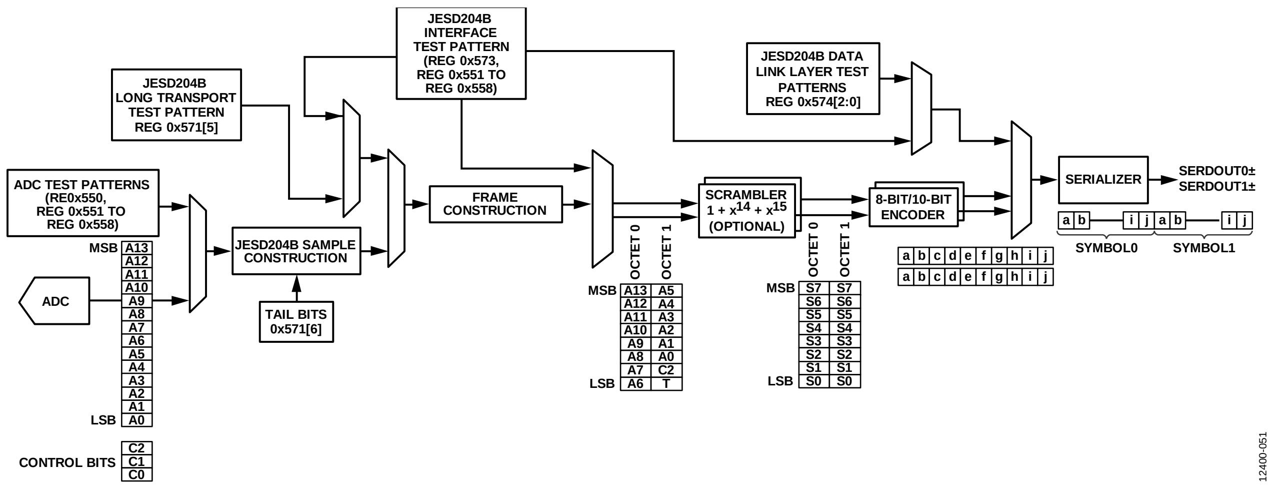

Figure 124. ADC Output Datapath Showing Data Framing

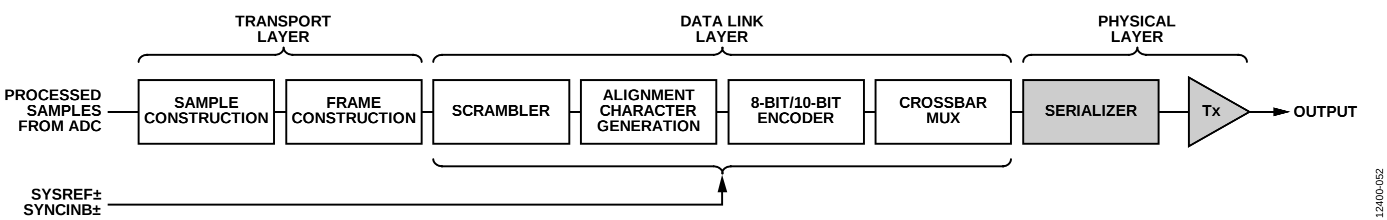

Figure 125. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 125 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open-source initiative (OSI) model that is widely used to describe the abstractions layers of communications systems. These are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer packs the data (consisting of samples and optional control bits) into JESD204B frames, which are mapped to 8-bit octets that are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. Use the following equation to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the ILAS, which contains the link configuration data, used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this section, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD6674 JESD204B Tx interface operates in Subclass 1 as defined in the JEDEC Standard No. 204B (July 2011) specification. The link establishment process is divided into the following steps: code group synchronization, ILAS, and user data.

Code Group Synchronization (CGS) and SYNCINB±

Code group synchronization (CGS) is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD6674 low. The JESD204B Tx begins sending /K/ characters. After the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD6674 then transmits an ILAS on the following LMFC boundary.

For more information on the CGS phase, refer to the JEDEC Standard No. 204B (July 2011), Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation, refer to Register 0x572. The SYNCINB± pin can also be configured to run in CMOS (single-ended) mode by setting Bit 4 in Register 0x572. When running SYNCINB± in CMOS mode, connect the CMOS SYNCINB signal to Pin 21 (SYNCINB+) and leave Pin 20 (SYNCINB−) floating.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 126. The four multiframes include the following:

- Multiframe 1: Begins with an /R/ character [K28.0] and ends with an /A/ character (K28.3).
- Multiframe 2: Begins with an /R/ character followed by a /Q/ (K28.4) character, followed by link configuration parameters over 14 configuration octets (see Table 33), and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3: Begins with an /R/ character (K28.0) and ends with an /A/ character (K28.3).
- Multiframe 4: Begins with an /R/ character (K28.0) and ends with an /A/ character (K28.3).

User Data and Error Detection

After the ILAS is complete, the user data is sent. Normally, in a frame all characters are user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default but can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/ and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B Rx checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames is equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion is enabled by default. For more information on the link controls, see Register 0x571 in the Memory Map section.

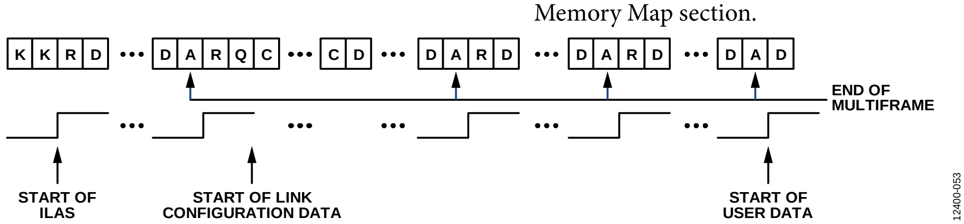

Figure 126. Initial Lane Alignment Sequence

Table 33. AD6674 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	K28.0	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	K28.3	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	K28.4	100 11100	001111 0010	110000 1101	Start of link configuration data
/K/	K28.5	101 11100	001111 1010	110000 0101	Group synchronization
/F/	K28.7	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD is running disparity.

8B/10B Encoder

The 8B/10B encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 33. The 8B/10B encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8B/10B interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are intended to be a troubleshooting tool for the verification of the digital front end (DFE). Refer to the Memory Map section, Register 0x572[2:1], for information on configuring the 8B/10B encoder.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing and Controls

The AD6674 physical layer consists of drivers that are defined in the JEDEC Standard No. 204B (July 2011). The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input, which results in a nominal 300 mV p-p swing at the receiver (see Figure 127). Alternatively, single-ended 50 Ω termination resistors can be used. When single-ended termination is used, the termination voltage is DRVDD/2; otherwise, 0.1 µF ac coupling capacitors can be used to terminate to any single-ended voltage.

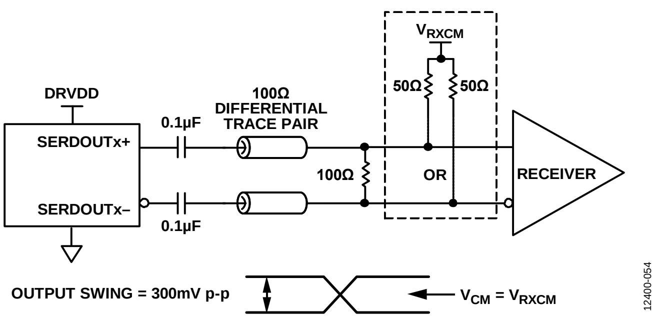

Figure 127. AC-Coupled Digital Output Termination Example

The AD6674 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible. The common mode of the digital output automatically biases itself to half the DRVDD supply of 1.2 V (V_{CM} = 0.6 V). See Figure 128 for an example of dc coupling the outputs to the receiver logic.

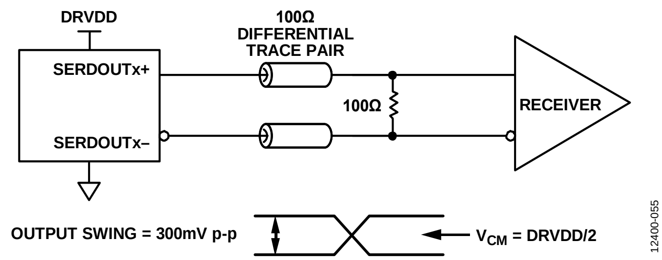

Figure 128. DC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 129 to Figure 131, Figure 132 to Figure 134, and Figure 135 to Figure 137 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one AD6674 lane running at 10 Gbps, 7.37 Gbps, and 6 Gbps, respectively. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x561 in Table 45).

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link may cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it may increase EMI. See the Memory Map section (Register 0x5C1 to Register 0x5C5 in Table 45) for more information.

PLL

The PLL is used to generate the serializer clock, which operates at the JESD204B lane rate. The JESD204B lane rate control bit (Register 0x56E[4]) must be set to correspond with the lane rate.

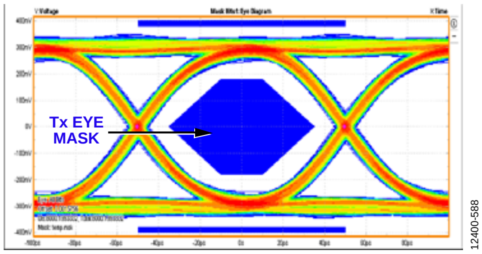

Figure 129. Digital Output Data Eye, External 100 Ω Terminations at 10 Gbps

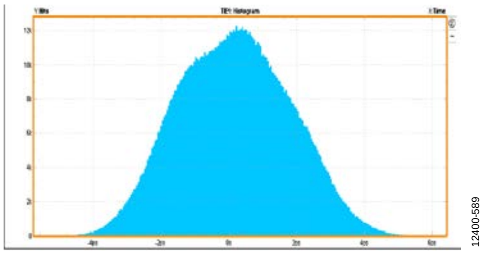

Figure 130. Histogram, External 100 Ω Terminations at 10 Gbps

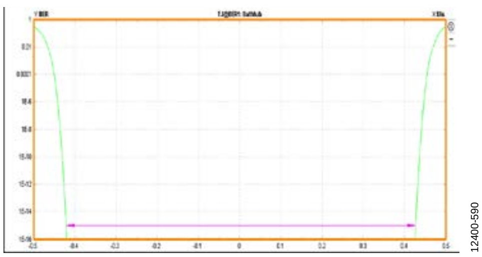

Figure 131. Bathtub, External 100 Ω Terminations at 10 Gbps

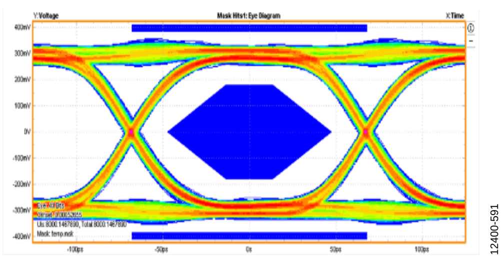

Figure 132. Digital Output Data Eye, External 100 Ω Terminations at 7.37 Gbps

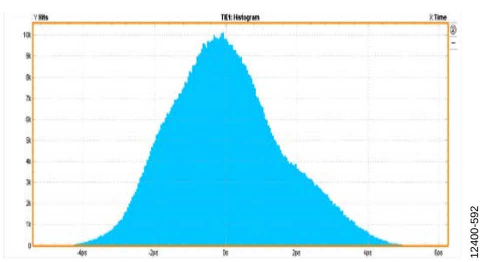

Figure 133. Histogram, External 100 Ω Terminations at 7.37 Gbps

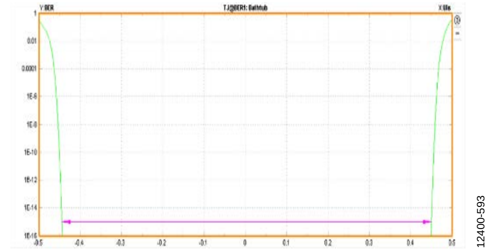

Figure 134. Bathtub, External 100 Ω Terminations at 7.37 Gbps

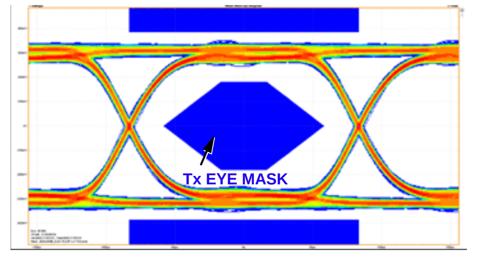

Figure 135. Digital Output Data Eye, External 100 Ω Terminations at 6 Gbps

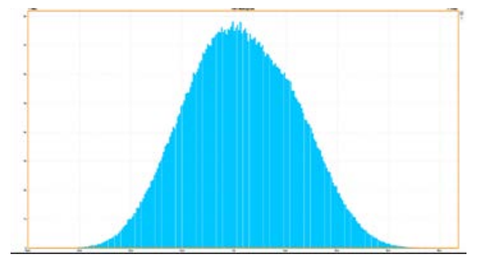

Figure 136. Histogram, External 100 Ω Terminations at 6 Gbps

Figure 137. Bathtub, External 100 Ω Terminations at 6 Gbps

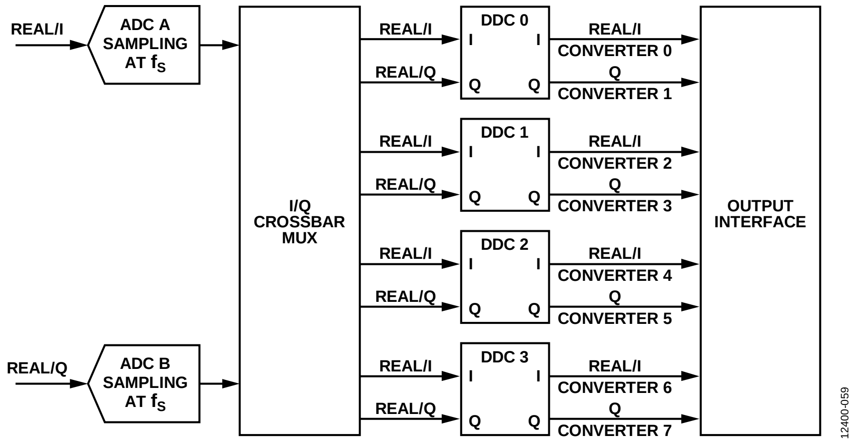

Figure 138. DDCs and Virtual Converter Mapping

JESD204B Tx CONVERTER MAPPING

To support the different chip operating modes, the AD6674 design treats each sample stream (real or I/Q) as originating from separate virtual converters. The I/Q samples are always mapped in pairs with the I samples mapped to the first virtual converter, and the Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters are the same whether a single real converter is used along with a DDC block producing I/Q outputs, or an analog downconversion is used with two real converters producing I/Q outputs.

Figure 139 shows a block diagram of the two scenarios described for I/Q transport layer mapping.

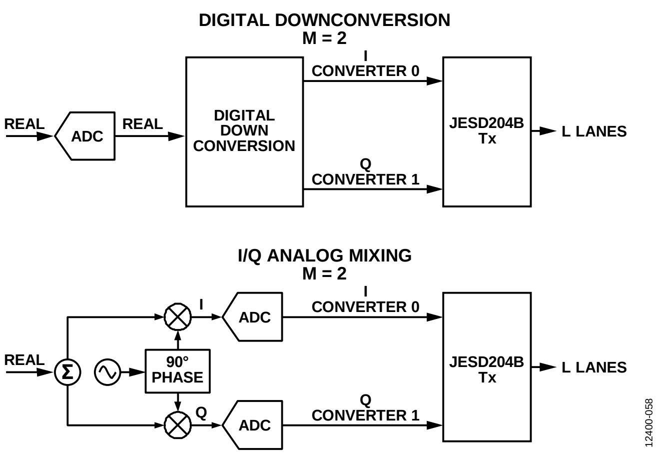

Figure 139. I/Q Transport Layer Mapping

The JESD204B Tx block for AD6674 supports up to four digital DDC blocks. Each DDC block outputs either two sample streams (I/Q) for the complex data components (real + imaginary) or one sample stream for real (I) data. The JESD204B interface can be configured to use up to eight virtual converters depending on the DDC configuration. Figure 138 shows the virtual converters and their relationship to DDC outputs when complex outputs are used. Table 34 shows the virtual converter mapping for each chip operating mode when channel swapping is disabled.

CONFIGURING THE JESD204B LINK

The AD6674 has one JESD204B link. It offers an easy way to set up the JESD204B link through the quick configuration register (Register 0x570). The serial outputs (SERDOUT0± to SERDOUT3±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDCs are used for on-chip digital processing, the M value represents the number of virtual converters. The virtual converter mapping setup is shown in Figure 138.

The maximum lane rate allowed by the JESD204B specification is 12.5 Gbps. The lane rate is related to the JESD204B parameters using the following equation:

$$Lane\ Line\ Rate = \frac{\left(M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT} \right)}{L}$$

where:

$$f_{OUT} = \frac{f_{ADC\_CLOCK}}{Decimation\ Ratio}$$

The decimation ratio (DCM) is the parameter programmed in Register 0x201.

Use the following steps to configure the output:

1. Power down the link.
2. Select the quick configuration options.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane rate calculated is less than 6.25 Gbps, select the low lane rate option by programming a value of 0x10 to Register 0x56E.

Table 35 and Table 36 show the JESD204B output configurations supported for both N′ = 16 and N′ = 8, respectively, for a given number of virtual converters. Take care to ensure that the serial lane rate for a given configuration is within the supported range of 3.125 Gbps to 12.5 Gbps.

See the Example 1: ADC with DDC Option (Two ADCs + Four DDCs) section and the Example 2: ADC with NSR Option (Two ADCs + NSR) section for two examples describing which JESD204B transport layer settings are valid for a given chip mode.

Table 34. Virtual Converter Mapping

No. of Virtual Converters Supported	Chip Operating Mode (Register 0x200[3:0])	Chip Q Ignore (Register 0x200[5])	Virtual Converter Mapping							
			0	1	2	3	4	5	6	7
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC 0 I samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	Unused	Unused	Unused	Unused
4	Four DDC mode (0x3)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	DDC 2 I samples	DDC 3 I samples	Unused	Unused	Unused	Unused
8	Four DDC mode (0x3)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	DDC 2 I samples	DDC 2 Q samples	DDC 3 I samples	DDC 3 Q samples
1 to 2	NSR mode (0x7)	Real or complex (0x0)	ADC A Samples	ADC B Samples	Unused	Unused	Unused	Unused	Unused	Unused
1 to 2	VDR mode (0x8)	Real or complex (0x0)	ADC A Samples	ADC B Samples	Unused	Unused	Unused	Unused	Unused	Unused

Table 35. JESD204B Output Configurations for N′ = 16

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x570)	JESD204B Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x01	$20 \times f_{OUT}$	1	1	2	1	0	8 to 16	16	0 to 3	Only valid K values that are divisible by 4 are supported
	0x40	$10 \times f_{OUT}$	2	1	1	1	1	8 to 16	16	0 to 3	
	0x41	$10 \times f_{OUT}$	2	1	2	2	0	8 to 16	16	0 to 3	
	0x80	$5 \times f_{OUT}$	4	1	1	2	1	8 to 16	16	0 to 3	
	0x81	$5 \times f_{OUT}$	4	1	2	4	0	8 to 16	16	0 to 3	
2	0x0A	$40 \times f_{OUT}$	1	2	4	1	0	8 to 16	16	0 to 3	
	0x49	$20 \times f_{OUT}$	2	2	2	1	0	8 to 16	16	0 to 3	
	0x88	$10 \times f_{OUT}$	4	2	1	1	1	8 to 16	16	0 to 3	
	0x89	$10 \times f_{OUT}$	4	2	2	2	0	8 to 16	16	0 to 3	
4	0x13	$80 \times f_{OUT}$	1	4	8	1	0	8 to 16	16	0 to 3	
	0x52	$40 \times f_{OUT}$	2	4	4	1	0	8 to 16	16	0 to 3	
	0x91	$20 \times f_{OUT}$	4	4	2	1	0	8 to 16	16	0 to 3	
8	0x1C	$160 \times f_{OUT}$	1	8	16	1	0	8 to 16	16	0 to 3	
	0x5B	$80 \times f_{OUT}$	2	8	8	1	0	8 to 16	16	0 to 3	
	0x9A	$40 \times f_{OUT}$	4	8	4	1	0	8 to 16	16	0 to 3	

[1] f_{OUT} is the output sample rate. f_{OUT} = *ADC sample rate/chip decimation*. The JESD204B serial lane rate must be ≥3.125 Gbps and ≤12.5 Gbps; when the serial lane rate is ≤12.5 Gbps and ≥6.25 Gbps, the low lane rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial lane rate is <6.25 Gbps and ≥3.125 Gbps, the low lane rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).
[2] JESD204B transport layer descriptions are as described in the JESD204B Overview section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Table 36. JESD204B Output Configurations for N′ = 8

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x570)	Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x00	10 × f_{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values that are divisible by 4 are supported
	0x01	10 × f_{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f_{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f_{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f_{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
	0x80	2.5 × f_{OUT}	4	1	1	4	0	7 to 8	8	0 to 1	
	0x81	2.5 × f_{OUT}	4	1	2	8	0	7 to 8	8	0 to 1	
2	0x09	20 × f_{OUT}	1	2	2	1	0	7 to 8	8	0 to 1	
	0x48	10 × f_{OUT}	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	10 × f_{OUT}	2	2	2	2	0	7 to 8	8	0 to 1	
	0x88	5 × f_{OUT}	4	2	1	2	0	7 to 8	8	0 to 1	
	0x89	5 × f_{OUT}	4	2	2	4	0	7 to 8	8	0 to 1	
	0x8A	5 × f_{OUT}	4	2	4	8	0	7 to 8	8	0 to 1	

[1] f_{OUT} is the output sample rate. f_{OUT} = *ADC sample rate/chip decimation*. The JESD204B serial lane rate must be ≥3.125 Gbps and ≤12.5 Gbps; when the serial lane rate is ≤12.5 Gbps and ≥6.25 Gbps, the low lane rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial lane rate is <6.25 Gbps and ≥3.125 Gbps, the low lane rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).
[2] JESD204B transport layer descriptions are as described in the JESD204B Overview section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Example 1: ADC with DDC Option (Two ADCs + Four DDCs)

The chip application mode is four-DDC mode (see Figure 140) with the following characteristics:

- Two 14-bit converters at 1 GSPS
- Four DDCs application layer mode with complex outputs (I/Q)
- Chip decimation ratio = 16
- DDC decimation ratio = 16 (see Table 15)

The JESD204B output configuration is as follows:

- Virtual converters required = 8 (see Table 35)
- Output sample rate (f_{OUT}) = 1000/16 = 62.5 MSPS

Supported JESD204B output configurations (see Table 35) include

- N′ = 16 bits
- N = 14 bits
- L = 1, M = 8, and F = 16; or L = 2, M = 8, and F = 8 (quick configuration = 0x1C or 0x5B)
- CS = 0 to 1
- K = 32
- Output serial lane rate = 10 Gbps per lane (L = 1) or 5 Gbps per lane (L = 2)
- For L = 1, low lane rate mode disabled
- For L = 2, low lane rate mode enabled

Example 1 shows the flexibility in the digital and lane configurations for the AD6674. The sample rate is 1 GSPS, but the outputs are all combined into either one or two lanes depending on the I/O speed capability of the receiving device.

Example 2: ADC with NSR Option (Two ADCs + NSR)

The chip application mode is NSR mode (see Figure 141) with the following characteristics:

- Two 14-bit converters at 500 MSPS
- NSR blocks enabled for each channel
- Chip decimation ratio = 1

The JESD204B output configuration is as follows:

- Virtual converters required = 2 (see Table 35)
- Output sample rate (f_{OUT}) = 500 MSPS

Supported JESD204B output configurations (see Table 35) include

- N′ = 16 bits
- N = 9 bits
- L = 2, M = 2, and F = 2; L = 4, M = 2, and F = 1 (quick configuration = 0x49 or 0x88)
- CS = 0 to 2
- K = 32
- Output serial lane rate = 10 Gbps per lane (L = 2) or 5 Gbps per lane (L = 4)
- For L = 2, low lane rate mode disabled
- For L = 4, low lane rate mode enabled

Example 2 shows the flexibility in the digital and lane configurations for the AD6674. The sample rate is 500 MSPS, but the outputs are all combined into either two or four lanes depending on the I/O speed capability of the receiving device.

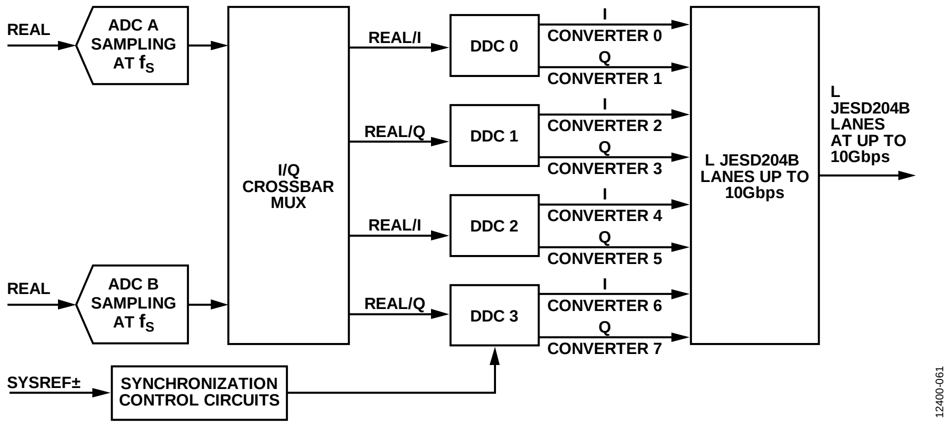

Figure 140. Two-ADC + Four-DDC Mode

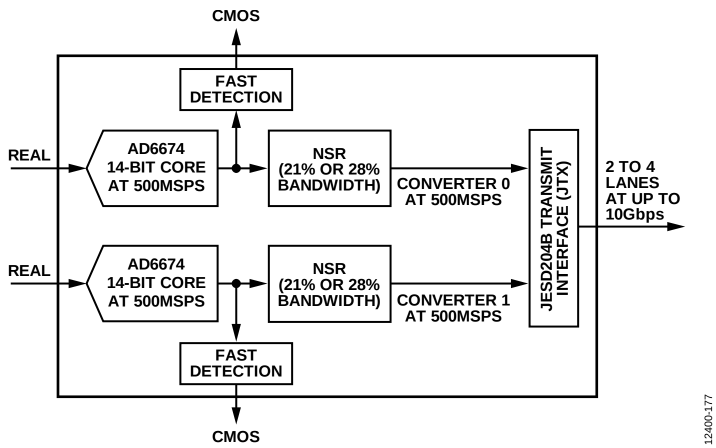

Figure 141. Two-ADC + NSR Mode

MULTICHIP SYNCHRONIZATION

The AD6674 has a SYSREF± input that allows the user flexible options for synchronizing the internal blocks. The SYSREF± input is a source synchronous system reference signal that enables multichip synchronization. The input clock divider, DDCs, signal monitor block, and JESD204B link can be synchronized using the SYSREF± input. For the highest level of timing accuracy, SYSREF± must meet setup and hold requirements relative to the CLK± input.

The flowchart in Figure 142 describes the internal mechanism by which multichip synchronization can be achieved in the AD6674. The AD6674 supports several features that aid users in meeting the requirements for capturing a SYSREF± signal. The SYSREF± sample event is defined as either a synchronous low to high transition or a synchronous high to low transition. Additionally, the AD6674 allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the CLK± input. The AD6674 also has the ability to ignore a programmable number (up to 16) of SYSREF± events. The SYSREF± control options can be selected using Register 0x120 and Register 0x121.

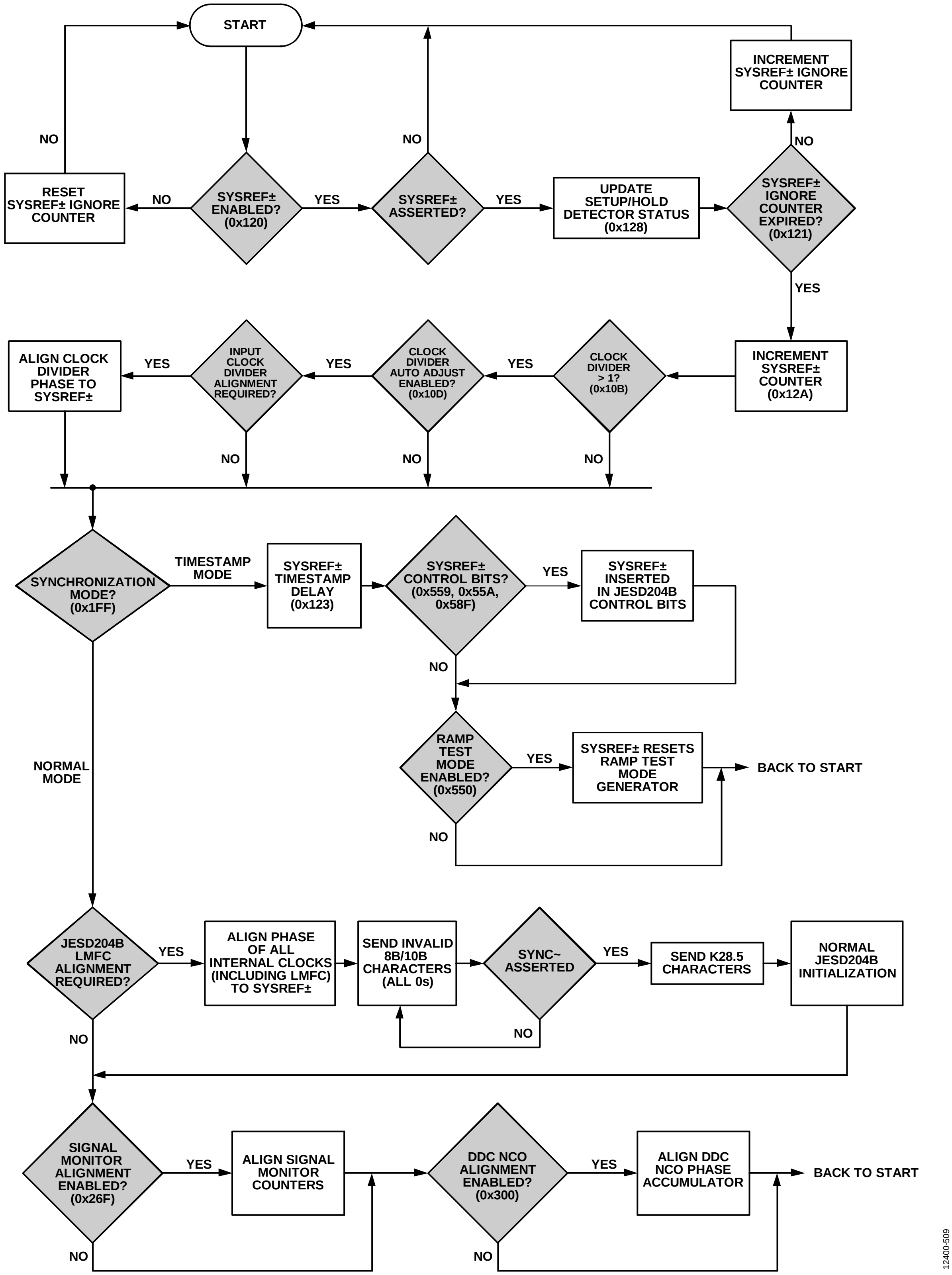

Figure 142. Multichip Synchronization

SYSREF± SETUP/HOLD WINDOW MONITOR

To assist in ensuring a valid SYSREF± capture, the AD6674 has a SYSREF± setup and hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map. Figure 143 and Figure 144 show both the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF± signal before the CLK± edge and the hold detector returns the status of the SYSREF± signal after the CLK± edge. Register 0x128 stores the status of SYSREF± and lets the user know if the SYSREF± signal was successfully captured by the ADC.

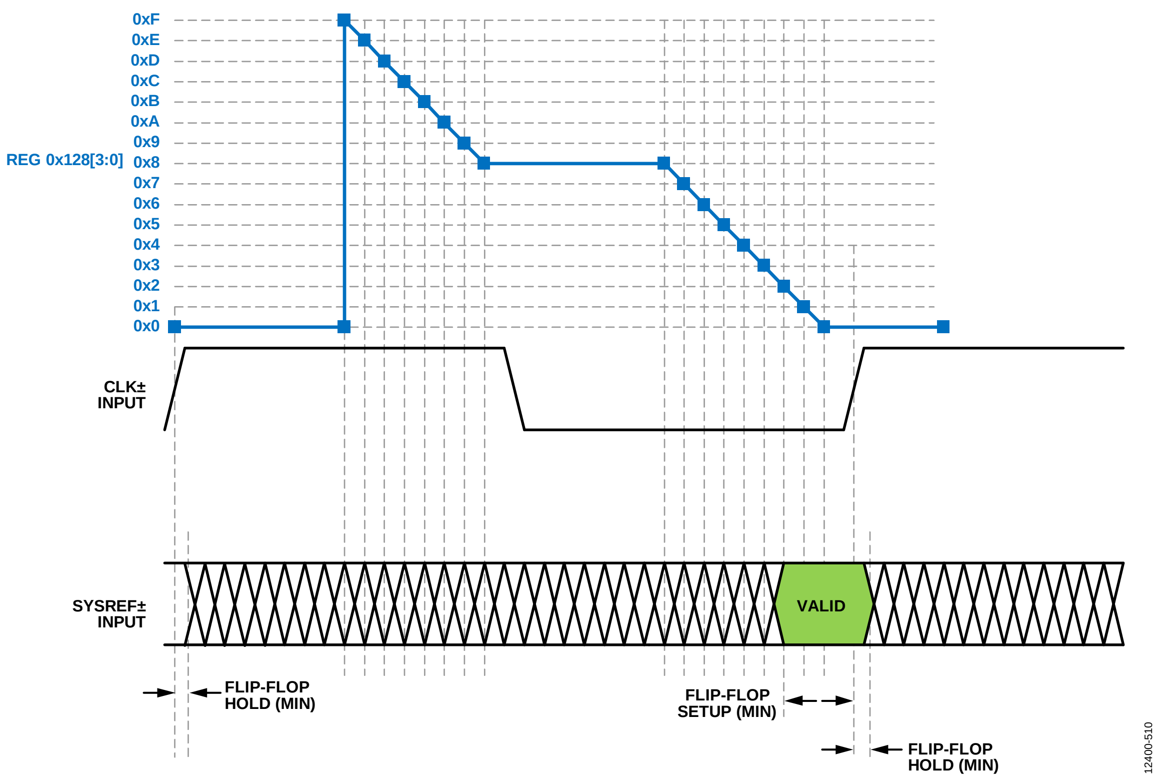

Figure 143. SYSREF± Setup Detector

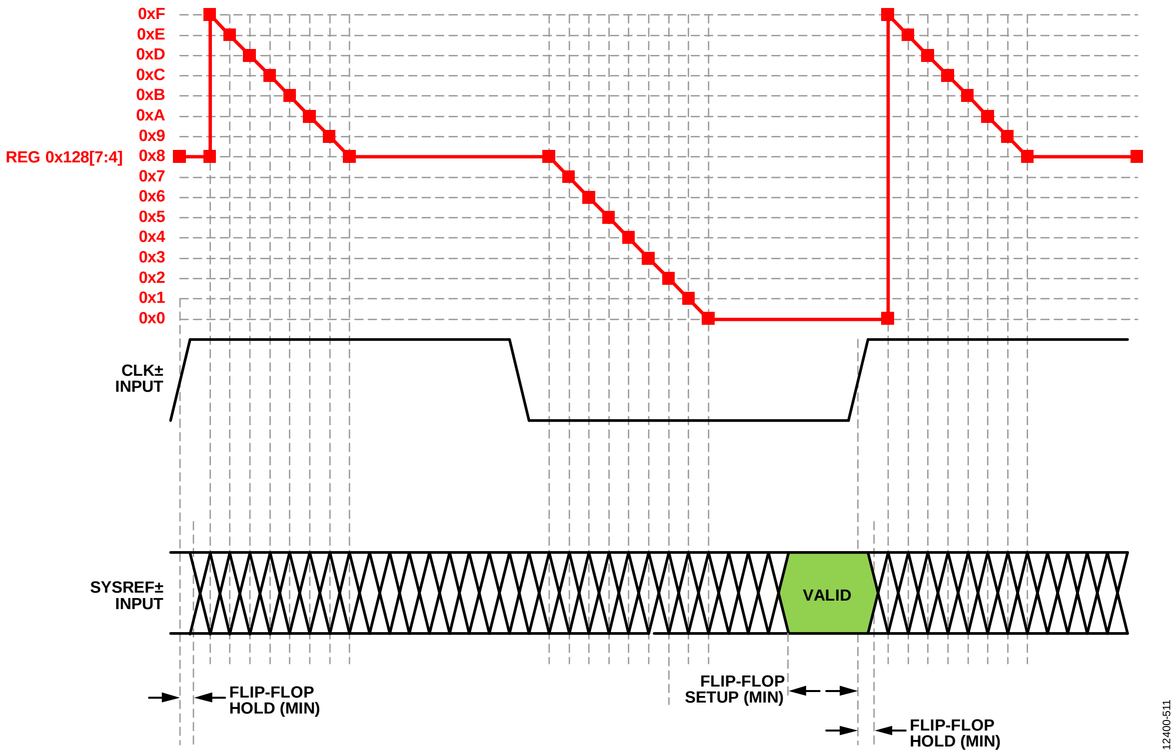

Figure 144. SYSREF± Hold Detector

Table 37 shows the description of the contents of Register 0x128 and how to interpret them.

Table 37. SYSREF± Setup/Hold Monitor, Register 0x128

Register 0x128[7:4] Hold Status	Register 0x128[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error; the smaller this number, the smaller the setup margin
0x0 to 0x8	0x8	No setup or hold error (best hold margin)
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin)
0x8	0x0	No setup or hold error (best setup margin)
0x9 to 0xF	0x0	Possible hold error; the larger this number, the smaller the hold margin
0x0	0x0	Possible setup or hold error

TEST MODES

ADC TEST MODES

The AD6674 has various test options that aid in the system level implementation. The AD6674 has ADC test modes that are available in Register 0x550. These test modes are described in Table 38. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock.

If the application mode is set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 2 and Bit 0 of Register 0x327, Register 0x347, and Register 0x367, depending on which DDC(s) are selected. The (I) data uses the test patterns selected for Channel A and the (Q) data uses the test patterns selected for Channel B. For the case of DDC3 only, the (I) data uses the test patterns from Channel A, and the (Q) data does not output test patterns. Bit 0 of Register 0x387 selects the Channel A test patterns to be used for the (I) data. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

JESD204B BLOCK TEST MODES

In addition to the ADC test modes, the AD6674 also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x573 and Register 0x574. These test patterns can be inserted at various points along the output data path. These test insertion points are shown in Figure 124. Table 39 describes the various test modes available in the JESD204B block. For the AD6674, a transition from the test modes (Register 0x573 ≠ 0x00) to normal mode (0x573 = 0x00) require a SPI soft reset. This is done by writing 0x81 to Register 0x00 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD6674 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are enabled via Register 0x571[5]. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x573, Bits[3:0]. These test modes are also explained in Table 39. The interface tests can be inserted at various points along the data. See Figure 124 for more information on the test insertion points. Register 0x573, Bits[5:4], show where these tests are inserted.

Table 38. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	+Full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	−Full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	Not applicable	For repeat mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2]… For single mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000…
1111	Ramp output	$(x) \% 2^{14}$	Not applicable	$(x) \% 2^{14}$, $(x + 1) \% 2^{14}$, $(x + 2) \% 2^{14}$, $(x + 3) \% 2^{14}$

Table 39. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555…	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000…	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^9 + x^5 + 1$	0x092
0111	7-bit PN sequence	$x^7 + x^6 + 1$	0x07
1000	Ramp output	$(x) \% 2^{16}$	Ramp size depends on test insertion point
1110	Continuous/repeat user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then zeros

Table 40, Table 41, and Table 42 show examples of some of the test modes when inserted at the JESD204B sample input, physical layer (PHY) 10-bit input, and scrambler 8-bit input. UP in the Table 40 to Table 42 represent the user pattern control bits from the memory map register table (see Table 45).

Data Link Layer Test Modes

The data link layer test modes are implemented in the AD6674 as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x574, Bits[2:0]. Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB± by writing 0xC0 to Register 0x572.

Table 40. JESD204B Sample Input for M = 2, S = 2, N′ = 16 (Register 0x573[5:4] = 'b00)

Frame No.	Converter No.	Sample No.	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 41. Physical Layer 10-Bit Input (Register 0x573[5:4] = 'b01)

10-Bit Symbol No.	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	$(x) \% 2^{10}$	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	$(x + 1) \% 2^{10}$	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	$(x + 2) \% 2^{10}$	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	$(x + 3) \% 2^{10}$	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	$(x + 4) \% 2^{10}$	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	$(x + 5) \% 2^{10}$	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	$(x + 6) \% 2^{10}$	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	$(x + 7) \% 2^{10}$	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	$(x + 8) \% 2^{10}$	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	$(x + 9) \% 2^{10}$	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	$(x + 10) \% 2^{10}$	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	$(x + 11) \% 2^{10}$	0x3DD	0x008	UP4[15:6]	0x000

Table 42. Scrambler 8-Bit Input (Register 0x573[5:4] = 'b10)

8-Bit Octet No.	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	(x) % 2^8	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^8	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^8	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^8	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^8	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) % 2^8	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^8	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^8	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^8	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^8	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^8	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^8	0xAC	0xFF	UP4[15:9]	0x00

SERIAL PORT INTERFACE (SPI)

The AD6674 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the serial port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the *Serial Control Interface Standard*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 43). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 43. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. See Figure 4 and Table 5 for an example of the serial timing and its definitions.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This bit allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the *Serial Control Interface Standard*.

HARDWARE INTERFACE

The pins described in Table 43 comprise the physical interface between the user programming device and the serial port of the AD6674. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6674 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 44 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the *Serial Control Interface Standard*. The AD6674 device specific features are described in the Memory Map section.

Table 44. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the clock divider via the SPI
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Serializer/Deserializer (SERDES) Output Setup	Allows the user to vary SERDES settings, including swing and emphasis

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into seven sections: the Analog Devices SPI registers, the analog input buffer control registers, ADC function registers, the DDC function registers, NSR decimate by 2 and noise shaping requantizer registers, variable dynamic range registers, and the digital outputs and test modes registers.

Table 45 (see the Memory Map Register Table section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the Table 45.

Open and Reserved Locations

All address and bit locations that are not included in Table 45 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is open (for example, Address 0x561). If the entire address location is open (for example, Address 0x013), do not write to this address location.

Default Values

After the AD6674 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 45.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- "X" denotes a "don't care".

Channel Specific Registers

Some channel setup functions such as buffer input termination (Register 0x016) can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 45 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 45 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x008 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the AD6674 requires 5 ms to recover. Therefore, when programming the AD6674 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

Datapath Soft Reset

After programming the desired settings to the SPI registers, issue a datapath soft reset by programming 0x02 to Register 0x001. This reset function is implemented upon the next rising edge of the input clock, after the register is programmed to issue the datapath soft reset. This reset does not affect the contents of the memory map registers; it only resets the datapath.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 45 are not currently supported for this device.

Table 45. Memory Map Registers

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Analog Devices SPI Registers											
0x000	INTERFACE_ CONFIG_A	Soft reset (self clearing): clears memory map registers	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing): clears memory map registers	0x00	
0x001	INTERFACE_ CONFIG_B	Single instruc-tion	0	0	0	0	0	Datapath soft reset (self clearing): does not clear memory map registers	0	0x00	
0x002	DEVICE_ CONFIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE					011 = high speed ADC				0x03	Read only
0x004	CHIP_ID (low byte)	1	1	0	0	1	1	1	1	0xCF	0
0x005	CHIP_ID (high byte)	0	0	0	0	0	0	0	0	0x00	0
0x006	CHIP_ GRADE	Chip speed grade 1010 = 1000 MSPS 0111 = 750 MSPS 0101 = 500 MSPS				0	X	X	X	X	Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x03	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
Analog Input Buffer Control Registers											
0x015	Analog Input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	
0x016	Input termination (local)	Analog input differential termination 0000 = 400 Ω 0001 = 200 Ω 0010 = 100 Ω 0110 = 50 Ω				1110 =AD6674-1000 and AD6674-750 1100 = AD6674-500				0x0C; 0x0E for AD6674 -1000 and AD6674 -750	
0x934	Input capacitance (local)	0	0	0	0x1F = 3 pF to GND (default) 0x00 = 1.5 pF to GND					0x1F	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x018	Buffer Control 1 (local)	0000 = 1.0× buffer current 0001 = 1.5× buffer current 0010 = 2.0× buffer current (default for AD6674-500) 0011 = 2.5× buffer current 0100 = 3.0× buffer current (default for AD6674-750 and AD6674-1000) 0101 = 3.5× buffer current … 1111 = 8.5× buffer current				0	0	0	0	0x40; 0x20 for AD6674 -500	
0x019	Buffer Control 2 (local)	0100 = Setting 1 (default for AD6674-750) 0101 = Setting 2 (default for AD6674-1000) 0110 = Setting 3 (default for AD6674-500) 0111 = Setting 4 (see Table 10 for setting per frequency range)				0	0	0	0	0xXX	
0x01A	Buffer Control 3 (local)	0	0	0	0	1000 = Setting 1 1001 = Setting 2 (default for AD6674-750 and AD6674-1000) 1010 = Setting 3 (default for AD6674-500) (see Table 10 for setting per frequency range)				0x09; 0x0A for AD6674 -500	
0x11A	Buffer Control 4 (local)	0	0	High frequency setting 0 = off (default) 1 = on	0	0	0	0	0	0x00	
0x935	Buffer Control 5 (local)	0	0	0	0	0	Low frequency operation 0 = off 1 = on (default)	0	0	0x04	
0x025	Input full-scale range (local)	0	0	0	0	Full-scale adjust 0000 = 1.94 V 1000 = 1.46 V 1001 = 1.58 V 1010 = 1.70 V (default for AD6674-750 and AD6674-1000) 1011 = 1.82 V 1100 = 2.06 V (default for AD6674-500)				0x0A; 0x0C for AD6674 -500	V p-p differ-ential; use in con-junction with Reg. 0x030
0x030	Input full-scale control (local)	0	0	0	Full-scale control See Table 10 for recommended settings for different frequency bands; default values: AD6674-1000 = 110 AD6674-750 = 101 AD6674-500 = 001 AD6674-500 = 110 (for <1.82 V)			0	0	0xXX	Used in conjunc-tion with Reg. 0x025
ADC Function Registers											
0x024	V_1P0 control	0	0	0	0	0	0	0	1.0 V reference select 0 = internal 1 = external	0x00	
0x028	Temp-erature diode	0	0	0	0	0	0	0	Diode selection 0 = no diode selected 1 = temper-ature diode selected	0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x03F	PDWN/ STBY pin control (local)	0 = PDWN/ STBY enabled 1 = disabled	0	0	0	0	0	0	0	0x00	Used in conjunction with Reg. 0x040
0x040	Chip pin control	PDWN/STBY function 00 = power down 01 = standby 10 = disabled		Fast Detect B (FD_B) 000 = Fast Detect B output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 111 = disabled			Fast Detect A (FD_A) 000 = Fast Detect A output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 011 = temperature diode 111 = disabled			0x3F	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1 001 = divide by 2 011 = divide by 4 111 = divide by 8			0x00	
0x10C	Clock divider phase (local)	0	0	0	0	Independently controls Channel A and Channel B clock divider phase offset 0000 = 0 input clock cycles delayed 0001 = ½ input clock cycles delayed 0010 = 1 input clock cycles delayed 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				0x00	
0x10D	Clock divider and SYSREF± control	Clock divider auto-phase adjust 0 = disabled 1 = enabled	0	0	0	Clock divider negative skew window 00 = no negative skew 01 = 1 device clock of negative skew 10 = 2 device clocks of negative skew 11 = 3 device clocks of negative skew		Clock divider positive skew window 00 = no positive skew 01 = 1 device clock of positive skew 10 = 2 device clocks of positive skew 11 = 3 device clocks of positive skew		0x00	Clock divider must be >1
0x117	Clock delay control	0	0	0	0	0	0	0	clock fine delay adjustment enable 0 = disabled 1 = enabled	0x00	Enabling the clock fine delay adjust causes a datapath soft reset
0x118	Clock fine delay	Clock Fine Delay Adjust[7:0] twos complement coded control to adjust the fine sample clock skew in ~1.7 ps steps ≤−88 = −151.7 ps skew −87 = −150.0 ps skew … 0 = 0 ps skew … ≥ +87 = +150 ps skew								0x00	Used in conjunction with Reg. 0x117
0x11C	Clock status	0	0	0	0	0	0	0	0 = no input clock detected 1 = input clock detected	0x00	Read only
0x120	SYSREF± Control 1	0	SYSREF± flag reset 0 = normal operation 1 = flags held in reset	0	SYSREF± transition select 0 = low to high 1 = high to low	CLK± edge select 0 = rising 1 = falling	SYSREF± mode select 00 = disabled 01 = continuous 10 = N shot		0	0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x121	SYSREF± Control 2	0	0	0	0	SYSREF± N shot ignore counter select 0000 = next SYSREF± only 0001 = ignore the first SYSREF± transitions 0010 = ignore the first two SYSREF± transitions … 1111 = ignore the first 16 SYSREF± transitions				0x00	Mode select (Reg. 0x120, Bits[2:1]) must be N shot
0x123	SYSREF± timestamp delay control		SYSREF± Timestamp Delay[6:0] 0x00 = no delay 0x01 = 1 clock delay … 0x7F = 127 clocks delay							0x00	Ignored when Reg. 0x1FF = 0x00
0x128	SYSREF± Status 1	SYSREF± hold status Refer to Table 37				SYSREF± setup status Refer to Table 37					Read only
0x129	SYSREF± and clock divider status	0	0	0	0	Clock divider phase when SYSREF± was captured 0000 = in phase 0001 = SYSREF± is ½ cycle delayed from clock 0010 = SYSREF± is 1 cycle delayed from clock 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed					Read only
0x12A	SYSREF± counter	SYSREF± counter, Bits[7:0], increments when a SYSREF± signal is captured									Read only
0x1FF	Chip sync mode	0	0	0	0	0	0	Synchronization mode 00 = normal 01 = timestamp		0x00	
0x200	Chip application mode	0	0	Chip Q ignore 0 = normal (I/Q) 1 = ignore (I only)	0	Chip operating mode 0001 = DDC 0 on 0010 = DDC 0 and DDC 1 on 0011 = DDC 0, DDC 1, DDC 2, and DDC3 on 0111 = NSR enabled (default) 1000 = VDR enabled				0x07	
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select 000 = decimate by 1 001 = decimate by 2 010 = decimate by 4 011 = decimate by 8 100 = decimate by 16			0x01; 0x00 for AD6674-500	
0x228	Customer offset	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x245	Fast detect (FD) control (local)	0	0	0	0	Force FD_A/FD_B pins; 0 = normal function; 1 = force to value	Force value of FD_A/FD_B pins; if force pins is true, this value is output on FD_x pins	0	Enable fast detect output	0x00	
0x247	FD upper threshold LSB (local)	Fast Detect Upper Threshold[7:0]								0x00	
0x248	FD upper threshold MSB (local)	0	0	0	Fast Detect Upper Threshold[12:8]					0x00	
0x249	FD lower threshold LSB (local)	Fast Detect Lower Threshold[7:0]								0x00	
0x24A	FD lower threshold MSB (local)	0	0	0	Fast Detect Lower Threshold[12:8]					0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x24B	FD dwell time LSB (local)	Fast Detect Dwell Time[7:0]								0x00	
0x24C	FD dwell time MSB (local)	Fast Detect Dwell Time[15:8]								0x00	
0x26F	Signal monitor synchro-nization control	0	0	0	0	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = 1 shot		0x00	See the Signal Monitor section
0x270	Signal monitor control (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
0x271	Signal Monitor Period Register 0 (local)	Signal Monitor Period[7:1]							0	0x80	In dec-imated output clock cycles
0x272	Signal Monitor Period Register 1 (local)	Signal Monitor Period[15:8]								0x00	In dec-imated output clock cycles
0x273	Signal Monitor Period Register 2 (local)	Signal Monitor Period[23:16]								0x00	In dec-imated output clock cycles
0x274	Signal monitor result control (local)	0	0	0	Result update 1 = update results (self clear)	0	0	0	Result selection 0 = reserved 1 = Peak detector	0x01	
0x275	Signal Monitor Result Register 0 (local)	Signal Monitor Result[7:0] When 0x0274[0] = 1, Result Bits[19:7] = Peak Detector Absolute Value[12:0]; Result Bits[6:0] = 0								Read only	Updated based on Reg. 0x0274, Bit 4
0x276	Signal Monitor Result Register 1 (local)	Signal Monitor Result[15:8]								Read-only	Updated based on Reg. 0x0274, Bit 4
0x277	Signal Monitor Result Register 1 (local)	0	0	0	0	Signal Monitor Result[19:16]				Read-only	Updated based on Reg. 0x0274, Bit 4
0x278	Signal monitor period counter result (local)	Period Count Result[7:0]								Read-only	Updated based on Reg. 0x0274, Bit 4
0x279	Signal monitor SPORT over JESD204B control (local)	0	0	0	0	0	0	00 = reserved 11 = enabled		0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x27A	SPORT over JESD204B input selection (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x02	
Digital Downconverter (DDC) Function Registers—see the Digital Downconverter (DDC) section											
0x300	DDC synchro-nization control	0	0	0	DDC NCO soft reset 0 = normal operation 1 = reset	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one shot		0x00	
0x310	DDC 0 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation ratio select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x311	DDC 0 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x314	DDC 0 frequency LSB	DDC 0 NCO FTW[7:0] twos complement								0x00	
0x315	DDC 0 frequency MSB	X	X	X	X	DDC 0 NCO FTW[11:8] twos complement				0x00	
0x320	DDC 0 phase LSB	DDC 0 NCO POW[7:0] twos complement								0x00	
0x321	DDC 0 phase MSB	X	X	X	X	DDC0 NCO POW[11:8] twos complement				0x00	
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x330	DDC 1 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation ratio select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x331	DDC 1 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x05	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x334	DDC 1 frequency LSB	DDC 1 NCO FTW[7:0] twos complement								0x00	
0x335	DDC 1 frequency MSB	X	X	X	X	DDC1 NCO FTW[11:8] twos complement				0x00	
0x340	DDC 1 phase LSB	DDC 1 NCO POW[7:0] twos complement								0x00	
0x341	DDC 1 phase MSB	X	X	X	X	DDC1 NCO POW[11:8] twos complement				0x00	
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x350	DDC 2 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation ratio select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x351	DDC 2 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x354	DDC 2 frequency LSB	DDC 2 NCO FTW[7:0] twos complement								0x00	
0x355	DDC 2 frequency MSB	X	X	X	X	DDC2 NCO FTW[11:8] twos complement				0x00	
0x360	DDC 2 phase LSB	DDC 2 NCO Phase Offset[7:0] twos complement								0x00	
0x361	DDC 2 phase MSB	X	X	X	X	DDC2 NCO Phase Offset[11:8] twos complement				0x00	
0x367	DDC 2 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x370	DDC 3 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_S/4 Hz IF mode (f_S/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation ratio select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x371	DDC 3 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x05	
0x374	DDC 3 frequency LSB	DDC3 NCO FTW[7:0] twos complement								0x00	
0x375	DDC 3 frequency MSB	X	X	X	X	DDC3 NCO FTW[11:8] twos complement				0x00	
0x380	DDC 3 phase LSB	DDC3 NCO POW[7:0] twos complement								0x00	
0x381	DDC 3 phase MSB	X	X	X	X	DDC3 NCO POW[11:8] twos complement				0x00	
0x387	DDC 3 output test mode selection	0	0	0	0	0	0	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
NSR Decimate by 2 and Noise Shaping Requantizer (NSR)											
0x41E	NSR decimate by 2	High-pass/ low-pass mode: 0 = enable LPF 1 = enable HPF	X	0	0	X	X	X	NSR decimate by 2 enable 0 = disabled 1 = enabled	0x01; 0x00 for AD6674-500	Bit 0 is ignored on AD6674-750 and AD6674-1000 when in NSR mode
0x420	NSR mode	X	X	X	X	NSR mode 000 = 21% BW mode 001 = 28% BW mode			X	0x00	
0x422	NSR tuning	X	X	NSR tuning word; see the Noise Shaping Requantizer (NSR) section; equations for the tuning word are dependent on the NSR mode						0x00	
Variable Dynamic Range (VDR)											
0x430	VDR control	X	X	X	0	X	X	VDR BW mode 0 = 25% BW mode 1 = 43% BW mode (only available for dual complex mode)	0 = dual real mode 1 = dual complex mode (Channel A = I, Channel B = Q)	0x01	
0x434	VDR tuning	X	X	X	X	VDR center frequency; see the Variable Dynamic Range (VDR) section for more details on the center frequency, which is dependent on the VDR mode				0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Digital Outputs and Test Modes											
0x550	ADC test modes (local)	User pattern selection 0 = contin-uous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off (normal operation) 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checker board 0101 = PN sequence, long 0110 = PN sequence, short 0111 = 1/0 word toggle 1000 = user pattern test mode (used with Register 0x550, Bit 7, and User Pattern 1 to User Patten 4 registers) 1111 = ramp output				0x00	
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550, Reg. 0x573

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x559	Output Mode Control 1	0	Converter Control Bit 1 selection (only used when CS (0x58F) = 2 or 3) 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit or VDR Punish Bit 0 011 = fast detect (FD) bit or VDR Punish Bit 1 100 = VDR high/low resolution bit 101 = system reference			0	Converter Control Bit 0 selection (only used when CS (0x58F) = 3) 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit or VDR Punish Bit 0 011 = fast detect (FD) bit or VDR Punish Bit 1 100 = VDR high/low resolution bit 101 = system reference			0x00	
0x55A	Output Mode Control 2	0	0	0	0	0	Converter Control Bit 2 selection (used when CS (0x58F) = 1, 2, or 3) 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit or VDR Punish Bit 0 011 = fast detect (FD) bit or VDR Punish Bit 1 100 = VDR high/low resolution bit 101 = system reference			0x01	
0x561	Output mode	0	0	0	0	0	Sample invert 0 = normal 1 = sample invert	Data format select 00 = offset binary 01 = twos complement		0x01	
0x562	Output overrange (OR) clear	Virtual Converter 7 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 6 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 5 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 4 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 3 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 2 OR 0 = or bit enabled 1 = OR bit cleared	Virtual Converter 1 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 0 OR 0 = OR bit enabled 1 = OR bit cleared	0x00	
0x563	Output overrange status	Virtual Converter 7 OR 0 = no OR 1 = OR occurred	Virtual Converter 6 OR 0 = no OR 1 = OR occurred	Virtual Converter 5 OR 0 = no OR 1 = OR occurred	Virtual Converter 4 OR 0 = no OR 1 = OR occurred	Virtual Converter 3 OR 0 = no OR 1 = OR occurred	Virtual Converter 2 OR 0 = no OR 1 = OR occurred	Virtual Converter 1 OR 0 = no OR 1 = OR occurred	Virtual Converter 0 OR 0 = no OR 1 = OR occurred	0x00	Read only
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	
0x56E	JESD204B lane rate control	0	0	0	0 = serial lane rate ≥ 6.25 Gbps and ≤ 12.5 Gbps 1 = serial lane rate must be ≥ 3.125 Gbps and <6.25 Gbps	0	0	0	0	0x10	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x56F	JESD204B PLL lock status	PLL lock 0 = not locked 1 = locked	0	0	0	0	0	0	0	0x00	Read only
0x570	JESD204B quick configur-ation	JESD204B quick configuration Number of lanes (L) = $2^{0x570[7:6]}$ Number of converters (M) = $2^{0x570[5:3]}$ Number of octets/frame (F) = $2^{0x570[2:0]}$								0x88	Refer to Table 35 and Table 36
0x571	JESD204B Link Mode Control 1	Standby mode 0 = all con-verter outputs 0 1 = CGS (K28.5)	Tail bit (T) PN 0 = disable 1 = enable T = N′ – N – CS	Long trans-port layer test 0 = disable 1 = enable	Lane synchron-ization 0 = disable FACI uses /K28.7/ 1 = enable FACI uses /K28.3/ and /K28.7/	ILAS sequence mode 00 = ILAS disabled 01 = ILAS enabled 11 = ILAS always on test mode		Frame align-ment character insertion (FACI) 0 = enabled 1 = disabled	Link control 0 = active 1 = power down	0x14	
0x572	JESD204B Link Mode Control 2	SYNCINB± pin control 00 = normal 10 = ignore SYNCINB± (force CGS) 11 = ignore SYNCINB± (force ILAS/user data)		SYNCINB± pin invert 0 = active low 1 = active high	SYNCINB± pin type 0 = differential 1 = CMOS	0	8B/10B bypass 0 = normal 1 = bypass	8B/10B bit invert 0 = normal 1 = invert abcde fghij symbols	0	0x00	
0x573	JESD204B Link Mode Control 3	CHKSUM mode 00 = sum of all 8-bit link configuration registers 01 = sum of individual link configuration bit fields 10 = checksum set to zero		Test insertion point 00 = N′ sample input 01 = 10-bit data at 8B/10B output (for PHY testing) 10 = 8-bit data at scrambler input		JESD204B test mode patterns 0000 = normal operation (test mode disabled) 0001 = alternating checker board 0010 = 1/0 word toggle 0011 = 31-bit PN sequence—$x^{31} + x^{28} + 1$ 0100 = 23-bit PN sequence—$x^{23} + x^{18} + 1$ 0101 = 15-bit PN sequence—$x^{15} + x^{14} + 1$ 0110 = 9-bit PN sequence—$x^{9} + x^{5} + 1$ 0111 = 7-bit PN sequence—$x^{7} + x^{6} + 1$ 1000 = ramp output 1110 = continuous/repeat user test 1111 = single user test				0x00	
0x574	JESD204B Link Mode Control 4	ILAS delay 0000 = transmit ILAS on first LMFC after SYNCINB± deasserted 0001 = transmit ILAS on second LMFC after SYNCINB± deasserted … 1111 = transmit ILAS on 16th LMFC after SYNCINB± deasserted				0	Link layer test mode 000 = normal operation (link layer test mode disabled) 001 = continuous sequence of /D21.5/ characters 100 = modified RPAT test sequence 101 = JSPAT test sequence 110 = JTSPAT test sequence			0x00	
0x578	JESD204B LMFC offset	0	0	0	LMFC Phase Offset Value[4:0]					0x00	
0x580	JESD204B DID config	JESD204B Tx DID Value[7:0]								0x00	
0x581	JESD204B BID config	0	0	0	0	JESD204B Tx BID Value[3:0]				0x00	
0x583	JESD204B LID Config 1	0	0	0	Lane 0 LID Value[4:0]					0x00	
0x584	JESD204B LID Config 2	0	0	0	Lane 1 LID Value[4:0]					0x01	
0x585	JESD204B LID Config 3	0	0	0	Lane 2 LID Value[4:0]					0x01	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x586	JESD204B LID Config 4	0	0	0	Lane 3 LID Value[4:0]					0x03	
0x58B	JESD204B parameters (SCR/L)	JESD204B scram-bling (SCR) 0 = disabled 1 = enabled	0	0	0	0	0	JESD204B lanes (L) 00 = 1 lane 01 = 2 lanes 11 = 4 lanes read only; see Register 0x570		0x83	
0x58C	JESD204B F config	Number of octets per frame, F = 0x58C[7:0] + 1								0x00	Read only, see Reg. 0x570
0x58D	JESD204B K config	0	0	0	Number of frames per multi-frame, K = 0x58D[4:0] + 1 Only values where (F × K) mod 4 = 0 are supported					0x1F	See Reg. 0x570
0x58E	JESD204B M config	Number of Converters per Link[7:0] 0x00 = link connected to one virtual converter (M = 1) 0x01 = link connected to two virtual converters (M = 2) 0x03 = link connected to four virtual converters (M = 4) 0x07 = link connected to eight virtual converters (M = 8)								0x01	Read only
0x58F	JESD204B parameters (CS/N)	Number of control bits (CS) per sample 00 = no control bits (CS = 0) 01 = 1 control bit (CS = 1); Control Bit 2 only 10 = 2 control bits (CS = 2); Control Bit 2 and Control Bit 1 only 11 = 3 control bits (CS = 3); all control bits (2, 1, 0)		0	Converter resolution (N) 0x06 = 7-bit resolution 0x07 = 8-bit resolution 0x08 = 9-bit resolution 0x09 = 10-bit resolution 0x0A = 11-bit resolution 0x0B = 12-bit resolution 0x0C = 13-bit resolution 0x0D = 14-bit resolution 0x0E = 15-bit resolution 0x0F = 16-bit Resolution					0x0F	
0x590	JESD204B parameter (NP)	Subclass support 000 = Subclass 0 (no deterministic latency) 001 = Subclass 1			Number of bits per sample (N') 0x7 = 8 bits 0xF = 16 bits					0x2F	
0x591	JESD204B parameter (S)	0	0	1	Samples per converter frame cycle (S) S value = 0x591[4:0] +1					0x20	Read only
0x592	JESD204B parameters (HD and CF)	HD value 0 = disabled 1 = enabled	0	0	Control words per frame clock cycle per link (CF) CF value = 0x592[4:0]					0x80	Read only
0x5A0	JESD204B CHKSUM 0	CHKSUM value for SERDOUT0±[7:0]								0x81	Read only
0x5A1	JESD204B CHKSUM 1	CHKSUM value for SERDOUT1±[7:0]								0x82	Read only
0x5A2	JESD204B CHKSUM 2	CHKSUM value for SERDOUT2±[7:0]								0x82	Read only
0x5A3	JESD204B CHKSUM 3	CHKSUM value for SERDOUT3±[7:0]								0x84	Read only
0x5B0	JESD204B lane power-down	1	SER-DOUT3± 0 = on 1 = off	1	SER-DOUT2± 0 = on 1 = off	1	SERDOUT1± 0 = on 1 = off	1	SER-DOUT0± 0 = on 1 = off	0xAA	
0x5B2	JESD204B lane SERDOUT0± assign	X	X	X	X	0	Physical Lane 0 assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x5B3	JESD204B lane SERDOUT1± assign	X	X	X	X	0	Physical Lane 1 assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x11	
0x5B5	JESD204B lane SERDOUT2± assign	X	X	X	X	0	Physical Lane 2 assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x22	
0x5B6	JESD204B lane SERDOUT3± assign	X	X	X	X	0	Physical Lane 3 assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			0x33	
0x5BF	JESD serializer drive adjust	0	0	0	0	Swing voltage 0000 = 237.5 mV 0001 = 250 mV 0010 = 262.5 mV 0011 = 275 mV 0100 = 287.5 mV 0101 = 300 mV 0110 = 312.5 mV 0111 = 325 mV 1000 = 337.5 mV 1001 = 350 mV 1010 = 362.5 mV 1011 = 375 mV 1100 = 387.5 mV 1101 = 400 mV 1110 = 412.5 mV 1111 = 425 mV				0x05	
0x5C1	De-emphasis select	0	SER-DOUT3± 0 = disable 1 = enable	0	SER-DOUT2± 0 = disable 1 = enable	0	SERDOUT1± 0 = disable 1 = enable	0	SER-DOUT0± 0 = disable 1 = enable	0x00	
0x5C2	De-emphasis setting for SERDOUT0±	0	0	0	0	De-emphasis settings 0000 = de-emphasis disabled 1000 = 0.5 dB 1001 = 1.0 dB 1010 = 1.7 dB 1011 = 2.5 dB 1100 = 3.5 dB 1101 = 4.9 dB 1110 = 6.7 dB 1111 = 9.6 dB				0x00	
0x5C3	De-emphasis setting for SERDOUT1±	0	0	0	0	De-emphasis settings 0000 = de-emphasis disabled 1000 = 0.5 dB 1001 = 1.0 dB 1010 = 1.7 dB 1011 = 2.5 dB 1100 = 3.5 dB 1101 = 4.9 dB 1110 = 6.7 dB 1111 = 9.6 dB				0x00	
0x5C4	De-emphasis setting for SERDOUT2±	0	0	0	0	De-emphasis settings 0000 = de-emphasis disabled 1000 = 0.5 dB 1001 = 1.0 dB 1010 = 1.7 dB 1011 = 2.5 dB 1100 = 3.5 dB 1101 = 4.9 dB 1110 = 6.7 dB 1111 = 9.6 dB				0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x5C5	De-emphasis setting for SERDOUT3±	0	0	0	0	De-emphasis settings 0000 = de-emphasis disabled 1000 = 0.5 dB 1001 = 1.0 dB 1010 = 1.7 dB 1011 = 2.5 dB 1100 = 3.5 dB 1101 = 4.9 dB 1110 = 6.7 dB 1111 = 9.6 dB				0x00	

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD6674 must be powered by the following seven supplies: AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP2164 and ADP2370 switching regulators be used to convert the 3.3 V, 5.0 V, or 12 V input rails to an intermediate rail (1.8 V and 3.8 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1741, ADM7172, and ADP125). Figure 145 shows the recommended method. For more detailed information on the recommended power solution, refer to the AD6674 evaluation board documentation.

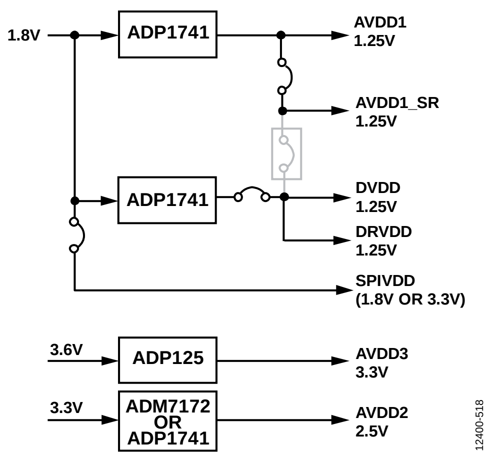

Figure 145. High Efficiency, Low Noise Power Solution for the AD6674

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 145 provides the lowest noise, highest efficiency power delivery system for the AD6674. If only one 1.25 V supply is available, it must be routed to AVDD1 first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for AVDD1_SR, DVDD, and DRVDD, in that order. The user can use several different decoupling capacitors to cover both high and low frequencies. These must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to ground to achieve the best electrical and thermal performance of the AD6674. Connect an exposed continuous copper plane on the PCB to the AD6674 exposed pad, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias must be solder filled or plugged. The number of vias and the fill determine the resultant θ_{JA} measured on the board.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 146 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

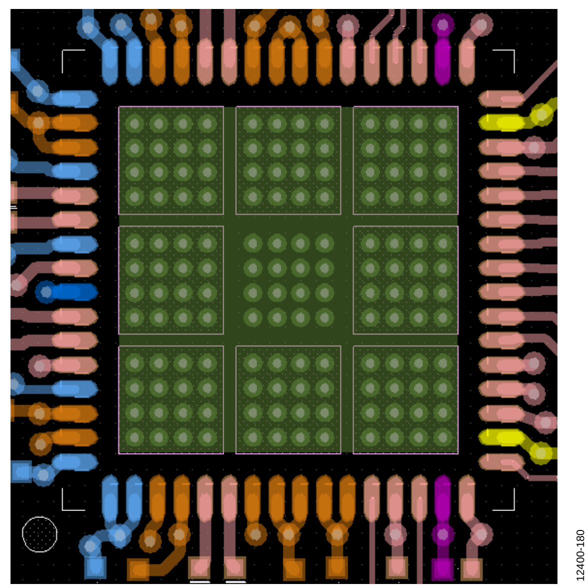

Figure 146. Recommended PCB Layout of Exposed Pad for the AD6674

AVDD1_SR (PIN 57) AND AGND (PIN 56, PIN 60)

AVDD1_SR (Pin 57) and AGND (Pin 56 and Pin 60) can be used to provide a separate power supply node to the SYSREF± circuits of the AD6674. If running in Subclass 1, the AD6674 can support periodic one-shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is needed.