

1.1 Scope.

This specification covers the detail requirements for a quad precision, low input current, low offset voltage, monolithic bipolar amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Part Number

AD704SE/883B

1.2.3 Case Outline.



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021106-A

| (X) Package | Description |
|-------------|-----------------------------------|
| E E-20A | 20-Terminal Leadless Chip Carrier |

1.3 Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$, unless otherwise noted).

| | |
|--|---|
| Supply Voltage | $\pm 18\text{ V}$ |
| Internal Power Dissipation ¹ | 650 mW |
| Input Voltage | $\pm V_S$ |
| Differential Input Voltage ² | $\pm 0.7\text{ V}$ |
| Output Short-Circuit Duration..... | Indefinite |
| Storage Temperature Range..... | -65°C to $+150^\circ\text{C}$ |
| Operating Temperature Range..... | -55°C to $+125^\circ\text{C}$ |
| Lead Temperature Range (Soldering 60 sec)..... | 300°C |

¹ Maximum package power dissipation vs. ambient temperature.

| Package Type | MAXIMUM AMBIENT Temperature for Rating | DERATE ABOVE MAXIMUM Ambient Temperature |
|--------------|--|--|
| LCC (E-20A) | 90°C | 5.7 mW/ $^\circ\text{C}$ |

² The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds $\pm 0.7\text{ V}$, external series protection resistors should be added to limit the input current to less than 25 mA.

1.4 Thermal Characteristics.

Thermal Resistance: $\theta_{JC} = 25^\circ\text{C}/\text{W}$ for E-20A Package
 $\theta_{JC} = 95^\circ\text{C}/\text{W}$ for E-20A Package

Rev. C

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Table 1.

| Test | Symbol | Sub Group | Limits | | Unit | Test Conditions ¹ |
|---------------------------------|------------------|-----------|--------|-----|------|--|
| | | | Min | Max | | |
| Input Offset Voltage | V _{OS} | 1 | | 150 | μV | |
| | | 2, 3 | | 250 | | |
| Power Supply Rejection Ratio | PSRR | 1 | 100 | | dB | ±2 V ≤ V _S ≤ ±18 V |
| | | 2, 3 | 100 | | | ±2.5 V ≤ V _S ≤ ±18 V |
| Input Bias Current ² | I _B | 1 | | 270 | pA | Either input, V _{CM} = 0 V |
| | | 2, 3 | | 600 | | |
| | I _B | 1 | | 300 | pA | Either input, V _{CM} = ±13.5 V |
| | | 2, 3 | | 700 | | |
| Input Offset Current | I _{OS} | 1 | | 250 | pA | V _{CM} = 0 V |
| | | 2, 3 | | 400 | | |
| | I _{OS} | 1 | | 300 | pA | V _{CM} = ±13.5 V |
| | | 2, 3 | | 500 | | |
| Matching Characteristics | V _{OS} | 1 | | 250 | μV | |
| | | 2, 3 | | 400 | | |
| | I _B | 1 | | 500 | pA | |
| | | 2, 3 | | 600 | | |
| | CMR | 1, 2, 3 | 94 | | dB | |
| PSR | 1, 2, 3 | 94 | | dB | | |
| Common-Mode Rejection Ratio | CMRR | 1 | 100 | | dB | V _{CM} = ±13.5 V |
| | | 2, 3 | 98 | | | |
| Open-Loop Gain | A _{OL} | 1 | 200 | | V/mV | V _O = ±12 V, R _L = 10 kΩ |
| | | 2, 3 | 150 | | | |
| | A _{OL} | 1 | 200 | | V/mV | V _O = ±10 V, R _L = 2 kΩ |
| | | 2, 3 | 100 | | | |
| Output Voltage Swing | V _{OUT} | 1, 2, 3 | ±13 | | V | R _L = 10 kΩ |
| Power Supply Quiescent Current | I _Q | 1 | | 2.5 | mA | |
| | | 2, 3 | | 2.8 | | |

¹ V_S = ±15 V, unless otherwise noted.

² Bias current specifications maximum at either input.

³ Input bias current match is the maximum difference between the corresponding inputs of all four amplifiers.

⁴ CMR match is the difference between ΔV_{OS}/ΔV_{CM} for any two amplifiers, expressed in dB.

⁵ PSR match is the difference between ΔV_{OS}/ΔV_{SUPPLY} for any two amplifiers, expressed in dB.