# Lithium Ion Battery Monitoring System

# AD7280A

## FEATURES

- 12-bit ADC, 1 µs per channel conversion time
- 6 analog input channels, common-mode range 0.5 V to 27.5 V
- 6 auxiliary ADC inputs
- ±1.6 mV cell voltage accuracy
- On-chip voltage regulator
- Cell balancing interface
- Daisy-chain interface
- Internal reference: ±3 ppm/°C
- 1.8 µA power-down current
- High input impedance
- Serial interface with alert function
- 1 SPI interface for up to 48 channels
- CRC protection on read and write commands
- On-chip registers for channel sequencing
- $V_{DD}$ operating range: 8 V to 30 V
- Temperature range: −40°C to +105°C
- 48-lead LQFP
- Qualified for automotive applications

## APPLICATIONS

- Lithium ion battery monitoring
- Electric and hybrid electric vehicles
- Power supply backup
- Power tools

## FUNCTIONAL BLOCK DIAGRAM

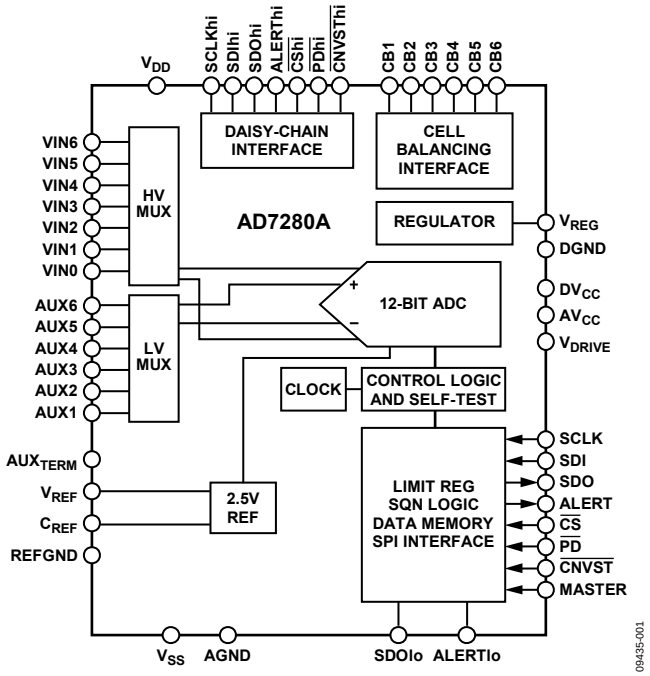


*Figure 1.*

## GENERAL DESCRIPTION

The AD7280A[1] contains all the functions required for general-purpose monitoring of stacked lithium ion batteries as used in hybrid electric vehicles, battery backup applications, and power tools. The part has multiplexed cell voltage and auxiliary ADC measurement channels for up to six cells of battery management. An internal ±3 ppm/°C reference is provided that allows a cell voltage accuracy of ±1.6 mV. The ADC resolution is 12 bits and allows conversion of up to 48 cells within 7 µs.

The AD7280A operates from a single $V_{DD}$ supply that has a range of 8 V to 30 V (with an absolute maximum rating of 33 V). The part provides six differential analog input channels to accommodate large common-mode signals across the full $V_{DD}$ range. Each channel allows an input signal range, VIN(+) − VIN(−), of 1 V to 5 V. The input pins assume a series stack of six cells. In addition, the part includes six auxiliary ADC input channels that can be used for temperature measurement or system diagnostics.

The AD7280A includes on-chip registers that allow a sequence of channel measurements to be programmed to suit the application requirements.

The AD7280A also includes a dynamic alert function that can detect whether the cell voltages or auxiliary ADC inputs exceed an upper or lower limit defined by the user. The AD7280A has cell balancing interface outputs designed to control external FET transistors to allow discharging of individual cells.

The AD7280A includes a built-in self-test feature that internally applies a known voltage to the ADC inputs.

A daisy-chain interface allows up to eight parts to be stacked without the need for individual device isolation.

The AD7280A requires only one supply pin that accepts 6.9 mA under normal operation while converting at 1 MSPS.

All this functionality is provided in a 48-lead LQFP package operating over a temperature range of −40°C to +105°C.

[1] Patents pending.

**Rev. 0**



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## REVISION HISTORY

**4/11—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 8 V to 30 V, $V_{SS}$ = 0 V, $DV_{CC}$ = $AV_{CC}$ = $V_{REG}$, $V_{DRIVE}$ = 2.7 V to 5.5 V, $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DC ACCURACY (VIN0 TO VIN6)[1] | | | | | |
| Resolution | 12 | | | Bits | No missing codes |
| Integral Nonlinearity | | ±1 | | LSB | |
| Differential Nonlinearity | | ±0.8 | | LSB | |
| Offset Error | | ±1 | | LSB | |
| Offset Error Match | | 1 | | LSB | |
| Gain Error | | ±1 | | LSB | |
| Gain Error Match | | 1 | | LSB | |
| ADC Unadjusted Error[2, 3] | | ±1.2 | | mV | |
| Total Unadjusted Error[4, 5] | | | ±9 | mV | $V_{IN}$ range[6] = 1 V to 4.1 V, −10°C to +85°C |
| | | | ±10 | mV | $V_{IN}$ range[6] = 1 V to 4.1 V, −40°C to +85°C |
| | | ±1.6 | ±14.5 | mV | $V_{IN}$ range[6] = 1 V to 4.1 V, −40°C to +105°C |
| CELL VOLTAGE INPUTS (VIN0 TO VIN6) | | | | | |
| Pseudo Differential Input Voltage | | | | | |
| VIN(x) − VIN(x − 1) | 1 | | 2 × $V_{REF}$ | V | |
| Absolute Input Voltage | $V_{CM}$ − $V_{REF}$ | | $V_{CM}$ + $V_{REF}$ | V | |
| Common-Mode Input Voltage | 0.5 | | 27.5 | V | |
| Static Leakage Current[7] | | ±5 | ±70 | nA | |
| Dynamic Leakage Current[7] | | | ±3 | nA | $\overline{\text{CNVST}}$ pulse every 100 ms |
| Input Capacitance | | 15 | | pF | |
| DC ACCURACY (AUX1 TO AUX6)[1, 8] | | | | | |
| Resolution | 12 | | | Bits | No missing codes |
| Integral Nonlinearity | | ±1 | | LSB | |
| Differential Nonlinearity | | ±0.8 | | LSB | |
| Offset Error | | ±2 | | LSB | |
| Offset Error Match | | 2 | | LSB | |
| Gain Error | | ±2 | | LSB | |
| Gain Error Match | | 2 | | LSB | |
| ADC Unadjusted Error[9] | | ±1.2 | | mV | |
| Total Unadjusted Error[10] | | | ±20 | mV | −40°C to +85°C |
| | | ±1.6 | ±22 | mV | −40°C to +105°C |
| AUXILIARY ADC INPUTS (AUX1 TO AUX6) | | | | | |
| Input Voltage Range | 0 | | 2 × $V_{REF}$ | V | |
| Static Leakage Current[7] | | ±15 | | nA | |
| Dynamic Leakage Current[7] | | | ±3 | nA | $\overline{\text{CNVST}}$ pulse every 100 ms |
| Input Capacitance | | 15 | | pF | |
| REFERENCE | | | | | |
| Reference Voltage | 2.494 | 2.5 | 2.506 | V | −40°C to +85°C |
| | 2.494 | 2.5 | 2.509 | V | −40°C to +105°C |
| Reference Voltage Temperature Coefficient | | ±3 | ±15 | ppm/°C | −40°C to +85°C |
| | | ±11 | | ppm/°C | −40°C to +105°C |
| Output Voltage Hysteresis | | 50 | | ppm | −40°C to +105°C |
| Long-Term Drift | | 150 | | ppm/1000 hours | |
| Line Regulation | | ±5 | | ppm/V | |
| Turn-On Settling Time[11, 12] | | 5.5 | 10 | ms | $V_{REG}$ = 1 µF, $V_{REF}$ = 1 µF, $C_{REF}$ = 100 nF |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| REGULATOR OUTPUT ($V_{REG}$) | | | | | |
| Input Voltage Range | 8 | | 30 | V | |
| Output Voltage, $V_{REG}$[13] | 4.9 | 5.2 | 5.5 | V | 5 mA external load |
| Output Current[14] | | | 5 | mA | |
| Line Regulation | | 0.5 | | mV/V | |
| Load Regulation | | 2.5 | | mV/mA | |
| Internal Short Protection Limit | | 25 | | mA | For a 10 Ω short |
| CELL BALANCING OUTPUTS[15] | | | | | |
| Output High Voltage, $V_{OH}$ | $V_{REG}$ − 1 | 5 | $V_{REG}$ + 0.2 | V | $I_{SOURCE}$ = 415 nA |
| Output Low Voltage, $V_{OL}$ | 0 | | | V | |
| CB1 Output Ramp-Up Time[16] | | 30 | | µs | For an 80 pF load |
| CB1 Output Ramp-Down Time[17] | | 30 | | µs | For an 80 pF load |
| CB2 to CB6 Output Ramp-Up Time[16] | | 380 | | µs | For an 80 pF load |
| CB2 to CB6 Output Ramp-Down Time[17] | | 30 | | µs | For an 80 pF load |
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | 2.4 | | | V | |
| Input Low Voltage, $V_{INL}$ | | | 0.4 | V | |
| Input Current, $I_{IN}$ | | | ±10 | µA | |
| Input Capacitance, $C_{IN}$ | | 5 | | pF | |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE}$ × 0.9 | | | V | $I_{SOURCE}$ = 200 µA |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 200 µA |
| Floating State Leakage Current | | | ±10 | µA | |
| Floating State Output Capacitance | | 5 | | pF | |
| Output Coding | | Straight binary | | | |

[1] For dc accuracy specifications, the LSB size for cell voltage measurements is (2 × $V_{REF}$ − 1 V)/4096. The LSB size for auxiliary ADC input voltage measurements is (2 × $V_{REF}$)/4096.
[2] ADC unadjusted error includes the INL of the ADC and the gain and offset errors of the VIN0 to VIN6 input channels.
[3] The conversion accuracy during cell balancing is decreased due to the activation of the cell balance circuitry. The ADC unadjusted error increases by a factor of 4.
[4] Total unadjusted error includes the INL of the ADC and the gain and offset errors of the VIN0 to VIN6 input channels, as well as the reference error, that is, the difference between the ideal and actual reference voltage and the temperature coefficient of the 2.5 V reference.
[5] The conversion accuracy during cell balancing is decreased due to the activation of the cell balance circuitry. The total unadjusted error increases by a factor of 4.
[6] For the full analog input range, that is, 1 V to 2 × $V_{REF}$, the total unadjusted error increases by 20%.
[7] The total current measured on the input pins while converting is the sum of the static and dynamic leakage currents. See the Terminology section.
[8] Bit D3 of the control register is set to 0 (thermistor termination resistor function is not in use).
[9] ADC unadjusted error includes the INL of the ADC and the gain and offset errors of the AUXx input channels.
[10] Total unadjusted error includes the INL of the ADC and the gain and offset errors of the AUXx input channels, as well as the reference error, that is, the difference between the ideal and actual reference voltage and the temperature coefficient of the 2.5 V reference.
[11] The turn-on settling time is the time from the rising edge of the $\overline{PD}$ signal until the conversion result settles to the specified accuracy. This includes the time required to power up the regulator and the reference. Note that a rising edge on the $\overline{CNVST}$ input is also required to power up the reference. This rising edge should occur after the rising edge on $\overline{PD}$.
[12] Sample tested during initial release to ensure compliance.
[13] The regulator output voltage is specified with an external 5 mA load in addition to the current required to drive the $AV_{CC}$, $DV_{CC}$, and $V_{DRIVE}$ supplies of the AD7280A.
[14] This specification refers to the maximum regulator output current that is available for external use.
[15] The CBx outputs can be set to 0 V or $V_{REG}$ with respect to the negative terminal of the cell being balanced.
[16] The CB1 to CB6 output ramp-up times are defined from the rising edge of the $\overline{CS}$ command until the CB output exceeds $V_{REG}$ − 1 V with respect to the negative terminal of the cell being balanced.
[17] The CB1 to CB6 output ramp-down times are defined from the rising edge of the $\overline{CS}$ command until the CB output falls below 50 mV with respect to the negative terminal of the cell being balanced.

## POWER SPECIFICATIONS

$V_{DD}$ = 8 V to 30 V, $V_{SS}$ = 0 V, $DV_{CC}$ = $AV_{CC}$ = $V_{REG}$, $V_{DRIVE}$ = 2.7 V to 5.5 V, $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | |
| $V_{DD}$ | 8 | | 30 | V | |
| Master Device | | | | | |
| $I_{DD}$ During Conversion | | 5.6 | 7.3 | mA | |
| $I_{DD}$ During Data Readback | | 5.3 | 7.0 | mA | |
| $I_{DD}$ During Cell Balancing | | 5.1 | 6.8 | mA | |
| $I_{DD}$ Software Power-Down | | 2.5 | 2.9 | mA | |
| $I_{DD}$ Full Power-Down Mode | | 1.8 | 5 | µA | |
| Slave Device | | | | | |
| $I_{DD}$ During Conversion | | 6.9 | 8.7 | mA | |
| $I_{DD}$ During Data Readback | | 6.5 | 8.2 | mA | |
| $I_{DD}$ During Cell Balancing | | 6.4 | 8.0 | mA | |
| $I_{DD}$ Software Power-Down | | 3.8 | 4.2 | mA | |
| $I_{DD}$ Full Power-Down Mode | | 1.8 | 5 | µA | |
| POWER DISSIPATION | | | | | |
| Master Device | | | | | $V_{DD}$ = 30 V |
| During Conversion | | 170 | 220 | mW | |
| During Data Readback | | 160 | 210 | mW | |
| During Cell Balancing | | 155 | 205 | mW | |
| Software Power-Down | | 75 | 90 | mW | |
| Full Power-Down Mode | | 54 | 150 | µW | |
| Slave Device | | | | | $V_{DD}$ = 30 V |
| During Conversion | | 210 | 265 | mW | |
| During Data Readback | | 195 | 250 | mW | |
| During Cell Balancing | | 192 | 240 | mW | |
| Software Power-Down | | 115 | 130 | mW | |
| Full Power-Down Mode | | 54 | 150 | µW | |

## TIMING SPECIFICATIONS

$V_{DD}$ = 8 V to 30 V, $V_{SS}$ = 0 V, $DV_{CC}$ = $AV_{CC}$ = $V_{REG}$, $V_{DRIVE}$ = 2.7 V to 5.5 V, $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 3.**

| Parameter[1] | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|
| $t_{CONV}$ | | | | | ADC conversion time |
| | 425 | 560 | 695 | ns | −40°C to +85°C |
| | 425 | | 720 | ns | −40°C to +105°C |
| $t_{ACQ}$ | | | | | ADC acquisition time, Bits[D6:D5] of the control register set to 00 |
| | 340 | 400 | 465 | ns | −40°C to +85°C |
| | 340 | | 470 | ns | −40°C to +105°C |
| $t_{ACQ}$ | | | | | ADC acquisition time, Bits[D6:D5] of the control register set to 01 |
| | 665 | 800 | 1010 | ns | −40°C to +85°C |
| | 665 | | 1030 | ns | −40°C to +105°C |
| $t_{ACQ}$ | | | | | ADC acquisition time, Bits[D6:D5] of the control register set to 10 |
| | 1005 | 1200 | 1460 | ns | −40°C to +85°C |
| | 1005 | | 1510 | ns | −40°C to +105°C |
| $t_{ACQ}$ | | | | | ADC acquisition time, Bits[D6:D5] of the control register set to 11 |
| | 1340 | 1600 | 1890 | ns | −40°C to +85°C |
| | 1340 | | 1945 | ns | −40°C to +105°C |
| $t_{DELAY}$ | | 200 | 250 | ns | Propagation delay between the falling edges of $\overline{CNVST}$ of adjacent parts in the daisy chain |
| $t_{WAIT}$ | 5 | | | µs | Time required between the end of conversions and the beginning of readback of the conversion results |
| $f_{SCLK}$ | | | 1 | MHz | Frequency of serial read clock |
| $t_{QUIET}$ | 200 | | | ns | Minimum quiet time required between the end of a serial read and the start of the next conversion |
| $t_1$[2] | 0.4 | | 50 | µs | $\overline{CNVST}$ low pulse |
| $t_2$ | 10 | | | ns | $\overline{CS}$ falling edge to SCLK rising edge |
| $t_3$ | | | 20 | ns | Delay from $\overline{CS}$ falling edge until SDO is three-state disabled |
| $t_4$ | 5 | | | ns | SDI setup time prior to SCLK falling edge |
| $t_5$ | 4 | | | ns | SDI hold time after SCLK falling edge |
| $t_6$[3] | | | 28 | ns | Data access time after SCLK rising edge |
| $t_7$ | 20 | | | ns | SCLK to data valid hold time |
| $t_8$ | 0.45 × $t_{SCLK}$ | | | ns | SCLK high pulse width |
| $t_9$ | 0.45 × $t_{SCLK}$ | | | ns | SCLK low pulse width |
| $t_{10}$[4] | 100 | | | ns | $\overline{CS}$ rising edge to SCLK rising edge |
| $t_{11}$ | | | 10 | ns | $\overline{CS}$ rising edge to SDO high impedance |
| $t_{12}$ | 3 | | | µs | $\overline{CS}$ high time required between each 32-bit write/read command |

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $V_{DRIVE}$) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.
[2] Maximum allowed $\overline{CNVST}$ low pulse time to ensure that a software power-down state is not entered when the $\overline{CNVST}$ pin is not gated.
[3] Time required for the output to cross 0.4 V or 2.4 V.
[4] $t_{10}$ applies when using a continuous SCLK. Guaranteed by design.

### *Timing Diagram*

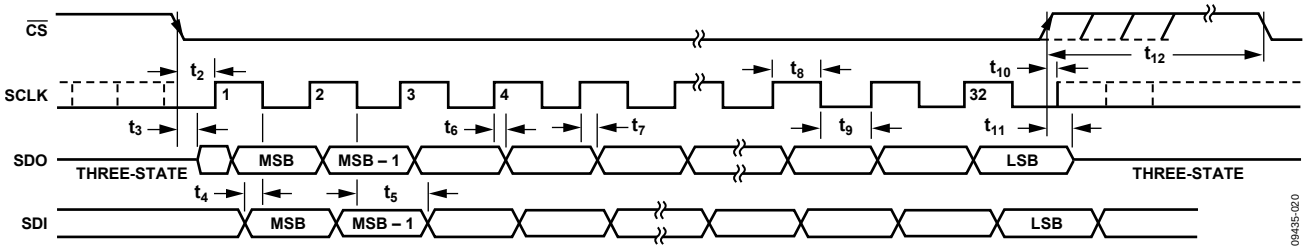


*Figure 2. Serial Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to $V_{SS}$, AGND | −0.3 V to +33 V |
| $V_{SS}$ to AGND, DGND | −0.3 V to +0.3 V |
| VIN0 to VIN5 Voltage to $V_{SS}$, AGND | $V_{SS}$ − 0.3 V to $V_{DD}$ + 0.3 V |
| VIN6 Voltage to $V_{SS}$, AGND | $V_{DD}$ − 0.3 V to $V_{DD}$ + 1 V |
| CB1 Output to $V_{SS}$, AGND | −0.3 V to $DV_{CC}$ + 0.3 V |
| CBx Output to VIN(x − 1)[1] | −0.3 V to VIN(x − 1)[1] + 7 V |
| AUX1 to AUX6 Voltage to $V_{SS}$, AGND | −0.3 V to $AV_{CC}$ + 0.3 V |
| $AUX_{TERM}$ Voltage to $V_{SS}$, AGND | −0.3 V to $AV_{CC}$ + 0.3 V |
| $AV_{CC}$ to $V_{SS}$, AGND, DGND | −0.3 V to +7 V |
| $DV_{CC}$ to $AV_{CC}$ | −0.3 V to +0.3 V |
| $DV_{CC}$ to $V_{SS}$, DGND | −0.3 V to +7 V |
| $V_{DRIVE}$ to $V_{SS}$, AGND | −0.3 V to +7 V |
| AGND to DGND | −0.3 V to +0.3 V |
| Digital Input Voltage to $V_{SS}$, DGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Digital Output Voltage to $V_{SS}$, DGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Input Current to Any Pin Except Supply Pins[2] | ±10 mA |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Pb-Free Temperature, Soldering Reflow | 260(+0)°C |
| ESD | 2 kV |

[1] x = 2 to 6.
[2] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

To conform with IPC 2221 industrial standards, it is advisable to use conformal coating on the high voltage pins.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 5. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 48-Lead LQFP (ST-48) | 76.2 | 17 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

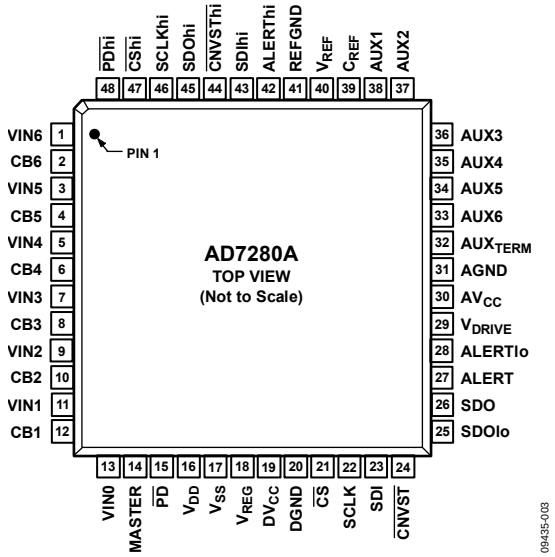


*Figure 3. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 3, 5, 7, 9, 11, 13 | VIN6 to VIN0 | Analog Input 6 to Analog Input 0. VIN0 should be connected to the base of the series-connected battery cells. VIN1 should be connected to the top of Cell 1, VIN2 should be connected to the top of Cell 2, and so on (see Figure 28 and Figure 29). |
| 2, 4, 6, 8, 10, 12 | CB6 to CB1 | Cell Balance Output 6 to Cell Balance Output 1. These pins provide a voltage output that can be used to supply the gate drive of an external cell balancing transistor. Each CBx output provides a 0 V or 5 V voltage output referenced to the absolute amplitude of the negative terminal of the battery cell that is being balanced. |
| 14 | MASTER | Voltage Input. Connect the MASTER pin of the AD7280A that is connected directly to the DSP/microprocessor to the $V_{DD}$ supply pin through a 10 kΩ resistor. In an application with two or more AD7280As in a daisy chain, the MASTER pins of the remaining AD7280As in the daisy chain should be tied to their respective $V_{SS}$ supply pins through 10 kΩ resistors. |
| 15 | $\overline{PD}$ | Power-Down Input. This input is used to power down the AD7280A. When the AD7280A acts as a master, the $\overline{PD}$ input is supplied from the DSP/microprocessor. When the AD7280A acts as a slave in a daisy chain, the $\overline{PD}$ input should be connected to the $\overline{PDhi}$ output of the AD7280A immediately below it in potential in the daisy chain. |
| 16 | $V_{DD}$ | Positive Power Supply Voltage for the High Voltage Analog Input Structure of the AD7280A. The supply must be greater than the minimum voltage of 8 V. $V_{DD}$ can be supplied directly from the cell with the highest potential of the four, five, or six cell battery stacks that the AD7280A is monitoring. The maximum voltage that should be applied between $V_{DD}$ and $V_{SS}$ is 30 V. Place 10 µF and 100 nF decoupling capacitors on the $V_{DD}$ pin. |
| 17 | $V_{SS}$ | Negative Power Supply Voltage for the High Voltage Analog Input Structure of the AD7280A. This input should be at the same potential as the AGND/DGND voltage. |
| 18 | $V_{REG}$ | Analog Voltage Output, 5.2 V. The internally generated $V_{REG}$ voltage, which provides the supply voltage for the ADC core, is available on this pin for use external to the AD7280A. Place 1 µF and 100 nF decoupling capacitors on the $V_{REG}$ pin. |
| 19 | $DV_{CC}$ | Digital Supply Voltage, 4.9 V to 5.5 V. The $DV_{CC}$ and $AV_{CC}$ voltages should ideally be at the same potential. For best performance, it is recommended that the $DV_{CC}$ and $AV_{CC}$ pins be shorted together to ensure that the voltage difference between them never exceeds 0.3 V, even on a transient basis. This supply should be decoupled to DGND. Place 100 nF decoupling capacitors on the $DV_{CC}$ pin. The $DV_{CC}$ supply pin should be connected to the $V_{REG}$ output. |
| 20 | DGND | Digital Ground. Ground reference point for all digital circuitry on the AD7280A. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 21 | $\overline{CS}$ | Chip Select Input. The $\overline{CS}$ input is used to frame the input and output data on the SPI and daisy-chain interfaces. On the master AD7280A device, the $\overline{CS}$ input is supplied from the DSP/microprocessor. When the AD7280A acts as a slave in a daisy chain, this input should be connected to the $\overline{CS}$hi output of the AD7280A immediately below it in potential in the daisy chain. |
| 22 | SCLK | Serial Clock Input. On the master AD7280A device, the SCLK input is supplied from the DSP/microprocessor. When the AD7280A acts as a slave in a daisy chain, this input should be connected to the SCLKhi output of the AD7280A immediately below it in potential in the daisy chain. |
| 23 | SDI | Serial Data Input. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7280A on the falling edge of the SCLK input. On the master AD7280A device, SDI is the data input of the SPI interface. When the AD7280A acts as a slave in a daisy chain, this input accepts data from the SDOhi output of the AD7280A immediately below it in potential in the daisy chain. |
| 24 | $\overline{CNVST}$ | Convert Start Input. The conversion is initiated on the falling edge of $\overline{CNVST}$. On the master AD7280A, the $\overline{CNVST}$ pulse is supplied from the DSP/microprocessor; this input can also be tied to $DV_{CC}$ and the conversion initiated through the serial interface. When the AD7280A acts as a slave in a daisy chain, this input should be connected to the $\overline{CNVST}$hi output of the AD7280A immediately below it in potential in the daisy chain. |
| 25 | SDOlo | Serial Data Output in Daisy-Chain Mode. On the master AD7280A device, this output should be connected to $V_{SS}$ either directly or through a pull-down, 1 kΩ resistor. When the AD7280A acts as a slave in a daisy chain, this output should be connected to the SDIhi input of the AD7280A immediately below it in potential in the daisy chain. |
| 26 | SDO | Serial Data Output. The conversion output data or the register output data is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the SCLK input; 32 SCLKs are required to access the data. On the master AD7280A device, the SDO output should be connected to the DSP/microprocessor. The SDO outputs of the remaining AD7280As in the daisy chain should be connected to $V_{SS}$ either directly or through a pull-down, 1 kΩ resistor. |
| 27 | ALERT | Digital Output. This flag indicates cell or auxiliary ADC input overvoltage or undervoltage. The ALERT output of the master AD7280A should be connected to the DSP/microprocessor. The ALERT outputs of the remaining AD7280As in the daisy chain should be connected to $V_{SS}$ either directly or through a pull-down, 1 kΩ resistor. |
| 28 | ALERTlo | Alert Output in Daisy-Chain Mode. On the master AD7280A, this output should be connected to $V_{SS}$ either directly or through a pull-down, 1 kΩ resistor. When the AD7280A acts as a slave in a daisy chain, this output should be connected to the ALERThi input of the AD7280A immediately below it in potential in the daisy chain. |
| 29 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage supplied at this pin determines the voltage at which the SPI interface operates. This pin should be decoupled to DGND. On the master AD7280A device, the voltage range on this pin is 2.7 V to 5.5 V. The $V_{DRIVE}$ voltage can be different from the voltage at $AV_{CC}$ and $DV_{CC}$, but it should never exceed either by more than 0.3 V. The $V_{DRIVE}$ pin of the remaining AD7280As in the daisy chain should be connected to $V_{REG}$. |
| 30 | $AV_{CC}$ | Analog Supply Voltage for the ADC Core, 4.9 V to 5.5 V. The $AV_{CC}$ and $DV_{CC}$ voltages should ideally be at the same potential. For best performance, it is recommended that the $AV_{CC}$ and $DV_{CC}$ pins be shorted together to ensure that the voltage difference between them never exceeds 0.3 V, even on a transient basis. This supply should be decoupled to AGND. Place 100 nF decoupling capacitors on the $AV_{CC}$ pin. The $AV_{CC}$ supply pin should be connected to the $V_{REG}$ output. |
| 31 | AGND | Analog Ground. This pin is the ground reference point for all analog circuitry on the AD7280A. This input should be at the same potential as the base of the series-connected battery cells. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 32 | $AUX_{TERM}$ | Thermistor Termination Resistor Input. If this function is not required in the application, it is recommended that this pin be connected to $V_{REG}$ through a 10 kΩ resistor. |
| 33 to 38 | AUX6 to AUX1 | Auxiliary, Single-Ended 5 V ADC Inputs. If any of these inputs is not required in the application, it is recommended that the pin be connected to $V_{REG}$ through a 10 kΩ resistor. |
| 39 | $C_{REF}$ | Reference Capacitor. A 100 nF decoupling capacitor to REFGND should be placed on this pin. |
| 40 | $V_{REF}$ | Reference Output, 2.5 V. The on-chip reference is available on this pin for use external to the AD7280A. A 1 µF decoupling capacitor to REFGND is recommended on this pin. |
| 41 | REFGND | Reference Ground. This pin is the ground reference point for the internal band gap reference circuitry on the AD7280A. The REFGND voltage should be at the same potential as the AGND voltage. |
| 42 | ALERThi | Alert Input in Daisy-Chain Mode. The alert signal from each AD7280A in the daisy chain is passed through the ALERTlo output and the ALERThi input of each AD7280A in the chain and is supplied to the DSP/microprocessor through the ALERT output of the master AD7280A. This input should be connected to the ALERTlo output of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require an alert input; in this case, the pin should be connected to $V_{DD}$ through a 1 kΩ resistor. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 43 | SDIhi | Serial Data Input in Daisy-Chain Mode. The data from each AD7280A in the daisy chain is passed through the SDOlo output and the SDIhi input of each AD7280A in the chain and is supplied to the DSP/microprocessor through the SDO output of the master AD7280A. This input should be connected to the SDOlo output of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a serial data input in daisy-chain mode; in this case, the pin should be connected to $V_{DD}$ through a 1 kΩ resistor. |
| 44 | $\overline{\text{CNVSThi}}$ | Conversion Start Output in Daisy-Chain Mode. The convert start signal from the DSP/microprocessor supplied to the $\overline{\text{CNVST}}$ input of the master AD7280A is passed through each AD7280A by means of the $\overline{\text{CNVST}}$ input and the $\overline{\text{CNVSThi}}$ output. This output should be connected to the $\overline{\text{CNVST}}$ pin of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain conversion start output; in this case, the pin should be connected to $V_{DD}$. |
| 45 | SDOhi | Serial Data Output in Daisy-Chain Mode. The serial data input from the DSP/microprocessor supplied to the SDI input of the master AD7280A is passed through each AD7280A by means of the SDI input and the SDOhi output. This output should be connected to the SDI input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain serial data output; in this case, the pin should be connected to $V_{DD}$. |
| 46 | SCLKhi | Serial Clock Output in Daisy-Chain Mode. The clock signal from the DSP/microprocessor supplied to the SCLK input of the master AD7280A is passed through each AD7280A by means of the SCLK input and the SCLKhi output. This output should be connected to the SCLK input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain serial clock output; in this case, the pin should be connected to $V_{DD}$. |
| 47 | $\overline{\text{CShi}}$ | Chip Select Output in Daisy-Chain Mode. The chip select signal from the DSP/microprocessor supplied to the $\overline{\text{CS}}$ input of the master AD7280A is passed through each AD7280A by means of the $\overline{\text{CS}}$ input and the $\overline{\text{CShi}}$ output. This output should be connected to the $\overline{\text{CS}}$ input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain chip select output; in this case, the pin should be connected to $V_{DD}$. |
| 48 | $\overline{\text{PDhi}}$ | Power-Down Output in Daisy-Chain Mode. The power-down signal from the DSP/microprocessor supplied to the $\overline{\text{PD}}$ input of the master AD7280A is passed through each AD7280A by means of the $\overline{\text{PD}}$ input and the $\overline{\text{PDhi}}$ output. This output should be connected to the $\overline{\text{PD}}$ input of the AD7280A immediately above it in potential in the daisy chain. The AD7280A at the highest potential in the stack does not require a daisy-chain power-down output; in this case, the pin should be connected to $V_{DD}$. |

# TYPICAL PERFORMANCE CHARACTERISTICS

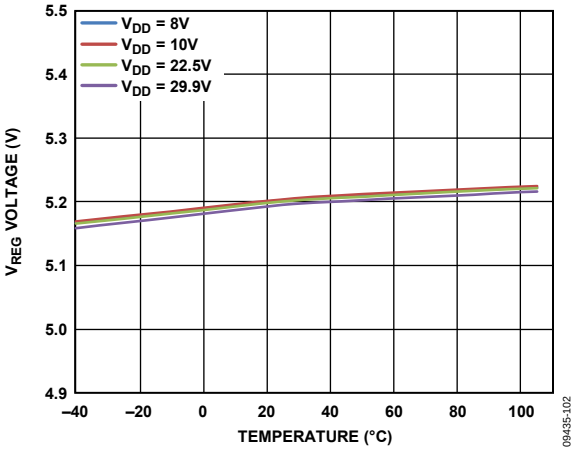


*Figure 4. $V_{REG}$ vs. Temperature for Different Supply Voltages, $V_{REG}$ Connected to $AV_{CC}$ and $DV_{CC}$*

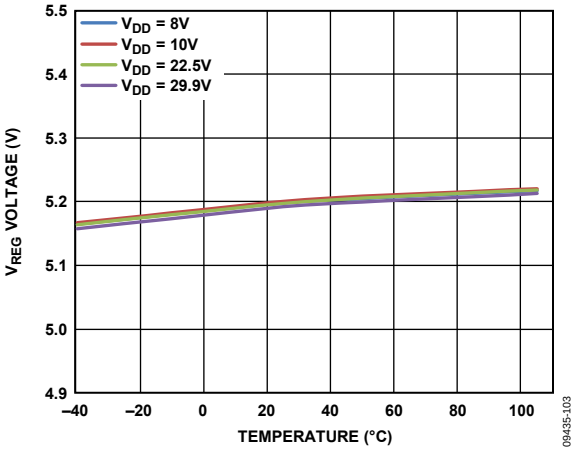


*Figure 5. $V_{REG}$ vs. Temperature for Different Supply Voltages, $V_{REG}$ Connected to $AV_{CC}$ and $DV_{CC}$, 5 mA External Load*

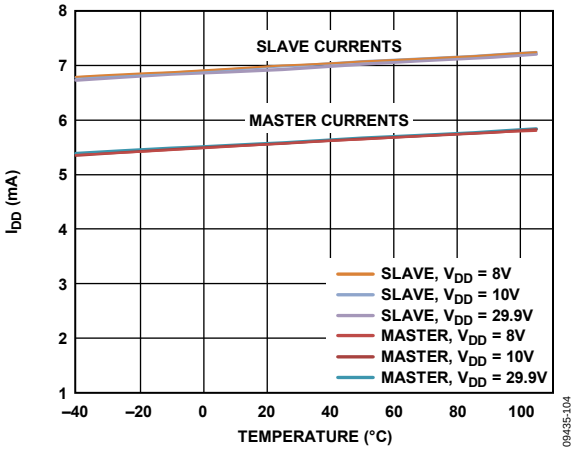


*Figure 6. $I_{DD}$ During Conversion vs. Temperature for Different Supply Voltages*

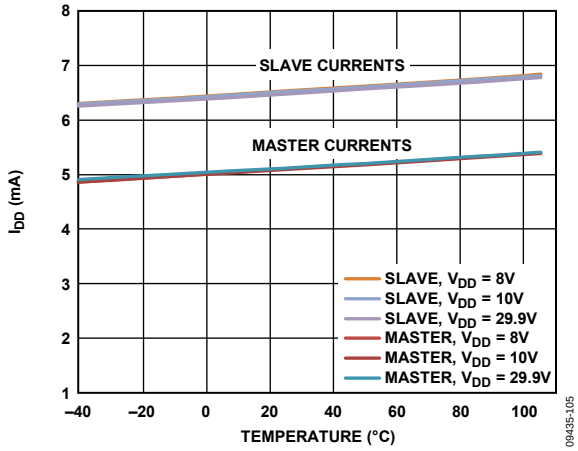


*Figure 7. $I_{DD}$ During Cell Balancing vs. Temperature for Different Supply Voltages*

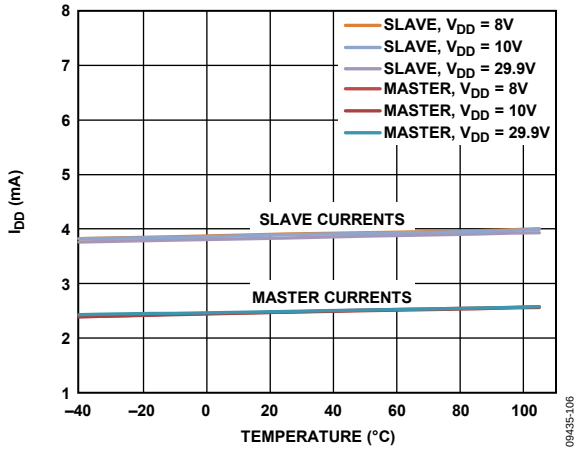


*Figure 8. $I_{DD}$ During Software Power-Down vs. Temperature for Different Supply Voltages*

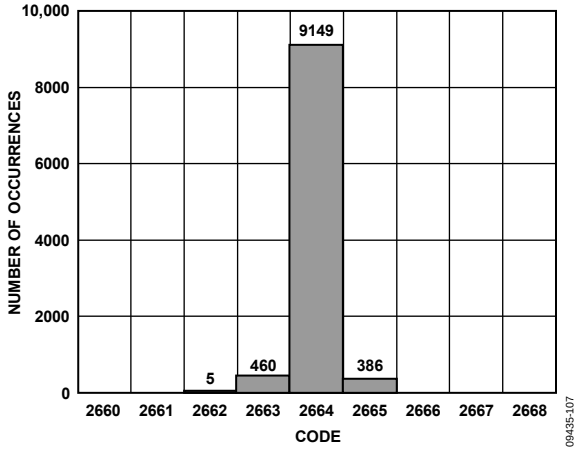


*Figure 9. Histogram of Codes for 10,000 Samples, Odd Cell Voltage Channels*

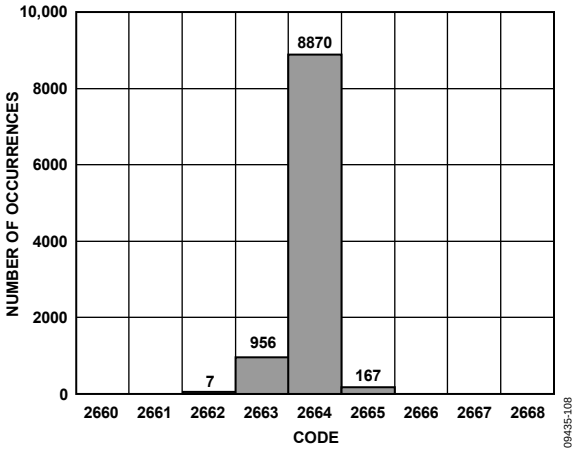


Figure 10. Histogram of Codes for 10,000 Samples, Even Cell Voltage Channels

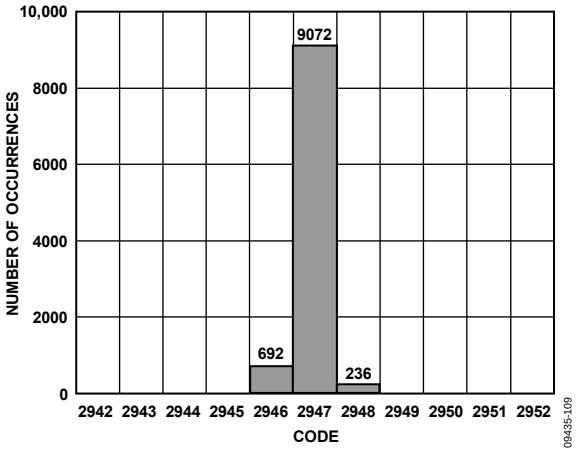


Figure 11. Histogram of Codes for 10,000 Samples, Auxiliary Channels

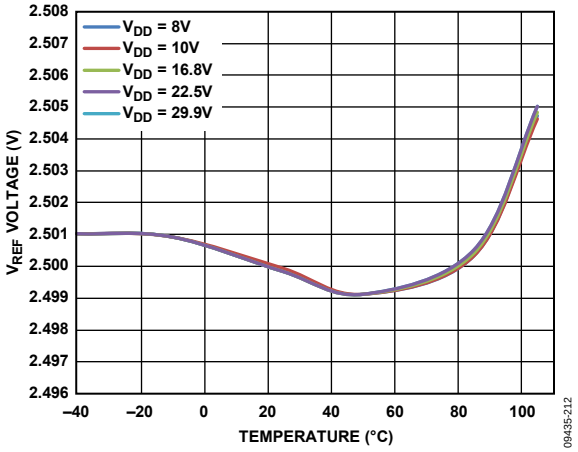


Figure 12. $V_{REF}$ vs. Temperature for Different Supply Voltages

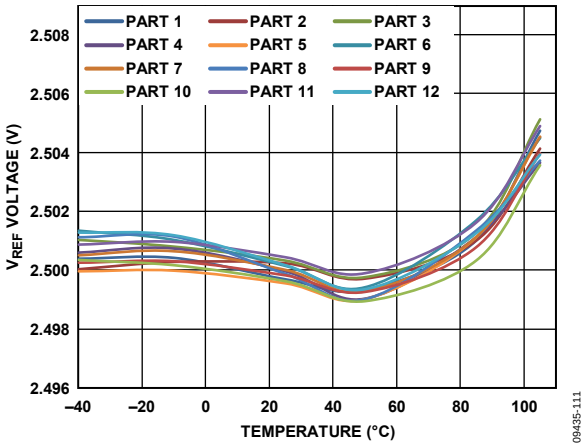


Figure 13. $V_{REF}$ vs. Temperature for Different Parts

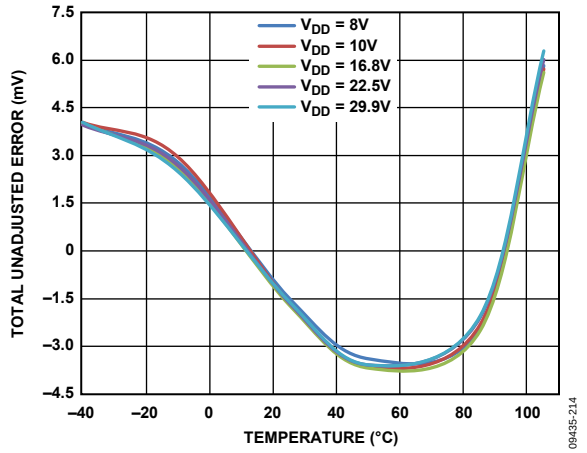


Figure 14. Total Unadjusted Error for Even Cell Voltage Channels (Absolute Value) vs. Temperature for Different Supply Voltages

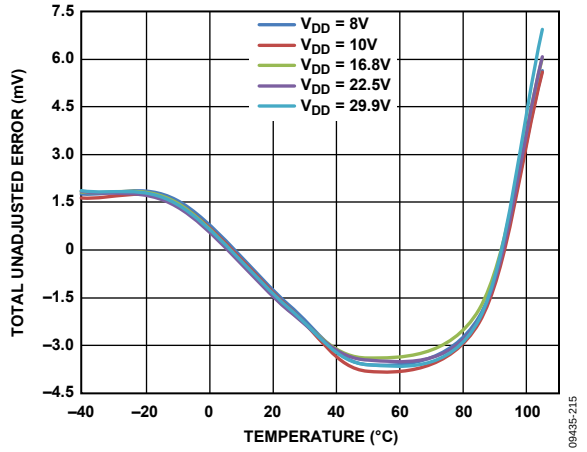


Figure 15. Total Unadjusted Error for Odd Cell Voltage Channels (Absolute Value) vs. Temperature for Different Supply Voltages

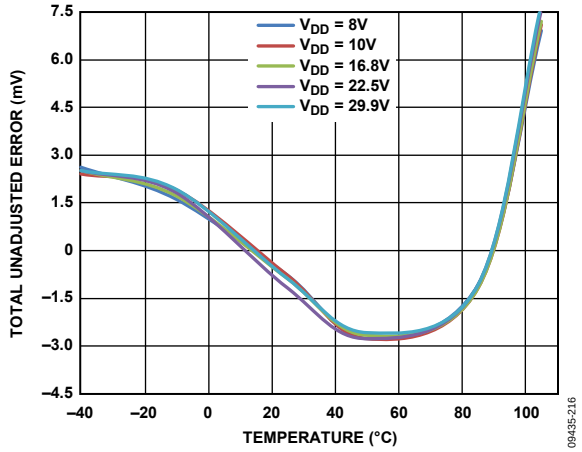


Figure 16. Total Unadjusted Error for Auxiliary Channels (Absolute Value) vs. Temperature for Different Supply Voltages

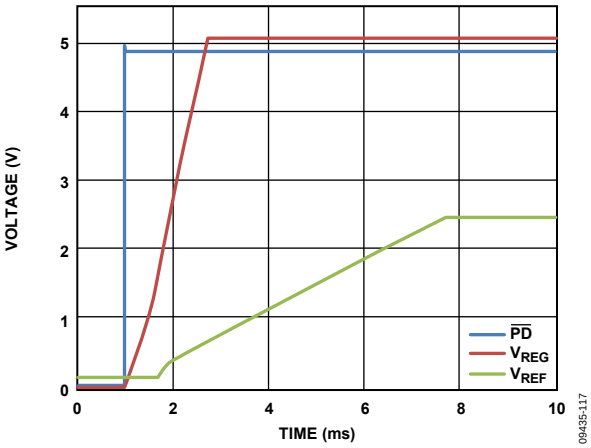


Figure 19. Power-Up Time, 10 µF Capacitor on the $V_{REF}$ and $V_{REG}$ Pins

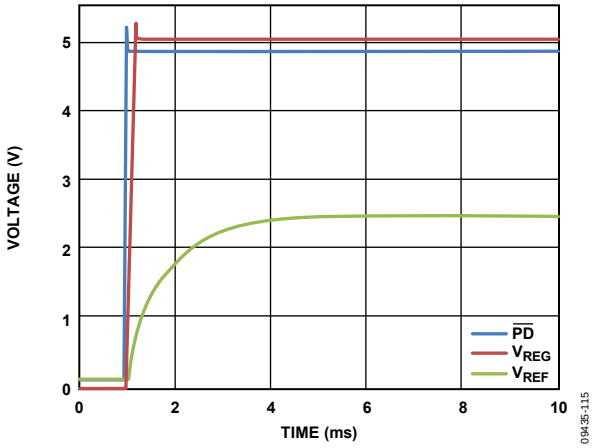


Figure 17. Power-Up Time, 1 µF Capacitor on the $V_{REF}$ and $V_{REG}$ Pins

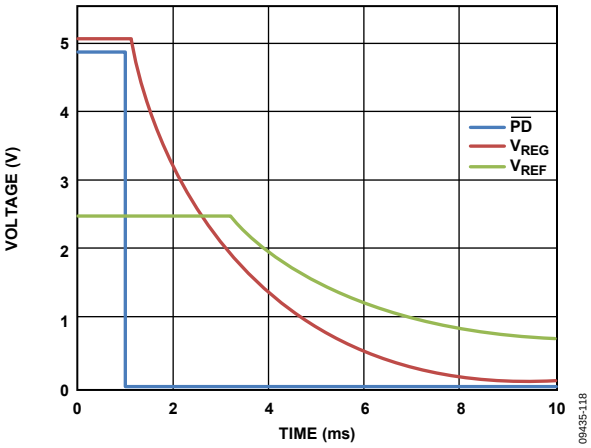


Figure 20. Power-Down Time, 10 µF Capacitor on the $V_{REF}$ and $V_{REG}$ Pins

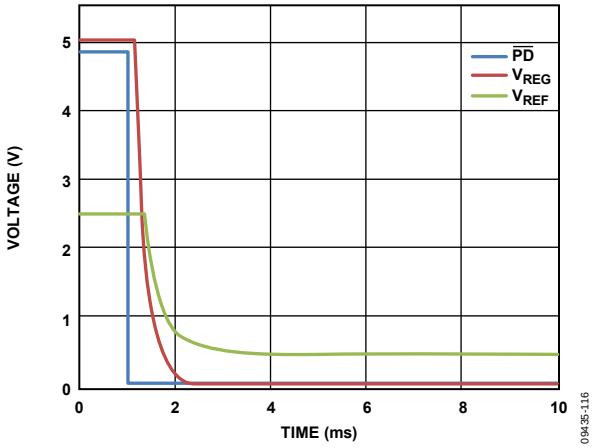


Figure 18. Power-Down Time, 1 µF Capacitor on the $V_{REF}$ and $V_{REG}$ Pins

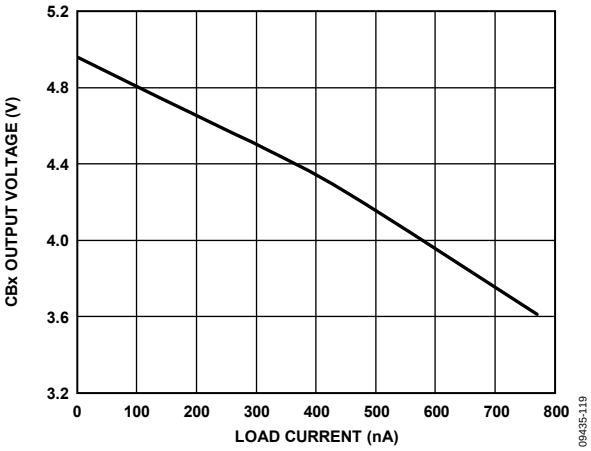


Figure 21. CBx Output Voltage vs. Load Current

# TERMINOLOGY

**Differential Nonlinearity (DNL)**
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Integral Nonlinearity (INL)**
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

**Offset Error**
Offset error applies to straight binary output coding. It is the deviation of the first code transition (000 ... 000) to (000 ... 001) from the ideal, that is, AGND + 1 LSB for AUX1 to AUX6 and 1 V + AGND + 1 LSB for VIN0 to VIN6.

**Offset Error Match**
Offset error match is the difference in zero code error across all six channels.

**Gain Error**
Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, 2 × $V_{REF}$ − 1 LSB) after adjusting for the offset error.

**Gain Error Match**
Gain error match is the difference in gain error across all six channels.

**ADC Unadjusted Error**
ADC unadjusted error includes the INL error and the offset and gain errors of the ADC and measurement channel.

**Total Unadjusted Error (TUE)**
TUE is the maximum deviation of the output code from the ideal. Total unadjusted error includes the INL error, the offset and gain errors, and the reference errors. Reference errors include the difference between the actual and ideal reference voltage (that is, 2.5 V) and the reference voltage temperature coefficient.

**Reference Voltage Temperature Coefficient**
The reference voltage temperature coefficient is derived from the maximum and minimum reference output voltage ($V_{REF}$) measured between $T_{MIN}$ and $T_{MAX}$. It is expressed in ppm/°C using the following equation:

$$TCV_{REF}\,(\text{ppm}/^\circ\text{C}) = \left(\frac{V_{REF}(Max) - V_{REF}(Min)}{2.5\,\text{V} \times (T_{MAX} - T_{MIN})}\right) \times 10^6$$

where:
$V_{REF}(Max)$ is the maximum $V_{REF}$ between $T_{MIN}$ and $T_{MAX}$.
$V_{REF}(Min)$ is the minimum $V_{REF}$ between $T_{MIN}$ and $T_{MAX}$.
$T_{MAX}$ = +85°C or +105°C.
$T_{MIN}$ = −40°C.

**Output Voltage Hysteresis**
Output voltage hysteresis, or thermal hysteresis, is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either T_HYS+ or T_HYS−, where:

*T_HYS*+ = +25°C to $T_{MAX}$ to +25°C
*T_HYS*− = +25°C to $T_{MIN}$ to +25°C

Output voltage hysteresis is expressed in ppm using the following equation:

$$V_{HYS}\,(\text{ppm}) = \left(\frac{V_{REF}(25^\circ\text{C}) - V_{REF}(T\_HYS)}{V_{REF}(25^\circ\text{C})}\right) \times 10^6$$

where:
$V_{REF}$(25°C) = $V_{REF}$ at 25°C.
$V_{REF}(T\_HYS)$ is the maximum change of $V_{REF}$ at T_HYS+ or T_HYS−.

**Static Leakage Current**
Static leakage current is the current measured on the cell voltage and/or the auxiliary ADC inputs when the device is static, that is, not converting.

**Dynamic Leakage Current**
Dynamic leakage current is the current measured on the cell voltage and/or the auxiliary ADC inputs when the device is converting, with the static leakage current subtracted. Dynamic leakage current is specified with a convert start pulse frequency of 10 Hz, that is, every 100 ms. The dynamic leakage current for a different conversion rate can be calculated using the following equation:

$$I_{DYN(B)} = \left(\frac{I_{DYN(A)} \times f_{CNVST(B)}}{f_{CNVST(A)}}\right)$$

where:
$I_{DYN(A)}$ is the dynamic leakage current at the convert start frequency, $f_{CNVST(A)}$ (see Table 1).
$I_{DYN(B)}$ is the dynamic leakage current at the desired convert start frequency, $f_{CNVST(B)}$.

# THEORY OF OPERATION

## CIRCUIT INFORMATION

The AD7280A is a lithium ion (Li-Ion) battery monitoring chip that can monitor the voltage and temperature of four, five, or six series-connected Li-Ion battery cells. The AD7280A also provides an interface that can be used to control external transistors for cell balancing.

The $V_{DD}$ and $V_{SS}$ supplies required by the AD7280A should be taken from battery cells being monitored by the part. An internal $V_{REG}$ rail is generated to provide power for the ADC and the internal interface circuitry. This $V_{REG}$ voltage is available on an output pin for use external to the AD7280A.

The AD7280A consists of a high voltage input multiplexer, a low voltage input multiplexer, and a SAR ADC. The high voltage multiplexer allows four, five, or six series-connected Li-Ion battery cells to be measured. The low voltage multiplexer provides the user with six single-ended ADC inputs that can be used in combination with external thermistors to measure the temperature of each battery cell. The auxiliary ADC inputs can also be used for external diagnostics in the application. Initiating conversions on all 12 channels, that is, the six cell voltage channels and the six auxiliary ADC channels, requires only a single $\overline{\text{CNVST}}$ pulse. Alternatively, the conversion can be initiated through the rising edge of $\overline{\text{CS}}$. Each conversion result is stored in an individual result register (see Table 13).

Each individual cell voltage and auxiliary ADC measurement requires a minimum of 1 µs to acquire and complete a conversion. Depending on the external components connected to the analog inputs of the AD7280A, additional acquisition time may be required. A higher acquisition time can be selected through the control register. The AD7280A also provides a conversion averaging option that can be selected through the control register. This option allows the user to complete two, four, or eight averages on each cell voltage and auxiliary ADC measurement. The averaged conversion results are stored in the result registers. On power-up, the default combined acquisition and conversion time is 1 µs, with the averaging register set to 0, that is, a single conversion per channel.

The results of the cell voltage and auxiliary ADC conversions are read back via the 4-wire serial peripheral interface (SPI). The SPI is also used to write to and read from the internal registers.

The AD7280A features an alert function that can be triggered if the voltage conversion results or the auxiliary ADC conversion results exceed the maximum and minimum voltage thresholds selected by the user. The alert modes and threshold levels are selected by writing to internal registers.

The AD7280A provides six analog output voltages that can be used to control external transistors as part of a cell balancing circuit. Each cell balance output provides a 0 V or 5 V voltage, with respect to the potential on the base of each individual cell, that can be applied to the gate of the external cell balancing transistors.

The AD7280A features a daisy-chain interface. Individual AD7280A devices can monitor the cell voltages and temperatures of six cells. A chain of AD7280As can be used to monitor the cell voltages and temperatures of a larger number of cells. The conversion data from each AD7280A in the chain passes to the system controller via a single SPI interface. Control data can similarly be passed via the SPI up the chain to each individual AD7280A.

The AD7280A includes an on-chip 2.5 V reference. The reference voltage is available for use external to the AD7280A.

The AD7280A also has a $V_{DRIVE}$ feature to control the voltage at which the serial interface operates. $V_{DRIVE}$ allows the ADC to easily interface to both 3 V and 5 V processors. For example, in the recommended configuration, the AD7280A is operated with a supply of 5 V; however, the $V_{DRIVE}$ pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors.

## CONVERTER OPERATION

The conversion paths of the AD7280A consist of a high voltage input multiplexer or a low voltage input multiplexer and a SAR ADC. The high voltage multiplexer selects the pair of analog inputs, VIN0 to VIN6, that is to be converted. The voltage of each individual cell is measured by converting the difference between adjacent analog inputs, that is, VIN1 − VIN0, VIN2 − VIN1, and so on (see Figure 22 and Figure 23). The low voltage multiplexer selects the auxiliary ADC input, AUX1 to AUX6, that is to be converted. The conversion results for each cell voltage and auxiliary ADC input can be accessed $t_{WAIT}$ after the programmed conversion sequence is completed.

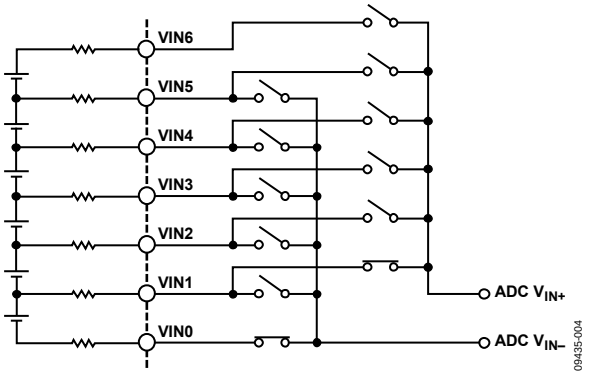


*Figure 22. Mux Configuration During VIN1 to VIN0 Sampling*

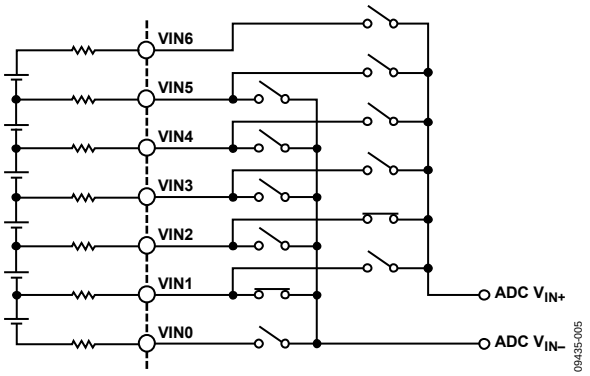


*Figure 23. Mux Configuration During VIN2 to VIN1 Sampling*

The ADC is a successive approximation register analog-to-digital converter (SAR ADC). The converter is composed of a comparator, a SAR, control logic, and two capacitive DACs. Figure 24 shows a simplified schematic of the converter. During the acquisition phase, the SW1, SW2, and SW3 switches are closed. The sampling capacitor array acquires the signal on the input during this phase.

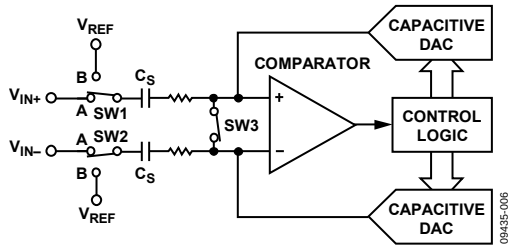


*Figure 24. ADC Configuration During Acquisition Phase*

When the ADC starts a conversion, SW3 opens, and SW1 and SW2 move to Position B, causing the comparator to become unbalanced (see Figure 25). The control logic and capacitive DACs are used to add and subtract fixed amounts of charge to return the comparator to a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. This output code is then stored in the appropriate register for the input that has been converted.

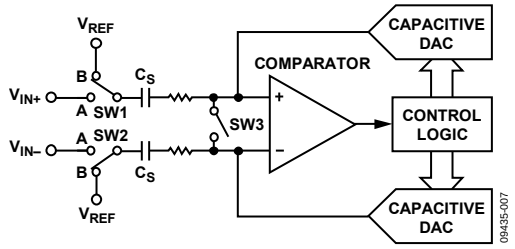


*Figure 25. ADC Configuration During Conversion Phase*

## ANALOG INPUT STRUCTURE

Figure 26 shows the equivalent circuit of the analog input structure of the AD7280A. The diodes provide ESD protection. The resistors are lumped components made up of the on resistance of the input multiplexer, internal track resistance, and other internal switches. The value of these resistors is approximately 300 Ω typical. Capacitor C1 is also a lumped component made up of pin capacitance, ESD diodes, and switch capacitance, whereas Capacitor C2 is the sampling capacitor of the ADC. The total lumped capacitance of C1 and C2 is approximately 15 pF.

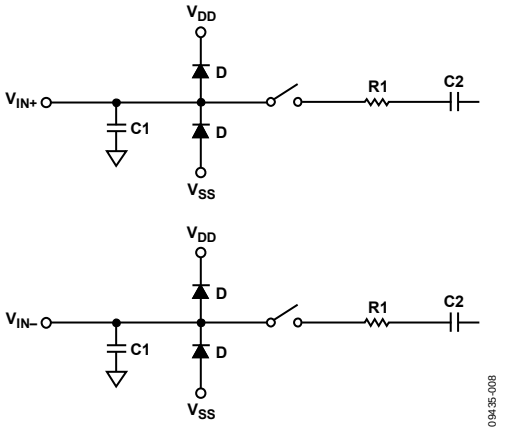


*Figure 26. Equivalent Analog Input Circuit*

## TRANSFER FUNCTION

The output coding of the AD7280A is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is dependent on whether the cell voltage or the auxiliary ADC inputs are being measured. The analog input range of the voltage inputs is 1 V to 5 V, and the analog input range of the auxiliary ADC inputs is 0 V to 5 V. The ideal transfer characteristic is shown in Figure 27.

**Table 7. LSB Sizes for Each Analog Input Range**

| Selected Inputs | Input Range | Full-Scale Range | LSB Size |
|---|---|---|---|
| Cell Voltage | 1 V to 5 V | 4 V/4096 | 976 µV |
| Auxiliary ADC Inputs | 0 V to 5 V | 5 V/4096 | 1.22 mV |

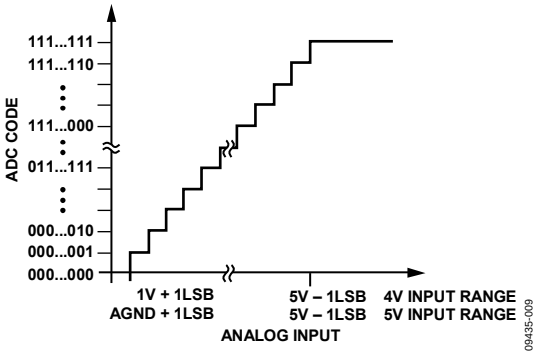


*Figure 27. Ideal Transfer Characteristic*

## TYPICAL CONNECTION DIAGRAMS

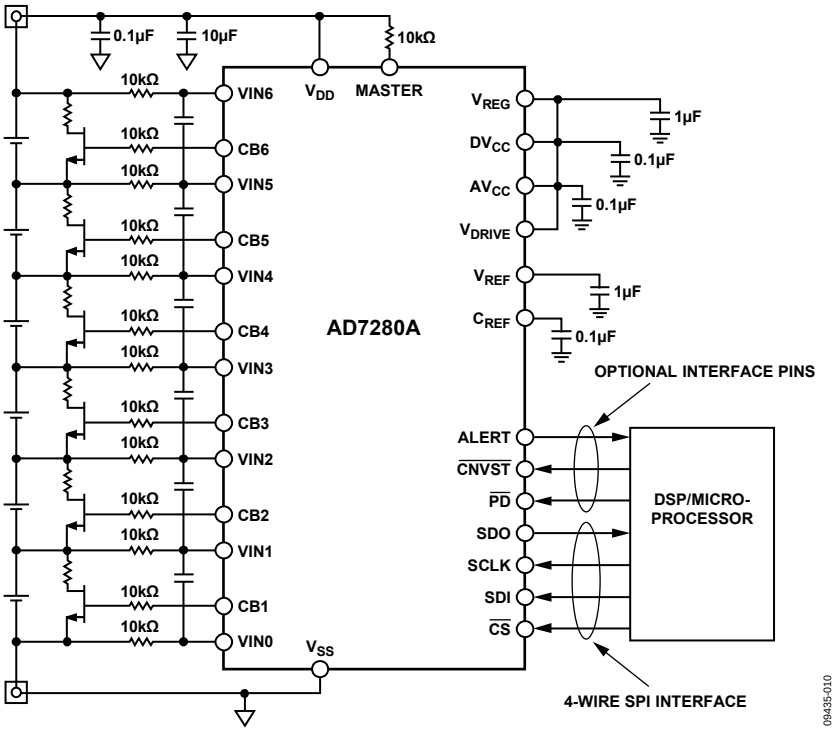


*Figure 28. AD7280A Configuration Diagram for Six Battery Cells*

The AD7280A can be used to monitor four, five, or six battery cells connected in series. A typical configuration for a six-cell battery monitoring application is shown in Figure 28. However, lithium ion battery applications require a significant number of individual cells to provide the required output voltage. Figure 29 shows the recommended configuration of a chain of AD7280As monitoring a larger battery stack. The daisy-chain interface of the AD7280A allows each individual AD7280A to communicate with the AD7280A immediately above and below it. The daisy-chain interface allows the AD7280As to be electrically connected to the battery management chip without the need for individual isolation devices between each AD7280A.

As shown in Figure 29, it is recommended that a Zener diode be placed across the supplies of each AD7280A. This prevents an overvoltage across the supplies of each AD7280A during the initial connection of the daisy chain of AD7280As to the battery stack. A voltage rating of 30 V is suggested for this Zener diode, but lower values can also be used to suit the application.

The 10 kΩ resistor in series with the inputs combined with a 100 nF capacitor across the adjacent differential inputs acts as a low-pass filter. The 10 kΩ resistors provide protection for the analog inputs in the event of an overvoltage or undervoltage on those inputs, for example, if any of the cell voltage inputs is incorrectly shorted to $V_{DD}$ or $V_{SS}$. The resistors also provide protection during the initial connection of the daisy chain of AD7280As to the battery stack. For more information about the daisy-chain interface, see the Daisy-Chain Interface section.

In an application that includes a safety mechanism designed to open circuit the battery stack, additional isolation is required between the AD7280A above the break point and the battery management chip.

A suggested configuration for the external cell balancing circuit is shown in Figure 28. This configuration also includes 10 kΩ resistors in series with the cell balance outputs. These resistors provide protection for the cell balance outputs in the event of an overvoltage or undervoltage on those inputs. See the Cell Balancing Outputs section for more information.

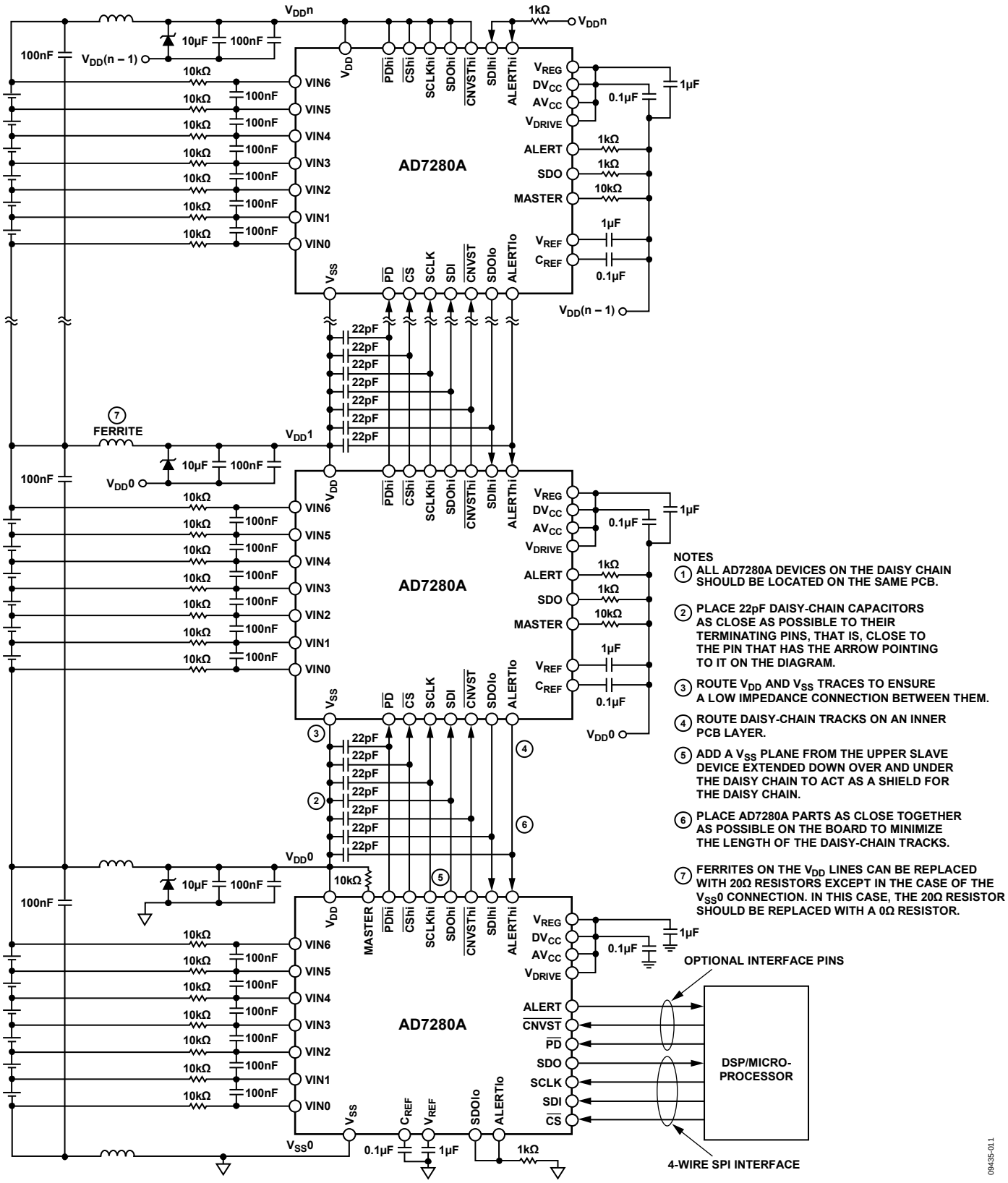


*Figure 29. AD7280A Daisy-Chain Configuration*

## REFERENCE

The internal reference is temperature compensated to 2.5 V. The reference is trimmed to provide a typical drift of ±3 ppm/°C. As shown in Figure 30, the internal reference circuitry consists of a 1.2 V band gap reference and a reference buffer. The 2.5 V reference is available at the $V_{REF}$ pin. The $V_{REF}$ pin should be decoupled to REFGND using a 1 µF or greater ceramic capacitor. The $C_{REF}$ pin should be decoupled to REFGND using a 0.1 µF or greater ceramic capacitor. The 2.5 V reference is capable of driving an external load of up to 10 kΩ.

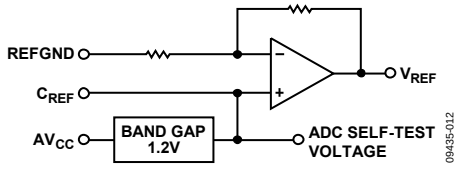


*Figure 30. AD7280A Internal Reference*

## CONVERTING CELL VOLTAGES AND AUXILIARY ADC INPUTS

A conversion can be initiated on the AD7280A using either the $\overline{\text{CNVST}}$ input or the serial interface (see the Conversion Start Format section). A single conversion command initiates conversions on all selected channels of the AD7280A. As described in the Converter Operation section, the voltage of each individual battery cell is measured by converting the difference between adjacent analog inputs. The first cell to be converted following a convert start command is Cell 6, which is the difference between VIN6 and VIN5. At the end of the first conversion, the AD7280A generates an internal end-of-conversion (EOC) signal. This internal EOC selects the next cell voltage inputs for measurement through the multiplexer, that is, the difference between VIN5 and VIN4. The new input is acquired, and a second internal convert start signal is generated, which initiates the conversion. This process is repeated until all the selected voltage and auxiliary ADC inputs have been converted.

The conversion sequence—that is, the order in which the cell voltages and auxiliary ADC inputs are converted—is shown in Figure 31 and Figure 32. The cell voltage inputs are converted in reverse order, that is, Cell 6 is followed by Cell 5, and so on. However, the auxiliary ADC inputs are converted in increasing numerical order, that is, AUX1 is followed by AUX2, and so on. For example, when all 12 inputs are selected for conversion, the conversion of Cell 1, that is, VIN1 to VIN0, is followed by the conversion of the AUX1 input.

When all selected conversions are completed, the VIN6 and VIN5 voltage inputs are again selected through the multiplexer, and the voltage across Cell 6 is acquired in preparation for the next conversion request. This is the default state for the multiplexer.

Bits[D15:D14] of the control register select the cell voltage and auxiliary ADC inputs to be converted. There are four options available (see Table 8).

**Table 8. Cell Voltage and Auxiliary ADC Input Selection**

| Bits[D15:D14] | Voltage Inputs | Auxiliary ADC Inputs |
|---|---|---|
| 00 | 6 to 1 | 1 to 6 |
| 01 | 6 to 1 | 1, 3, and 5 |
| 10 | 6 to 1 | None |
| 11 | ADC self-test | None |

Each voltage and auxiliary ADC input conversion requires a minimum of 1 µs to acquire and convert the cell voltage or auxiliary ADC input voltage. For example, when Bits[D15:D14] are set to 00, the falling edge of $\overline{\text{CNVST}}$ triggers a series of 12 conversions. This requires a minimum of 12 µs to convert all selected measurements on a single AD7280A. If no auxiliary ADC input conversions are required, Bits[D15:D14] are set to 10. In this case, the conversion request triggers a series of six conversions, requiring a minimum of 6 µs.

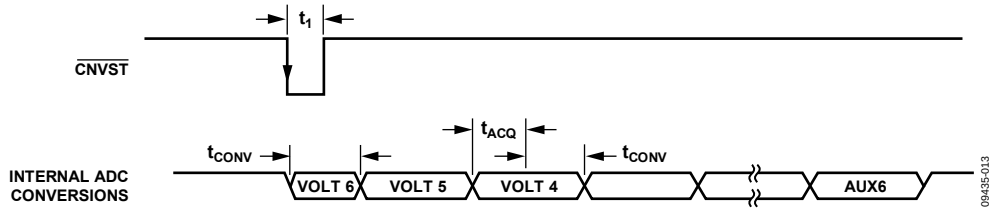


*Figure 31. ADC Conversions on the AD7280A*

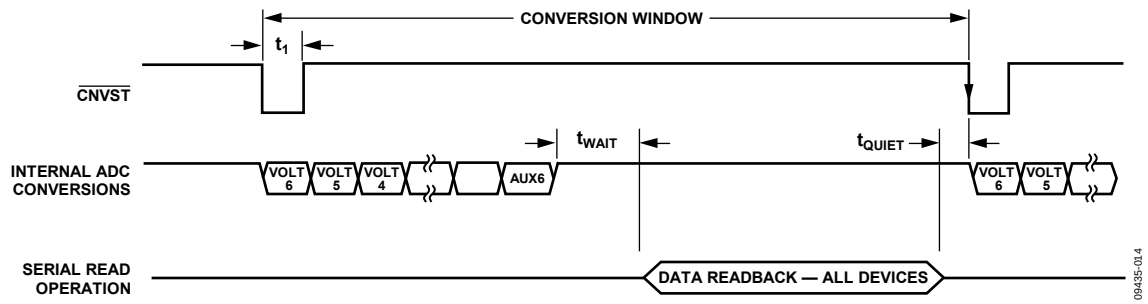


*Figure 32. ADC Conversions and Readback on the AD7280A*

Note that 90 µs should be allowed before initiating any conversions following any change to Bits[D15:D14]. This time should be allowed between writing to the control register to change the selected conversions and initiating the first conversion. Conversions that are initiated by the rising edge of the $\overline{CS}$ pin require two separate write commands to the control register. The first command configures the AD7280A for the required acquisition time; the second command, following a delay of 90 µs, initiates the conversion on the rising edge of $\overline{CS}$.

After the completion of all requested conversions, the results can be read back from either a single device or from all devices in a daisy chain by using the SPI and daisy-chain interfaces. For more information, see the Serial Interface section and the Daisy-Chain Interface section.

As shown in Figure 32, a wait time, $t_{WAIT}$, is required between the completion of conversions and the start of readback. This time is required to synchronize the high speed conversion clock and the lower speed clock used for all other AD7280A operations. The minimum value of $t_{WAIT}$ is 5 µs.

### *Acquisition Time*

The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. This, in turn, depends on the input impedance and any external components placed on the analog inputs. The default acquisition time of the AD7280A on initial power-up is 400 ns. This time can be increased in steps of 400 ns up to 1.6 µs to provide flexibility in selecting external components on the analog inputs. The acquisition time is selected by writing to Bits[D6:D5] in the control register (see Table 9).

**Table 9. Analog Input Acquisition Time**

| Bits[D6:D5] | Acquisition Time |
|---|---|
| 00 | 400 ns |
| 01 | 800 ns |
| 10 | 1.2 µs |
| 11 | 1.6 µs |

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R) \times C)$$

where:

$R_{SOURCE}$ should include any extra source impedance on the analog input between the external capacitors (100 nF) and the input pins. It does not include any extra source impedance, for example, the 10 kΩ series resistors, which are between the battery cells and the external capacitors.

$R$ is the resistance seen by the track-and-hold amplifier looking at the input, 300 Ω.

$C$ is the sampling capacitance, that is, the value of the sampling capacitor, 15 pF.

### *Conversion Averaging*

The AD7280A includes an option where the acquisition and conversion of each cell input can be repeated with an averaged conversion result being stored in the individual register. The averaged conversion result can then be read back through the SPI interface in the same manner as a standard conversion result. The AD7280A can be programmed, through Bits[D10:D9] of the control register, to complete one, two, four, or eight conversions. The default on power-up is a single conversion per channel, that is, no averaging.

Selection of the two, four, or eight average options through the control register causes the control sequence of both the high voltage and low voltage input multiplexers to be reconfigured to allow the additional acquisitions and conversions to be completed. In each case, the requested number of conversions is completed on each channel before beginning the acquisition and conversion of the next channel in sequence. For example, if an average of two conversions is requested, the new sequence is Voltage Channel 6, Voltage Channel 6, Voltage Channel 5, Voltage Channel 5, Voltage Channel 4, and so on.

It should also be noted that when the high voltage multiplexer is reconfigured, 90 µs should be allowed before initiating any conversions. This time should be allowed between writing to the control register to select averaging and initiating the first conversion. Conversions that are being initiated by the rising edge of the $\overline{CS}$ pin require two separate write commands to the control register. The first command configures the AD7280A for the required averaging, and the second command, after a delay of 90 µs, initiates the conversion on the rising edge of $\overline{CS}$.

### *Suggested External Component Configuration on Analog Inputs*

As described in the Acquisition Time section, the acquisition time of the AD7280A is selected by the status of Bits[D6:D5] in the control register. This provides flexibility in selecting external components on the analog inputs. A suggested configuration for placing external components on the analog inputs to the AD7280A is shown in Figure 33.

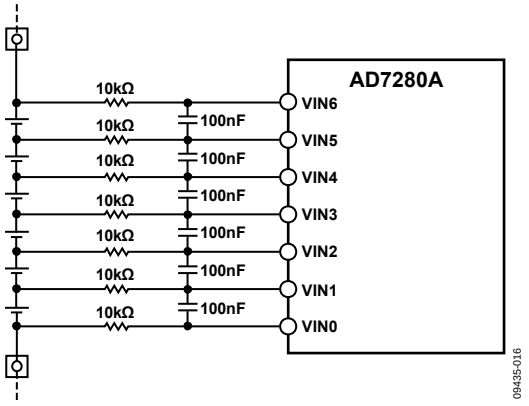


*Figure 33. External Series Resistance and Shunt Capacitance*

The 10 kΩ resistors in series with the inputs provide protection for the analog inputs in the event of an overvoltage or undervoltage on those inputs. The 100 nF capacitor across the differential inputs acts as a low-pass filter in conjunction with the 10 kΩ resistor. The cutoff frequency of the low-pass filter is 80 Hz. Using these external components, the default acquisition time of 400 ns can be used, which allows a combined acquisition and conversion time of 1 µs.

## CONVERTING CELL VOLTAGES AND AUXILIARY ADC INPUTS IN A CHAIN OF AD7280As

The AD7280A provides a daisy-chain interface that allows up to eight parts to be stacked without the need for individual isolation. One feature of the daisy-chain interface is the ability to initiate conversions on all parts in the daisy-chain stack with a single convert start command. The convert start command is transferred up the daisy chain, from the master device to each AD7280A in turn. The delay time between each AD7280A is $t_{DELAY}$, as shown in Figure 34. The maximum delay between the start of conversions on the master AD7280A and the last AD7280A device in the chain can be determined by multiplying $t_{DELAY}$ by the number of slave AD7280As in the daisy chain. The total conversion time for all cell voltage and auxiliary ADC input conversions can be calculated using the following equation:

$$Total\ Conversion\ Time = ((t_{ACQ} + t_{CONV}) \times (Number\ of\ Conversions\ per\ Part)) - t_{ACQ} + ((N - 1) \times t_{DELAY})$$

where:

$t_{ACQ}$ is the analog input acquisition time of the AD7280A (see Table 9).

$t_{CONV}$ is the conversion time of the AD7280A, as specified in Table 3.

*Number of Conversions per Part* is the number of inputs selected for conversion (6, 9, or 12, as listed in Table 8), multiplied by the number of averages selected for each input (1, 2, 4, or 8).

$N$ is the number of AD7280As in the daisy chain.

$t_{DELAY}$ is the delay time when transferring the convert start command between adjacent AD7280A devices, as specified in Table 3.

The total conversion times calculated for three possible configurations of the AD7280A are included in Table 10.

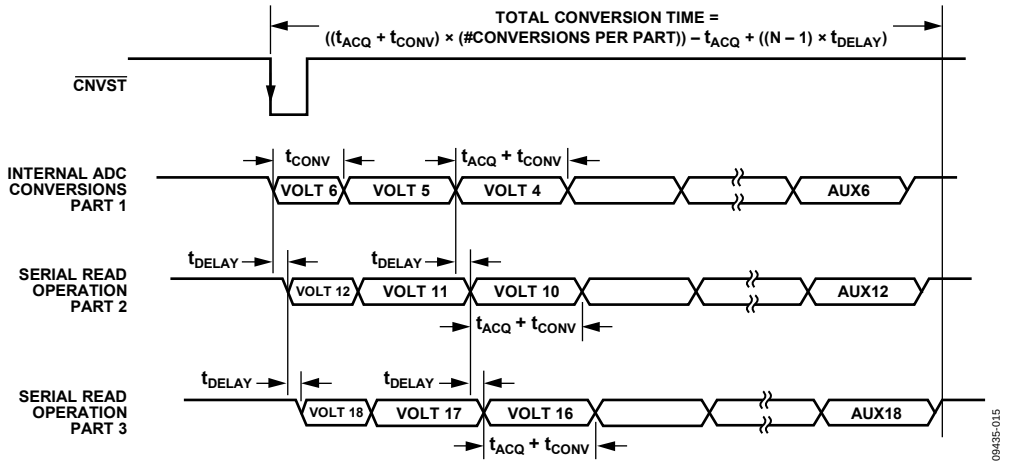


*Figure 34. ADC Conversions and Readback on a Chain of Three AD7280As*

**Table 10. Calculated Conversion Times for Three Example AD7280A Configurations, $T_A$ = −40°C to +85°C**

| Bits [D15:D14] | Bits [D10:D9] | Bits [D6:D5] | Configuration | Conversion Time per Part | Total Conversion Time per 48 Channel Stack |
|---|---|---|---|---|---|
| 00 | 00 | 00 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 465 ns; average = 0 | 13.46 µs | 15.2 µs |
| | | 01 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.01 µs; average = 0 | 19.45 µs | 21.2 µs |
| | | 10 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.46 µs; average = 0 | 24.4 µs | 26.15 µs |
| | | 11 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.89 µs; average = 0 | 29.13 µs | 30.9 µs |
| 10 | 00 | 00 | 6 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 465 ns; average = 0 | 6.5 µs | 8.23 µs |
| | | 01 | 6 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.01 µs; average = 0 | 9.22 µs | 10.97 µs |
| | | 10 | 6 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.46 µs; average = 0 | 11.47 µs | 13.22 µs |
| | | 11 | 6 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.89 µs; average = 0 | 13.62 µs | 15.37 µs |
| 00 | 11 | 00 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 465 ns; average = 8 | 110.9 µs | 112.65 µs |
| | | 01 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.01 µs; average = 8 | 162.67 µs | 164.42 µs |
| | | 10 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.46 µs; average = 8 | 205.42 µs | 207.17 µs |
| | | 11 | 12 channels; $t_{CONV}$ = 695 ns; $t_{ACQ}$ = 1.89 µs; average = 8 | 246.27 µs | 248.02 µs |

## CONVERSION WINDOW

As described in the Converting Cell Voltages and Auxiliary ADC Inputs section, the AD7280A converts the selected cell voltage and auxiliary ADC inputs in a defined sequence (see Figure 31). As described in the Circuit Information section, the AD7280A consists primarily of a high voltage input multiplexer, a low voltage input multiplexer, and a SAR ADC. The six cell voltage channels are presented to the ADC in turn by the high voltage multiplexer. Control is then handed to the low voltage multiplexer that allows the six auxiliary ADC channels to be converted. Following completion of all selected conversions, control is handed back to the high voltage multiplexer, and the AD7280A is ready to receive the next valid convert start command.

The conversion window of the AD7280A includes the actual conversion time for the selected channels (see Table 10), as well as the additional time required to return control to the high voltage multiplexer and configure it to start acquiring the cell voltage between VIN6 and VIN5. The conversion window defines the minimum time that should be allowed between successive convert start commands.

The conversion window for the AD7280A can be calculated using the following equation:

$$Conversion\ Window = Total\ Conversion\ Time + 80\ \mu s$$

where *Total Conversion Time* can be calculated for either a single device or for a chain of devices, as described in the Converting Cell Voltages and Auxiliary ADC Inputs section.

## SELF-TEST CONVERSION

A self-test conversion can be initiated on the AD7280A, which allows the operation of the ADC and reference buffer to be verified. The self-test conversion is completed on the internal 1.2 V band gap reference voltage, and the voltage range for the conversion is 0 V to 5 V. The self-test conversion can be initiated on either a single AD7280A or on all AD7280As in the daisy chain simultaneously.

The conversion results can be read back though the read protocols defined in the Serial Interface section. The self-test conversion result typically varies between Code 970 and Code 990.

The self-test conversion can also be used to verify the operation of the alert outputs, as described in the Alert Output section.

## CONNECTION OF FEWER THAN SIX VOLTAGE CELLS

The AD7280A provides six input channels for battery cell voltage measurement. The AD7280A can also be used in applications that require fewer than six voltage measurements. In these applications, care should be taken to ensure that the sum of the individual cell voltages still exceeds the minimum $V_{DD}$ supply voltage. For this reason, the recommended minimum number of battery cells connected to each AD7280A is 4. Care should also be taken to ensure that the voltage on the VIN6 input is always greater than or equal to the voltage on the $V_{DD}$ supply pin. For example, in an application with five battery cells connected to the AD7280A, the cell voltage on Cell 5 should be applied across VIN6 and VIN5, and the VIN4 and VIN5 inputs should be shorted together. Figure 35 shows an example of the battery connections to the AD7280A in a four-cell battery monitoring application.

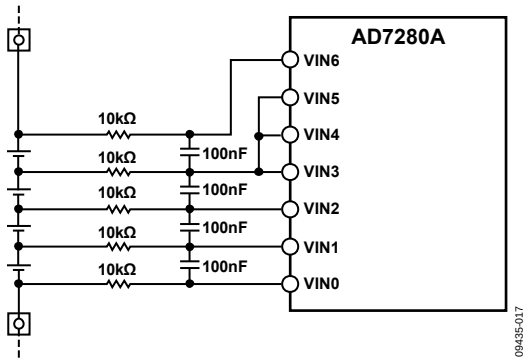


*Figure 35. Typical Connections for a Four-Cell Application*

Regardless of how many cell voltage measurements are required in the user application, the AD7280A acquires and converts the voltages on all six cell voltage input channels. The conversion data on all six voltage channels is supplied to the DSP/microprocessor using the SPI/daisy-chain interfaces. Users should ignore the conversion data that is not required in their application.

It is also possible to read back a single cell voltage conversion result from each device in the daisy chain. This can be done by programming the read register on each device to read back the required conversion result (see Example 4 in the Examples of Interfacing with the AD7280A section). However, as previously described, all six cell voltage channels are converted. When using the device in this mode, the overall conversion sample rate should be limited by the conversion window required for the number of channels selected by Bits[D15:D14] of the control register.

When using the alert function, the user should program the alert register to ensure that the shorted channels do not incorrectly trigger an alert output (see the Alert Output section).

## AUXILIARY ADC INPUTS

The AD7280A provides six single-ended analog inputs to the ADC—AUX1 to AUX6—which can be used to convert the voltage output of a thermistor temperature measurement circuit. In the event that no temperature measurements are required or that individual cell temperature measurements are not required, the auxiliary ADC inputs can be used to convert any other 0 V to 5 V input signal.

The AD7280A can be programmed to complete conversions on all six auxiliary ADC channels, on three auxiliary ADC channels (AUX1, AUX3, and AUX5), or on none of the auxiliary ADC input channels. The number of conversions is programmed through Bits[D15:D14] of the control register. The number of conversion results supplied by the AD7280A for readback by the DSP/microprocessor is programmed through Bits[D13:D12] of the control register. It is also possible to read back a single auxiliary ADC conversion result from each device in the daisy chain. This can be done by programming the read register on each device to read back the required conversion result (see Example 4 in the Examples of Interfacing with the AD7280A section). If the device is used in this mode, the overall conversion sample rate should be limited by the conversion window required for the number of channels selected by Bits[D15:D14] of the control register.

In an application where the alert function is used but only one or two auxiliary ADC inputs are required, the AD7280A should first be programmed to complete and read back only three auxiliary ADC conversions by setting Bits[D15:D12] of the control register to 0101. Channel AUX5 and Channel AUX3 can be removed from the alert detection by writing to Bits[D1:D0] of the alert register (see Table 12 in the Alert Output section).

### *Thermistor Termination Input*

If thermistor circuits are used to measure each individual cell temperature, the thermistor termination pin, $AUX_{TERM}$, can be used to terminate the thermistor inputs for each auxiliary ADC input measurement. This reduces the termination resistor requirement from six resistors to one. Bit D3 in the control register should be set to 1 when using the $AUX_{TERM}$ input.

Note that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280A is set to its highest value (1.6 µs). The acquisition time is configured by setting Bits[D6:D5] of the control register (see Table 9).

In Figure 36, the termination resistor is placed between $V_{SS}$ and $AUX_{TERM}$. The $AUX_{TERM}$ input can be used to terminate the thermistor inputs to the high or low voltage of the thermistor circuit.

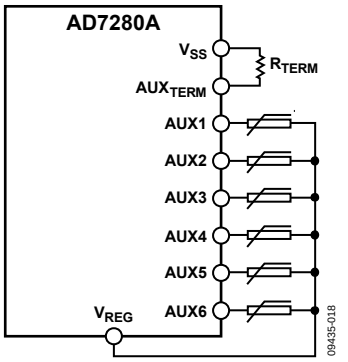


*Figure 36. Typical Circuit Using the Thermistor Termination Resistor*

## POWER REQUIREMENTS

The current consumed by the AD7280A in normal operation, that is, when not in power-down mode, is dependent on the mode in which the part is being operated. The three distinct modes of operation can be described as follows:

- Voltage and auxiliary ADC input conversion
- AD7280A configuration and data readback
- Cell balancing

The AD7280A consumes its highest level of current while converting voltage and/or auxiliary ADC inputs to digital outputs. Depending on the configuration of the AD7280A, the conversion time can be as little as 6 µs. The typical current required by the AD7280A during conversion is 6.9 mA (see Table 2).

When configuring a chain of AD7280As or when reading back the voltage and/or auxiliary ADC conversion results from a chain of AD7280As, the current required for each AD7280A is typically 6.5 mA (see Table 2). The time required to read back the voltage conversions results from 48 lithium ion cells depends on the speed of the interface clock used, that is, SCLK, but it can be as low as 1.54 ms.

The typical current consumed by the AD7280A when the cell balance outputs are switched on is 6.4 mA (see Table 2). The length of time for which the cell balance outputs are switched on is defined by the user.

When the AD7280A is not being used in any of the aforementioned modes of operation, it is recommended that the device be powered down, as described in the Power-Down section. This significantly reduces the current drawn by each AD7280A in the chain, which avoids unnecessary draining of the lithium ion cells and aids in current matching between devices across the full battery stack.

## POWER-DOWN

The AD7280A provides two power-down options.

- Full power-down (hardware)
- Software power-down

### *Full Power-Down (Hardware)*

The AD7280A can be placed into full power-down mode, which requires only 5 µA maximum current, by taking the $\overline{PD}$ pin low. The falling edge of the $\overline{PD}$ pin powers down all analog and digital circuitry.

The AD7280A includes a digital delay filter on the $\overline{PD}$ pin, which protects against a power-down being initiated by noise or glitches on the hardware $\overline{PD}$ pin. A hardware power-down is not initiated until the $\overline{PD}$ pin is held low for approximately 130 µs. Similarly, the AD7280A is not taken out of power-down mode until the $\overline{PD}$ pin is held high for approximately 130 µs. The digital delay filter does not apply on initial power-up. The power-on request is accepted by the AD7280A approximately 5 µs after the rising edge of $\overline{PD}$.

When placing the AD7280A into full power-down mode, $AV_{CC}$ and $DV_{CC}$ must fall to 0 V and must not be held high by any external means. $AV_{CC}$ and $DV_{CC}$ can be held high unintentionally if the auxiliary ADC inputs are greater than the forward bias on the internal ESD protection diodes. For this reason, it is recommended that the auxiliary ADC inputs return to 0 V when the part is placed in full power-down mode.

In addition, all digital inputs on the AD7280A master device must return to 0 V when the part is placed in full power-down mode (see Figure 37). However, if an external $V_{DRIVE}$ supply is used—that is, $V_{DRIVE}$ is not connected to $V_{REG}$—then only the $\overline{CNVST}$ line must return low (see Figure 38).

When the AD7280A is placed into full power-down mode, the device must be left in full power-down for a minimum of 2 ms when the $V_{REG}$ and $V_{REF}$ pins are decoupled with 1 µF capacitors. This ensures that the charge on the $V_{REG}$ and $V_{REF}$ decoupling capacitors dissipates sufficiently to allow the internal power-on reset circuit to activate when powering the AD7280A back up.

This time is measured from the falling edge of the $\overline{PD}$ pin. Figure 18 shows a plot of the voltage on the $V_{REG}$ and $V_{REF}$ pins as the AD7280A is powering down with 1 µF decoupling capacitors on the pins. Figure 20 shows a similar plot but with 10 µF decoupling capacitors on the $V_{REG}$ and $V_{REF}$ pins.

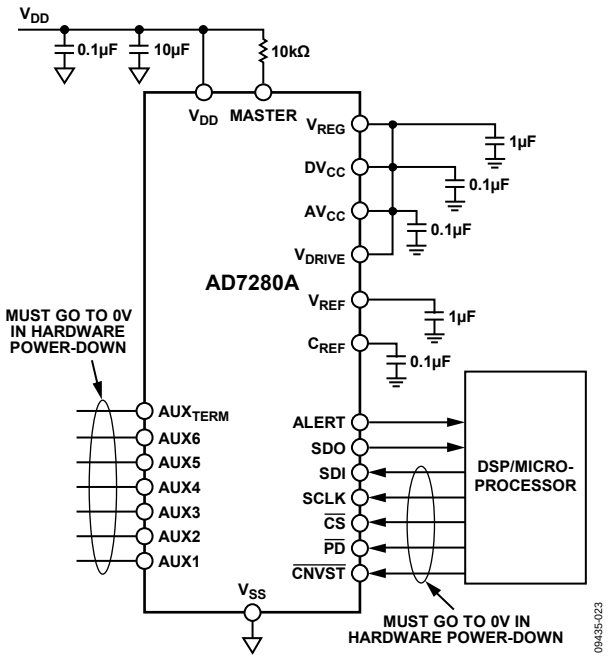


*Figure 37. $V_{DRIVE}$ Powered from $V_{REG}$*

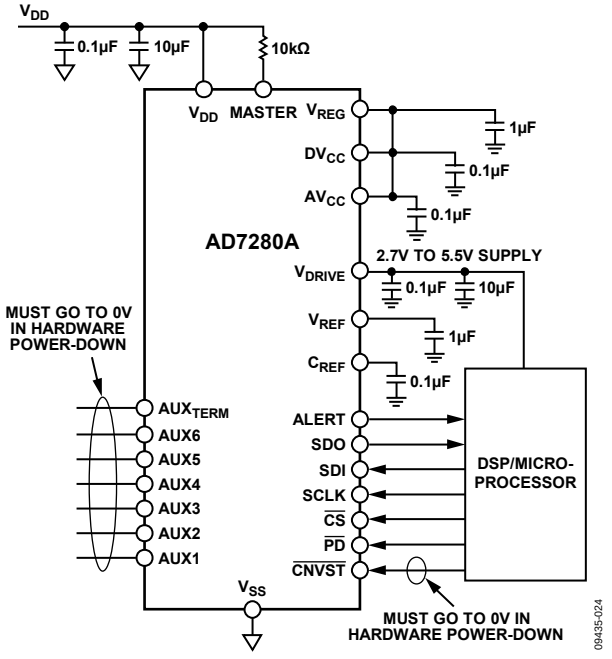


*Figure 38. $V_{DRIVE}$ Powered from DSP/Microprocessor*

### *Software Power-Down*

The AD7280A can be placed into software power-down mode, which requires 3.8 mA of current, by setting Bit D8 in the control register through the serial interface. The $\overline{\text{CNVST}}$ pin should be gated out before generating a software power-down (see the $\overline{\text{CNVST}}$ Control Register section). When the AD7280A is powered down through the serial interface, the regulator, the reference, and the daisy-chain circuitry stay powered up, but the remaining analog and digital circuitry is powered down. This is necessary to ensure that the signal to power on the part, or the chain of parts, is correctly received.

### *Power-Down Timer*

The PD timer register allows the user to program a set time after which the AD7280A is automatically powered down. This timer functions as a time delay between the falling edge of the $\overline{\text{PD}}$ input (or the setting of Bit D8 in the control register) and the AD7280A powering down. The PD timer can be set to a value from 0 minutes to 36.9 minutes, with a resolution of 71.5 sec. The user should first write to the PD timer register to define the desired delay. Any subsequent falling edge on the $\overline{\text{PD}}$ input or setting of Bit D8 in the control register starts the PD timer. When the programmed time elapses, the AD7280A checks the state of the $\overline{\text{PD}}$ pin. If the $\overline{\text{PD}}$ pin is low, the AD7280A powers down. If the $\overline{\text{PD}}$ pin is high, the part does not power down and continues to operate as normal. The default value of the PD timer register on power-up is 0x00.

If the PD timer register is written to after the counter starts, the counter is reset to 0. The count then restarts automatically, without further input from the user, and counts to the new value in the PD timer register. If the new time in the PD timer register is 0, the part checks the state of the $\overline{\text{PD}}$ pin and powers down if the $\overline{\text{PD}}$ pin is low. Note that when the PD timer is activated—for example, by a falling edge on the $\overline{\text{PD}}$ pin—a subsequent rising edge on the $\overline{\text{PD}}$ pin does not disable the active PD timer. It is recommended that the $\overline{\text{PD}}$ pin be held low until an active PD timer expires.

## POWER-UP TIME

As described in the Power-Down section, a full power-down of the AD7280A (active low on the $\overline{\text{PD}}$ input) powers down all analog and digital circuitry. The recommended power-up time from hardware power-down, when the internal reference is decoupled with a 1 µF capacitor, is 5.5 ms. It is recommended that no conversions be initiated until the 5.5 ms power-up time elapses because such conversions can result in inaccurate data.

A software power-down powers down all analog and digital circuitry on the AD7280A except for the regulator, the 1.2 V band gap reference, and the daisy-chain circuitry. The recommended power-up time from software power-down, when the $V_{REF}$ pin is decoupled with a 1 µF capacitor, is 1 ms.

## CELL BALANCING OUTPUTS

The AD7280A provides six cell balance outputs that can be used to drive the gate of external transistors as part of a cell balancing circuit. Each CBx output can be set to provide either a 0 V or 5 V output with respect to the absolute amplitude of the negative terminal of the battery cell that is being balanced. For example, the CB6 output provides a 0 V or 5 V output with respect to the voltage on the VIN5 analog input. The CBx outputs are set by writing to the cell balance register. The default value of the cell balance register on power-up is 0x00.

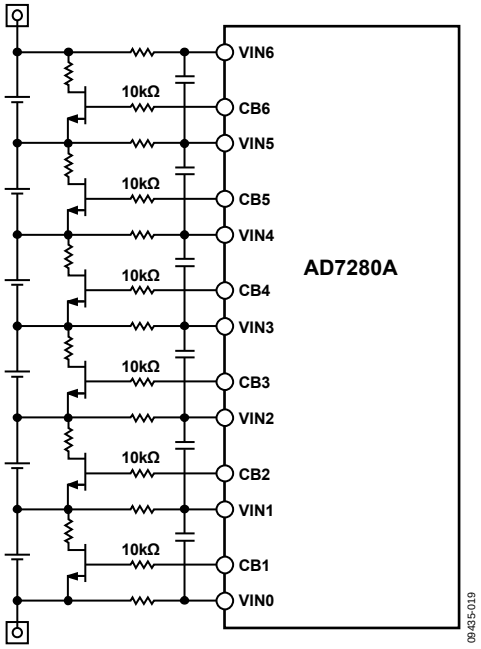


*Figure 39. Cell Balancing Configuration*

As noted in the Power-Down Timer section, a power-down timer can be programmed on the AD7280A. This timer can be used to allow cell balancing to occur for a set time before powering down the AD7280A. The power-down timer is independent of the cell balance timers. If no power-down timer is set—that is, if the PD timer register is at its default value of 0x00—a falling edge on the $\overline{\text{PD}}$ pin switches off the CBx outputs and powers down the AD7280A. If a power-down timer is set, the CBx outputs are powered down when the programmed power-down timer elapses and the AD7280A is powered down.

In an application with two or more AD7280A devices in a daisy chain, it is recommended that series resistors be placed between the CBx outputs of the AD7280A and the gates of the external cell balancing transistors. These resistors are recommended to protect the AD7280A in the event that the external cell balancing transistors are damaged during the initial connection of the monitoring circuitry to the battery stack. Consideration should also be given to the protection of these external transistors during the initial connection of the monitoring circuitry to the battery stack.

An example of how damage to the external transistors can occur is a connection sequence that first provides the system ground (the ground supply to the master AD7280A in the daisy chain) followed by a connection from any of the battery cells at a potential high enough to exceed the $V_{GS}$ of the cell balancing transistor, for example 40 V. If these two connections are the first battery connections made in the system, the result is 40 V being applied to one of the VINx pins of the AD7280A through a series resistor. The 40 V battery connection is also directly applied to the source input of one of the cell balancing transistors. However, because no power has been supplied to the $V_{DD}$ pin of the AD7280A, all the CBx outputs are at 0 V. This results in a reverse voltage of 40 V across the $V_{GS}$ of the external transistor, which can damage the device.

### *Cell Balance Timers*

The AD7280A offers six cell balance timer registers that allow the on time of each CBx output to be programmed. The CBx timers can be set to a value from 0 minutes to 36.9 minutes. The resolution of the CBx timers is 71.5 sec. A value of 0x00 in a CBx timer register means that the timer is not activated. A nonzero value programmed to a CBx timer register configures the CBx timer for use, but the CBx outputs and the CBx timers are not activated until the cell balance register is written to. At the end of the individually programmed CBx time, the respective CBx output returns to its default state of 0 V output with respect to the absolute amplitude of the negative terminal of the battery cell that is being balanced. Also at this time, the cell balance register is reset and the CBx timer registers continue to hold their programmed values. The default value of the CBx timer registers on power-up is 0x00.

When using the cell balance timer feature, note that the timer on each cell balance output is operated from a single CB counter. When a nonzero value is programmed to any CBx timer register, this counter is activated by writing a nonzero value to the cell balance register. The current value of the counter is compared to the values programmed to each CBx timer register at 4.5 sec intervals (71.5 sec/16). When the value in the counter reaches the value in the CBx timer register, the cell balance output corresponding to that CBx timer register is switched off. Note that the cell balance register has a higher priority than the CBx timer registers. A CBx output can be switched off by writing to the cell balance register even if the value programmed to the respective CBx timer register has not expired.

Writing a zero or a nonzero value to an active CBx timer register (corresponding CB output switched on) results in the cell balance counter being reset and automatically restarted. Note that overwriting the CBx timer with 0 restarts the counter, but, because the timer value is now 0, the corresponding CB output is switched off. Any write to a nonactive CBx timer register (corresponding CB output not switched on) has no effect on the cell balance counter.

### *Programming the Cell Balance Timers*

It is recommended that the required CBx timer values be programmed to each individual CBx timer register before activating the CB counter. Changing the CBx timer values while the counter is running is possible; however, writing to an active CBx timer register resets the counter, as described in the Cell Balance Timers section.

#### Cell Balance Timer Example 1

The following sequence of steps programs a value of 214.5 sec to the CB1 and CB2 timer registers.

1. Set Bits[D4:D3] of the CB1 timer register and the CB2 timer register high.
2. Set Bits[D3:D2] of the cell balance register high.
3. Wait 60 sec.
4. Set Bits[D4:D3] of the CB3 timer register high.
5. Set Bits[D4:D2] of the cell balance register high.

In this example, the CB1 and CB2 outputs are switched on and the cell balance counter is activated. Following the 60 sec wait, a value of 214.5 sec is written to the CB3 timer register, the CB3 output is switched on, and the on state of the CB1 and CB2 outputs is maintained. In this example, all three CB outputs are switched off at the same time (214.5 sec). This is because the CB counter was already active before the CB3 timer register was programmed and the CB3 output selected.

#### Cell Balance Timer Example 2

In this example, follow the same sequence of steps described in the Cell Balance Timer Example 1 section, but increase the wait step from 60 sec to any value greater than 214.5 sec.

The initial steps set up the CB1 and CB2 timers and activate the CB1 and CB2 outputs. However, because the wait state is now longer than the time programmed to the CB1 and CB2 timers, the CB1 and CB2 timers expire before the additional writes to configure CB3. The CB1 and CB2 outputs switch off, a 0 is written to Bits[D3:D2] of the cell balance register, and the CB counter is reset to 0x00 before the commands to program the CB3 timer and to switch on the CB3 output are received.

In this example, the second write to the cell balance registers—which selects the CB1, CB2, and CB3 outputs—is considered a new activation of the CB counter. The CB1, CB2, and CB3 outputs switch on and, if no further commands are written to the AD7280A, all three outputs switch off 214.5 sec after this second activation of the CB counter.

## ALERT OUTPUT

The alert output on the AD7280A can be used to indicate whether any of the following faults has occurred:

- Cell overvoltage
- Cell undervoltage
- Auxiliary ADC overvoltage
- Auxiliary ADC undervoltage

Following each completed conversion, the cell voltage and auxiliary ADC measurement results are compared to the alert thresholds. The alert thresholds are set by writing to the cell overvoltage, cell undervoltage, AUX ADC overvoltage, and AUX ADC undervoltage registers. An alert output is generated if the cell voltage and/or the auxiliary ADC results are outside the programmed alert thresholds.

The alert output can be configured as a static or dynamic output by writing to the alert register. The static alert output is a high signal that is pulled low in the event of an overvoltage or undervoltage on the cell voltage or auxiliary ADC input conversions. The dynamic alert is a square wave that can be programmed to a frequency of 100 Hz, 1 kHz, or 10 kHz. The alert output can be used as part of a daisy chain, in which case the AD7280A at the top of the chain, that is, farthest away from the DSP/microprocessor, should be programmed to generate the initial alert output, and all other devices in the chain should be programmed to allow the alert signal to pass through. If a conversion result outside the programmed thresholds occurs, either on the device generating the initial alert signal or on any device in the chain, the alert signal is pulled low to indicate that an alert condition has occurred. At the end of the daisy chain, the master AD7280A, which is connected to the DSP/microprocessor, takes the alert signal from the chain and passes it in standard digital voltage format to the DSP/microprocessor. The configuration settings for the alert register are described in Table 11 and Table 12.

**Table 11. Alert Register Settings, Bits[D7:D4][1]**

| Bits[D7:D6] | Bits[D5:D4] | Action |
|---|---|---|
| 00 | XX | No alert signal generated or passed (default) |
| 01 | XX | Generates a static (high) alert signal to be passed down the daisy chain |
| 10 | 00 | Generates a 100 Hz square wave alert signal to be passed down the daisy chain |
| 10 | 01 | Generates a 1 kHz square wave alert signal to be passed down the daisy chain |
| 10 | 10 | Generates a 10 kHz square wave alert signal to be passed down the daisy chain |
| 10 | 11 | Reserved |
| 11 | XX | Passes an alert signal from the AD7280A at higher potential in the daisy chain |

[1] X is don't care.

**Table 12. Alert Register Settings, Bits[D3:D0][1]**

| Bits[D3:D2] | Bits[D1:D0] | Action |
|---|---|---|
| 00 | XX | Includes all six voltage channels in alert detection (default) |
| 01 | XX | Removes VIN5 from alert detection |
| 10 | XX | Removes VIN5 and VIN4 from alert detection |
| 11 | XX | Reserved |
| XX | 00 | Includes all AUX ADC channels selected for conversion in alert detection[2] (default) |
| XX | 01 | Removes AUX5 from alert detection[3] |
| XX | 10 | Removes AUX5 and AUX3 from alert detection[3] |
| XX | 11 | Reserved |

[1] X is don't care.
[2] Includes six auxiliary ADC channels in the alert detection if conversions on six auxiliary ADC channels are selected in the control register; includes three auxiliary ADC channels in the alert detection if conversions on three auxiliary ADC channels are selected in the control register.
[3] To remove AUX5 or AUX5 and AUX3 from the alert detection, conversions on three auxiliary ADC input channels only must be selected in the control register.

Some applications require fewer than six voltage measurements (see the Connection of Fewer Than Six Voltage Cells section). As shown in Figure 35, it is recommended that a channel that is not being used on the AD7280A be shorted to the channel below it. To prevent the incorrect triggering of the alert output in this application, the AD7280A allows the user to select up to two voltage channels that can be taken out of the overvoltage/undervoltage detection circuit. This is programmed through Bits[D3:D2] of the alert register. The user can also remove all or selected auxiliary ADC channels from the detection circuit. This is programmed through Bits[D1:D0] of the alert register in combination with Bits[D15:D14] of the control register.

The operation of the alert output can be verified by initiating a self-test conversion. The self-test conversion converts the band gap reference voltage, 1.2 V, which triggers an alert output if the cell undervoltage threshold is set higher than 1.2 V. To test the alert output, a self-test conversion should be initiated on the AD7280A farthest away from the DSP/microprocessor.

The operation of the alert output can also be verified by increasing or decreasing the thresholds around a known input voltage to trigger an alert condition. The alert operation of each device in the daisy chain of AD7280As can be verified by, for example, decreasing the cell overvoltage threshold of that device below the value of the input voltage on the cells. Initiating a conversion on all devices in the daisy chain pulls the alert signal low as it passes through that device. The relevant threshold on that device can then be returned to its previous value and the process repeated on the next device in the daisy chain.

# REGISTER MAP

**Table 13.**

| Register Name | Register Address | Register Data | Read/Write Register |
|---|---|---|---|
| Cell Voltage 1 | 0x00 | D11 to D0 | Read only |
| Cell Voltage 2 | 0x01 | D11 to D0 | Read only |
| Cell Voltage 3 | 0x02 | D11 to D0 | Read only |
| Cell Voltage 4 | 0x03 | D11 to D0 | Read only |
| Cell Voltage 5 | 0x04 | D11 to D0 | Read only |
| Cell Voltage 6 | 0x05 | D11 to D0 | Read only |
| AUX ADC 1 | 0x06 | D11 to D0 | Read only |
| AUX ADC 2 | 0x07 | D11 to D0 | Read only |
| AUX ADC 3 | 0x08 | D11 to D0 | Read only |
| AUX ADC 4 | 0x09 | D11 to D0 | Read only |
| AUX ADC 5 | 0x0A | D11 to D0 | Read only |
| AUX ADC 6 | 0x0B | D11 to D0 | Read only |
| Self-Test | 0x0C | D11 to D0 | Read only |
| Control | 0x0D | D15 to D8 | Read/write |
| | 0x0E | D7 to D0 | Read/write |
| Cell Overvoltage | 0x0F | D7 to D0 | Read/write |
| Cell Undervoltage | 0x10 | D7 to D0 | Read/write |
| AUX ADC Overvoltage | 0x11 | D7 to D0 | Read/write |
| AUX ADC Undervoltage | 0x12 | D7 to D0 | Read/write |
| Alert | 0x13 | D7 to D0 | Read/write |
| Cell Balance | 0x14 | D7 to D0 | Read/write |
| CB1 Timer | 0x15 | D7 to D0 | Read/write |
| CB2 Timer | 0x16 | D7 to D0 | Read/write |
| CB3 Timer | 0x17 | D7 to D0 | Read/write |
| CB4 Timer | 0x18 | D7 to D0 | Read/write |
| CB5 Timer | 0x19 | D7 to D0 | Read/write |
| CB6 Timer | 0x1A | D7 to D0 | Read/write |
| PD Timer | 0x1B | D7 to D0 | Read/write |
| Read | 0x1C | D7 to D0 | Read/write |
| $\overline{\text{CNVST}}$ Control | 0x1D | D7 to D0 | Read/write |

## CELL VOLTAGE REGISTERS

The cell voltage registers store the conversion result from each cell input. The conversion result is in 12-bit straight binary format.

## AUXILIARY ADC REGISTERS

The AUX ADC registers store the conversion result from each auxiliary ADC input. The conversion result is in 12-bit straight binary format.

## SELF-TEST REGISTER

The self-test register stores the conversion result of the ADC self-test. The conversion result is in 12-bit straight binary format.

## CONTROL REGISTER

The control register is a 16-bit register that is used to configure the AD7280A. Table 14 describes the operation of each bit in the control register.

**Table 14. Control Register Settings**

| Bits | Description |
|---|---|
| [D15:D14] | Select conversion inputs |
| | 00 = six cell voltages and six AUX ADCs (default) |
| | 01 = six cell voltages and AUX1, AUX3, and AUX5 |
| | 10 = six cell voltages only |
| | 11 = ADC self-test |
| [D13:D12] | Read conversion results |
| | 00 = six voltages and six AUX ADCs (default) |
| | 01 = six voltages and AUX1, AUX3, and AUX5 |
| | 10 = six cell voltages only |
| | 11 = no-read operation |
| D11 | Conversion start format |
| | 0 = falling edge of $\overline{\text{CNVST}}$ input (default) |
| | 1 = rising edge of $\overline{\text{CS}}$ |
| [D10:D9] | Conversion averaging |
| | 00 = single conversion only (default) |
| | 01 = average by 2 |
| | 10 = average by 4 |
| | 11 = average by 8 |
| D8 | Power-down format |
| | 0 = falling edge of $\overline{\text{PD}}$ input (default) |
| | 1 = software power-down |
| D7 | Software reset |
| | 0 = take the AD7280A out of reset (default) |
| | 1 = reset the AD7280A |
| [D6:D5] | Set acquisition time |
| | 00 = 400 ns (default) |
| | 01 = 800 ns |
| | 10 = 1.2 µs |
| | 11 = 1.6 µs |
| D4 | Reserved; set to 1 |
| D3 | Thermistor termination resistor |
| | 0 = function not in use (default) |
| | 1 = termination resistor connected |
| D2 | Lock device address |
| | 0 = does not lock to new device address; continues to operate with Device Address 0x00 (default) |
| | 1 = part locks to new device address that it is presented with |
| D1 | Increment device address |
| | 0 = does not increment the device address when transferring data up the daisy chain |
| | 1 = increments the device address when transferring data up the daisy chain (default) |
| D0 | Daisy-chain register readback |
| | 0 = function not in use; registers are read in single register readback mode |
| | 1 = set daisy chain for register readback (default) |

#### *Select Conversion Inputs*

Bits[D15:D14] of the control register determine which cell voltages and auxiliary ADC inputs are converted following a convert start command. The default value of D15 and D14 on power-up is 00.

#### *Read Conversion Results*

Bits[D13:D12] of the control register determine which cell voltage and auxiliary ADC conversion results are supplied to the serial or daisy-chain data output pins for readback. The default value of D13 and D12 on power-up is 00.

#### *Conversion Start Format*

A conversion on the AD7280A can be initiated through the hardware $\overline{\text{CNVST}}$ pin or by issuing a software convert start command. Bit D11 of the control register determines whether a conversion is initiated on the falling edge of the $\overline{\text{CNVST}}$ input or on the rising edge of the $\overline{\text{CS}}$ input. The default format on power-up is the $\overline{\text{CNVST}}$ pin, that is, 0. When using the rising edge of the $\overline{\text{CS}}$ input to initiate conversions, Bit D11 is reset to 0 following the initiation of conversions.

#### *Conversion Averaging*

Bits[D10:D9] of the control register determine the number of conversions completed on each input with the averaged results stored in the relevant result registers. The user can select a single conversion only or the average of two, four, or eight conversions. The default value of Bits[D10:D9] on power-up is 00, that is, single conversion only.

#### *Power-Down Format*

Setting Bit D8 of the control register places the AD7280A into software power-down. See the Power-Down section for more information. The default value of Bit D8 on power-up is 0.

#### *Software Reset*

Bit D7 of the control register allows the user to initiate a software reset of the AD7280A. Two write commands are required to complete the reset operation. Bit D7 must be set high to put the AD7280A into reset. Bit D7 must then be set low to take the AD7280A out of reset. A software reset resets all user configurable registers to their default values with the exception of the lower byte of the control register (Address 0x0E). When executing a software reset, care should be taken to ensure that Bits[D6:D0] are not incorrectly overwritten.

#### *Set Acquisition Time*

Bits[D6:D5] of the control register determine the acquisition time of the ADC. See the Acquisition Time section for more information. The default value of the acquisition time is 400 ns, that is, 00.

#### *Thermistor Termination Resistor*

Bit D3 of the control register should be set if the user wishes to use a single thermistor termination resistor on the $AUX_{TERM}$ pin. Note that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280A is set to its highest value, that is, 1.6 μs (set Bits[D6:D5] to 11). The default value of D3 is 0.

#### *Lock Device Address*

Bit D2 of the control register is used in conjunction with Bit D1 to allow individual device addresses for each AD7280A in the daisy chain to be defined and locked to the part. Bit D1 is used to generate the individual device addresses that are presented to each AD7280A in the daisy chain in the form of a write command. When Bit D2 is set high, the AD7280A locks to the device address presented to it. This new device address is used for all subsequent CRC calculations. When Bit D2 is set low, the device address of the AD7280A is not locked. In this case, a device address of 0x00 is used for CRC calculations. The default value of D2 is 0.

#### *Increment Device Address*

Bit D1 of the control register determines whether the AD7280A increments the device address that it receives as part of a write command when transferring that command up the daisy chain. When Bit D1 is set to 1, the device address is incremented as the command is passed up the chain. This mode of operation is used on initial power-up and when coming out of a hardware power-down to allow individual device addresses for each AD7280A in the daisy-chain stack to be defined. When D1 is set low, no change is made to the device address as the command is passed up the chain. The default value of D1 is 1.

#### *Daisy-Chain Register Readback*

Bit D0 of the control register enables the readback of individual registers from each AD7280A in a daisy chain. When Bit D0 is set high, the application of sufficient clocks allows the data stored in the register address identified by the read register to be shifted out of each AD7280A in turn. This data is passed down the daisy chain and read back by the DSP/microprocessor. When Bit D0 is set low, daisy-chain read is disabled. See the Daisy-Chain Interface section and the Examples of Interfacing with the AD7280A section. The default value of D0 is 1.

### CELL OVERVOLTAGE REGISTER

The cell overvoltage register determines the high voltage threshold of the AD7280A. Cell voltage conversions that exceed the overvoltage threshold trigger the alert output. The AD7280A allows the user to set the overvoltage threshold to a value from 1 V to 5 V. The resolution of the overvoltage threshold is eight bits, that is, 16 mV. The default value of the overvoltage threshold on power-up is 0xFF (5 V).

## CELL UNDERVOLTAGE REGISTER

The cell undervoltage register determines the low voltage threshold of the AD7280A. Cell voltage conversions lower than the undervoltage threshold trigger the alert output. The AD7280A allows the user to set the undervoltage threshold to a value from 1 V to 5 V. The resolution of the undervoltage threshold is eight bits, that is, 16 mV. The default value of the undervoltage threshold on power-up is 0x00 (1 V).

## AUX ADC OVERVOLTAGE REGISTER

The AUX ADC overvoltage register determines the high voltage threshold of the AD7280A auxiliary ADC inputs. Conversions that exceed this threshold trigger the alert output. The AD7280A allows the user to set the threshold to a value from 0 V to 5 V. The resolution is eight bits, that is, 19 mV. The default value of the auxiliary ADC overvoltage threshold on power-up is 0xFF (5 V).

## AUX ADC UNDERVOLTAGE REGISTER

The AUX ADC undervoltage register determines the low voltage threshold of the AD7280A auxiliary ADC inputs. Conversions that are lower than this threshold trigger the alert output. The AD7280A allows the user to set the threshold to a value from 0 V to 5 V. The resolution is eight bits, that is, 19 mV. The default value of the AUX ADC undervoltage threshold on power-up is 0x00 (0 V).

## ALERT REGISTER

The alert register determines the configuration of the alert function. The alert can be configured as a static or dynamic signal.

- The static signal is a high signal that is pulled low to indicate that an overvoltage or undervoltage on a cell or on the auxiliary ADC has occurred.
- The dynamic signal is a square wave, the frequency of which can be set to 100 Hz, 1 kHz, or 10 kHz.

When a number of AD7280As are operating in daisy-chain mode, the selection of static or dynamic alert is set on the AD7280A at the highest potential in the chain only. The alert registers on the remaining AD7280As in the chain should be programmed to pass the alert signal through the chain. Each part passes the static or dynamic alert signal through the chain or pulls the signal low to indicate that an overvoltage or undervoltage on a cell or on the auxiliary ADC has occurred.

See Table 11 and Table 12 for more information about the alert register settings. The default value of the alert register on power-up is 0x00.

## CELL BALANCE REGISTER

The cell balance register determines the status of the six cell balance outputs. The six CBx outputs are set by writing to Bits[D7:D2] of the cell balance register. The cell balance register is reset by a software reset or following a hardware power-down. The default value of the cell balance register on power-up is 0x00.

**Table 15. Cell Balance Register Settings**

| Bits | Description |
|---|---|
| D7 | Set CB6 output |
| | 0 = output off |
| | 1 = output on |
| D6 | Set CB5 output |
| | 0 = output off |
| | 1 = output on |
| D5 | Set CB4 output |
| | 0 = output off |
| | 1 = output on |
| D4 | Set CB3 output |
| | 0 = output off |
| | 1 = output on |
| D3 | Set CB2 output |
| | 0 = output off |
| | 1 = output on |
| D2 | Set CB1 output |
| | 0 = output off |
| | 1 = output on |
| [D1:D0] | Reserved; set to 0 |

## CBx TIMER REGISTERS

The CBx timer registers allow the user to program individual times for each cell balance output. The AD7280A allows the user to set the CBx timer to a value from 0 minutes to 36.9 minutes. The resolution of the CBx timers is 71.5 sec. The default value of the CBx timer registers on power-up is 0x00. When the CBx timer value is set to 0x00, the CBx timer is not activated; that is, the CBx outputs are all controlled by the contents of the cell balance register only. For more information, see the Cell Balancing Outputs section.

**Table 16. CBx Timer Register Settings**

| Bits | Description |
|---|---|
| [D7:D3] | 5-bit binary code to set the CB timer to a value from 0 minutes to 36.9 minutes |
| [D2:D0] | Reserved; set to 000 |

## PD TIMER REGISTER

The PD timer register allows the user to configure a set time after which the AD7280A is automatically powered down. The AD7280A allows the user to set the PD timer to a value from 0 minutes to 36.9 minutes. The resolution of the PD timer is 71.5 sec. When using the PD timer in conjunction with the CBx timers, the value programmed to the PD timer should exceed that programmed to the CBx timer by at least 71.5 sec because the PD timer takes priority over the CBx timers. The default value of the PD timer register on power-up is 0x00.

**Table 17. PD Timer Register Settings**

| Bits | Description |
|---|---|
| [D7:D3] | 5-bit binary code to set the PD timer to a value from 0 minutes to 36.9 minutes |
| [D2:D0] | Reserved; set to 000 |

## READ REGISTER

The read register, in conjunction with Bits[D13:D12] and Bit D0 of the control register, defines the read operations of the AD7280A. To read back a single register from either a single AD7280A or from a chain of AD7280A devices, the desired register address should first be written to the read register. To read back a series of conversion results from either a single AD7280A or from a chain of AD7280A devices, an address of 0x00 should be written to the read register. The default value of the read register on power-up is 0x00.

**Table 18. Read Register Settings**

| Bits | Description |
|---|---|
| [D7:D2] | 6-bit binary address for the register to be read |
| [D1:D0] | Reserved; set to 00 |

## $\overline{\text{CNVST}}$ CONTROL REGISTER

The $\overline{\text{CNVST}}$ control register allows the user to gate the input signal from the $\overline{\text{CNVST}}$ pin.

Bit D0 of the $\overline{\text{CNVST}}$ control register allows the user to hold the internal $\overline{\text{CNVST}}$ signal high regardless of any external noise or glitches on the $\overline{\text{CNVST}}$ pin. This setting can be used in noisy environments to prevent incorrect initiation of conversions. When using the rising edge of $\overline{\text{CS}}$ to perform a software convert start, it is recommended that the $\overline{\text{CNVST}}$ pin be gated out by setting Bit D0 high (see the Conversion Start Format section).

Bit D1 of the $\overline{\text{CNVST}}$ control register allows the user to open a window in the $\overline{\text{CNVST}}$ gate that allows a single $\overline{\text{CNVST}}$ pulse through. The window is closed automatically following a falling edge on the $\overline{\text{CNVST}}$ pin. To use this functionality, the user should write 10 to Bits[D1:D0] of the $\overline{\text{CNVST}}$ control register immediately before each conversion start request.

The default value of the $\overline{\text{CNVST}}$ control register on power-up is 0x00.

**Table 19. $\overline{\text{CNVST}}$ Control Register Settings**

| Bits [D7:D2] | Bit D1 | Bit D0 | Description |
|---|---|---|---|
| 000000 | 0 | 0 | $\overline{\text{CNVST}}$ input not gated (default). |
| 000000 | X | 1 | $\overline{\text{CNVST}}$ input gated. |
| 000000 | 1 | 0 | Allow single $\overline{\text{CNVST}}$ pulse. Additional $\overline{\text{CNVST}}$ pulses are gated. |

# SERIAL INTERFACE

The AD7280A serial interface is Mode 1 SPI compliant, that is, the clock polarity (CPOL) is 0, and the clock phase (CPHA) is 1. The interface consists of four signals: $\overline{CS}$, SCLK, SDI, and SDO. The SDI line is used to transfer data into the on-chip registers, and the SDO line is used to read the on-chip registers and conversion result registers. SCLK is the serial clock input for the device; all data transfers, either on SDI or on SDO, take place with respect to SCLK. Data is clocked into the AD7280A on the SCLK falling edge. Data is clocked out of the AD7280A on the SCLK rising edge. The $\overline{CS}$ input is used to frame the serial data being transferred to or from the device.

The AD7280A allows 32-bit data transfer only and resets a counter on the rising edge of $\overline{CS}$ to ensure that the AD7280A is automatically resynchronized with the DSP/microprocessor on every falling edge of $\overline{CS}$. Individual 8-bit or 16-bit words can be used to assemble a 32-bit command, but a single 32-bit wide $\overline{CS}$ frame is required to correctly structure the assembly of the 32-bit command.

The rising edge of $\overline{CS}$ can also be used to initiate the sequence of conversions by writing to the upper byte of the control register. Figure 2 shows the timing diagram for the serial interface of the AD7280A. See the Daisy-Chain Interface section for more information about the daisy-chain interface.

## WRITING TO THE AD7280A

In a battery monitoring application, up to eight AD7280As can be daisy-chained to allow up to 48 individual Li-Ion cell voltages to be monitored. Each write operation must, therefore, include a device address and a register address, in addition to the data to be written. An additional identifier bit is also required when addressing all AD7280As in the daisy chain. The AD7280A SPI interface, in combination with the daisy-chain interface, allows any register in the stack of eight AD7280As to be updated using one 32-bit write cycle. The 32-bit write sequence is shown in Table 20. The AD7280A also requires an 8-bit CRC to be included in each write command.

### *Device Address*

The device address is a 5-bit address that allows each individual AD7280A in the battery monitoring stack to be uniquely identified. On initial power-up, each AD7280A is configured with a default address of 0x00. A simple sequence of commands allows each AD7280A to recognize its unique device address in the stack (see the Initializing the AD7280A section).

This device address can then be locked to the AD7280A and used in subsequent read and write commands. The device address is written to and read from the AD7280A stack in reverse order, that is, LSB first.

### *Register Address*

The register map for the AD7280A is provided in Table 13. Each register address is six bits long and is used when writing to or reading from the on-chip registers of the AD7280A.

### *Register Data*

When issuing a write command to a part in the stack of AD7280A devices, the data to be written is an 8-bit word. As shown in Table 13, all read/write registers are eight bits wide. For more information about the correct settings for each register, see the Register Map section.

### *Address All Parts*

The AD7280A allows write commands to be issued simultaneously to all devices in the daisy chain, as well as write commands to individual AD7280As. A write to all devices in the daisy chain is completed by setting Bit D12 of the write command to 1. When issuing a write all command, the device address should be set to 0x00. This device address is also used to calculate the 8-bit CRC for transmission with the write all command.

### *8-Bit CRC*

The AD7280A includes an 8-bit cyclic redundancy check (CRC) on all write commands to either individual devices or to a chain of devices. An AD7280A that receives an invalid CRC in the write command does not execute the command. The CRC on the write command is calculated based on Bits[D31:D11] of the write command. These bits include the device address, the register address, the data to be written, the address all parts bit, and Bit D11. For more information about the CRC, see the Cyclic Redundancy Check section.

### *Bit Pattern (010)*

A required fixed bit pattern of 010 to Bits[D2:D0] of the 32-bit write command of the AD7280A provides an additional stage of verification. The correct position of this bit pattern is verified on each write command received by the AD7280A. An AD7280A that receives an incorrect bit pattern in the write command does not execute the command.

**Table 20. 32-Bit Write Cycle**

| Device Address[1] | Register Address | Register Data | Address All Parts | Reserved (0 Bit) | 8-Bit CRC | Bit Pattern (010) |
|---|---|---|---|---|---|---|
| D31 to D27 | D26 to D21 | D20 to D13 | D12 | D11 | D10 to D3 | D2 to D0 |

[1] The device address is configured LSB first. For example, to address the second device in the stack, that is, the first slave device, the sequence of bits input to the AD7280A should be 10000. The register address, data bits, and CRC bits are input MSB first.

## READING FROM THE AD7280A

There are two types of read operation for the AD7280A:

- Conversion results read
- Register data read

The data returned from a conversion result read operation includes the device address, the channel address, the write acknowledge bit, and the 8-bit CRC information, in addition to the 12 bits of conversion data. Table 21 illustrates the 32-bit read cycle for a conversion result read.

The data returned from a register data read operation includes the device address, the register address, the write acknowledge bit, and the 8-bit CRC information, in addition to the eight bits of register data. Table 22 illustrates the 32-bit read cycle for a register data read.

The AD7280A SPI interface, in combination with the daisy-chain interface, allows the conversion results of any AD7280A in a stack of eight AD7280As to be read back using an N × 8 × 32-bit read cycle, where N is defined as the number of conversions completed on that part, that is, 12, 9, or 6 (see Table 8).

### *Device Address*

The device address is described in the Writing to the AD7280A section. When reading back register or conversion data from the device using the daisy-chain readback mode, the SDI line must be set to write to a specific address. That is, the SDI line should not be allowed to idle high or low, and the address all parts bit must be set to 0. The address must be either the top part in the chain of AD7280A devices or an address with a value higher than that of the top part in the chain. Writing to the highest available address (Address 0x1F) and setting the address all parts bit to 0 is recommended. The 32-bit write command is 0xF800030A.

### *Channel Address*

The channel address allows each individual voltage and auxiliary ADC input result to be uniquely identified. Each channel address is four bits wide. The address for each channel is provided in the register map (see Table 13).

### *Register Address*

The register map for the AD7280A is provided in Table 13. Each register address is six bits long and is used when writing to or reading from the on-chip registers of the AD7280A.

### *Register Data*

The register data is the 8-bit register data that was requested in a previous write command.

### *Conversion Data*

The conversion data is the 12-bit conversion result from the cell voltage inputs, the auxiliary ADC inputs, or the ADC self-test conversion.

### *Write Acknowledge Bit*

As described in the Writing to the AD7280A section, an 8-bit CRC is included in the write command transmitted to the AD7280A. The CRC is calculated based on Bits[D31:D11]. A CRC check is completed before the write command is executed on the device.

Using the same CRC algorithm, the AD7280A calculates the CRC and compares it to the CRC that was received by the part in the transmitted write command. If the two CRC values match, the command is executed and the write acknowledge bit in the subsequent transmission of data from the device is set. If the transmitted and calculated CRCs do not match, the write command is not executed, and the write acknowledge bit is set to 0. For examples of the use of the write acknowledge bit, see the Write Acknowledge section.

### *8-Bit CRC*

The AD7280A includes an 8-bit cyclic redundancy check (CRC) on all data read back from the device. When reading back conversion data from the AD7280A, the 8-bit CRC includes the device address, the channel address, the conversion data, and the write acknowledge bit. When reading back register data from the AD7280A, the 8-bit CRC includes the device address, the register address, the register data, two reserved zero bits, and the write acknowledge bit. In both cases, the CRC is generated on Bits[D31:D10] of the 32-bit read cycle and is transmitted using Bits[D9:D2] of the same read cycle. For more information about the CRC, see the Cyclic Redundancy Check section.

**Table 21. 32-Bit Read Conversion Result Cycle**

| Device Address[1] | Channel Address | Conversion Data | Write Acknowledge | 8-Bit CRC | Reserved (0 Bits) |
|---|---|---|---|---|---|
| D31 to D27 | D26 to D23 | D22 to D11 | D10 | D9 to D2 | D1 to D0 |

[1] The device address is configured LSB first. For example, to address the second device in the stack, that is, the first slave device, the sequence of bits input to the AD7280A should be 10000. The register address, channel address, data bits, and CRC bits are input MSB first.

**Table 22. 32-Bit Read Register Data Cycle**

| Device Address[1] | Register Address | Register Data | Reserved (0 Bits) | Write Acknowledge | 8-Bit CRC | Reserved (0 Bits) |
|---|---|---|---|---|---|---|
| D31 to D27 | D26 to D21 | D20 to D13 | D12 to D11 | D10 | D9 to D2 | D1 to D0 |

[1] The device address is configured LSB first. For example, to address the second device in the stack, that is, the first slave device, the sequence of bits input to the AD7280A should be 10000. The register address, data bits, and CRC bits are input MSB first.

# DAISY-CHAIN INTERFACE

In a battery monitoring application, up to eight AD7280As can be daisy-chained together to allow up to 48 individual lithium ion cell voltages to be monitored. Each AD7280A is capable of monitoring up to six Li-Ion cells and is powered from the top and bottom voltage of the six Li-Ion cells. As a result, the supply voltages of each AD7280A are offset by up to 30 V from adjacent AD7280As in the chain. For this reason, a standard serial interface daisy-chain method cannot be used.

The AD7280A includes a daisy-chain interface separate from the standard SPI interface. This daisy-chain interface allows each AD7280A in the chain to relay data to and from adjacent AD7280As.

As described in the Serial Interface section, the SPI interface consists of four signals: $\overline{CS}$, SCLK, SDI, and SDO. In addition to these pins, there are three optional interface pins: ALERT, $\overline{CNVST}$, and $\overline{PD}$. Each of these seven interface signals is mirrored in the daisy-chain interface to allow communication between adjacent devices in a daisy chain. For example, the serial clock of each AD7280A is received on the SCLK pin and passed to the device above it in the daisy chain using the SCLKhi pin.

The $\overline{CS}$, SCLK, SDI, $\overline{CNVST}$, and $\overline{PD}$ pins, which pass data up the daisy chain, operate as 3 V or 5 V logic interface pins when the AD7280A is configured as a master device; these pins operate as daisy-chain interface pins when the AD7280A is configured as a slave device.

The SDO and ALERT pins operate as 3 V or 5 V logic interface pins when the AD7280A is configured as a master device. These pins are tristated when the AD7280A is configured as a slave device. Two additional pins, SDOlo and ALERTlo, are required to pass data down the daisy chain.

As described in the Serial Interface section, only one 32-bit write cycle is required to write to any register in a stack of eight AD7280As. The readback of conversion data from all channels monitoring the battery stack requires an $N \times 8 \times 32$-bit read cycle, where N is defined as the number of conversions completed on that part, that is, 12, 9, or 6. The recommended SCLK frequency to ensure correct operation of the daisy-chain interface is 1 MHz. With a 1 MHz SCLK, it takes approximately 1.54 ms to read back the voltage conversions on 48 channels.

When reading from a single device in a stack of AD7280A devices (daisy-chain register readback is disabled; Bit D0 of the control register = 0), the SCLK frequency must be lower than 1 MHz to read back the register data from parts up the chain of AD7280As. This is due to the propagation delay between adjacent parts in the daisy chain (see $t_{DELAY}$ in Table 3). This delay does not apply if the part is reading registers or conversion data from the part in daisy-chain mode; that is, the maximum SCLK of 1 MHz can always be used in daisy-chain mode.

## ADDRESSING THE AD7280A WHILE READING BACK CONVERSION OR REGISTER DATA

An SPI interface reads data and writes data at the same time: as the device is reading in one command, it provides output data on the SDO pin in the same read/write cycle. When reading both register and conversion data from the AD7280A using the daisy-chain readback mode, the SDI line must not idle high or low; it must be set up to address and write to either the top device used in the daisy chain or to a device with an address higher than the top device used in the daisy chain. In either case, the address all parts bit (Bit D12 in the write command) should be set to 0, and a valid CRC must be included. Writing to the highest available address, that is, Address 0x1F, and setting the address all parts bit to 0 is recommended. The 32-bit write command is 0xF800030A.

## INITIALIZING THE AD7280A

On initial power-up and when coming out of power-down, all AD7280As default to a device address of 0x00. The following sequence of commands should be followed to allow each AD7280A in the daisy chain to recognize its unique position in the chain. The following sequence allows device addresses on all parts in the chain to be configured and confirmed through daisy-chain readback. A subset of these commands can also be used to configure the device addresses without readback confirmation.

1. A single command should be sent to all devices in the chain to assert the lock device address bit (D2), to deassert the increment device address bit (D1), and to assert the daisy-chain register readback bit (D0). The 32-bit write command is 0x01C2B6E2.
2. A second command should be sent to all devices in the chain to write the address of the lower byte of the control register, 0x0E, to the read register on all devices. The 32-bit write command is 0x038716CA.
3. To verify that all AD7280As in the chain have received and locked their unique device address, a daisy-chain register read should be requested from all devices. This can be done by continuing to apply sets of 32 SCLKs framed by $\overline{CS}$ until the lower byte of the control register of each device in the daisy chain has been read back. The user should confirm that all device addresses are in sequence. The 32-bit write command is 0xF800030A.
4. This command should be repeated until the control register data has been read back from all devices in the daisy chain.

## WRITE ACKNOWLEDGE

For all write commands received by the AD7280A, the device internally performs a CRC calculation on Bits[D31:D11] of the received data and verifies this CRC against the CRC transmitted by the DSP/microprocessor. If there is a difference between the CRC generated internally and the CRC received from the DSP/microprocessor, the AD7280A does not perform the write operation. The AD7280A also checks for the correct position of the bit pattern 010 in the write command, as described in the Serial Interface section. If there is a difference between the expected 010 pattern and the pattern received from the DSP/microprocessor, the AD7280A does not perform the write operation.

If a subsequent 32 SCLK cycle framed by a $\overline{CS}$ pulse is applied to the AD7280A, Bit D10 (the write acknowledge bit) on SDO indicates to the processor whether the last write to the device was successful (the write acknowledge bit is set if the write was successful). The write acknowledge bit is included in the 8-bit CRC on the read cycle. Note that the read register must be loaded with any value other than 0x00 for the write acknowledge bit to be correctly passed down the chain of AD7280A devices.

Following is an example of how the write acknowledge bit can be used when writing to and configuring a stack of AD7280A devices. This example sets the high byte of the control register settings on all devices in a stack of eight AD7280As.

1. Execute a write all command to load the read register with 0x0E (addresses the low byte of the control register).
2. Execute a write all command to set the high byte of the control register (Address 0x0D) to the desired values.
3. Apply an additional eight sets of 32 SCLKs, each framed by $\overline{CS}$, to the master device. The device address bits, D31 to D27, should be set to 0x1F for each 32 SCLK frame. The 32-bit write command is 0xF800030A. The data read back from the master device on the first 32 SCLK frame includes the write acknowledge bit for the control register high byte write to the master device. The data read back on the second 32 SCLK frame includes the write acknowledge bit for the control register high byte write to the first slave device in the stack, and so on.

To read back the write acknowledge bit from slave AD7280As in a daisy chain when single registers are being written to, Bits[D13:D12] of the control register on lower devices in the chain must be set to 1 (a no-read operation on those devices). For example, to read back the write acknowledge bit from Device 1 in the chain after writing to a register on that device, the read operation of Device 0, the master device, must be turned off. Also, the SCLK frequency must be lower than 1 MHz when reading back the write acknowledge bit from devices higher in the chain than the master device in this mode.

## CYCLIC REDUNDANCY CHECK

The AD7280A 32-bit SPI interface includes an 8-bit cyclic redundancy check (CRC) on the read and write cycles. The CRC can be used to detect alterations in the data during transmission to and from the AD7280A. The principle of a cyclic redundancy check is that the data to be transmitted is divided by a fixed polynomial. The remainder of this mathematical operation is then attached to the data and forms part of the transmission. At the receiving end, the same mathematical operation should be completed on the data received. This operation confirms that the data received is the same as the data that was originally transmitted.

The polynomial used by the AD7280A to calculate the CRC bits is $x^8 + x^5 + x^3 + x^2 + x + 1$. This CRC polynomial has a Hamming distance of 4 for calculations up to 22 bits of data. The division is implemented using the digital circuit shown in Figure 40.

### *Write Operation CRC*

For writes to the AD7280A, the CRC must be computed in the DSP/microprocessor and sent as part of the write command. The CRC must be computed on Bits[D31:D11] of the write command, that is, the device address, the register address, the data to be written, the address all parts bit, and Bit D11, which is a reserved zero input bit. The data is divided by the CRC polynomial, and the 8-bit remainder, following the division, becomes the CRC bits, CRC_7 to CRC_0.

If the user is addressing all parts in a stack of AD7280As (by asserting the address all parts bit, D12), the CRC must be computed using a device address of 0x00, and the data written to the device must have a device address of 0x00. The AD7280A performs the same CRC calculation on Bits[D31:D11] of the received data, and it verifies this CRC against the CRC transmitted by the DSP/microprocessor. If there is a difference between the CRC generated within the AD7280A and the CRC received from the DSP/microprocessor, the AD7280A does not perform the write operation. To allow the user to verify that the command has been received and implemented by the AD7280As in the stack, a write acknowledge bit is also included in the 32-bit read cycles. For more information about the write acknowledge bit, see the Write Acknowledge section.

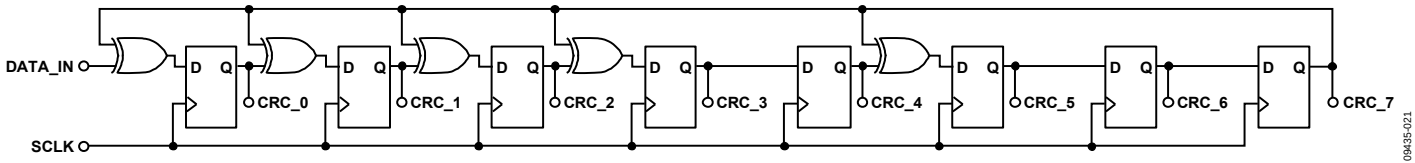


*Figure 40. CRC Implementation*

### Read Operation CRC

For reads from the AD7280A, the 8-bit CRC is generated by the AD7280A based on Bits[D31:D10] of the 32-bit read cycle and is transmitted using Bits[D9:D2] of the same read cycle. The data received is divided by the CRC polynomial, and the 8-bit remainder, following the division, becomes the CRC bits, CRC_7 to CRC_0. The user can compare the CRC bits calculated with the CRC that was received from the AD7280A to verify that there was no alteration in the data that was transmitted by the AD7280A.

When operating in a daisy chain, each AD7280A receives conversion or register data from the device above it in the daisy chain and performs a CRC calculation on the received data. If there is a difference between the CRC generated internally and the CRC received from the device above it in the daisy chain, the AD7280A replaces the received CRC by an inversion of the internally generated CRC.

### CRC Pseudocode

The following pseudocode can be used to calculate the CRC. The following variables must first be declared:

- Num_Bits is the number of data bits used to calculate the CRC result: 21 for a data write to the AD7280A, and 22 for a data read from the AD7280A.
- i is an integer variable.
- xor_1, xor_2, xor_3, xor_4, and xor_5 are integer variables. These outputs of the XOR gates start with the leftmost XOR gate in the circuit implementation (see Figure 40).
- data_in represents the data bits that the CRC is calculated on: Bits[D31:D11] for a write operation, and Bits[D31:D10] for a read operation. This data supplies the input to the first XOR gate.
- CRC_0, CRC_1, CRC_2, CRC_3, CRC_4, CRC_5, CRC_6, and CRC_7 are integer variables. The outputs of the shift registers start at the leftmost shift register in the circuit implementation (see Figure 40).

With the exception of data_in, all variables should be initialized to 0. The following code implements the CRC calculation as shown in Figure 40.

```
for (i=Num_Bits; i>=0; i--)
      {
      xor_5 = CRC_4 ^ CRC_7;
      xor_4 = CRC_2 ^ CRC_7;
      xor_3 = CRC_1 ^ CRC_7;
      xor_2 = CRC_0 ^ CRC_7;
      xor_1 = data_in[i] ^ CRC_7;

      CRC_7 = CRC_6;
      CRC_6 = CRC_5;
      CRC_5 = xor_5;
      CRC_4 = CRC_3;
      CRC_3 = xor_4;
      CRC_2 = xor_3;
      CRC_1 = xor_2;
      CRC_0 = xor_1;
      }
```

### CRC Calculation Example 1

This example shows how a 32-bit write command, including the CRC calculation, to the high byte of the control register on the master device (Device 0) is assembled. The data to be written is 0x0C.

The CRC is computed in the DSP/microprocessor on Bits[D31:D11], that is, the device address, the register address, the data to be written to the register, the address all parts bit, and the reserved bit.

- Device address: 00000 (0x00)
- Register address: 001101 (0x0D)
- Data: 00001100 (0x0C)
- Address all parts bit: 0 (0x0)
- Reserved bit: 0 (0x0)

The data input to the CRC algorithm is, therefore, 00000011010000110000 (0x003430).

Following the completion of the calculation, the value of CRC_7 to CRC_0 is 01010001 (0x51). The data that is sent to the AD7280A for this serial write is, therefore, 0000 0001 1010 0001 1000 0010 1000 1010 (0x01A1828A).

### CRC Calculation Example 2

This example shows how a 32-bit write command, including the CRC calculation, to the high byte of the control register on Device 1 in the daisy chain is assembled. The data to be written is 0x0C.

The CRC is computed in the DSP/microprocessor on Bits[D31:D11], that is, the device address, the register address, the data to be written to the register, the address all parts bit, and the reserved bit.

- Device address (written LSB first): 10000 (0x10)
- Register address: 001101 (0x0D)
- Data: 00001100 (0x0C)
- Address all parts bit: 0 (0x0)
- Reserved bit: 0 (0x0)

The data input to the CRC algorithm is, therefore, 10000011010000110000 (0x103430).

Following the completion of the calculation, the value of CRC_7 to CRC_0 is 01110100 (0x74). The data that is sent to the AD7280A for this serial write is, therefore, 1000 0001 1010 0001 1000 0011 1010 0010 (0x81A183A2).

### *CRC Calculation Example 3*

This example shows the breakdown of a 32-bit register read from the low byte of the control register of the master device, that is, Device 0.

The CRC is computed in the AD7280A on Bits[D31:D10], that is, the device address, the register address, the register data, two reserved zero bits, and the write acknowledge bit. The calculated CRC is sent along with Bits[D31:D10] and Bits[D1:D0] to the DSP/microprocessor.

The data received from the AD7280A is as follows:
0000 0001 1100 0010 1000 0110 0110 1000 (0x01C28668).

- Device address: 00000 (0x00)
- Register address: 001110 (0x0E)
- Register data: 00010100 (0x14)
- Reserved 0s: 0 (0x0)
- Write acknowledge: 1 (0x1)
- CRC: 10011010 (0x9A)
- Reserved 0s: 0 (0x0)

The CRC bits are computed again in the DSP/microprocessor on Bits[D31:D10] of the data that is read back from the AD7280A. The data input to the CRC algorithm is, therefore, 00000001110000010100001 (0x0070A1).

Following the completion of the calculation, the value of CRC_7 to CRC_0 is 10011010 (0x9A). This result matches the CRC that was sent from the AD7280A; therefore, this transmission of data is valid.

### *CRC Calculation Example 4*

This example shows the breakdown of a 32-bit conversion result read from the Cell Voltage 3 conversion result register of Device 1.

The CRC is computed in the AD7280A on Bits[D31:D10], that is, the device address, the channel address, the conversion data, and the write acknowledge bit. The calculated CRC is sent along with Bits[D31:D10] and Bits[D1:D0] to the DSP/microprocessor.

The data received from the AD7280A is as follows:
1000 0001 0100 1100 1101 0101 0001 1000 (0x814CD518).

- Device address (read LSB first): 10000 (0x10)
- Channel address: 0010 (0x2)
- Conversion data: 100110011010 (0x99A)
- Write acknowledge: 1 (0x1)
- CRC: 01000110 (0x46)
- Reserved 0s: 0 (0x0)

The CRC bits are computed again in the DSP/microprocessor on Bits[D31:D10] of the data that is read back from the AD7280A. The data input to the CRC algorithm is, therefore, 10000001010011001101 01 (0x205335).

Following the completion of the calculation, the value of CRC_7 to CRC_0 is 01000110 (0x46). This result matches the CRC that was sent from the AD7280A; therefore, this transmission of data is valid.

# EXAMPLES OF INTERFACING WITH THE AD7280A

The AD7280A supports a number of read options. The user can read back the results from

- All conversions completed on all parts in the chain
- Individual registers on all parts in the chain
- Individual registers on selected parts in the chain

In each case, the user must first write to the read register on the selected parts to configure that part to supply the correct data on the outputs. When reading back an individual register, the address of that register should be written to the read register of the selected part. When reading back conversion results from any or all parts in the chain, an address of 0x00 should be written to the read register of the selected parts.

When the address written to the read register is 0x00, the conversion results selected for readback are controlled by setting Bits[D13:D12] of the control register (see Table 14). These bits allow the user to select one of four different read-back options:

- Read back 12 conversion results: six voltage and six auxiliary.
- Read back nine conversion results: six voltage and three auxiliary.
- Read back six conversion results: six voltage results only.
- Switch off the read operation on this part.

To read back an individual register from a single AD7280A in the daisy chain, follow these steps:

1. On all other parts in the chain, set Bits[D13:D12] of the control register to 11 to select the no-read operation on those parts.
2. On the targeted part, set Bits[D13:D12] of the control register to turn on the read operation.

Note that it is more efficient in terms of 32-bit write cycles to first switch off the read operation on all AD7280As in the daisy chain. This is achieved with a single write cycle, using Bit D12 in the write command to address all parts in the chain. The user can then address the individual part and set Bits[D13:D12] of the control register to turn on the read operation for that part.

## CONVERT AND READBACK ROUTINE

When conversion data from any or all of the AD7280As in a daisy chain is read back, the conversion results returned from the AD7280A are the last completed set of conversions on that part. It is recommended that the user also set Bits[D15:D14] of the control register to select the number of conversions to be completed on each part and initiate the conversions through either the $\overline{\text{CNVST}}$ pin or the rising edge of $\overline{\text{CS}}$ as part of the read operation. In this way, the user can implement a simple convert and readback routine with the most efficient number of 32-bit write and read operations.

A general example of this routine, which converts and reads back from all parts in the AD7280A daisy chain, is as follows:

1. Write 0x00 to the read register on all parts in the daisy chain. Note that 0x00 is the default value of this register on power-up and following a software reset operation.
2. Write to the control register on all parts. Set Bits[D15:D14] to select the required conversions. Set Bits[D13:D12] to select the required conversion results for readback.
3. Initiate the conversions through either the falling edge of $\overline{\text{CNVST}}$ or the rising edge of $\overline{\text{CS}}$ (set Bit D11 of the control register to select the conversion start format).
4. Allow sufficient time for each conversion to be completed plus $t_{WAIT}$. See the Converting Cell Voltages and Auxiliary ADC Inputs section.
5. Apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back.

## EXAMPLES

The following examples of conversion and/or readback routines can be used in an application that implements a chain of AD7280A devices to monitor the voltage and/or auxiliary ADC inputs of the AD7280A on a stack of lithium ion batteries.

### *Example 1: Initialize All Parts in a Daisy Chain on Initial Power-Up and When Coming Out of Power-Down*

Example 1 shows a typical device initialization routine.

1. To initialize all device addresses, set Bit D2 and Bit D0 of the control register to 1, and set Bit D1 of the control register to 0 on all parts in the chain. The 32-bit write command is 0x01C2B6E2 (see Table 23, Write 1).
2. Write the register address corresponding to the lower byte of the control register to the read register on all parts. The 32-bit write command is 0x038716CA (see Table 23, Write 2).
3. Apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each device in the chain to be read back. All conversion readbacks should simultaneously write the 32-bit command 0xF800030A, as described in the Serial Interface section (see Table 23, Write 3). This read is used to verify that all AD7280As in the chain have received and locked their unique device addresses. Confirm that all device addresses are in sequence.

### *Example 2: Convert and Read All Parts, All Voltages, and All Auxiliary ADC Inputs*

In this example, it is assumed that all AD7280As in the daisy chain have been initialized to their correct device addresses.

1. Write Register Address 0x00 to the read register on all parts. A device address of 0x00 is used when computing the CRC for commands to write to all parts. The 32-bit write command is 0x38011CA (see Table 24, Write 1).

   Note that 0x00 is the default value of the read register on power-up and after a software reset; therefore, this write operation may not be necessary.
2. Set Bits[D15:D12] of the control register to 0 on all parts. The 32-bit write command is 0x01A0131A (see Table 24, Write 2).

   Note that this is the default value of Bits[D15:D12] of the control register on power-up and after a software reset; therefore, this write operation may not be necessary.
3. Program the $\overline{CNVST}$ control register to 0x02 on all parts to allow conversions to be initiated using the $\overline{CNVST}$ pin. The 32-bit write command is 0x03A0546A (see Table 24, Write 3).
4. Initiate conversions through the falling edge of $\overline{CNVST}$.
5. Allow sufficient time for all conversions to be completed plus $t_{WAIT}$. Following the completion of all conversions, apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each conversion result to be read back. The 32-bit write command is 0xF800030A, as described in the Serial Interface section (see Table 24, Write 4).

**Table 23. Example 1: Initializing All AD7280A Devices in a Daisy Chain**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 001110 | 00010101 | 1 | 0 | 11011100 | 010 | 0x01C2B6E2 |
| Write 2 | 00000 | 011100 | 00111000 | 1 | 0 | 11011001 | 010 | 0x038716CA |
| Write 3 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

**Table 24. Example 2: Converting and Reading All Voltages and All Auxiliary ADC Inputs from All AD7280A Devices**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 011100 | 00000000 | 1 | 0 | 00111001 | 010 | 0x038011CA |
| Write 2 | 00000 | 001101 | 00000000 | 1 | 0 | 01100011 | 010 | 0x01A0131A |
| Write 3 | 00000 | 011101 | 00000010 | 1 | 0 | 10000101 | 010 | 0x03A0546A |
| Write 4 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

### *Example 3: Convert and Read All Parts, All Voltages, and Three Auxiliary ADC Inputs per Part*

In this example, it is assumed that all AD7280As in the daisy chain have been initialized to their correct device addresses.

1. Write Register Address 0x00 to the read register on all parts. A device address of 0x00 is used when computing the CRC for commands to write to all parts. The 32-bit write command is 0x038011CA (see Table 25, Write 1).

   Note that 0x00 is the default value of the read register on power-up and after a software reset; therefore, this write operation may not be necessary.

2. Set Bit D15 and Bit D13 of the control register to 0 on all parts. Set Bit D14 and Bit D12 of the control register to 1 on all parts. The 32-bit write command is 0x01AA1062 (see Table 25, Write 2).
3. Program the $\overline{\text{CNVST}}$ control register to 0x02 on all parts to allow conversions to be initiated using the $\overline{\text{CNVST}}$ pin. The 32-bit write command is 0x03A0546A (see Table 25, Write 3).
4. Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
5. Allow sufficient time for all conversions to be completed plus $t_{WAIT}$. Following the completion of all conversions, apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs for each conversion result to be read back. The 32-bit write command is 0xF800030A, as described in the Serial Interface section (see Table 25, Write 4).

**Table 25. Example 3: Converting and Reading All Voltages and Three Auxiliary ADC Inputs from All AD7280A Devices**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 011100 | 00000000 | 1 | 0 | 00111001 | 010 | 0x038011CA |
| Write 2 | 00000 | 001101 | 01010000 | 1 | 0 | 00001100 | 010 | 0x01AA1062 |
| Write 3 | 00000 | 011101 | 00000010 | 1 | 0 | 10000101 | 010 | 0x03A0546A |
| Write 4 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

### *Example 4: Convert and Read a Single Voltage or Auxiliary ADC Input Result from One Part*

In this example, it is assumed that all AD7280As in the daisy chain have been initialized to their correct device addresses.

1. The register address corresponding to the voltage or auxiliary ADC input result to be read should be written to the read register of the part to be read (see Table 13 for register addresses). In this example, the Cell Voltage 6 register result is read from Device 3 in the stack. The 32-bit write command is 0xC382865A (see Table 26, Write 1).
2. Set Bits[D13:D12] of the control register to 1 on all parts. This setting turns off the read operation on all parts. The 32-bit write command is 0x01B617EA (see Table 26, Write 2).
3. Set Bits[D13:D12] of the control register of the part to be read from such that the required voltage is read back. With the exception of a self-test conversion, it is not possible to convert on a single channel; six, nine, or 12 conversions must be completed. This example reads a voltage conversion from Device 3 in the stack; therefore, Bit D14 and Bit D12 of the control register should be set to 0, and Bit D15 and Bit D13 should be set to 1 on Device 3. The 32-bit write command is 0xC1B400FA (see Table 26, Write 3).
4. Program the $\overline{\text{CNVST}}$ control register to 0x02 on Device 3 to allow conversions to be initiated using the $\overline{\text{CNVST}}$ pin on that part. The 32-bit write command is 0xC3A0417A (see Table 26, Write 4).
5. Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
6. Allow sufficient time for all conversions to be completed plus $t_{WAIT}$.
7. Program the $\overline{\text{CNVST}}$ control register to gate the $\overline{\text{CNVST}}$ signal on all parts. The 32-bit write command is 0x03A0340A (see Table 26, Write 5). This write prevents unintentional conversions from being initiated by noise or glitches on the $\overline{\text{CNVST}}$ pin. This write also updates the on-chip output registers of all devices in the daisy chain.
8. Apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs to read back the desired voltage or auxiliary ADC result. This frame should simultaneously write the 32-bit command 0xF800030A, as described in the Serial Interface section (see Table 26, Write 6).

   Note that when reading from a single device in a stack of AD7280As, the SCLK frequency must be lower than 1 MHz to read back the register data from parts higher in the chain than the master device.

**Table 26. Example 4: Converting and Reading a Single Voltage or Auxiliary ADC Result from One AD7280A Device**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 11000 | 011100 | 00010100 | 0 | 0 | 11001011 | 010 | 0xC382865A |
| Write 2 | 00000 | 001101 | 10110000 | 1 | 0 | 11111101 | 010 | 0x01B617EA |
| Write 3 | 11000 | 001101 | 10100000 | 0 | 0 | 00011111 | 010 | 0xC1B400FA |
| Write 4 | 11000 | 011101 | 00000010 | 0 | 0 | 10000111 | 010 | 0xC3A0417A |
| Write 5 | 00000 | 011101 | 00000001 | 1 | 0 | 10000001 | 010 | 0x03A0340A |
| Write 6 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

### *Example 5: Read a Single Configuration Register on All Parts*

In this example, it is assumed that all AD7280As in the daisy chain have been initialized to their correct device addresses.

1. Set Bit D0 of the control register to 1 on all parts. This write enables the daisy-chain register read operation on all parts. The 32-bit write command is 0x01C2B6E2 (see Table 27, Write 1).
2. The register address corresponding to the configuration register to be read should be written to the read register on all parts (see Table 13 for register addresses). In this example, the cell balance register is read from all parts. The 32-bit write command is 0x038A12B2 (see Table 27, Write 2).
3. Apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each device in the stack to read back the desired register contents from all parts. This frame should simultaneously write the 32-bit command 0xF800030A, as described in the Serial Interface section (see Table 27, Write 3).

### *Example 6: Read a Single Configuration Register from One Part*

In this example, it is assumed that all AD7280As in the daisy chain have been initialized to their correct device addresses.

1. Set Bits[D13:D12] of the control register to 1 on all parts. This setting turns off the read operation on all parts. The 32-bit write command is 0x01A6151A (see Table 28, Write 1).
2. Set Bits[D13:D12] of the control register of the part to be read from to 0. In this example, Device 1 in the stack is to be read from. The 32-bit write command is 0x81A00222 (see Table 28, Write 2).
3. The register address corresponding to the configuration register to be read should be written to the read register of the part that is to be read (see Table 13 for register addresses). This example reads the alert register from Device 1 in the stack. The 32-bit write command is 0x8389800A (see Table 28, Write 3).
4. Apply a $\overline{CS}$ low pulse that frames 32 SCLKs to read back the desired register contents. This frame should simultaneously write the 32-bit command 0xF800030A, as described in the Serial Interface section (see Table 28, Write 4). When reading from a single device in a stack of AD7280As, the SCLK frequency must be lower than 1 MHz to read back the register data from parts higher in the chain than the master device.

**Table 27. Example 5: Reading a Single Configuration Register from All AD7280A Devices**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 001110 | 00010101 | 1 | 0 | 11011100 | 010 | 0x01C2B6E2 |
| Write 2 | 00000 | 011100 | 01010000 | 1 | 0 | 01010110 | 010 | 0x038A12B2 |
| Write 3 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

**Table 28. Example 6: Reading a Single Configuration Register from One AD7280A Device**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 001101 | 00110000 | 1 | 0 | 10100011 | 010 | 0x01A6151A |
| Write 2 | 10000 | 001101 | 00000000 | 0 | 0 | 01000100 | 010 | 0x81A00222 |
| Write 3 | 10000 | 011100 | 01001100 | 0 | 0 | 00000001 | 010 | 0x8389800A |
| Write 4 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

### *Example 7: Self-Test Conversion on All Parts*

Example 7 shows a self-test conversion routine for all parts in a daisy chain.

1. To select the self-test conversion, set Bits[D15:D14] of the control register to 1, and set Bits[D13:D12] of the control register to 0 on all parts. The 32-bit write command is 0x01B81092 (see Table 29, Write 1).
2. Set Bit D0 of the control register to 1 on all parts. This setting enables the daisy-chain register read operation on all parts. The 32-bit write command is 0x01C2B6E2 (see Table 29, Write 2).
3. The register address corresponding to the self-test conversion should be written to the read register of all parts (see Table 13 for register addresses). The 32-bit write command is 0x038617CA (see Table 29, Write 3).
4. Program the $\overline{\text{CNVST}}$ control register to 0x02 on all parts to allow conversions to be initiated using the $\overline{\text{CNVST}}$ pin. The 32-bit write command is 0x03A0546A (see Table 29, Write 4).
5. Initiate conversions through the falling edge of $\overline{\text{CNVST}}$.
6. Allow sufficient time for the self-test conversions to be completed plus $t_{WAIT}$.
7. The $\overline{\text{CNVST}}$ control register should be programmed to gate the $\overline{\text{CNVST}}$ signal on all parts. The 32-bit write command is 0x03A0340A (see Table 29, Write 5). This write prevents unintentional conversions from being initiated by noise or glitches on the $\overline{\text{CNVST}}$ pin. This write also updates the on-chip output registers of all devices in the daisy chain.
8. Apply a $\overline{\text{CS}}$ low pulse that frames 32 SCLKs to read back the desired voltage. This frame should simultaneously write the 32-bit command 0xF800030A, as described in the Serial Interface section (see Table 29, Write 6).

### *Example 8: Software Reset on All Parts*

Example 8 shows a software reset routine for all parts in a daisy chain.

1. Set Bit D7 of the control register to 1 on all parts to place the AD7280A into software reset. The 32-bit write command is 0x01D2B412 (see Table 30, Write 1).
2. Set Bit D7 of the control register to 0 on all parts to take the AD7280A out of software reset. The 32-bit write command is 0x01C2B6E2 (see Table 30, Write 2).

**Table 29. Example 7: Self-Test Conversion on All AD7280A Devices**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 001101 | 11000000 | 1 | 0 | 00010010 | 010 | 0x01B81092 |
| Write 2 | 00000 | 001110 | 00010101 | 1 | 0 | 11011100 | 010 | 0x01C2B6E2 |
| Write 3 | 00000 | 011100 | 00110000 | 1 | 0 | 11111001 | 010 | 0x038617CA |
| Write 4 | 00000 | 011101 | 00000010 | 1 | 0 | 10000101 | 010 | 0x03A0546A |
| Write 5 | 00000 | 011101 | 00000001 | 1 | 0 | 10000001 | 010 | 0x03A0340A |
| Write 6 | 11111 | 000000 | 00000000 | 0 | 0 | 01100001 | 010 | 0xF800030A |

**Table 30. Example 8: Software Reset for All AD7280A Devices**

| Write Command | Device Address | Register Address | Data | Write All | D11 | 8-Bit CRC | D2 to D0 | 32-Bit Write Command |
|---|---|---|---|---|---|---|---|---|
| Write 1 | 00000 | 001110 | 10010101 | 1 | 0 | 10000010 | 010 | 0x01D2B412 |
| Write 2 | 00000 | 001110 | 00010101 | 1 | 0 | 11011100 | 010 | 0x01C2B6E2 |

# EMC GUIDELINES

## SCHEMATIC AND LAYOUT GUIDELINES

To optimize the performance of a chain of AD7280A devices under noisy conditions—for example, when experiencing electromagnetic interference—the following schematic and layout guidelines should be observed (see Figure 29).

1. All AD7280A devices in a daisy chain should be physically located on a single printed circuit board (PCB). Daisy-chain connections between PCBs are not recommended. Individual PCBs can be used for separate daisy chains. In this case, however, communication between PCBs is via a communication protocol such as SPI or CAN.
2. Individual 22 pF capacitors should be placed on each daisy-chain connection. The capacitors should be terminated to either the $V_{SS}$ pin of the upper device or the $V_{DD}$ pin of the lower device, depending on the direction in which data is flowing in the daisy chain. The $\overline{PD}$, $\overline{CS}$, SCLK, SDI, and $\overline{CNVST}$ daisy-chain connections pass data up the chain. The 22 pF capacitors on these pins should be terminated to the $V_{SS}$ pin of the upper device in the chain. The SDOlo and ALERTlo daisy-chain connections pass data down the chain. The 22 pF capacitors on these pins should be terminated to the $V_{DD}$ pin of the lower device in the chain.
3. A direct, low impedance trace should connect the $V_{DD}$ pin of the lower device with the $V_{SS}$ pin of the upper device. The AD7280A daisy-chain connections operate at the $V_{DD}/V_{SS}$ voltage of the adjacent AD7280As. Ensuring a low impedance path between the supplies optimizes the performance of the daisy-chain communications.
4. The application PCB should have a minimum of four layers. The AD7280A daisy-chain connections should be routed on an inner layer of the PCB.
5. The AD7280A daisy-chain connections should be shielded above and below by a $V_{SS}$ supply plane connected to the $V_{SS}$ pin of the upper device in the chain. The shield should extend from the $V_{SS}$ and daisy-chain low pins of the upper device (Pin 15, Pin 17, and Pin 21 to Pin 28) to cover the daisy-chain high pins of the lower device (Pin 42 to Pin 48), as well as a low impedance trace to the $V_{DD}$ pin. This shield provides maximum protection to the daisy-chain connections when operating in a noisy environment.
6. The AD7280A devices should be placed as close together as possible on the PCB to minimize the length of the daisy-chain connections.
7. To minimize noise reaching the $V_{DD}/V_{SS}$ pins of the AD7280A, ferrite beads should be inserted into the $V_{DD}$ and $V_{SS}$ supply traces coming from the battery. These beads can be inserted into the PCB traces between the battery cell connection on the PCB and the individual supply pins.

   Note that these ferrite beads can be replaced with a small value of resistance. The maximum value of resistance that can be used is 20 Ω. A resistor should not be included on the $V_{SS}$ line to the master chip. Instead, a direct connection should be made from the battery cell connector to the $V_{SS}$ pin.

Analog Devices, Inc., also recommends the following:

- Inclusion of a 100 nF capacitor across the six individual cells that are monitored by the AD7280A. This capacitor should be placed physically close to the battery cell connector on the PCB.
- Correct termination of all unused pins on the device. More information about the correct termination of unused pins can be found in the Pin Configuration and Function Descriptions section.

## OPERATION IN A NOISY ENVIRONMENT

When the AD7280A is operating in a noisy environment—for example, when electromagnetic interference is experienced—glitches can occur on the SPI or daisy-chain inputs and outputs. To limit the effect that such glitches may have on the operation of the AD7280A, each daisy-chain input is passed through a filter before being applied internally within the device. The filter on the $\overline{PD}$ pin is 130 µs wide (see the Power-Down section for more information). The filter on the remaining daisy-chain inputs ($\overline{CS}$, SCLK, SDI, $\overline{CNVST}$, SDIhi, and ALERThi) is 150 ns wide. Glitches wider than these values on any of the pins can have an effect on the AD7280A, and care should be taken to ensure correct operation.

Glitches that occur on the SCLK and $\overline{CS}$ pins can result in the AD7280A losing synchronization with the DSP/microprocessor. However, such a loss of synchronization affects only the 32-bit word during which the glitch occurred. The AD7280A interface is reset on the rising edge of $\overline{CS}$ to ensure that the part is resynchronized, as described in the Serial Interface section.

Glitches that occur on the SDI or SDOhi pin can result in a change of state of any of the bits in the 32-bit words that are written to or read from the chain of AD7280As. In this event, the 8-bit CRC received by the AD7280A or by the DSP/microprocessor should not match the CRC that is calculated based on the 32-bit word that was transmitted.

Glitches that occur on the ALERThi pin are observed on the alert signal when output from the master device. Care should be taken when designing the alert response software or hardware to ensure that such glitches are treated appropriately in the system.

Glitches that occur on the $\overline{CNVST}$ pin may be interpreted as a conversion start request. If this occurs during a read operation, it can result in incorrect data being read back from the AD7280A.

If a second convert start signal is received by the AD7280A while the conversion results are being read back, the data being read back from the device, or chain of devices, can be corrupted. The corruption of data occurs at the point in which the second convert start signal is introduced. Any data read back prior to the second convert start signal is correct, but data read back after the second convert start signal may be corrupted.

Note that the corruption of data is not limited to the conversion result. The device address, channel address, and CRC data can also be corrupted. The $\overline{\text{CNVST}}$ control register should be used to gate the convert start signal. This prevents any glitches that occur on the $\overline{\text{CNVST}}$ pin from being applied directly to the internal circuitry of the AD7280A.

## SOFTWARE FLOWCHART

See Figure 41 for a software flowchart of a suggested sequence of steps that should be considered when operating the AD7280A in a noisy environment.

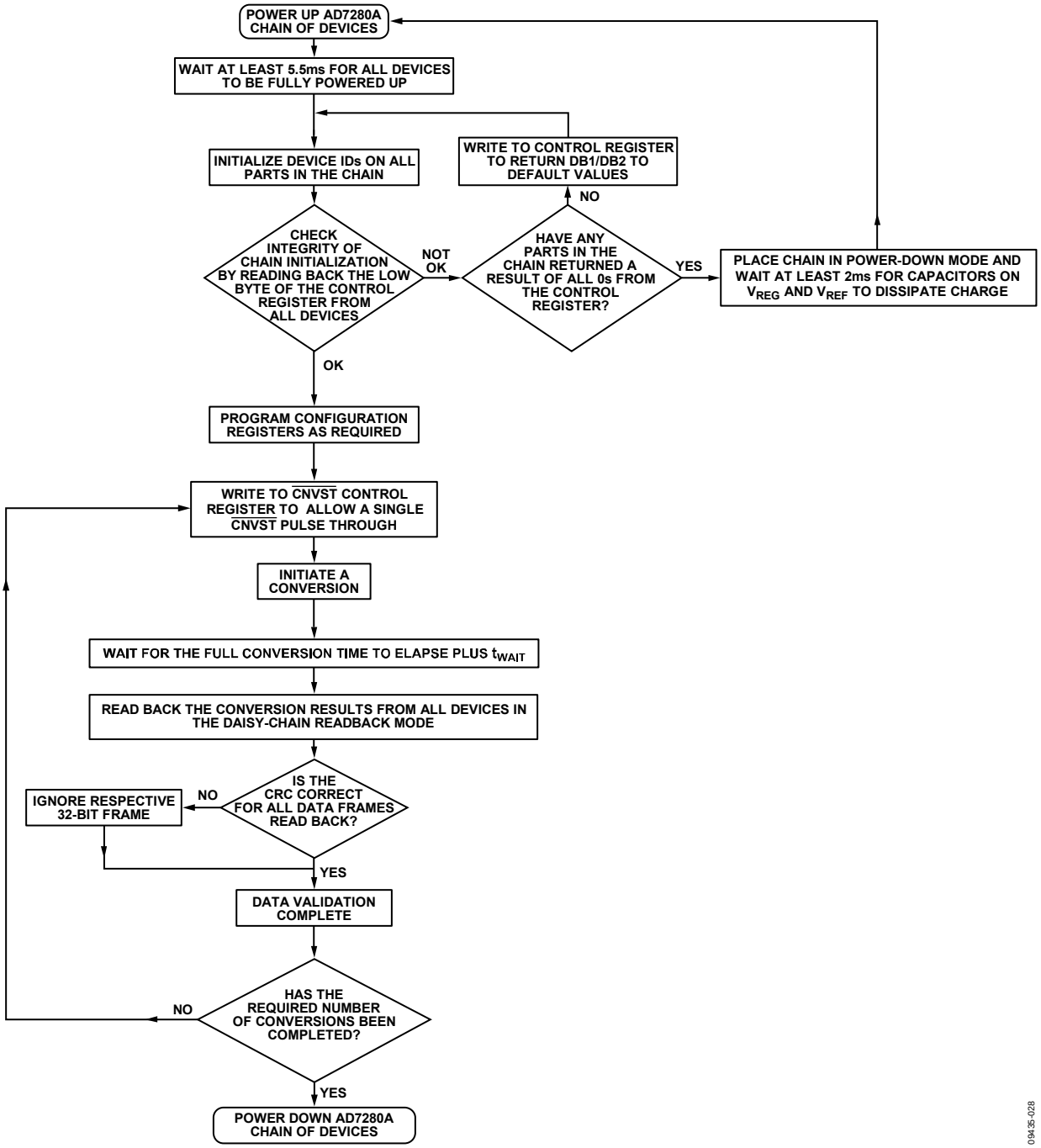


*Figure 41. Suggested Software Flowchart When Operating in a Noisy Environment*

# OUTLINE DIMENSIONS

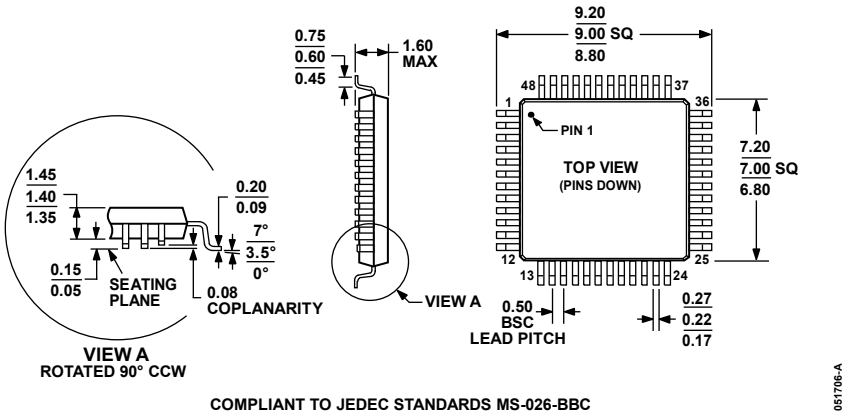


*Figure 42. 48-Lead Low Profile Quad Flat Package [LQFP]*
*(ST-48)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7280ABSTZ | −40°C to +105°C | 48-Lead LQFP | ST-48 |
| AD7280ABSTZ-RL | −40°C to +105°C | 48-Lead LQFP | ST-48 |
| AD7280AWBSTZ | −40°C to +105°C | 48-Lead LQFP | ST-48 |
| AD7280AWBSTZ-RL | −40°C to +105°C | 48-Lead LQFP | ST-48 |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The AD7280AW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

# NOTES