Dual 600 MHz, 50 mW Current Feedback Amplifier

Data Sheet **AD8002**

FEATURES

- **Excellent video specifications (R_L = 150 Ω, G = +2)**
  - **Gain flatness: 0.1 dB to 60 MHz**
  - **Differential gain error: 0.01%**
  - **Differential phase error: 0.02°**
- **Low power**
  - **Maximum power supply current (50 mW): 5.0 mA/amp**
- **High speed and fast settling**
  - **−3 dB bandwidth (G = +1): 600 MHz**
  - **−3 dB bandwidth (G = +2): 500 MHz**
  - **Slew rate: 1200 V/µs**
  - **Settling time to 0.1%: 16 ns**
- **Low distortion**
  - **THD at f_C = 5 MHz: −65 dBc**
  - **Third-order intercept at f_1 = 10 MHz: 33 dBm**
  - **SFDR at f = 5 MHz: −66 dB**
  - **Crosstalk at f = 5 MHz: −60 dB**
- **High output drive**
  - **Over 70 mA output current**
  - **Drives up to eight back terminated 75 Ω loads (four loads/side) while maintaining good differential gain/phase performance (0.01%/0.17°)**
- **Available in 8-lead SOIC and MSOP packages**

APPLICATIONS

- **Analog-to-digital drivers**
- **Video line drivers**
- **Differential line drivers**
- **Professional cameras**
- **Video switchers**
- **Special effects**
- **RF receivers**

GENERAL DESCRIPTION

The AD8002 is a dual, low power, high speed amplifier designed to operate on ±5 V supplies. The AD8002 features unique transimpedance linearization circuitry, which allows the AD8002 to drive video loads with excellent differential gain and phase performance on only 50 mW of power per amplifier. The AD8002 is a current feedback amplifier and features gain flatness of 0.1 dB to 60 MHz while offering differential gain and phase error of 0.01% and 0.02°, which makes the AD8002 ideal for professional video electronics such as cameras and video switchers. Additionally, the low distortion and fast settling of the AD8002 make it ideal for buffer high speed analog-to-digital converters (ADCs).

PIN CONNECTION BLOCK DIAGRAM

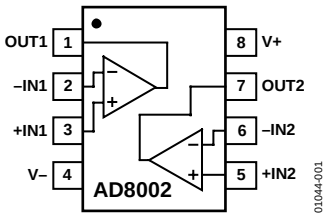


Figure 1.

The AD8002 offers a low power of 5.0 mA/amp maximum (V_S = ±5 V) and can run on a single 12 V power supply, yet is capable of delivering over 70 mA of load current. It is offered in 8-lead SOIC and MSOP packages. These features make this amplifier ideal for portable and battery-powered applications where size and power are critical.

The bandwidth of 600 MHz along with 1200 V/µs of slew rate make the AD8002 useful in many general-purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8002 is available in the industrial temperature range of −40°C to +85°C.

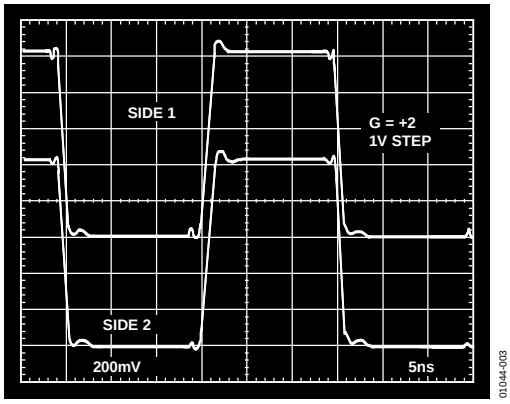


Figure 2. 1 V Step Response, G = +1

Rev. E **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

8/15—Rev. D to Rev. E

Updated Format ... Universal
Deleted 8-Lead Plastic DIP ... Universal
Changes to Features Section ... 1
Deleted Figure 1; Renumbered Sequentially ... 1
Changes to Table 1 ... 3
Change to Figure 3 ... 5
Added Pin Configurations and Function Descriptions Section, Figure 4, Figure 5, and Table 3; Renumbered Sequentially ... 6
Change to Figure 10 ... 7
Change to Figure 16 ... 8
Change to Figure ... 9
Change to Figure 34 ... 11
Change to Figure 32 ... 11
Added Test Circuits Section and Figure 42 to Figure 47 ... 13
Change to Theory of Operation Section ... 14
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 21

4/01—Rev. C to Rev. D

Max Ratings Changed ... 3

SPECIFICATIONS

At T_A = 25°C, V_S = ±5 V, R_L = 100 Ω, R_C[1] = 75 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth					
R Package	G = +2, R_F = 681 Ω		500		MHz
	G = +1, R_F = 953 Ω		600		MHz
RM Package	G = +2, R_F = 681 Ω		500		MHz
	G = +1, R_F = 1 kΩ		600		MHz
Bandwidth for 0.1 dB Flatness					
R Package	G = +2, R_F = 681 Ω		90		MHz
RM Package	G = +2, R_F = 681 Ω		60		MHz
Slew Rate	G = +2, V_{OUT} = 2 V step		700		V/µs
	G = −1, V_{OUT} = 2 V step		1200		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		16		ns
Rise and Fall Time	G = +2, V_{OUT} = 2 V step, R_F = 750 Ω		2.4		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion (THD)	f_C = 5 MHz, V_{OUT} = 2 V p-p, G = +2, R_L = 100 Ω		−65		dBc
Crosstalk (Output to Output)	f = 5 MHz, G = +2		−60		dB
Input Voltage Noise	f = 10 kHz, R_C = 0 Ω		2.0		nV/√Hz
Input Current Noise	f = 10 kHz, +IN1,+IN2		2.0		pA/√Hz
	f = 10 kHz, −IN1, −IN2		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.02		Degrees
Third-Order Intercept	f_1= 10 MHz		33		dBm
1 dB Gain Compression	f = 10 MHz		14		dBm
Spurious-Free Dynamic Range (SFDR)	f = 5 MHz		−66		dB
DC PERFORMANCE					
Input Offset Voltage			2.0	6	mV
	T_{MIN} to T_{MAX}		2.0	9	mV
Offset Drift			10		µV/°C
Input Bias Current (−IN1, −IN2)		−25	+5.0	+25	µA
	T_{MIN} to T_{MAX}	−35		+35	µA
Input Bias Current (+IN1, +IN2)		−6.0	+3.0	+6.0	µA
	T_{MIN} to T_{MAX}	−10		+10	µA
Open-Loop Transresistance	V_{OUT} = ±2.5 V	250	900		kΩ
	T_{MIN} to T_{MAX}	175			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+IN1, +IN2		10		MΩ
	−IN1, −IN2		50		Ω
Input Capacitance	+IN1, +IN2		1.5		pF
Input Common-Mode Voltage Range			±3.2		V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	49	54		dB
Input Current (−IN1, −IN2)	V_{CM} = ±2.5 V, T_{MIN} to T_{MAX}		0.3	1.0	µA/V
Input Current (+IN1, +IN2)	V_{CM} = ±2.5 V, T_{MIN} to T_{MAX}		0.2	0.9	µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	±2.7	±3.1		V
Output Current[2]			70		mA
Short-Circuit Current[2]		85	110		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		±3.0		±6.0	V
Quiescent Current/Both Amplifiers	T_{MIN} to T_{MAX}		10.0	11.5	mA
Power Supply Rejection Ratio	$+V_S$ = +4 V to +6 V, $-V_S$ = −5 V	60	75		dB
	$-V_S$ = −4 V to −6 V, $+V_S$ = +5 V	49	56		dB
Input Current (–IN1, –IN2)	T_{MIN} to T_{MAX}		0.5	2.5	µA/V
Input Current (+IN1, +IN2)	T_{MIN} to T_{MAX}		0.1	0.5	µA/V

[1] R_C is recommended to reduce peaking and minimize input reflections at frequencies above 300 MHz. However, R_C is not required.
[2] Output current is limited by the maximum power dissipation in the package. See Figure 3.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	13.2 V
Internal Power Dissipation[1]	
SOIC (R)	0.9 W
MSOP (RM)	0.6 W
Input Common-Mode Voltage	$\pm V_S$
Differential Input Voltage	±1.2 V
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C

[1] Specification is for device in free air:
8-lead SOIC: θ_{JA} = 155°C/W.
8-lead MSOP: θ_{JA} = 200°C/W.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8002 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

Although the AD8002 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

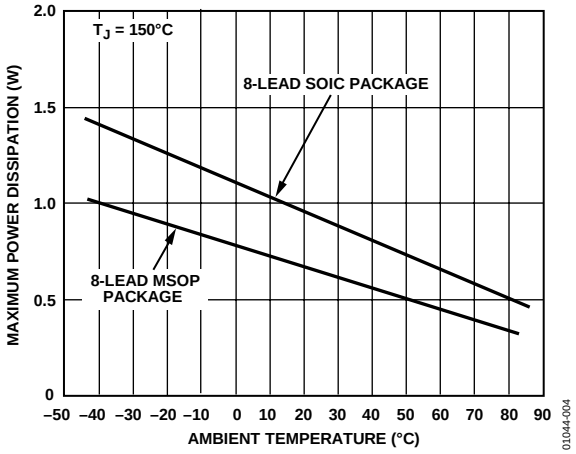


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

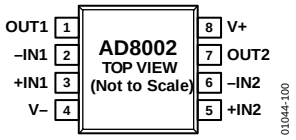


Figure 4. 8-Lead SOIC

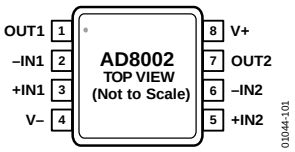


Figure 5. 8-Lead MSOP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT1	Output 1
2	−IN1	Inverting Input 1
3	+IN1	Noninverting Input 1
4	V−	V_{EE} or Negative Supply
5	+IN2	Noninverting Input 2
6	−IN2	Inverting Input 2
7	OUT2	Output 2
8	V+	V_{CC} or Positive Supply

TYPICAL PERFORMANCE CHARACTERISTICS

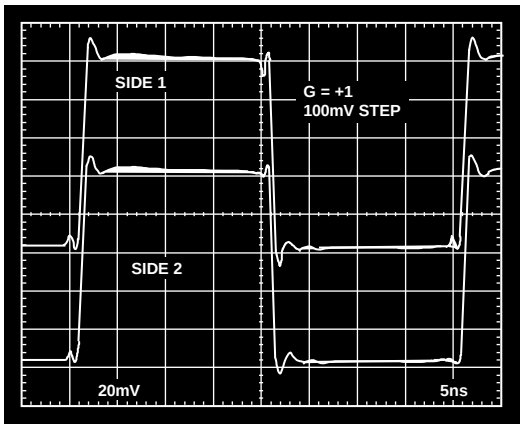


Figure 6. 100 mV Step Response, G = +1

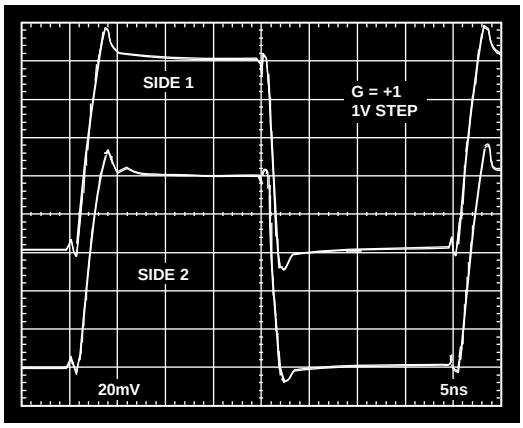


Figure 7. 1 V Step Response, G = +1

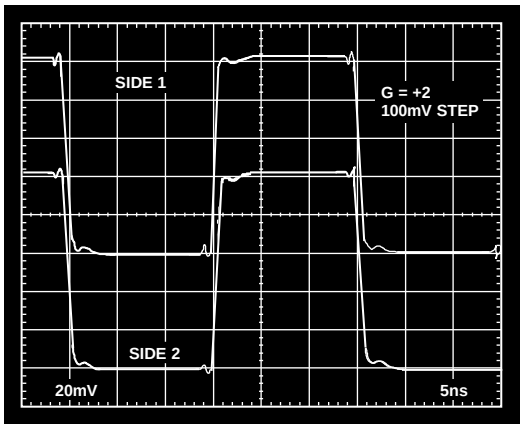


Figure 8. 100 mV Step Response, G = +2

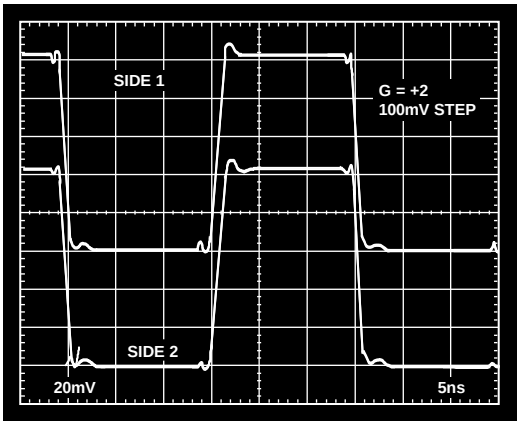


Figure 9. 1 V Step Response, G = +2

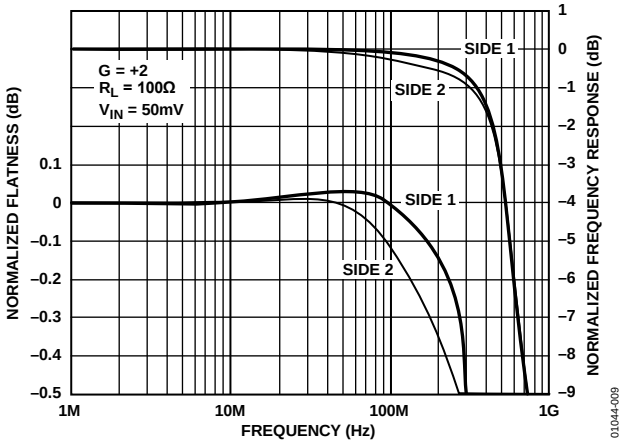


Figure 10. Frequency Response and Flatness, G = +2 (See Figure 41)

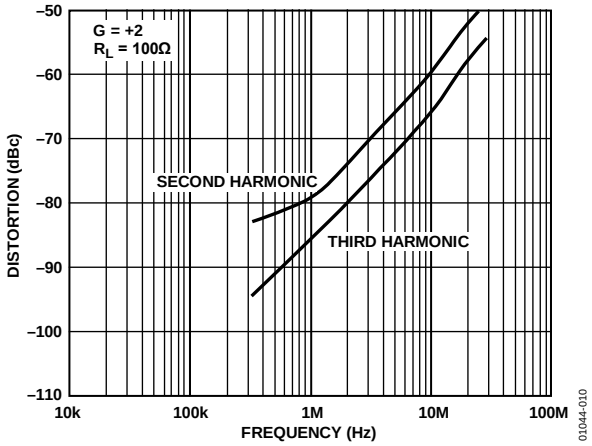


Figure 11. Distortion vs. Frequency, G = +2, R_L = 100 Ω

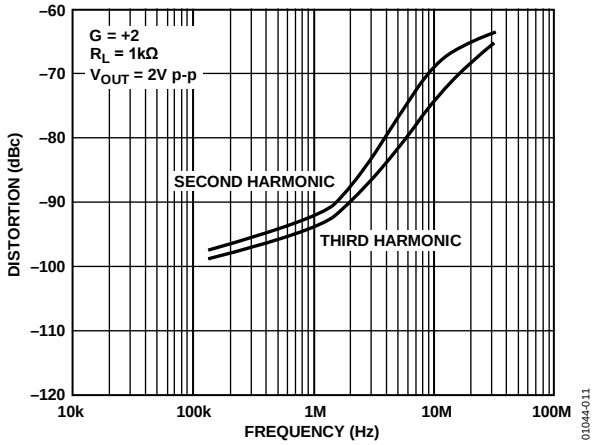


Figure 12. Distortion vs. Frequency, G = +2, R_L = 1 kΩ

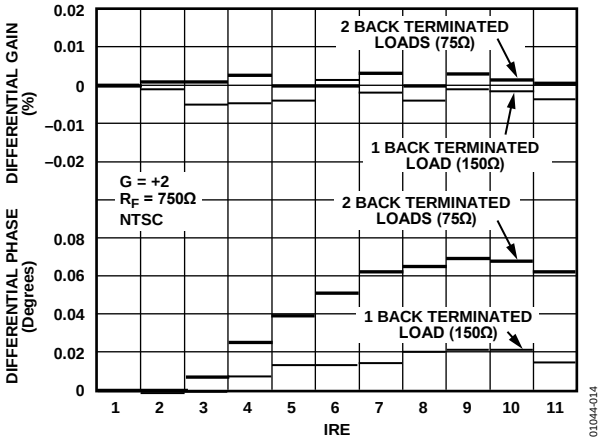


Figure 15. Differential Gain and Differential Phase (per Amplifier)

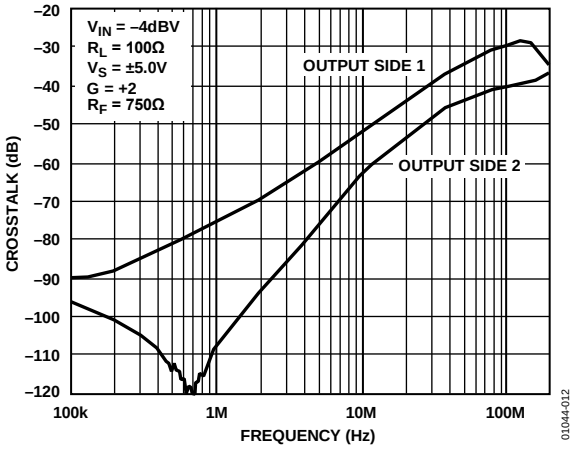


Figure 13. Crosstalk (Output to Output) vs. Frequency

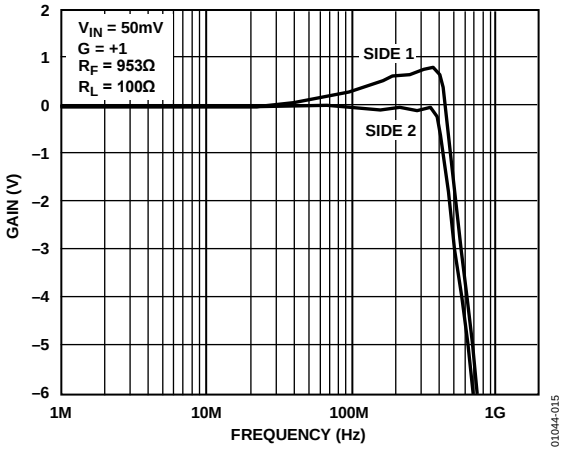
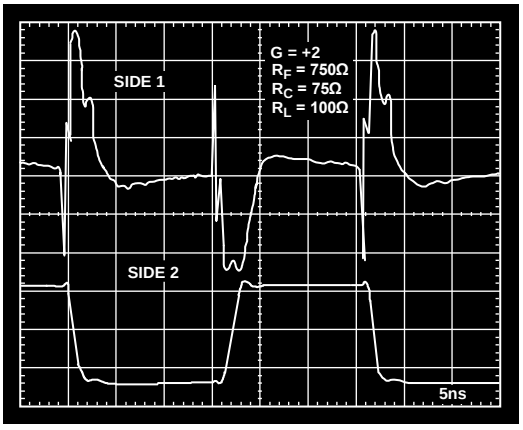


Figure 16. Gain vs. Frequency Response, G = +1 (See Figure 42)



SIDE 1: V_{IN} = 0V; 8mV/DIV RTO
SIDE 2: 1V STEP RTO; 400mV/DIV

Figure 14. Pulse Crosstalk, Worst Case, 1 V Step

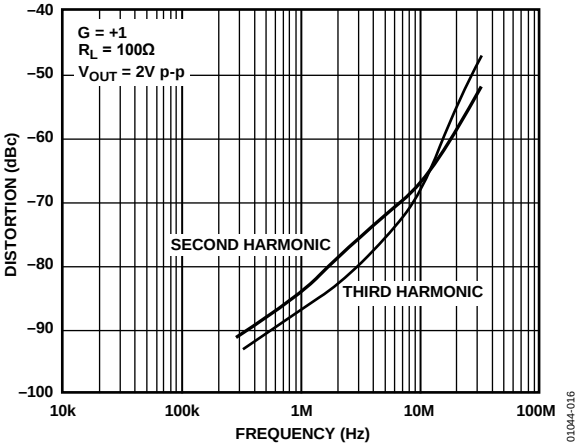


Figure 17. Distortion vs. Frequency, G = +1, R_L = 100 Ω

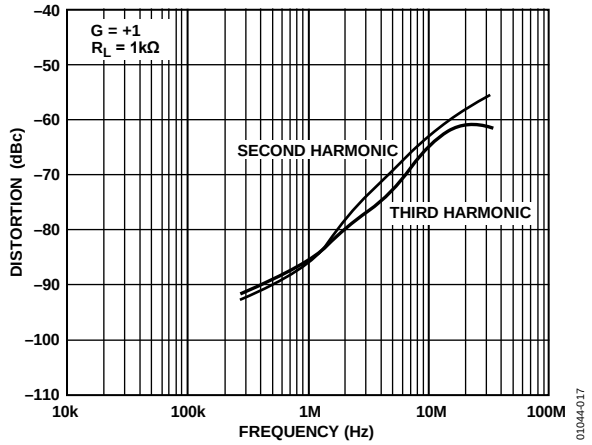


Figure 18. Distortion vs. Frequency, G = +1, R_L = 1 kΩ

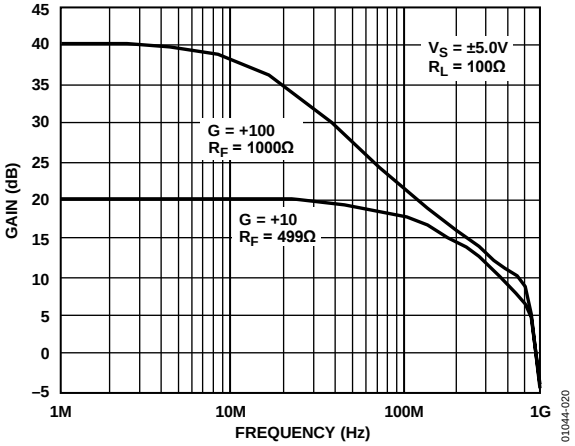


Figure 21. Frequency Response, G = +10, G = +100

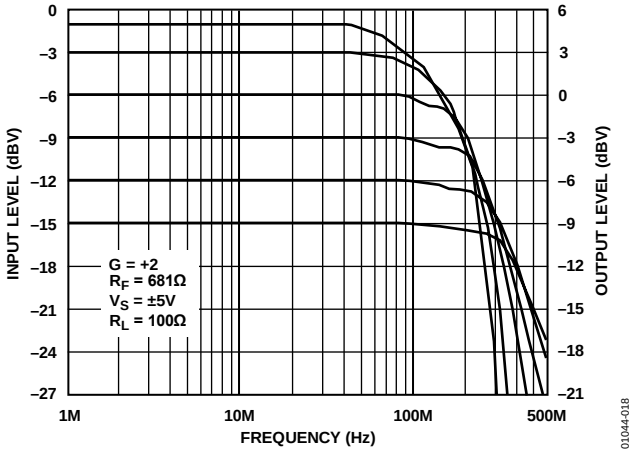


Figure 19. Large Signal Frequency Response, G = +2

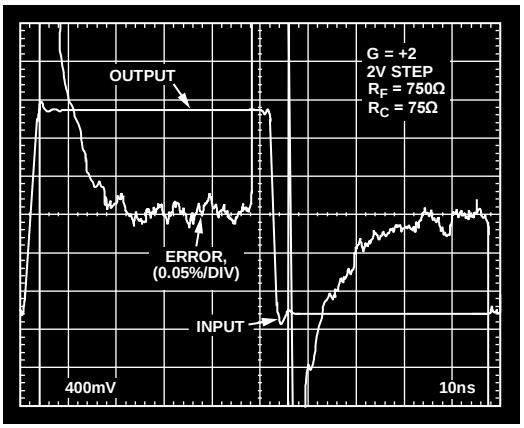


Figure 22. Short Term Settling Time

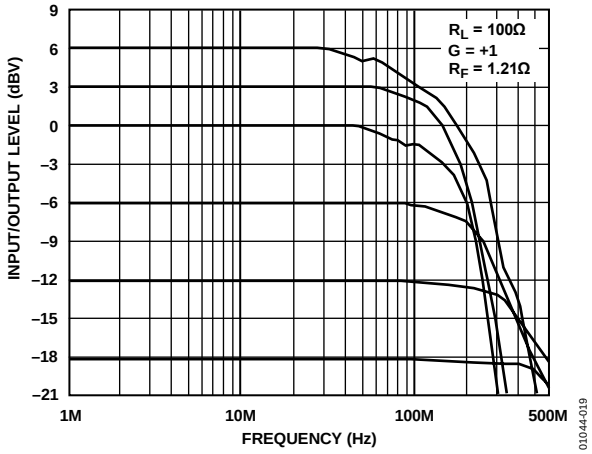


Figure 20. Large Signal Frequency Response, G = +1 (See Figure 43)

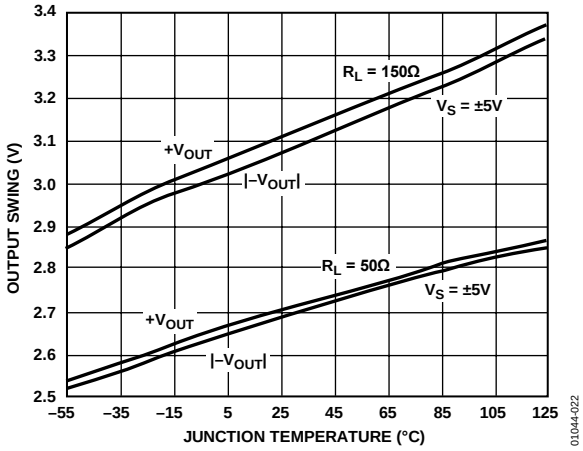


Figure 23. Output Swing vs. Junction Temperature

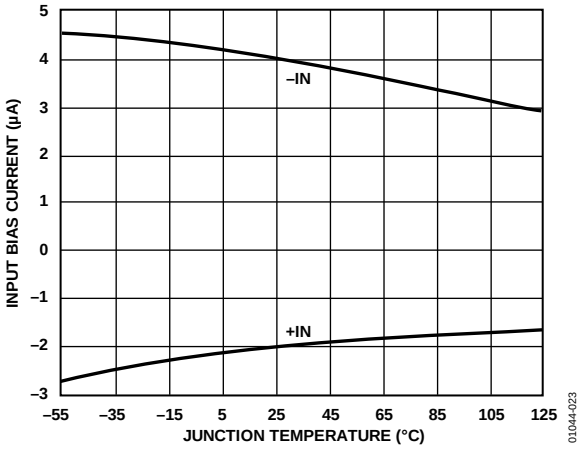


Figure 24. Input Bias Current vs. Junction Temperature

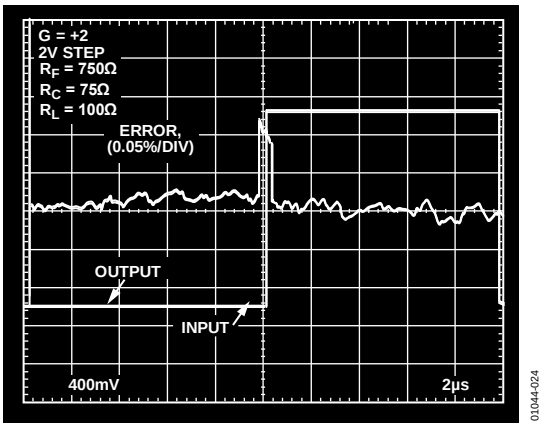


Figure 25. Long Term Settling Time

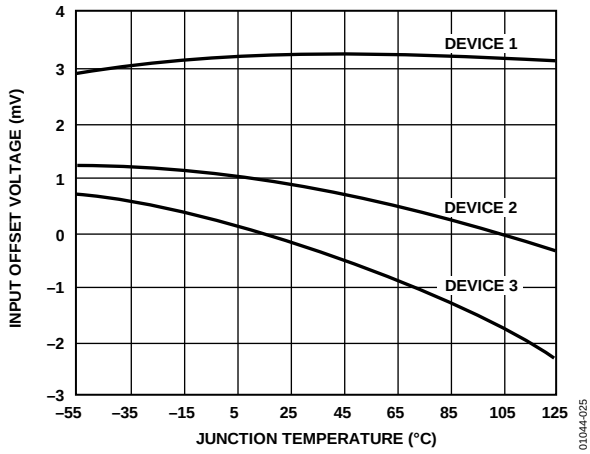


Figure 26. Input Offset Voltage vs. Junction Temperature

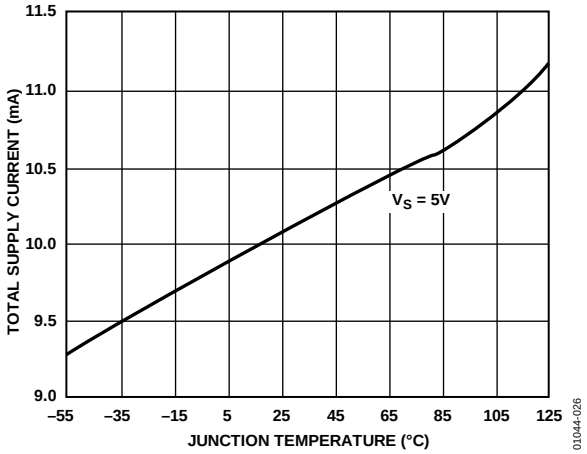


Figure 27. Total Supply Current vs. Junction Temperature

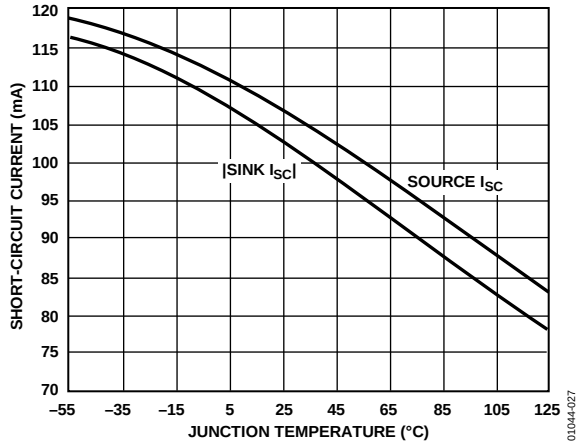


Figure 28. Short-Circuit Current vs. Junction Temperature

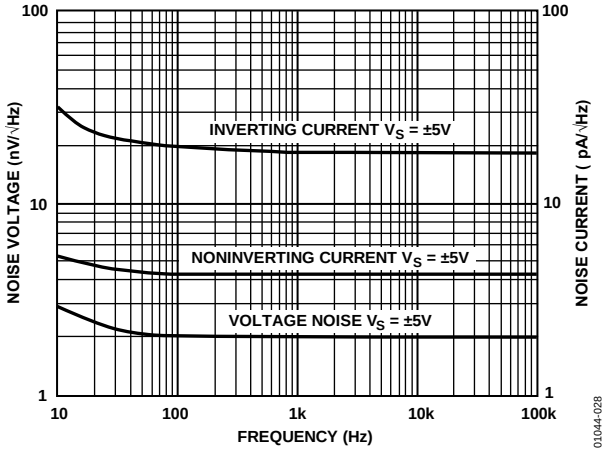


Figure 29. Noise Voltage vs. Frequency

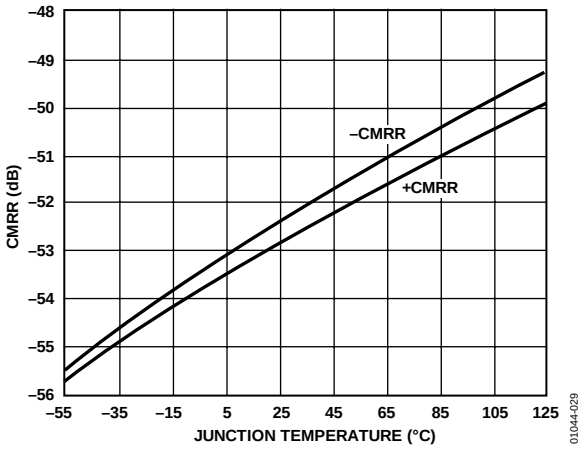


Figure 30. Common-Mode Rejection Ratio (CMRR) vs. Junction Temperature

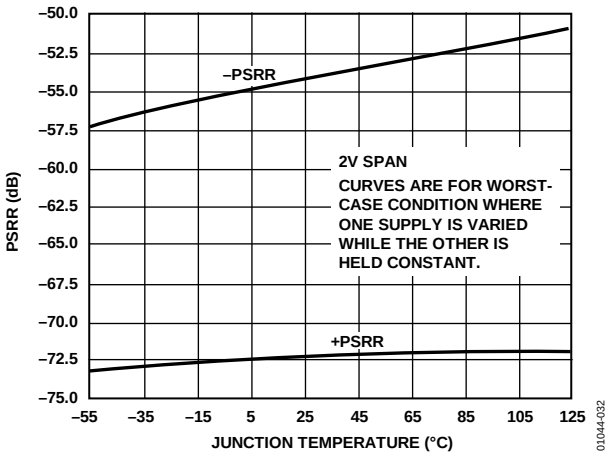


Figure 33. Power Supply Rejection Ration (PSRR) vs. Junction Temperature

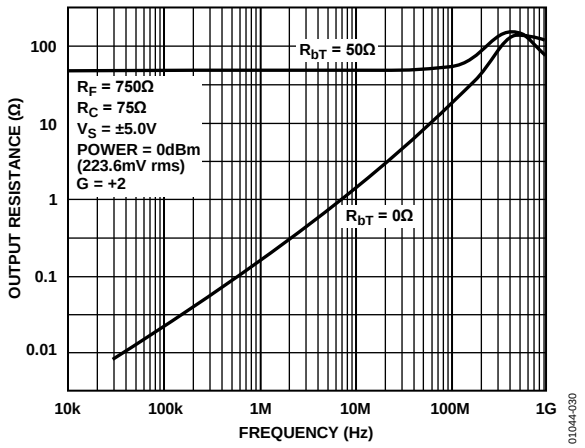


Figure 31. Output Resistance vs. Frequency

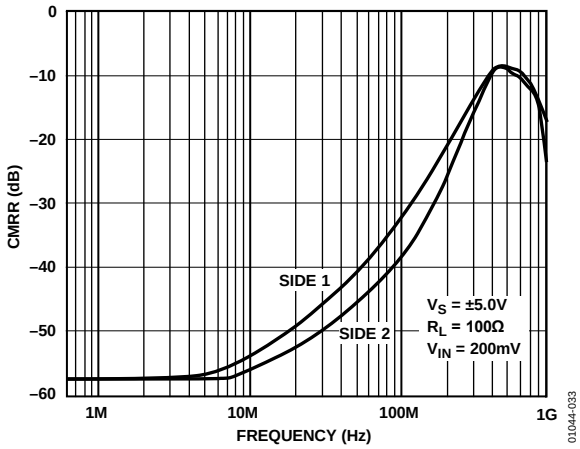


Figure 34. CMRR vs. Frequency (See Figure 45)

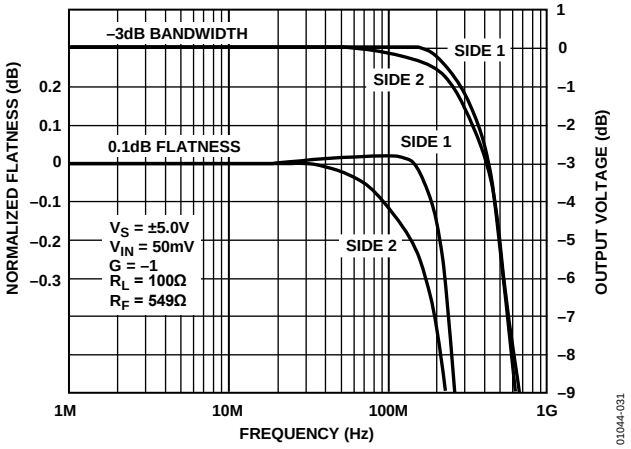


Figure 32. –3 dB Bandwidth vs. Frequency, G = –1

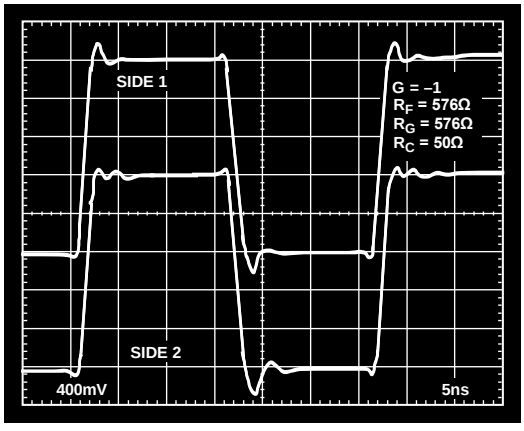


Figure 35. 2 V Step Response, G = –1

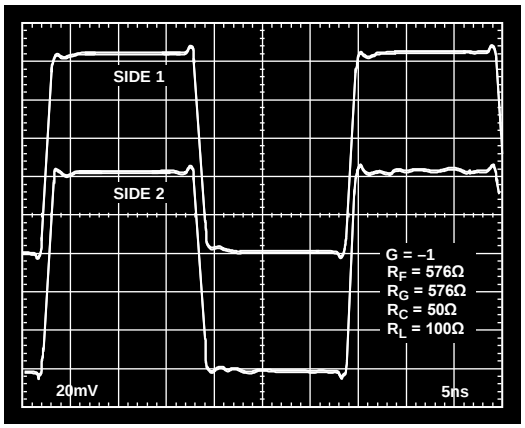


Figure 36. 100 mV Step Response, G = –1

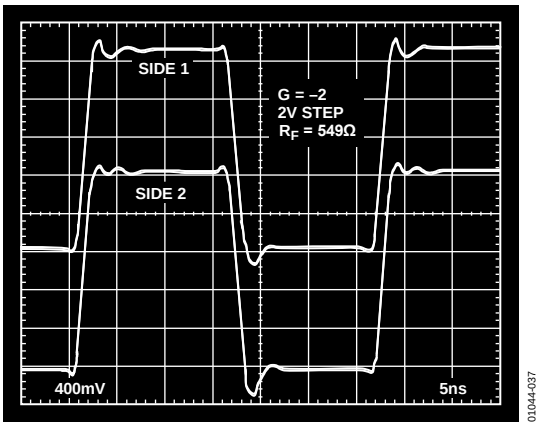


Figure 38. 2 V Step Response, G = –2

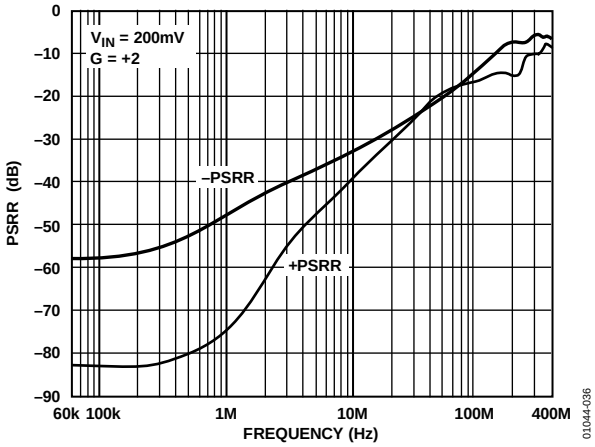


Figure 37. PSRR vs. Frequency

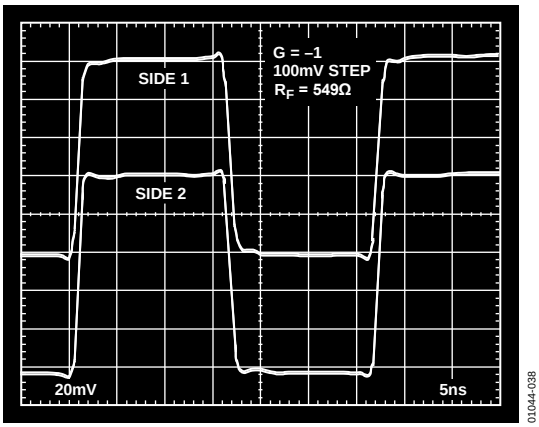


Figure 39. 100 mV Step Response, G = –1

TEST CIRCUITS

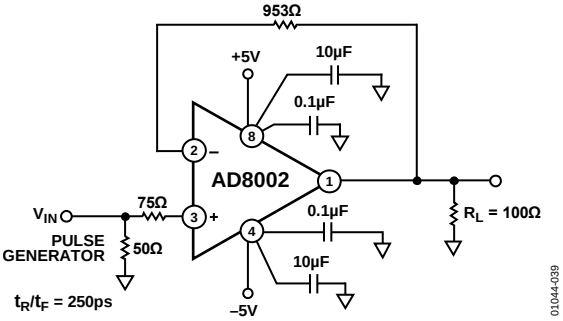


Figure 40. Test Circuit, Gain = +1

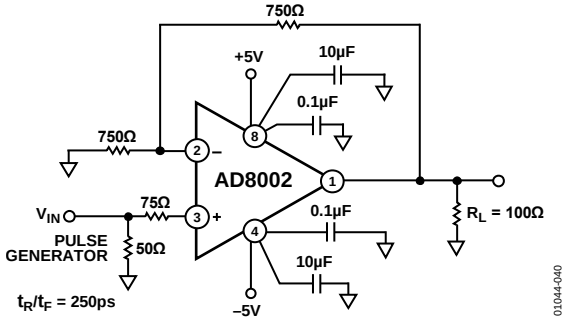


Figure 44. Test Circuit, Gain = +2

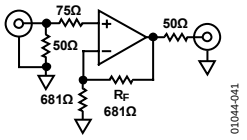


Figure 41. Frequency Response and Flatness Test Circuit (See Figure 10)

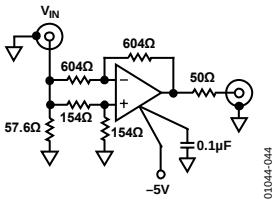


Figure 45. CMRR Test Circuit (See Figure 34)

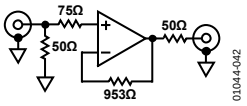


Figure 42. Frequency Response Test Circuit (See Figure 16)

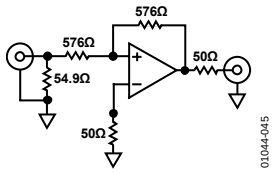


Figure 46. 100 mV Step Response, G = –1

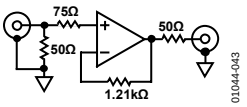


Figure 43. Large Signal Frequency Response Test Circuit (See Figure 20)

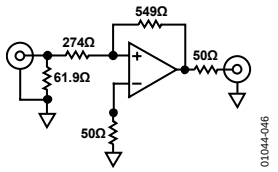


Figure 47. 100 mV Step Response, G = –2

THEORY OF OPERATION

An analysis of the AD8002 can put the operation in familiar terms. The open-loop behavior of the AD8002 is expressed as transimpedance, $\Delta V_{OUT}/\Delta I_{-INx}$, or T_Z. The open-loop transimpedance behaves just as the open-loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Because the value of R_{IN} is proportional to $1/g_m$, the equivalent voltage gain is just $T_Z \times g_m$, where the g_m in question is the transconductance of the input stage. This results in a low open-loop input impedance at the inverting input. Using this amplifier as a follower with gain (see Figure 48) basic analysis yields the following result:

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{T_Z(s)}{T_Z(s) + G \times R_{IN} + R1}$$

where:
$T_Z(s)$ implies the transimpedance as a function of the frequency.
$G = 1 + R1/R2$.
$R_{IN} = 1/g_m \approx 50\ \Omega$.

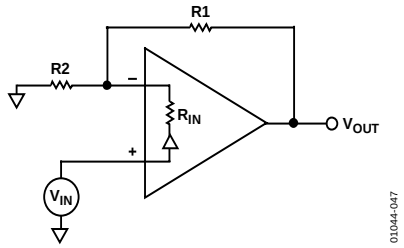


Figure 48. Small Signal Schematic

Recognizing that $G \times R_{IN} << R1$ for low gains, the amplifier can be seen to the first-order that the bandwidth for it is independent of gain (G).

Considering that additional poles contribute excess phase at high frequencies, there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice, parasitic capacitance at the inverting input terminal also adds phase in the feedback loop; thus selecting an optimum value for R_F can be difficult.

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues discussed in the following sections.

CHOICE OF FEEDBACK AND GAIN RESISTORS

The fine scale gain flatness varies to some extent with feedback resistance. Therefore, it is recommended that as soon as optimum resistor values are determined, use 1% tolerance values if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance of the characterization. It is not recommended to use leaded components with the AD8002.

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

As expected for a wideband amplifier, PCB parasitics can affect the overall closed-loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, leave a space (5 mm minimum) around the signal lines to minimize coupling. Additionally, make signal lines connecting the feedback and gain resistors short enough so that their associated inductance does not cause high frequency gain errors. Line lengths of less than 5 mm are recommended. If long runs of coaxial cable are being driven, dispersion and loss must be considered.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the response of the amplifier. In addition, if large current transients must be delivered to the load, bypass capacitors (typically greater than 1 µF) are required to provide the best settling time and lowest distortion. A parallel combination of 4.7 µF and 0.1 µF is recommended. Some brands of electrolytic capacitors require a small series damping resistor ≈4.7 Ω for optimum results.

DC ERRORS AND NOISE

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors, refer to Equation 1. For noise error, the terms are root-sum-squared to give a net output error. In Figure 49, the terms are input offset (V_{IO}), which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_I$), noninverting input current ($I_{BN} \times R_N$), also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_I and subsequently multiplied by the noise gain, always appears at the output as $I_{BN} \times R_F$.

The input voltage noise of the AD8002 is a low 2 nV/√Hz. At low gains, though, the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to a better offset and drift specifications for the AD8002.Use the typical performance curves in conjunction with Equation 1 to predict the performance of the AD8002 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \times I_{BI} \times R_F \quad (1)$$

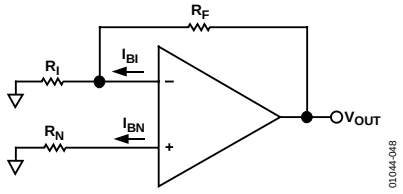


Figure 49. Output Offset Voltage

DRIVING CAPACITIVE LOADS

The AD8002 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance as shown in Figure 50.

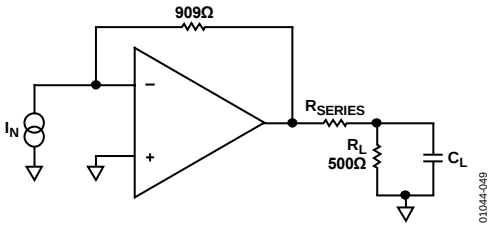


Figure 50. Driving Capacitive Loads

Figure 51 shows the optimum value for R_{SERIES} vs. capacitive load (C_L). It is worth noting that the frequency response of the circuit when driving large capacitive loads is dominated by the passive roll-off of R_{SERIES} and C_L.

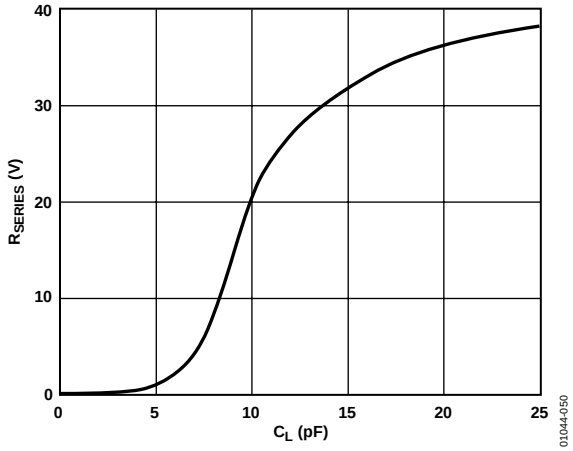


Figure 51. Recommended R_{SERIES} vs. Capacitive Load

COMMUNICATIONS

Distortion is a key specification in communications applications. Intermodulation distortion (IMD) is a measure of the ability of an amplifier to pass complex signals without the generation of spurious harmonics. Third-order products are usually the most problematic because several of them fall near the fundamentals and do not lend themselves to filtering. Theory predicts that the third-order harmonic distortion components increase in power at three times the rate of the fundamental tones. The specification of the third-order intercept as the virtual point where fundamental and harmonic power are equal is one standard measure of distortion performance. Op amps used in closed-loop applications do not always obey this simple theory. Figure 52 shows the AD8002 performance summarized at a gain of +2. Here, the worst third-order products are plotted vs. input power. The third-order intercept of the AD8002 is 33 dBm at 10 MHz.

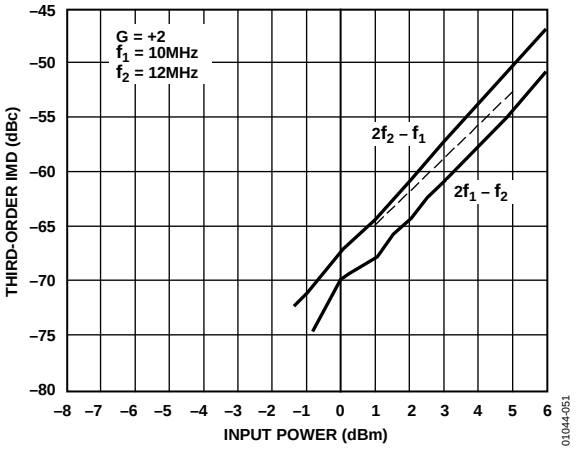


Figure 52. Third-Order IMD vs. Input Power; f_1 = 10 MHz, f_2 = 12 MHz

OPERATION AS A VIDEO LINE DRIVER

The AD8002 has been designed to offer good performance as a video line driver. The important specifications of differential gain (0.01%) and differential phase (0.02°) meet the most exacting HDTV demands for driving one video load with each amplifier. The AD8002 also drives four back terminated loads (two each), as shown in Figure 53, with equally impressive performance (0.01%, 0.07°). Another important consideration is isolation between loads in a multiple load application. The AD8002 has more than 40 dB of isolation at 5 MHz when driving two 75 Ω back terminated loads.

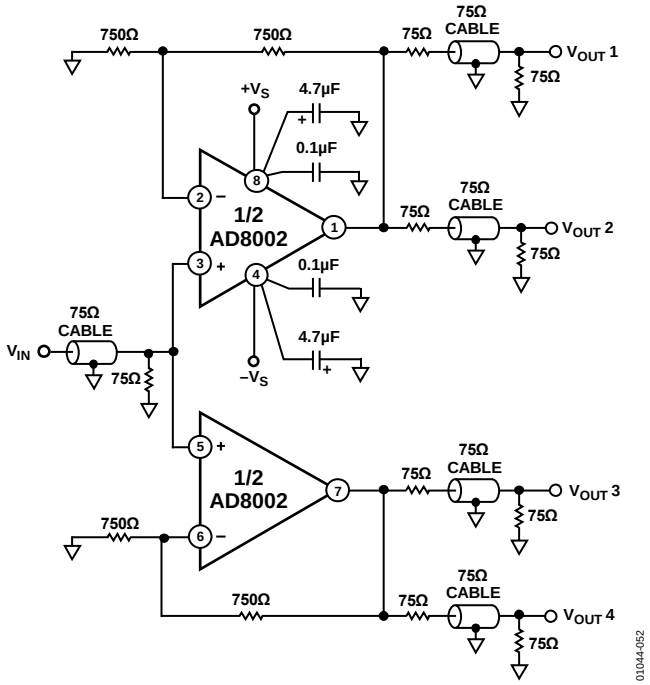


Figure 53. Video Line Driver

DRIVING ADCs

The AD8002 is well suited for driving high speed analog-to-digital converters, such as the AD9058. The AD9058 is a dual, 8-bit, 50 MSPS ADC. In Figure 55, the AD8002 drives the inputs of the AD9058, which are configured for 0 V to 2 V ranges. Bipolar input signals are buffered, amplified (−2×), and offset (by 1.0 V) into the proper input range of the ADC. Using the internal 2 V reference of the AD9058 connected to both ADCs (as shown in Figure 55) reduces the number of external components required to create a complete data acquisition system. The 20 Ω resistors in series with the ADC inputs help the ADCs drive the 10 pF ADC input capacitance. The AD8002 adds only 100 mW to the power consumption, while not limiting the performance of the circuit.

SINGLE-ENDED-TO-DIFFERENTIAL DRIVER USING AN AD8002

The two halves of an AD8002 can be configured to create a single-ended-to-differential high speed driver with a −3 dB bandwidth in excess of 200 MHz, as shown in Figure 54. Although the individual op amps are each current feedback op amps, the overall architecture yields a circuit with attributes normally associated with voltage feedback amplifiers, yet offers the speed advantages inherent in current feedback amplifiers. In addition, the gain of the circuit can be changed by varying a single resistor, R_F, which is often not possible in a dual op amp differential driver.

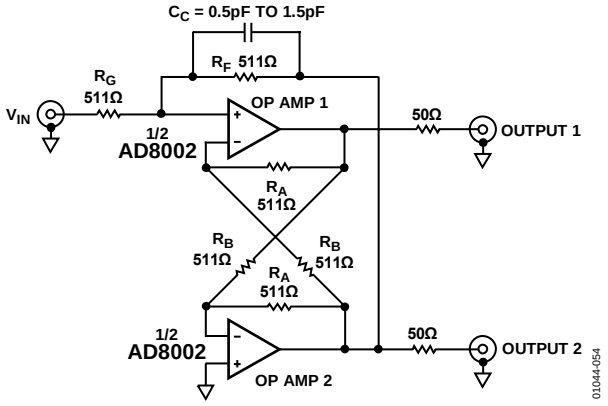


Figure 54. Differential Line Driver

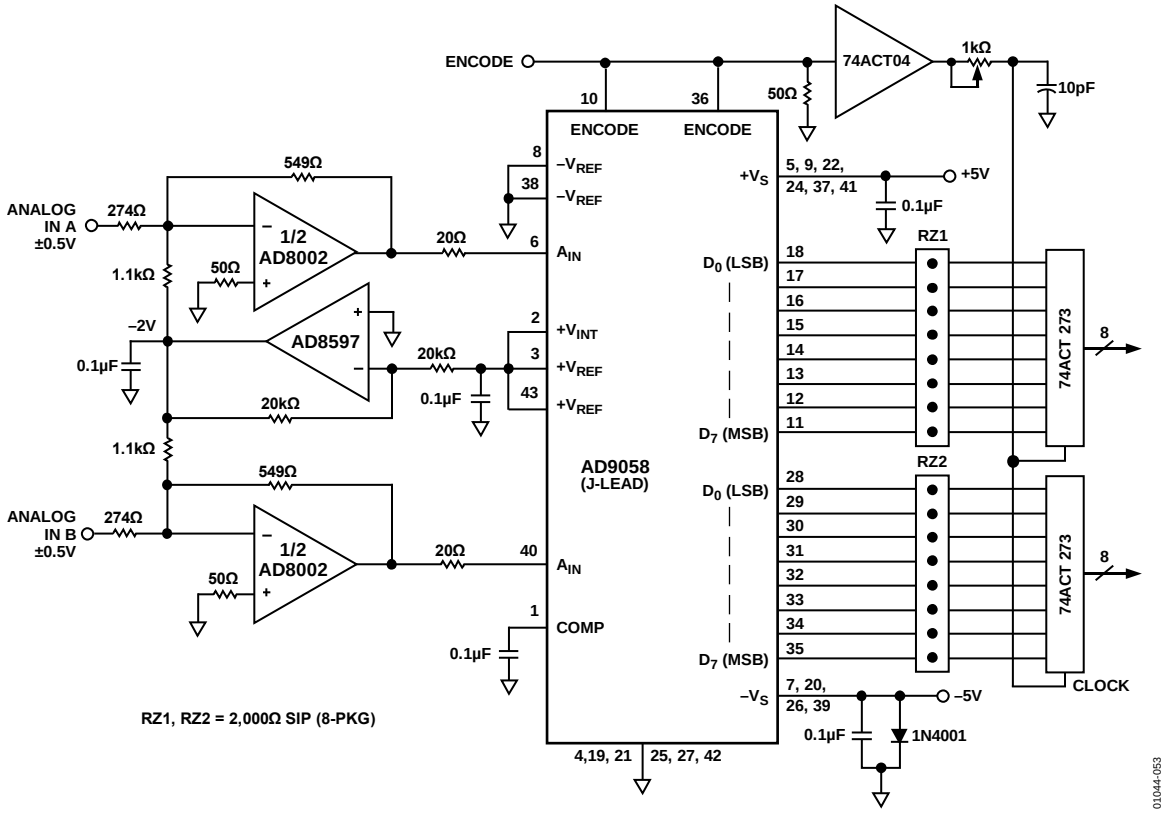


Figure 55. AD8002 Driving a Dual ADC

The current feedback nature of the op amps, in addition to enabling the wide bandwidth, provides an output drive of more than 3 V p-p into a 20 Ω load for each output at 20 MHz. Conversely, the voltage feedback nature provides symmetrical high impedance inputs and allows the use of reactive components in the feedback network.

The circuit consists of the two op amps, each configured as a unity-gain follower by the 511 Ω R_A feedback resistors between the output and inverting input of each op amp. The output of each op amp has a 511 Ω R_B resistor to the inverting input of the other op amp. Thus, each output drives the other op amp through a unity-gain inverter configuration. By connecting the two amplifiers as cross-coupled inverters, the outputs of the amplifiers are freed to be equal and opposite, assuring zero output common-mode voltage.

Using this circuit configuration, the common-mode signal of the outputs is reduced. If one output increases slightly, the negative input to the other op amp drives its output slightly lower and thus preserves the symmetry of the complementary outputs, which reduces the common-mode signal. The common-mode output signal was measured as −50 dB at 1 MHz.

Looking at this configuration overall, there are two high impedance inputs (the +IN1, +IN2 of each op amp), two low impedance outputs, and a high open-loop gain. The two noninverting inputs and the output of the Op Amp 2 structure looks like a voltage feedback op amp having two symmetrical, high impedance inputs and one output. The +IN1, +IN2 to Op Amp 2 is the noninverting input (it has the same polarity as OUT2) and the +IN1, +IN2 to Op Amp 1 is the inverting input (opposite polarity of Output 2).

With a feedback resistor, R_F, an input resistor, R_G, and the grounding of the +IN1, +IN2 of Op Amp 2, a feedback amplifier is formed. This configuration is similar to a voltage feedback amplifier in an inverting configuration if only OUT2 is considered. The addition of OUT1 makes the amplifier a differential output.

The differential gain of this circuit is

$$G = \frac{R_F}{R_G} \times \left(1 + \frac{R_A}{R_B}\right)$$

where:
R_F/R_G is the gain of the overall op amp configuration and is the same as for an inverting op amp except for the polarity. If OUT1 is used as the output reference, the gain is positive.
$1 + R_A/R_B$ is the noise gain of each individual op amp in its noninverting configuration.

The resulting architecture offers several advantages. First, the gain can be changed by changing a single resistor. Changing either R_F or R_G changes the gain as in an inverting op amp circuit. For most types of differential circuits, more than one resistor must be changed to change gain and still maintain good common-mode rejection (CMR).

Reactive elements can be used in the feedback network. This is in contrast to current feedback amplifiers that restrict the use of reactive elements in the feedback op amp. The circuit described requires about 0.9 pF of capacitance in shunt across R_F to optimize peaking and realize a −3 dB bandwidth of more than 200 MHz.

The peaking exhibited by the circuit is very sensitive to the value of this capacitor. Parasitics in the board layout on the order of tenths of picofarads influences the frequency response and the value required for the feedback capacitor, thus a good layout is essential.

The shunt capacitor type selection is also critical. A good microwave type chip capacitor with high Q was found to yield best performance. The device selected for this circuit was a Murata Erie MA280R9B.

The distortion was measured at 20 MHz with a 3 V p-p input and a 100 Ω load on each output. For OUT1, the distortion is −37 dBc and −41 dBc for the second and third harmonics, respectively. For OUT2, the second harmonic is −35 dBc and the third harmonic is −43 dBc.

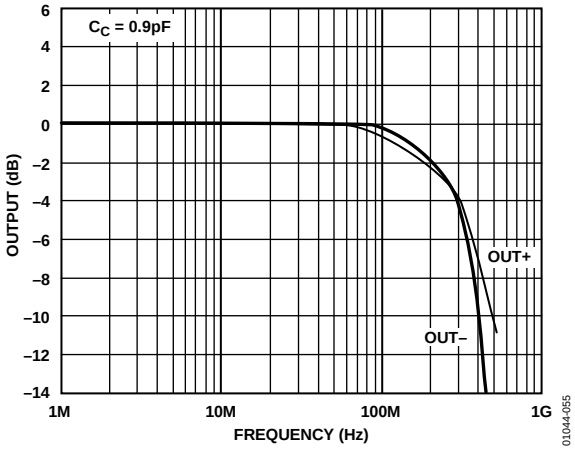


Figure 56. Differential Driver Frequency Response

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8002 requires careful attention to board layout and component selection. Proper R_F design techniques and low parasitic component selection are mandatory.

Use a ground plane to cover all unused portions of the component side of the board to provide a low impedance ground path. Remove the ground plane from the area near the input pins to reduce stray capacitance.

Use chip capacitors for supply bypassing (see Figure 58). Connect one end to the ground plane and the other within ⅛ inch of each power pin. Connect an additional large tantalum electrolytic capacitor (4.7 µF to 10 µF) in parallel, but not necessarily so close, to supply current for fast, large signal changes at the output.

Locate the feedback resistor close to the inverting input pin to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input significantly affects high speed performance.

Use stripline design techniques for long signal traces (greater than about 1 inch). Design these with a characteristic impedance of 50 Ω or 75 Ω and ensure they are properly terminated at each end.

Table 4 and Table 5 show the recommended component values.

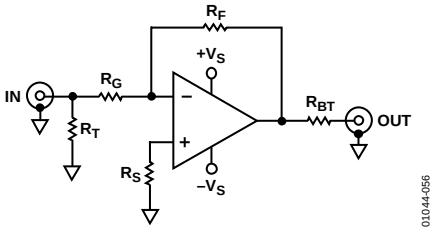


Figure 57. Inverting Configuration

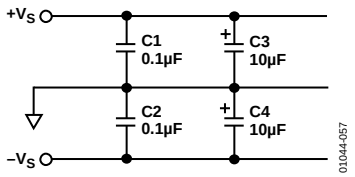


Figure 58. Supply Bypassing

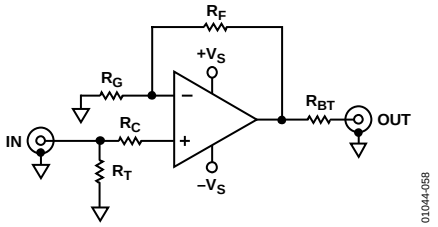


Figure 59. Noninverting Configuration

Table 4. AD8002AR (SOIC) Recommended Component Values[1]

	Gain							
Component	**−10**	**−2**	**−1**	**+1**	**+2**	**+10**	**+100**	**Unit**
R_F	499	499	549	953	681	499	1000	Ω
R_G	49.9	249	549	N/A	681	54.9	10	Ω
R_{BT} (Nominal)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	Ω
R_C[2]	N/A	N/A	N/A	75	75	0	0	Ω
R_S	49.9	49.9	49.9	N/A	N/A	N/A	N/A	Ω
R_T (Nominal)	N/A	61.9	54.9	49.9	49.9	49.9	49.9	Ω
Small Signal Bandwidth	250	410	410	600	500	170	17	MHz
0.1 dB Flatness	50	100	100	35	90	24	3	MHz

[1] N/A means not applicable
[2] R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

Table 5. AD8002ARM (MSOP) Recommended Component Values[1]

	Gain							
Component	**−10**	**−2**	**−1**	**+1**	**+2**	**+10**	**+100**	**Unit**
R_F	499	499	590	1000	681	499	1000	Ω
R_G	49.9	249	590	N/A	681	54.9	10	Ω
R_{BT} (Nominal)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	Ω
R_C[2]	N/A	N/A	N/A	75	75	0	0	Ω
R_S	49.9	49.9	49.9	N/A	N/A	N/A	N/A	Ω
R_T (Nominal)	N/A	61.9	49.9	49.9	49.9	49.9	49.9	Ω
Small Signal Bandwidth	270	400	410	600	450	170	19	MHz
0.1 dB Flatness	60	100	100	35	70	35	3	MHz

[1] N/A means not applicable
[2] R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

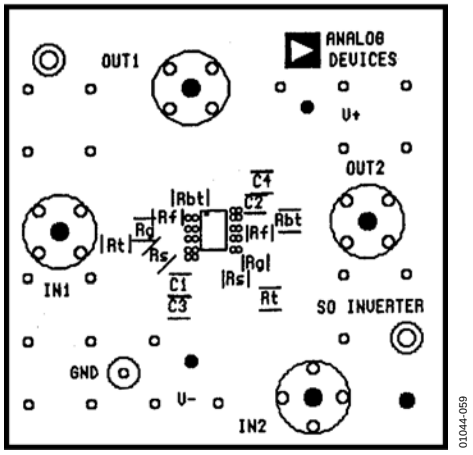


Figure 60. Inverter SOIC Board Layout (Silkscreen)

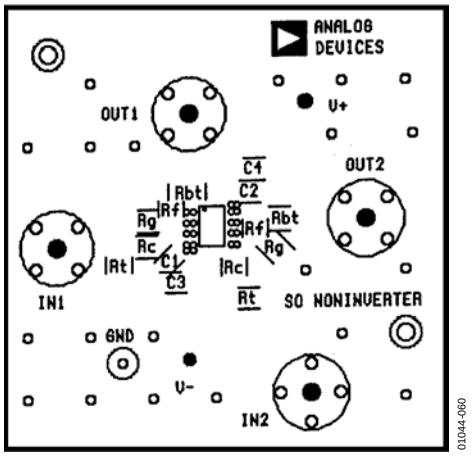


Figure 61. Noninverter SOIC Board Layout (Silkscreen)

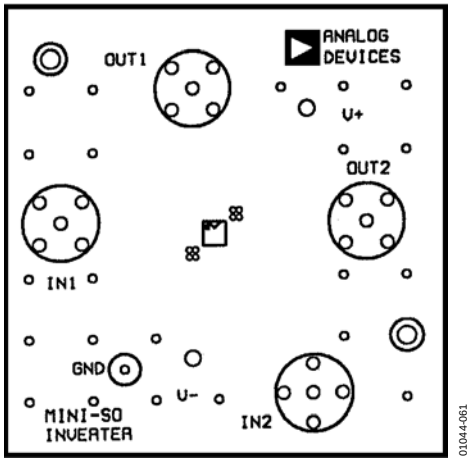


Figure 62. Inverter MSOP Board Layout (Silkscreen)

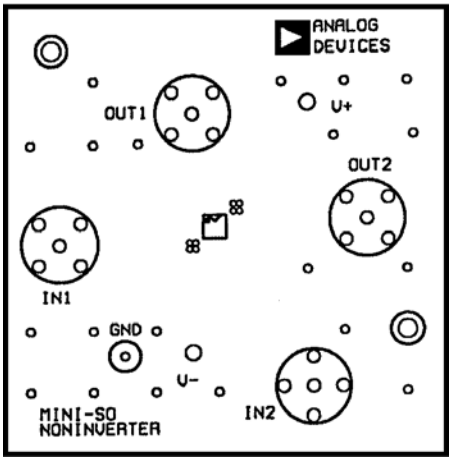


Figure 63. Noninverter MSOP Board Layout (Silkscreen)

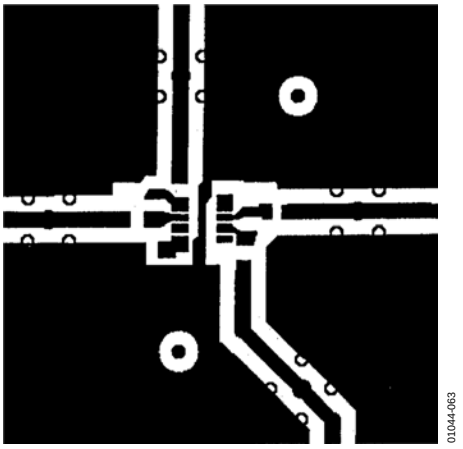


Figure 64. Inverter SOIC Board Layout (Component Layer)

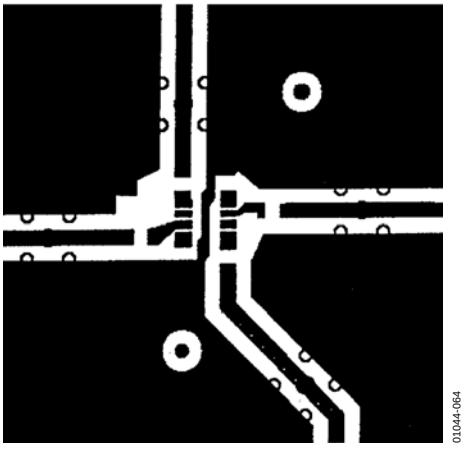


Figure 65. Noninverter SOIC Board Layout (Component Layer)

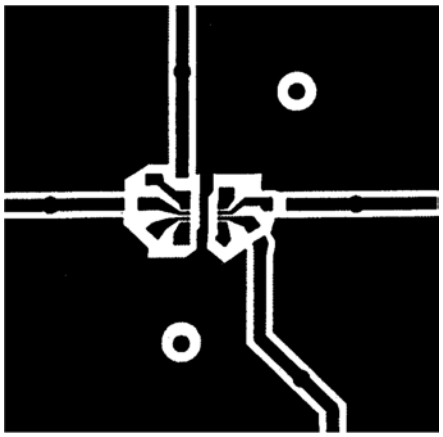


Figure 66. Inverter MSOP Board Layout (Component Layer)

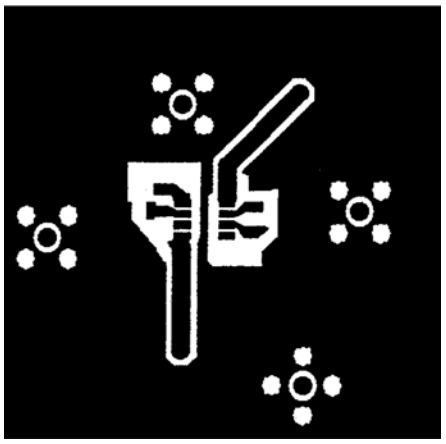


Figure 69. Noninverter SOIC Board Layout (Solder Side) (Looking Through the Board)

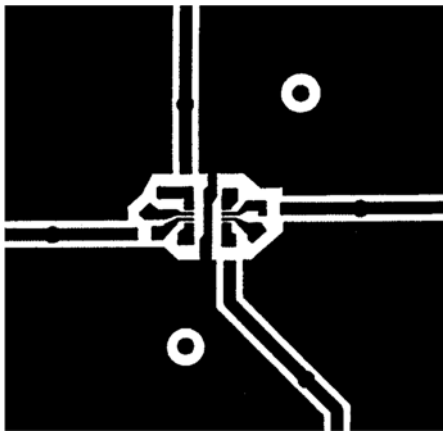


Figure 67. Noninverter MSOP Board Layout (Component Layer)

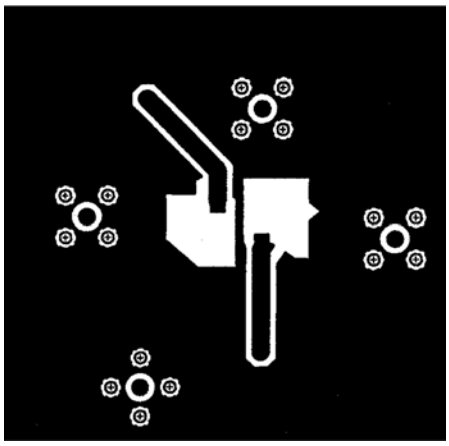


Figure 70. Inverter MSOP Board Layout (Solder Side) (Looking Through the Board)

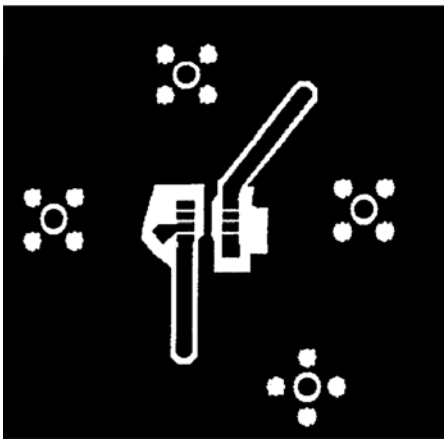


Figure 68. Inverter SOIC Board Layout (Solder Side) (Looking Through the Board)

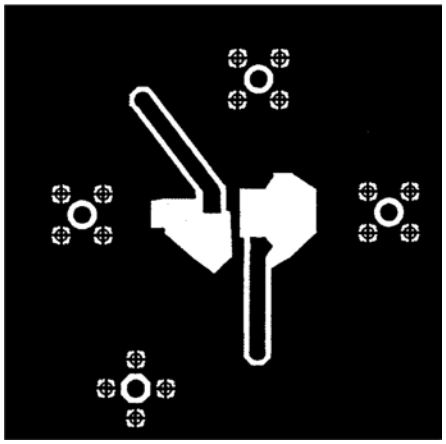


Figure 71. Noninverter MSOP Board Layout (Solder Side) (Looking Through the Board)