

FEATURES

High speed

190 MHz, -3 dB bandwidth ($G = +1$)

100 V/ μ s slew rate

Low distortion

120 dBc at 1 MHz SFDR

80 dBc at 5 MHz SFDR

Selectable input crossover threshold

Low noise

4.3 nV/ $\sqrt{\text{Hz}}$

1.6 pA/ $\sqrt{\text{Hz}}$

Low offset voltage: 900 μ V maximum

Low power: 6.5 mA per amplifier supply current

Power-down mode

No phase reversal: $V_{IN} > |V_S| + 200$ mV

Wide supply range: 2.7 V to 12 V

Small packaging: 8-lead SOIC, 6-lead SOT-23, 10-lead MSOP

Qualified for automotive applications ([AD8028WARMZ-R7](#) only)

APPLICATIONS

Filters

ADC drivers

Level shifting

Buffering

Professional video

Low voltage instrumentation

GENERAL DESCRIPTION

The [AD8027/AD8028](#)¹ are high speed amplifiers with rail-to-rail input and output that operate on low supply voltages and are optimized for high performance and a wide dynamic signal range. The [AD8027/AD8028](#) have low noise (4.3 nV/ $\sqrt{\text{Hz}}$, 1.6 pA/ $\sqrt{\text{Hz}}$) and low distortion (120 dBc at 1 MHz). In applications that use a fraction of or use the entire input dynamic range and require low distortion, the [AD8027/AD8028](#) are ideal choices.

Many rail-to-rail input amplifiers have an input stage that switches from one differential pair to another as the input signal crosses a threshold voltage, which causes distortion. The [AD8027/AD8028](#) have a unique feature that allows the user to select the input crossover threshold voltage through the DISABLE/SELECT pin (DISABLE/SELECT x in the 10-lead MSOP, hereafter referred to as DISABLE/SELECT throughout this data sheet). This feature controls the voltage at which the complementary transistor input pairs switch. The [AD8027/AD8028](#) also have intrinsically low crossover distortion.

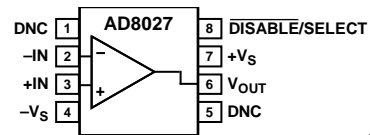
¹ Protected by U.S. patent numbers 6,486,737B1; 6,518,842B1.

Rev. D

Document Feedback

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PIN CONNECTION DIAGRAM



DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

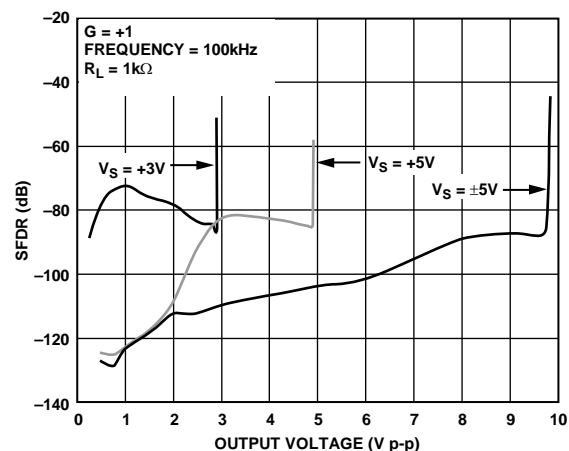
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Figure 1. 8-Lead SOIC, [AD8027](#)

See the Pin Configurations and Function Descriptions section for additional pin configurations and information about the pin functions.

With their wide supply voltage range (2.7 V to 12 V) and wide bandwidth (190 MHz), the [AD8027/AD8028](#) amplifiers are designed to work in a variety of applications where speed and performance are needed on low supply voltages. The high performance of the [AD8027/AD8028](#) is achieved with a quiescent current of only 6.5 mA (typical) per amplifier. The [AD8027/AD8028](#) have a shutdown mode that is controlled via the DISABLE/SELECT pin.

The [AD8027/AD8028](#) are available in 8-lead SOIC, 6-lead SOT-23, and 10-lead MSOP packages. The [AD8028WARMZ-R7](#) is an automotive grade version, qualified for automotive applications. See the Automotive Products section for more details. The [AD8027/AD8028](#) family is designed to work over the extended temperature range of -40°C to +125°C.



03327-063

Figure 2. SFDR vs. Output Voltage

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REVISION HISTORY

7/15—Rev. C to Rev. D

Changed SELECT to <u>DISABLE/SELECT</u> , NC to DNC, V_{S+} to $+V_S$, and V_{S-} to $-V_S$	Throughout
Changes to Features Section, Figure 1, and General Description Section	1
Changes to Table 1	3
Changes to Table 2	4
Changes to Table 3	5
Added Pin Configurations and Function Descriptions Section	8
Added Figure 4, Figure 5, Table 5, and Table 6; Renumbered Sequentially	8
Added Figure 6, Figure 7, Table 7, and Table 8	9
Changes to Figure 10 Caption and Figure 13 Caption	10
Changes to Figure 16 Caption and Figure 19 Caption	11
Changes to Figure 20 Caption and Figure 21	12
Changes to Figure 26 Caption	13
Changes to Figure 36 and Figure 37	14
Changes to Figure 42	15
Changes to Figure 50 Caption	17
Added Test Circuit Section and Figure 59	19
Changes to Theory of Operation Section	20
Changes to Crossover Selection Section and Figure 61	21
Changes to Wideband Operation Section, Figure 62, Figure 63, and Figure 64	22
Changes to PCB Layout Section	23

Changes to Using the <u>DISABLE/SELECT</u> Pin Section and Table 6	24
Changes to Figure 67 and Design Tools and Technical Support Section	25
Updated Outline Dimensions	26
Changes to Ordering Guide	27
Added Automotive Products Section	27

3/05—Rev. B to Rev. C

Updated Format	Universal
Change to Figure 1	1

10/03—Rev. A to Rev. B

Changes to Figure 1	1
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8/03—Rev. 0 to Rev. A

Addition of AD8028	Universal
Changes to General Description	1
Changes to Figure 1, Figure 3, Figure 4, Figure 8, Figure 13, Figure 15, Figure 17	1, 6, 7, 8, 9
Changes to Figure 58, Figure 60	18, 20
Changes to Specifications	3
Updated Outline Dimensions	22
Updated Ordering Guide	23

3/03—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 5\text{ V}$ at $T_A = 25^\circ\text{C}$, $R_L = 1\text{ k}\Omega$ to midsupply, $G = +1$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$G = +1, V_{OUT} = 0.2\text{ V p-p}$	138	190		MHz
	AD8028W only: T_{MIN} to T_{MAX}	138			MHz
Bandwidth for 0.1 dB Flatness	$G = +1, V_{OUT} = 2\text{ V p-p}$	20	32		MHz
	AD8028W only: T_{MIN} to T_{MAX}	20			MHz
Slew Rate	$G = +2, V_{OUT} = 0.2\text{ V p-p}$		16		MHz
Settling Time to 0.1%	$G = +1, V_{OUT} = 2\text{ V step}$		90		V/ μs
	$G = -1, V_{OUT} = 2\text{ V step}$		100		V/ μs
	$G = +2, V_{OUT} = 2\text{ V step}$		35		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	$f_C = 1\text{ MHz}, V_{OUT} = 2\text{ V p-p}, R_F = 24.9\ \Omega$		120		dBc
	$f_C = 5\text{ MHz}, V_{OUT} = 2\text{ V p-p}, R_F = 24.9\ \Omega$		80		dBc
Input Voltage Noise	$f = 100\text{ kHz}$		4.3		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $G = +2, R_L = 150\ \Omega$		0.1		%
Differential Phase Error	NTSC, $G = +2, R_L = 150\ \Omega$		0.2		Degrees
Crosstalk, Output to Output	$G = +1, R_L = 100\ \Omega, V_{OUT} = 2\text{ V p-p}, V_S = \pm 5\text{ V}$ at 1 MHz		–93		dB
DC PERFORMANCE					
Input Offset Voltage	DISABLE/SELECT = tristate or open, PNP active		200	800	μV
	AD8028W only: T_{MIN} to T_{MAX}			850	μV
	DISABLE/SELECT = high, NPN active		240	900	μV
	AD8028W only: T_{MIN} to T_{MAX}			900	μV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.50		$\mu\text{V}/^\circ\text{C}$
Input Bias Current ¹	$V_{CM} = 0\text{ V}$, NPN active		4	6	μA
	T_{MIN} to T_{MAX}		4		μA
	AD8028W only: T_{MIN} to T_{MAX}			6	μA
	$V_{CM} = 0\text{ V}$, PNP active		–8	–11	μA
	T_{MIN} to T_{MAX}		–8		μA
	AD8028W only: T_{MIN} to T_{MAX}			–11	μA
Input Offset Current	AD8028W only: T_{MIN} to T_{MAX}		± 0.1	± 0.9	μA
Open-Loop Gain	$V_{OUT} = \pm 2.5\text{ V}$, AD8028W only: T_{MIN} to T_{MAX}	100	110		dB
INPUT CHARACTERISTICS					
Input Impedance			6		M Ω
Input Capacitance			2		pF
Input Common-Mode Voltage Range			–5.2 to +5.2		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5\text{ V}$	90	110		dB
	AD8028W only: T_{MIN} to T_{MAX}	88			dB
DISABLE/SELECT PIN					
Selection Input Voltage	T_{MIN} to T_{MAX}	–3.0	Crossover Low		V
			Crossover High ²	–3.9 to –3.7	V
Disable Input Voltage	T_{MIN} to T_{MAX}			–4.6	V
Disable Switching Speed	50% of input to <10% of final V_{OUT}		980		ns
Enable Switching Speed			45		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	$V_{IN} = +6V$ to $-6V$, $G = -1$		40/45		ns
Output Voltage Swing	AD8028W only: T_{MIN} to T_{MAX}	-4.9 to +4.9	-4.94 to +4.94		V
Short-Circuit Output	Sinking and sourcing		120		mA
Off Isolation	$V_{IN} = 0.2V$ p-p, $f = 1MHz$, $\overline{DISABLE}/SELECT = low$		-49		dB
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current per Amplifier			6.5	8.5	mA
Quiescent Current (Disabled)	AD8028W only: T_{MIN} to T_{MAX} $\overline{DISABLE}/SELECT = low$		370	500	μA
Power Supply Rejection Ratio	AD8028W only: T_{MIN} to T_{MAX} $V_S \pm 1V$, AD8028W only: T_{MIN} to T_{MAX}	90	110	500	dB

¹ No sign or a plus sign indicates current into the pin; a minus sign indicates current out of the pin.

² It is recommended to float the $\overline{DISABLE}/SELECT$ pin for crossover high mode.

$V_S = 5V$ at $T_A = 25^\circ C$, $R_L = 1k\Omega$ to midsupply, $G = +1$, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1$, $V_{OUT} = 0.2V$ p-p	131	185		MHz
	AD8028W only: T_{MIN} to T_{MAX}	131			MHz
	$G = +1$, $V_{OUT} = 2V$ p-p	18	28		MHz
	AD8028W only: T_{MIN} to T_{MAX}	18			MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_{OUT} = 0.2V$ p-p		12		MHz
Slew Rate	$G = +1$, $V_{OUT} = 2V$ step		85		V/ μs
	$G = -1$, $V_{OUT} = 2V$ step		100		V/ μs
Settling Time to 0.1%	$G = +2$, $V_{OUT} = 2V$ step		40		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	$f_C = 1MHz$, $V_{OUT} = 2V$ p-p, $R_F = 24.9\Omega$		90		dBc
	$f_C = 5MHz$, $V_{OUT} = 2V$ p-p, $R_F = 24.9\Omega$		64		dBc
Input Voltage Noise	$f = 100kHz$		4.3		nV/ \sqrt{Hz}
Input Current Noise	$f = 100kHz$		1.6		pA/ \sqrt{Hz}
Differential Gain Error	NTSC, $G = +2$, $R_L = 150\Omega$		0.1		%
Differential Phase Error	NTSC, $G = +2$, $R_L = 150\Omega$		0.2		Degrees
Crosstalk, Output to Output	$G = +1$, $R_L = 100\Omega$, $V_{OUT} = 2V$ p-p, $V_S = \pm 5V$ at 1 MHz		-92		dB
DC PERFORMANCE					
Input Offset Voltage	$\overline{DISABLE}/SELECT = tristate$ or open, PNP active		200	800	μV
	AD8028W only: T_{MIN} to T_{MAX}			850	μV
	$\overline{DISABLE}/SELECT = high$ NPN active		240	900	μV
	AD8028W only: T_{MIN} to T_{MAX}			900	μV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2		$\mu V/^\circ C$
Input Bias Current ¹	$V_{CM} = 2.5V$, NPN active		4	6	μA
	T_{MIN} to T_{MAX}		4		μA
	AD8028W only: T_{MIN} to T_{MAX}			6	μA
	$V_{CM} = 2.5V$, PNP active		-8	-11	μA
	T_{MIN} to T_{MAX}		-8		μA
	AD8028W only: T_{MIN} to T_{MAX}			-11	μA
Input Offset Current	AD8028W only: T_{MIN} to T_{MAX}		± 0.1	± 0.9	μA
Open-Loop Gain	$V_{OUT} = 1V$ to $4V$, AD8028W only: T_{MIN} to T_{MAX}	96	105		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			-0.2 to +5.2		V
Common-Mode Rejection Ratio	$V_{CM} = 0\text{ V to } 2.5\text{ V}$ AD8028W only: T_{MIN} to T_{MAX}	90 84	105		dB dB
DISABLE/SELECT PIN					
Selection Input Voltage		2.0			V
Crossover Low	T_{MIN} to T_{MAX}				V
Crossover High ²	Tristate < $\pm 20\ \mu\text{A}$, T_{MIN} to T_{MAX}		1.1 to 1.3		V
Disable Input Voltage	T_{MIN} to T_{MAX}			0.4	V
Disable Switching Speed	50% of input to <10% of final V_{OUT}		1100		ns
Enable Switching Speed			50		ns
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	$V_{IN} = -6\text{ V to } +1\text{ V}$, $G = -1$		50/50		ns
Output Voltage Swing	AD8028W only: T_{MIN} to T_{MAX}	0.08 to 4.92	0.04 to 4.96		V
Off Isolation	$V_{IN} = 0.2\text{ V p-p}$, $f = 1\text{ MHz}$, $\overline{\text{DISABLE/SELECT}} = \text{low}$		-49		dB
Short-Circuit Current	Sinking and sourcing		105		mA
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current per Amplifier			6	8.5	mA
	AD8028W only: T_{MIN} to T_{MAX}			9	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE/SELECT}} = \text{low}$		320	450	μA
	AD8028W only: T_{MIN} to T_{MAX}			450	μA
Power Supply Rejection Ratio	$V_S \pm 1\text{ V}$, AD8028W only: T_{MIN} to T_{MAX}	90	105		dB

¹ No sign or a plus sign indicates current into the pin; a minus sign indicates current out of the pin.

² It is recommended to float the $\overline{\text{DISABLE/SELECT}}$ pin for crossover high mode.

$V_S = 3\text{ V}$ at $T_A = 25^\circ\text{C}$, $R_L = 1\text{ k}\Omega$ to midsupply, $G = +1$, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1$, $V_{OUT} = 0.2\text{ V p-p}$	125	180		MHz
	AD8028W only: T_{MIN} to T_{MAX}	125			MHz
	$G = +1$, $V_{OUT} = 2\text{ V p-p}$	19	29		MHz
	AD8028W only: T_{MIN} to T_{MAX}	19			MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_{OUT} = 0.2\text{ V p-p}$		10		MHz
Slew Rate	$G = +1$, $V_{OUT} = 2\text{ V step}$		73		V/ μs
	$G = -1$, $V_{OUT} = 2\text{ V step}$		100		V/ μs
Settling Time to 0.1%	$G = +2$, $V_{OUT} = 2\text{ V step}$		48		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	$f_C = 1\text{ MHz}$, $V_{OUT} = 2\text{ V p-p}$, $R_F = 24.9\ \Omega$		85		dBc
	$f_C = 5\text{ MHz}$, $V_{OUT} = 2\text{ V p-p}$, $R_F = 24.9\ \Omega$		64		dBc
Input Voltage Noise	$f = 100\text{ kHz}$		4.3		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $G = +2$, $R_L = 150\ \Omega$		0.15		%
Differential Phase Error	NTSC, $G = +2$, $R_L = 150\ \Omega$		0.20		Degrees
Crosstalk, Output to Output	$G = +1$, $R_L = 100\ \Omega$, $V_{OUT} = 2\text{ V p-p}$, $V_S = 3\text{ V}$ at 1 MHz		-89		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE					
Input Offset Voltage	$\overline{\text{DISABLE/SELECT}}$ = tristate or open, PNP active		200	800	μV
	AD8028W only: T_{MIN} to T_{MAX}			850	μV
Input Offset Voltage Drift	$\overline{\text{DISABLE/SELECT}}$ = high NPN active		240	900	μV
	AD8028W only: T_{MIN} to T_{MAX}			900	μV
Input Bias Current ¹	T_{MIN} to T_{MAX}		2		$\mu\text{V}/^{\circ}\text{C}$
	$V_{\text{CM}} = 1.5\text{ V}$, NPN active		4	6	μA
Input Offset Current	T_{MIN} to T_{MAX}		4		μA
	AD8028W only: T_{MIN} to T_{MAX}			6	μA
Open-Loop Gain	$V_{\text{CM}} = 1.5\text{ V}$, PNP active		-8	-11	μA
	T_{MIN} to T_{MAX}		-8		μA
Open-Loop Gain	AD8028W only: T_{MIN} to T_{MAX}			-11	μA
	AD8028W only: T_{MIN} to T_{MAX}		± 0.1	± 0.9	μA
Open-Loop Gain	$V_{\text{OUT}} = 1\text{ V}$ to 2 V , AD8028W only: T_{MIN} to T_{MAX}	90	100		dB
INPUT CHARACTERISTICS					
Input Impedance			6		$\text{M}\Omega$
Input Capacitance			2		pF
Input Common-Mode Voltage Range	$R_{\text{L}} = 1\text{ k}\Omega$		-0.2 to +3.2		V
Common-Mode Rejection Ratio	$V_{\text{CM}} = 0\text{ V}$ to 1.5 V	88	100		dB
	AD8028W only: T_{MIN} to T_{MAX}	78			dB
DISABLE/SELECT PIN					
Selection Input Voltage		2.0			V
Crossover Low	T_{MIN} to T_{MAX}		1.1 to 1.3		V
Crossover High ²	Tristate < $\pm 20\text{ }\mu\text{A}$, T_{MIN} to T_{MAX}			0.4	V
Disable Input Voltage	T_{MIN} to T_{MAX}				V
Disable Switching Speed	50% of input to <10% of final V_{OUT}		1150		ns
Enable Switching Speed			50		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	$V_{\text{IN}} = -4\text{ V}$ to $+1\text{ V}$, $G = -1$		55/55		ns
Output Voltage Swing	AD8028W only: T_{MIN} to T_{MAX}	0.07 to 4.93	0.03 to 4.97		V
Short-Circuit Current	Sinking and sourcing		72		mA
Off Isolation	$V_{\text{IN}} = 0.2\text{ V}$ p-p, $f = 1\text{ MHz}$, $\overline{\text{DISABLE/SELECT}}$ = low		-49		dB
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current per Amplifier			6.0	8.0	mA
	AD8028W only: T_{MIN} to T_{MAX}			9	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE/SELECT}}$ = low		300	420	μA
	AD8028W only: T_{MIN} to T_{MAX}			420	μA
Power Supply Rejection Ratio	$V_{\text{S}} \pm 1\text{ V}$, AD8028W only: T_{MIN} to T_{MAX}	88	100		dB

¹ No sign or a plus sign indicates current into the pin; a minus sign indicates current out of the pin.

² It is recommended to float the $\overline{\text{DISABLE/SELECT}}$ pin for crossover high mode.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$\pm V_S \pm 0.5$ V
Differential Input Voltage	± 1.8 V
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8027/AD8028 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C , which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8027/AD8028. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L} \right) - \frac{V_{OUT}^2}{R_L}$$

It is recommended that rms output voltages be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA} . Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA} . Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps, as described in the PCB Layout section.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC ($125^\circ\text{C}/\text{W}$), 6-lead SOT-23 ($170^\circ\text{C}/\text{W}$), and 10-lead MSOP ($130^\circ\text{C}/\text{W}$) packages on a JEDEC standard 4-layer board.

Output Short Circuit

Shorting the output to ground or drawing excessive current from the AD8027/AD8028 can cause catastrophic failure.

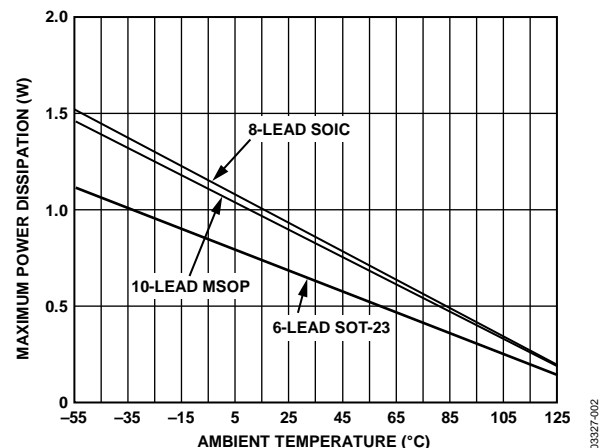


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

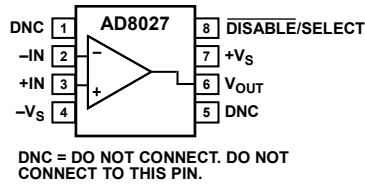


Figure 4. 8-Lead SOIC, AD8027 Pin Configuration

03327-001

Table 5. 8-Lead SOIC, AD8027 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5	DNC	Do Not Connect. Do not connect to these pins.
2	-IN	Negative Input.
3	+IN	Positive Input.
4	-Vs	Negative Supply.
6	V _{OUT}	Output Voltage.
7	+Vs	Positive Supply
8	DISABLE/SELECT	Power-Down/Select. The power-down function places the device into low power consumption mode. The select function of this pin shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail.

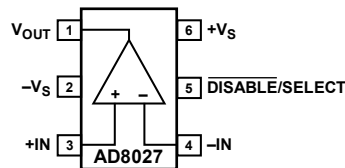


Figure 5. 6-Lead SOT-23, AD8027 Pin Configuration

03327-102

Table 6. 6-Lead SOT-23, AD8027 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{OUT}	Output Voltage.
2	-Vs	Negative Supply.
3	+IN	Positive Input.
4	-IN	Negative Input.
5	DISABLE/SELECT	Power-Down/Select. The power-down function places the device into low power consumption mode. The select function of this pin shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail.
6	+Vs	Positive Supply.

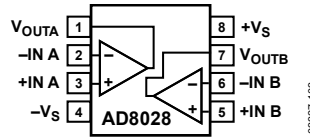


Figure 6. 8-Lead SOIC, AD8028 Pin Configuration

Table 7. 8-Lead SOIC, AD8028 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{OUTA}	Output Voltage, Channel A.
2	-IN A	Negative Input, Channel A.
3	+IN A	Positive Input, Channel A.
4	-V _S	Negative Supply.
5	+IN B	Positive Input, Channel B.
6	-IN B	Negative Input, Channel B.
7	V _{OUTB}	Output Voltage, Channel B.
8	+V _S	Positive Supply.

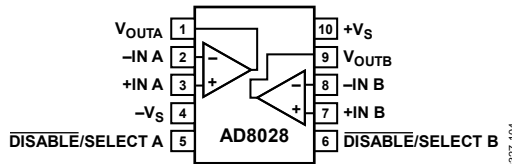


Figure 7. 10-Lead MSOP, AD8028 Pin Configuration

Table 8. 10-Lead MSOP, AD8028 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{OUTA}	Output Voltage, Channel A.
2	-IN A	Negative Input, Channel A.
3	+IN A	Positive Input, Channel A.
4	-V _S	Negative Supply.
5	DISABLE/SELECT A	Power-Down/Select, Channel A. The power-down function places the device into low power consumption mode. The select function of this pin shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail.
6	DISABLE/SELECT B	Power-Down/Select, Channel B. The power-down function places the device into low power consumption mode. The select function of this pin shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail.
7	+IN B	Positive Input, Channel B.
8	-IN B	Negative Input, Channel B.
9	V _{OUTB}	Output Voltage, Channel B.
10	+V _S	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: $V_S = 5\text{ V}$ at $T_A = 25^\circ\text{C}$, $R_L = 1\text{ k}\Omega$, unless otherwise noted.

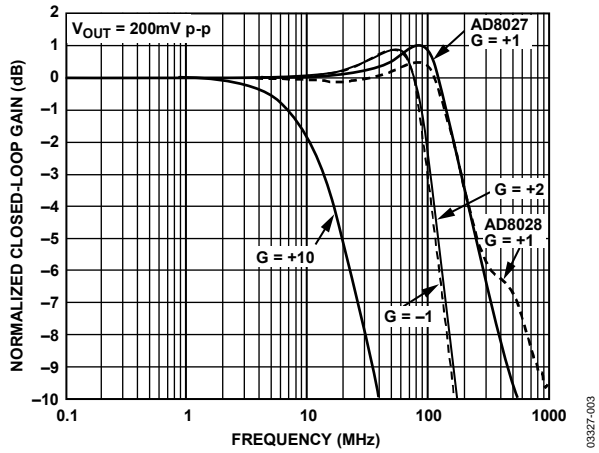


Figure 8. Small Signal Frequency Response for Various Gains

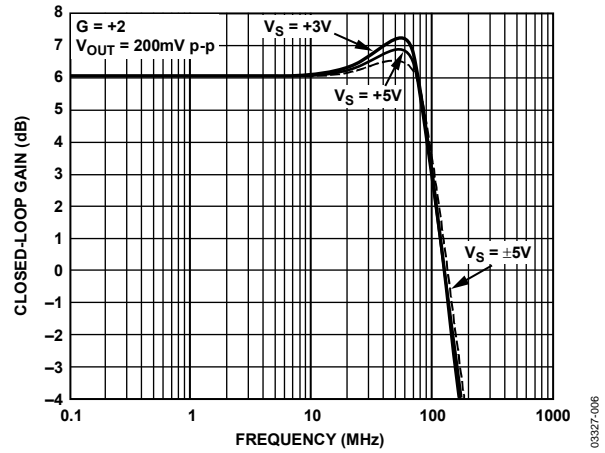


Figure 11. Small Signal Frequency Response for Various Supplies

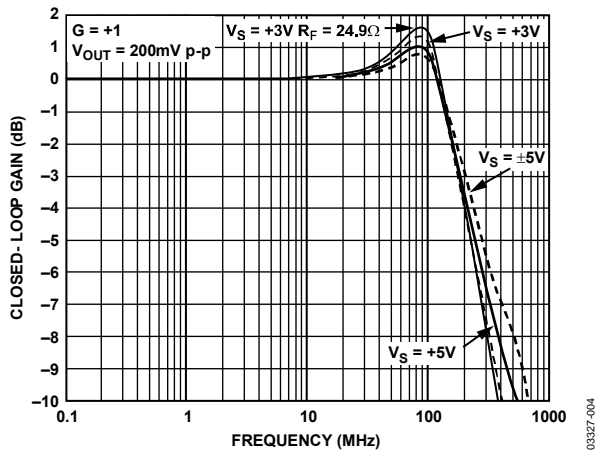


Figure 9. AD8027 Small Signal Frequency Response for Various Supplies

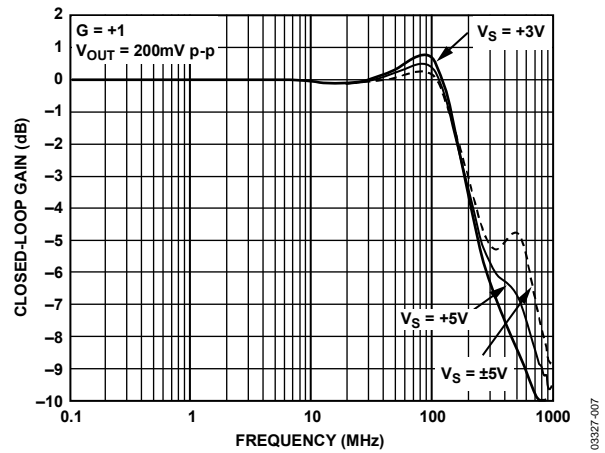


Figure 12. AD8028 Small Signal Frequency Response for Various Supplies

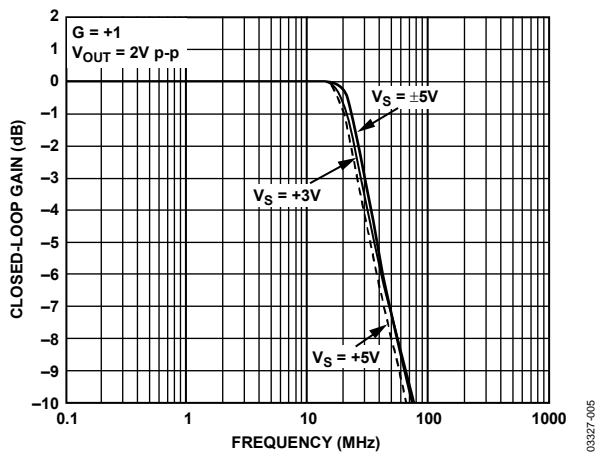


Figure 10. Large Signal Frequency Response for Various Supplies, $G = +1$

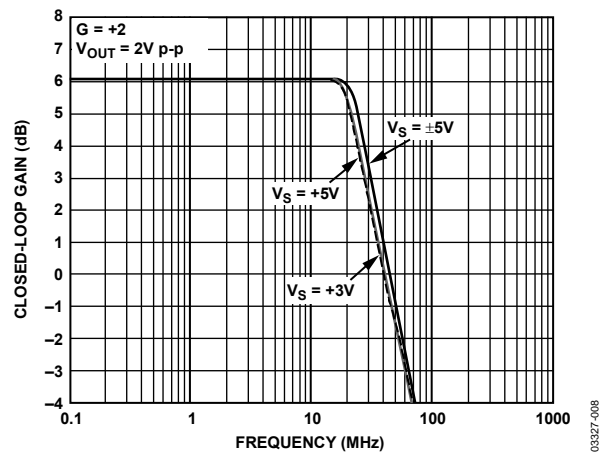


Figure 13. Large Signal Frequency Response for Various Supplies, $G = +2$

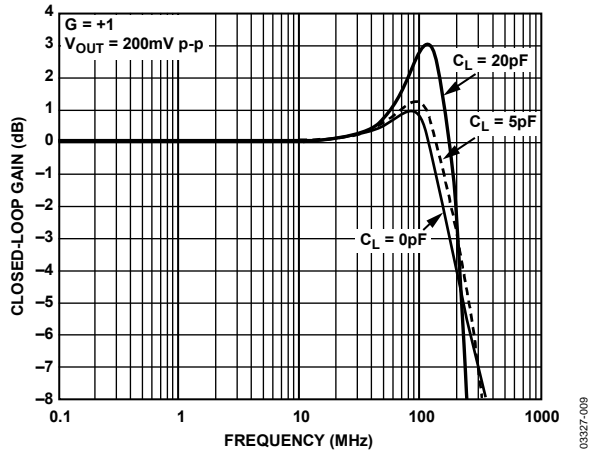


Figure 14. AD8027 Small Signal Frequency Response for Various C_{LOAD} Values

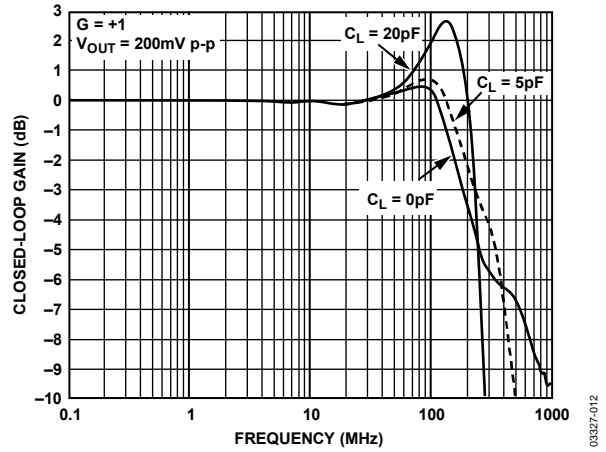


Figure 17. AD8028 Small Signal Frequency Response for Various C_{LOAD} Values

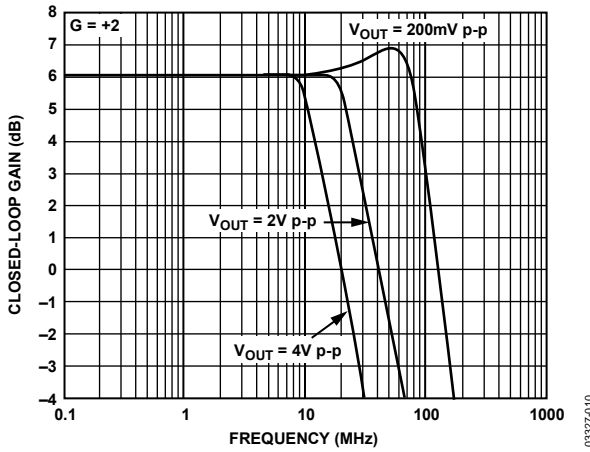


Figure 15. Frequency Response for Various Output Amplitudes

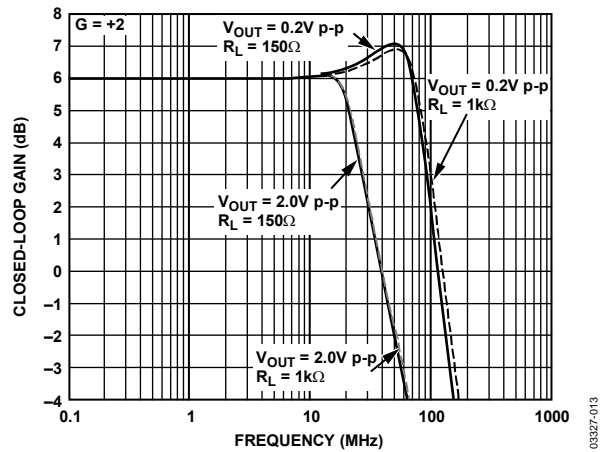


Figure 18. Small Signal Frequency Response for Various R_{LOAD} Values

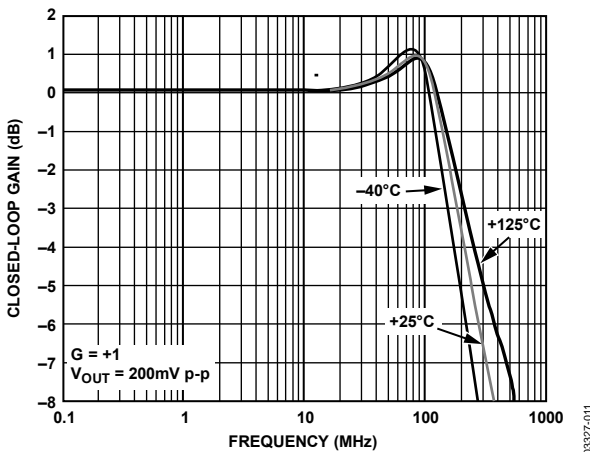


Figure 16. AD8027 Small Signal Frequency Response vs. Frequency for Various Temperatures

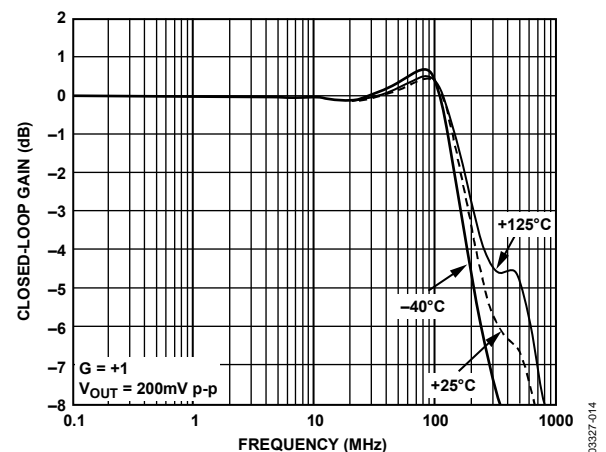


Figure 19. AD8028 Small Signal Frequency Response vs. Frequency for Various Temperatures

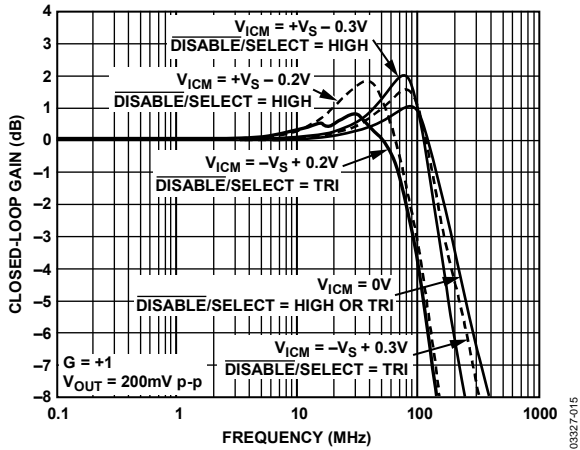


Figure 20. Small Signal Frequency Response vs. Frequency for Various Input Common-Mode Voltages

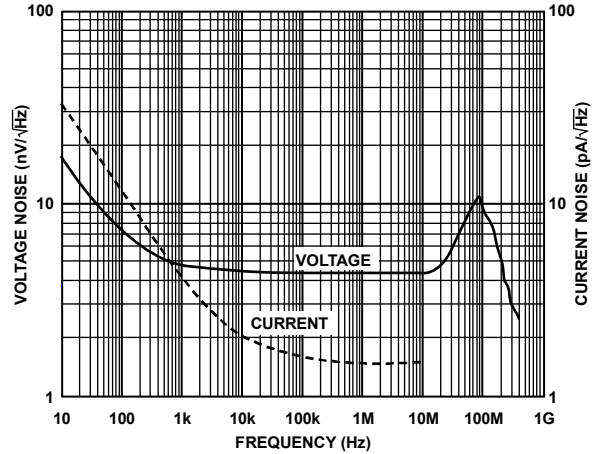


Figure 23. Voltage and Current Noise vs. Frequency

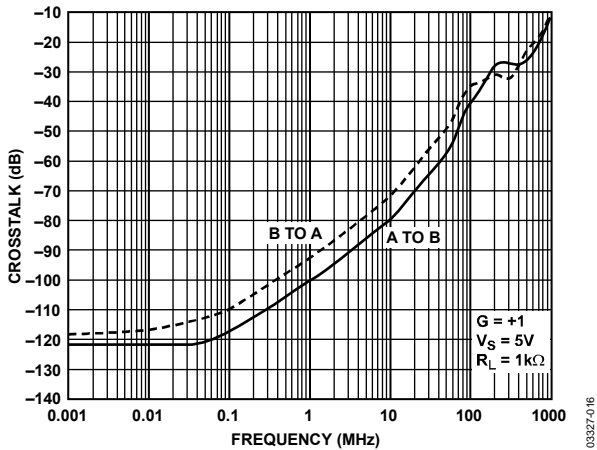


Figure 21. AD8028 Crosstalk, Output to Output (see Figure 59)

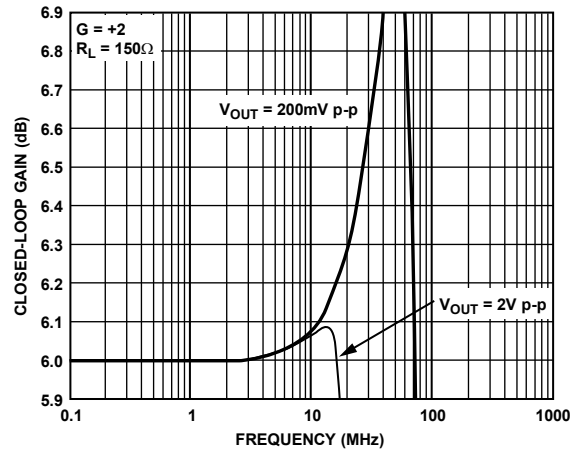


Figure 24. 0.1 dB Flatness Frequency Response

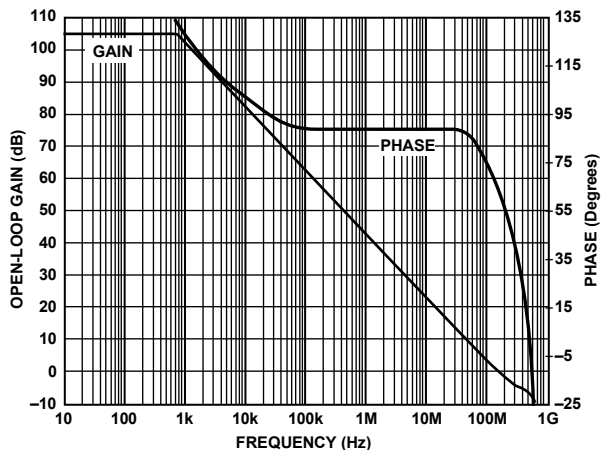


Figure 22. Open-Loop Gain and Phase vs. Frequency

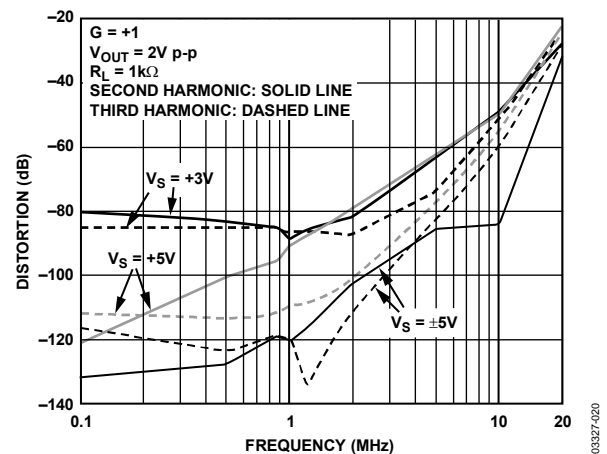


Figure 25. Harmonic Distortion vs. Frequency and Supply Voltage

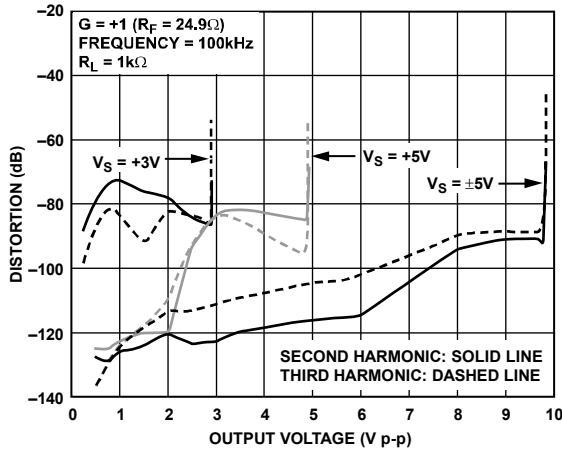


Figure 26. Harmonic Distortion vs. Output Voltage

03327-021

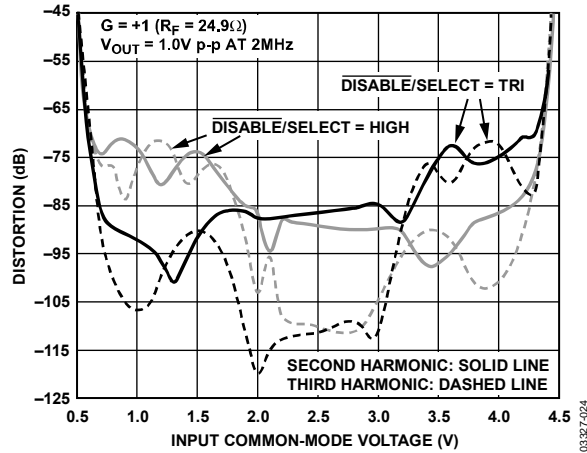


Figure 29. Harmonic Distortion vs. Input Common-Mode Voltage, $V_S = 5V$

03327-024

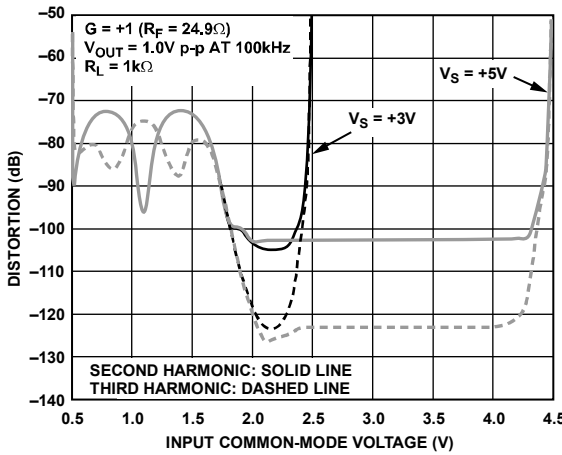


Figure 27. Harmonic Distortion vs. Input Common-Mode Voltage, $\overline{\text{DISABLE/SELECT}} = \text{High}$

03327-022

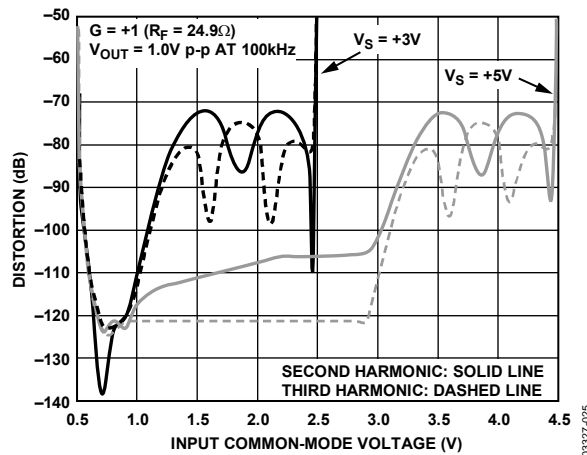


Figure 30. Harmonic Distortion vs. Input Common-Mode Voltage, $\overline{\text{DISABLE/SELECT}} = \text{Trisate or Open}$

03327-025

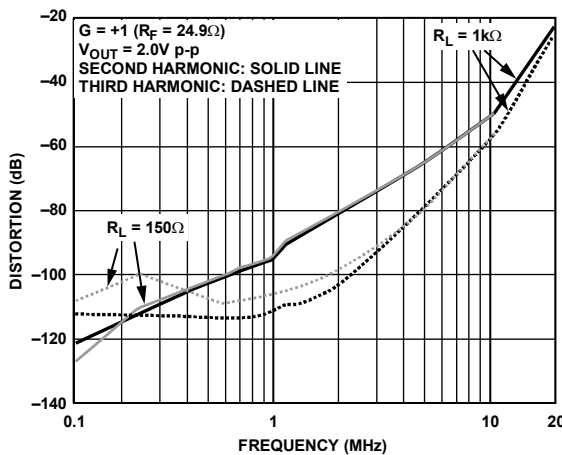


Figure 28. Harmonic Distortion vs. Frequency and Load

03327-023

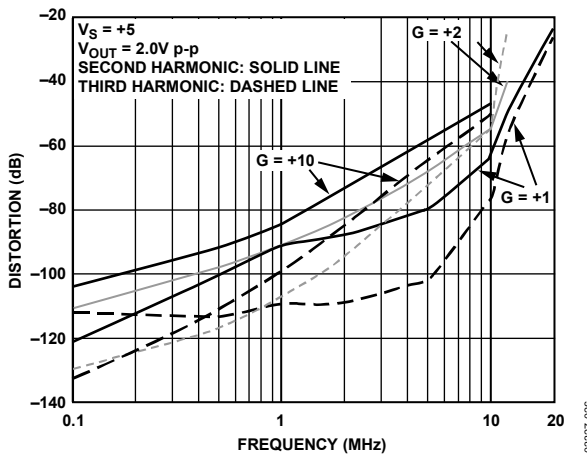


Figure 31. Harmonic Distortion vs. Frequency and Gain

03327-026

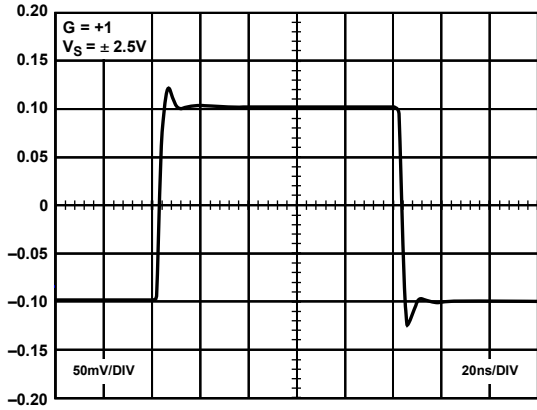


Figure 32. Small Signal Transient Response

03327-027

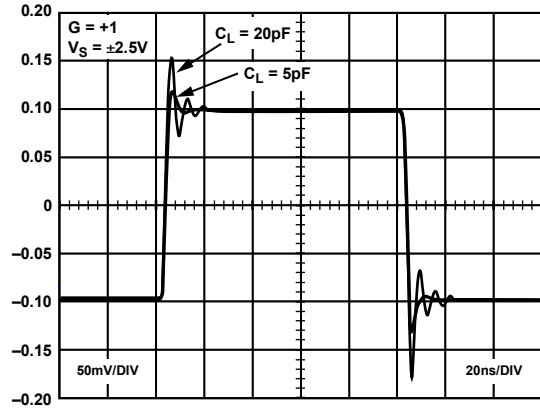


Figure 35. Small Signal Transient Response with Capacitive Load

03327-030

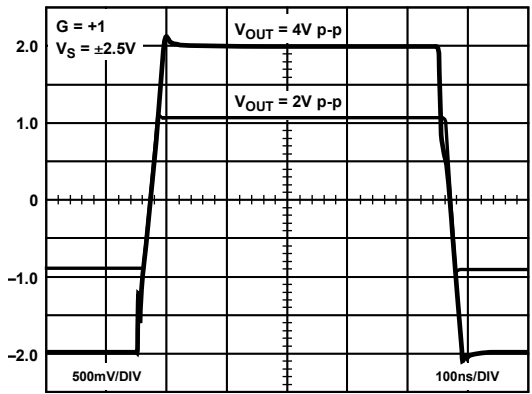


Figure 33. Large Signal Transient Response, $G = +1$

03327-028

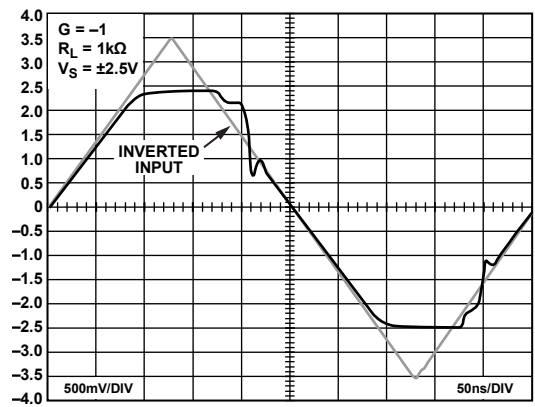


Figure 36. Overdrive Recovery, $G = -1$

03327-031

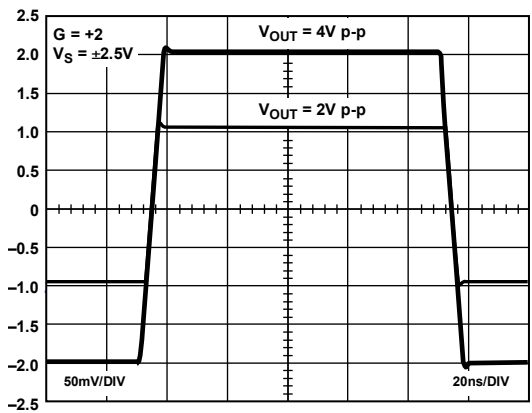


Figure 34. Large Signal Transient Response, $G = +2$

03327-029

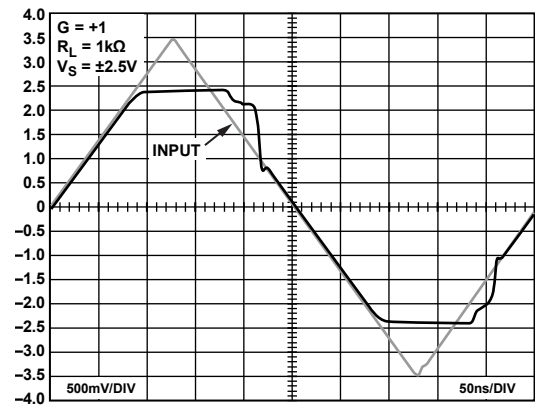


Figure 37. Overdrive Recovery, $G = +1$

03327-032

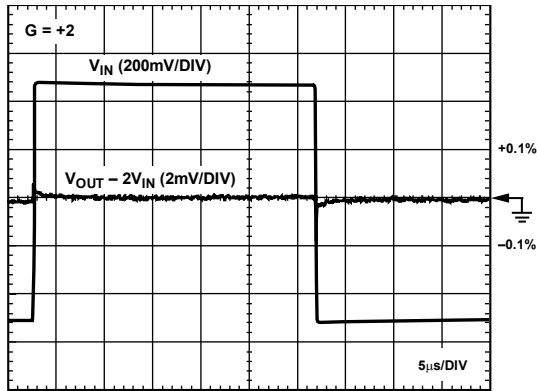


Figure 38. Long-Term Settling Time

03327-033

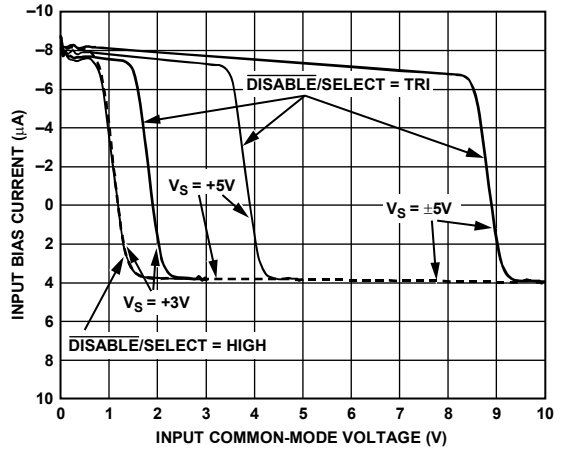


Figure 41. Input Bias Current vs. Input Common-Mode Voltage

03327-036

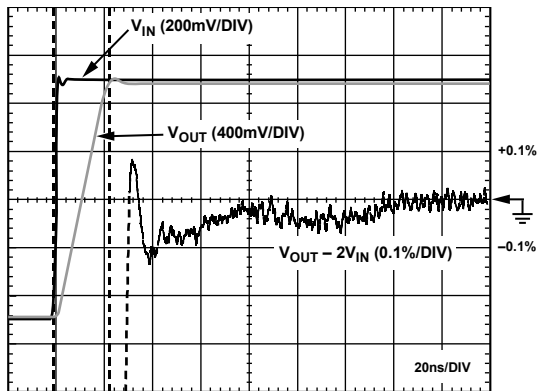


Figure 39. 0.1% Short-Term Settling Time

03327-034

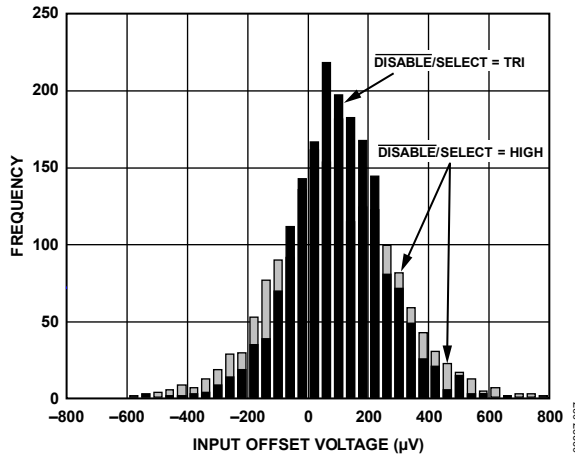


Figure 42. Input Offset Voltage Distribution

03327-037

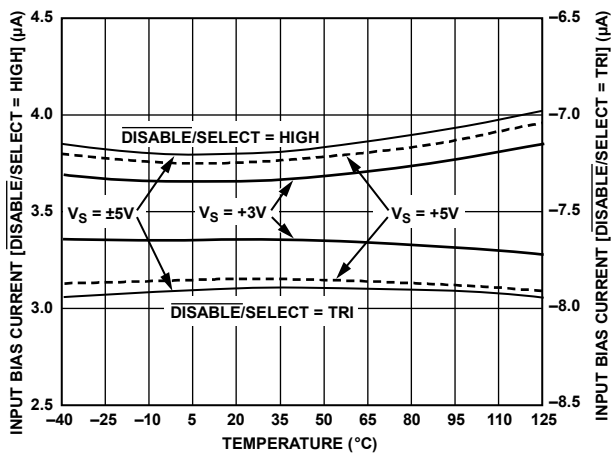


Figure 40. Input Bias Current vs. Temperature

03327-035

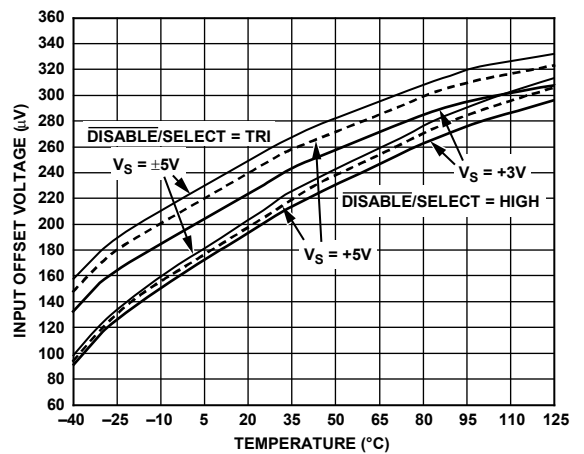


Figure 43. Input Offset Voltage vs. Temperature

03327-038

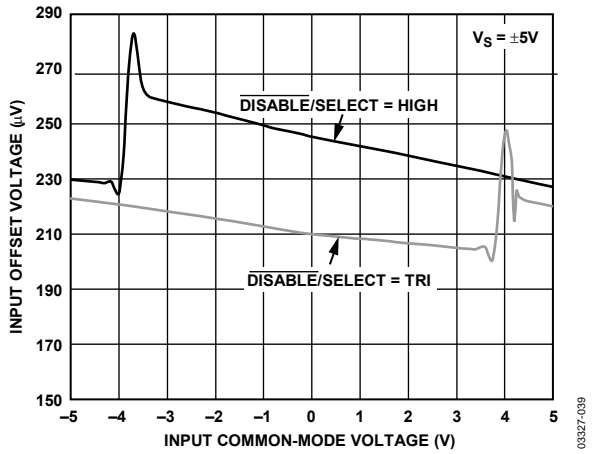


Figure 44. Input Offset Voltage vs. Input Common-Mode Voltage, $V_S = \pm 5V$

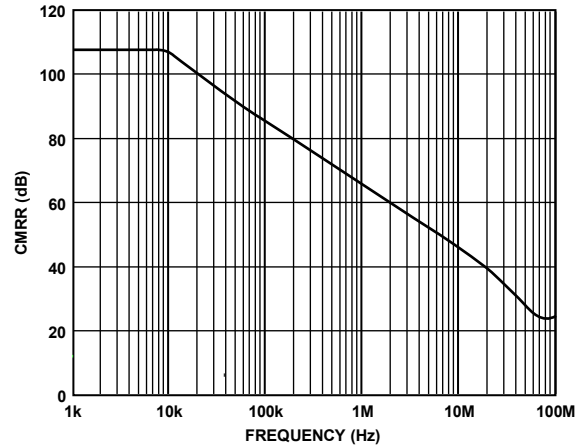


Figure 47. Common-Mode Rejection Ratio (CMRR) vs. Frequency

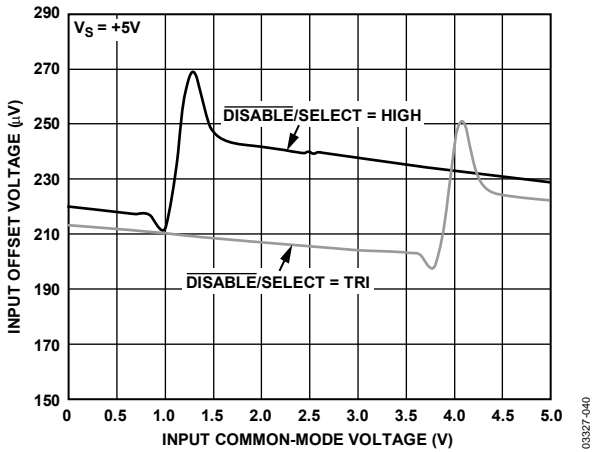


Figure 45. Input Offset Voltage vs. Input Common-Mode Voltage, $V_S = 5V$

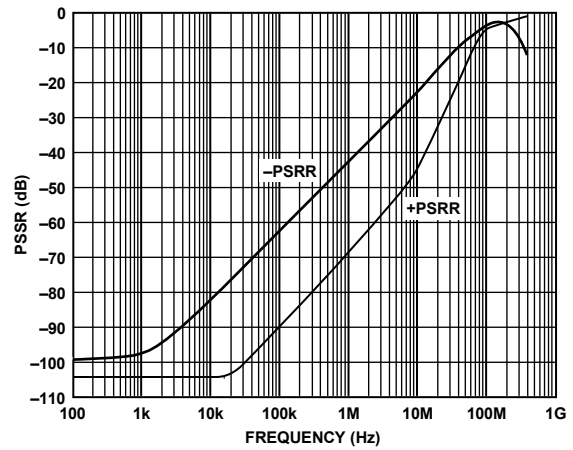


Figure 48. Power Supply Rejection Ratio (PSRR) vs. Frequency

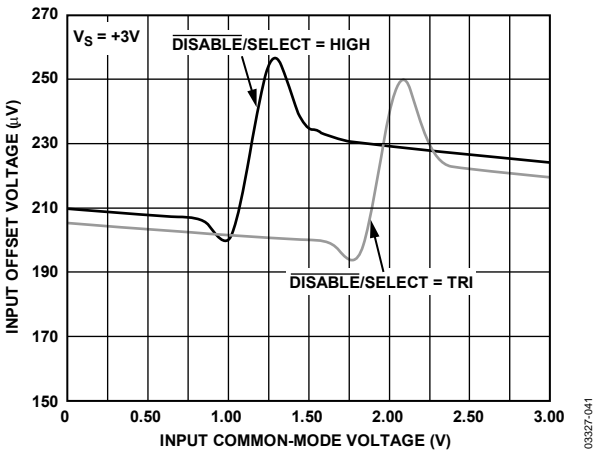


Figure 46. Input Offset Voltage vs. Input Common-Mode Voltage, $V_S = 3V$

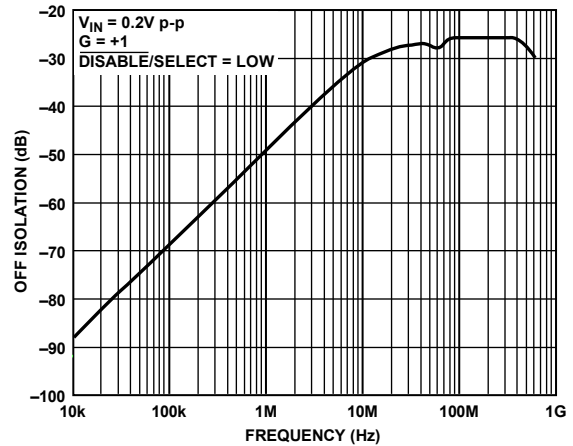


Figure 49. Off Isolation vs. Frequency

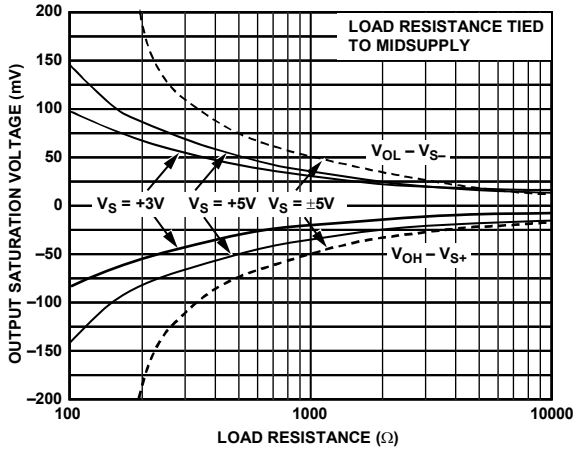


Figure 50. Output Saturation Voltage vs. Load Resistance

03327-045

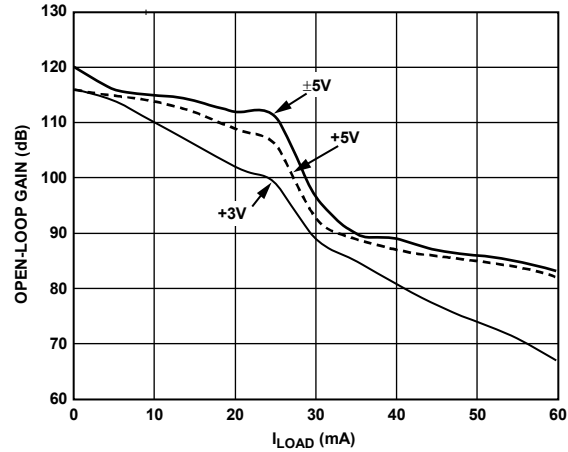


Figure 53. Open-Loop Gain vs. Load Current

03327-048

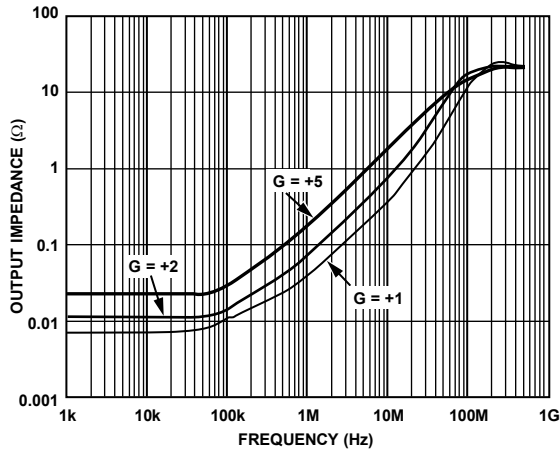


Figure 51. Output Enabled—Impedance vs. Frequency

03327-046

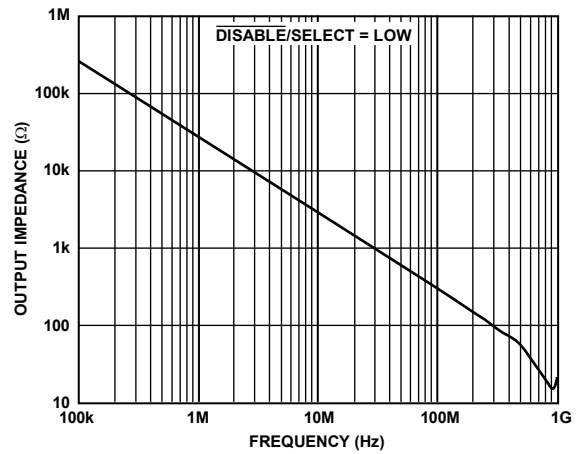


Figure 54. Output Disabled—Impedance vs. Frequency

03327-049

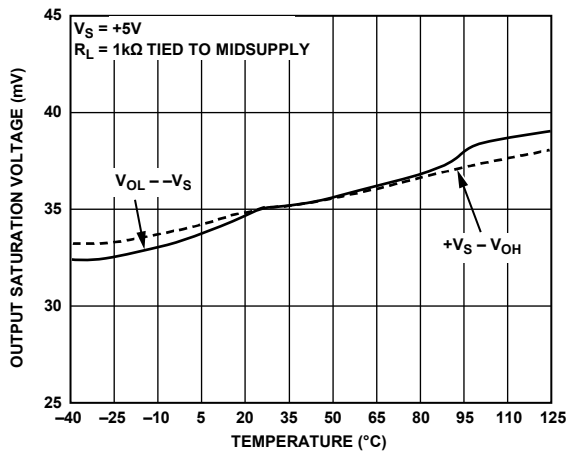


Figure 52. Output Saturation Voltage vs. Temperature

03327-047

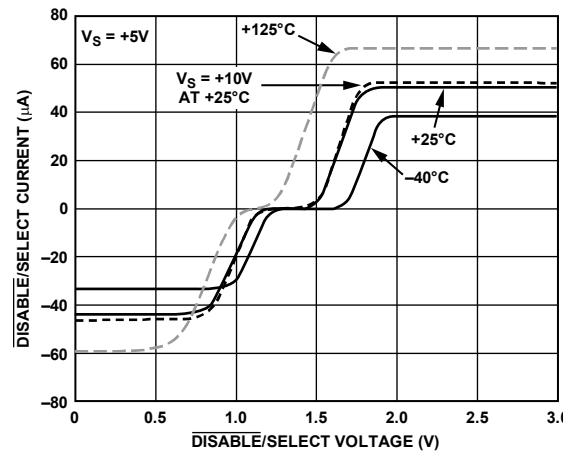


Figure 55. $\overline{\text{DISABLE}}/\text{SELECT}$ Current vs. $\overline{\text{DISABLE}}/\text{SELECT}$ Voltage and Temperature

03327-050

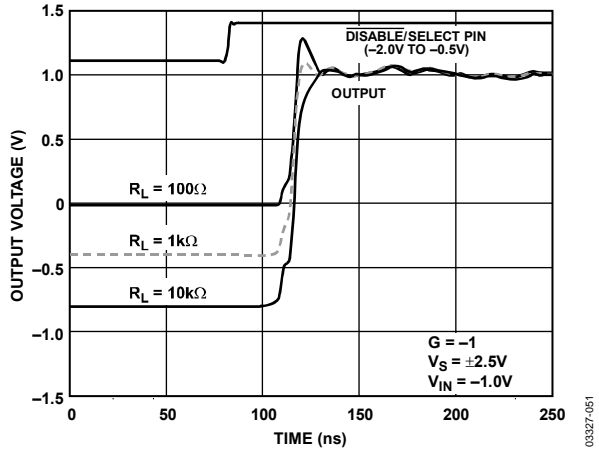


Figure 56. Enable Turn On Timing

03327-061

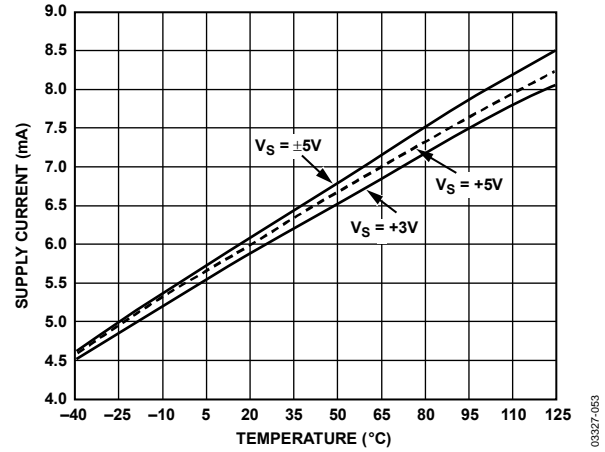


Figure 58. Quiescent Supply Current vs. Temperature and Supply Voltage

03327-063

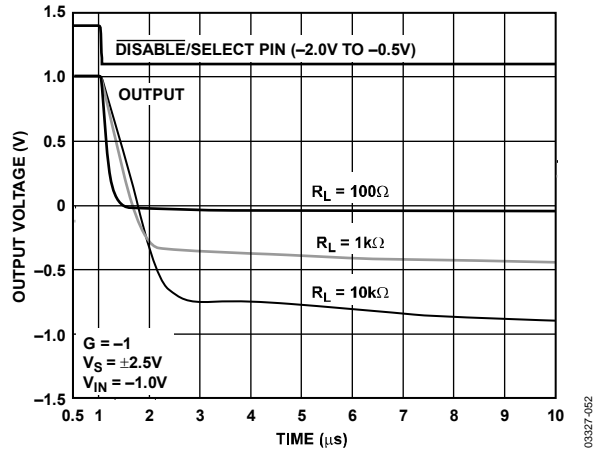


Figure 57. Disable Turn-Off Timing

03327-062

TEST CIRCUIT

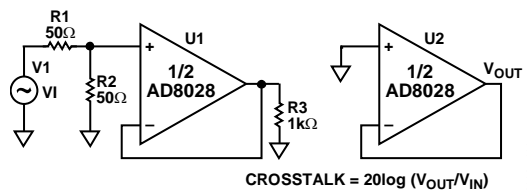


Figure 59. Crosstalk Test Circuit (see Figure 21)

THEORY OF OPERATION

The AD8027/AD8028 are rail-to-rail input/output amplifiers designed in the Analog Devices, Inc., extra fast complementary bipolar (XFCB) process. The XFCB process enables the AD8027/AD8028 to run on 2.7 V to 12 V supplies with 190 MHz of bandwidth and a 100 V/ μ s slew rate. The AD8027/AD8028 have 4.3 nV/ $\sqrt{\text{Hz}}$ of wideband noise with 17 nV/ $\sqrt{\text{Hz}}$ noise at 10 Hz. This noise performance, with an offset of less than 900 μ V maximum and drift performance of 1.50 μ V/ $^{\circ}\text{C}$ typical, makes the AD8027/AD8028 ideal for high speed, precision applications. Additionally, the input stage operates 200 mV beyond the supply rails and shows no phase reversal. The amplifiers feature overvoltage protection on the input stage. When the inputs exceed the supply rails by 0.7 V, ESD protection diodes turn on, drawing excessive current through the differential input pins. Include a series input resistor to limit the input current to less than 10 mA.

INPUT STAGE

The rail-to-rail input performance is achieved by operating complementary input pairs. The common-mode level of the differential input signal determines which pair is on. As shown in Figure 60, a tail current (I_{TAIL}) is generated that sources the PNP differential input structure consisting of Q1 and Q2. A reference voltage is generated internally that is connected to the base of Q5. This voltage is continually compared against the common-mode input voltage. When the common-mode level exceeds the internal reference voltage, Q5 diverts the tail current (I_{TAIL}) from the PNP input pair to a current mirror that sources the NPN input pair consisting of Q3 and Q4.

The NPN input pair can then operate at 200 mV above the positive rail. Both input pairs are protected from differential input signals above 1.4 V by four diodes across the input (see Figure 60). In the event of differential input signals that exceed 1.4 V, the diodes conduct and excessive current flows through them. Include a series input resistor to limit the input current to 10 mA.

CROSSOVER SELECTION

The AD8027/AD8028 have a crossover selection feature that allows the user to choose the crossover point between the PNP/NPN differential pairs. Although the crossover region is small, avoid operating in this region because it can introduce offset and distortion to the output signal. To help avoid operating in the crossover region, the AD8027/AD8028 allow the user to select from two preset crossover locations (voltage levels) using the DISABLE/SELECT pin. The crossover region is about 200 mV and is defined by the voltage level at the base of Q5 in Figure 60. Internally, two separate voltage sources are created approximately 1.2 V from either rail. One rail or the other is connected to Q5, based on the voltage applied to the DISABLE/SELECT pin. This allows either dominant PNP pair operation, when the DISABLE/SELECT pin is left open, or dominant NPN pair operation, when the DISABLE/SELECT pin is pulled high.

The DISABLE/SELECT pin also provides the traditional power-down function when it is pulled low. This pin allows the designer to achieve the best precision and ac performance for high-side and low-side signal applications. See Figure 54 through Figure 57 for DISABLE/SELECT pin characteristics.

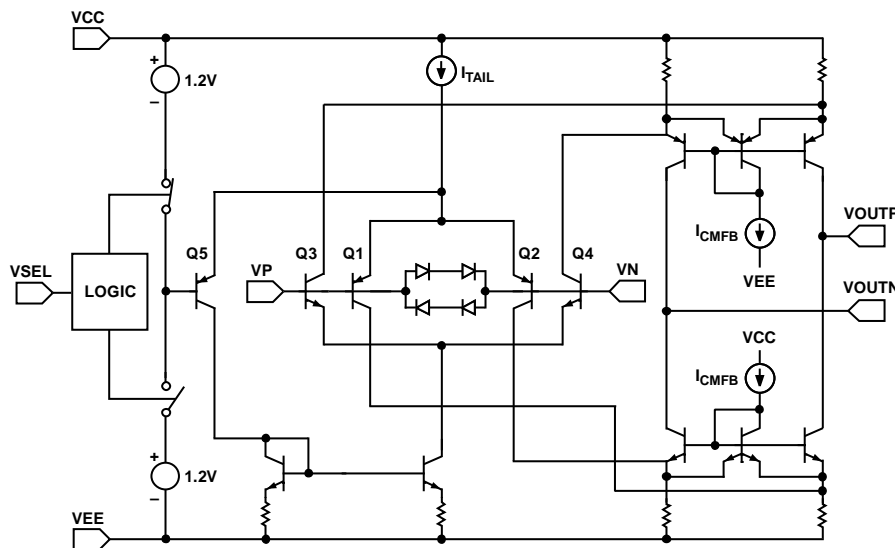


Figure 60. Simplified Input Stage

03327-054

In the event that the crossover region cannot be avoided, specific attention is given to the input stage to ensure constant transconductance and minimal offset in all regions of operation. The regions are PNP input pair running, NPN input pair running, and both running at the same time (in the 200 mV crossover region). Maintaining constant transconductance in all regions ensures the best wideband distortion performance when going between these regions. With this technique, the AD8027/AD8028 can typically achieve 85 dBc SFDR for a 2 V p-p, 1 MHz, and $G = +1$ signal on ± 1.5 V supplies. Another requirement needed to achieve this level of distortion is that the offset of each pair must be laser trimmed, even for low frequency signals.

OUTPUT STAGE

The AD8027/AD8028 use a common emitter output structure to achieve rail-to-rail output capability. The output stage is designed to drive 50 mA of linear output current, 40 mA within 200 mV of the rail, and 2.5 mA within 35 mV of the rail. Loading of the output stage, including any possible feedback network, lowers the open-loop gain of the amplifier. Refer to Figure 53 for the loading behavior. Capacitive load can degrade the phase margin of the amplifier. The AD8027/AD8028 can drive up to 20 pF, $G = +1$, as shown in Figure 14. Include a small (25 Ω to 50 Ω) series resistor, R_{SNUB} , if the capacitive load is to exceed 20 pF for a gain of 1. Increasing the closed-loop gain increases the amount of capacitive load that can be driven before a series resistor must be included.

DC ERRORS

The AD8027/AD8028 use two complementary input stages to achieve rail-to-rail input performance, as described in the Input Stage section. To use the dc performance over the entire common-mode range, the input bias current and input offset voltage of each pair must be considered.

Referring to Figure 61, the output offset voltage of each pair is calculated by

$$V_{OS,PNP,OUT} = V_{OS,PNP} \left(\frac{R_G + R_F}{R_G} \right)$$

$$V_{OS,NPN,OUT} = V_{OS,NPN} \left(\frac{R_G + R_F}{R_G} \right)$$

where the difference of the two input stages is the discontinuity experienced when going through the crossover region.

The size of the discontinuity is defined as

$$V_{DIS} = (V_{OS,PNP} - V_{OS,NPN}) \times \left(\frac{R_G + R_F}{R_G} \right)$$

Using the crossover select feature of the AD8027/AD8028 helps to avoid this region. In the event that the region cannot be avoided, the quantity $(V_{OS,PNP} - V_{OS,NPN})$ is trimmed to minimize this effect.

Because the input pairs are complementary, the input bias current reverses polarity when going through the crossover region shown in Figure 41. The offset between pairs is described by

$$V_{OS,PNP} - V_{OS,NPN} = (I_{B,PNP} - I_{B,NPN}) \times \left(R_S \left(\frac{R_G + R_F}{R_G} \right) - R_F \right)$$

where:

$I_{B,PNP}$ is the input bias current of either input when the PNP input pair is active.

$I_{B,NPN}$ is the input bias current of either input pair when the NPN pair is active.

If R_S is sized so that it equals R_F when multiplied by the gain factor, this effect is eliminated. It is strongly recommended to balance the impedances in this manner when traveling through the crossover region to minimize the dc error and distortion. As an example, assuming that the PNP input pair has an input bias current of 6 μ A and the NPN input pair has an input bias current of -2 μ A, a 200 μ V shift in offset occurs when traveling through the crossover region with R_F equal to 0 Ω and R_S equal to 25 Ω .

In addition to the input bias current shift between pairs, each input pair has an input bias current offset that contributes to the total offset in the following manner:

$$\Delta V_{OS} = I_{B+} R_S \left(\frac{R_G + R_F}{R_G} \right) - I_{B-} R_F$$

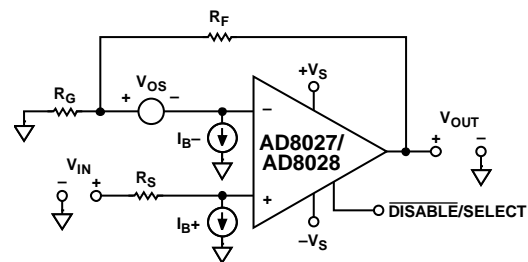


Figure 61. Op Amp DC Error Sources

WIDEBAND OPERATION

Voltage feedback amplifiers can use a wide range of resistor values to set their gain. Proper design of the feedback network of the application requires consideration of the following issues:

- Poles formed by the amplifier input capacitances with the resistances seen at the amplifier input terminals
- Effects of mismatched source impedances
- Resistor value impact on the voltage noise of the application
- Amplifier loading effects

The AD8027/AD8028 have an input capacitance of 2 pF. This input capacitance forms a pole with the amplifier feedback network, destabilizing the loop. For this reason, it is generally desirable to keep the source resistances below 500 Ω, unless some capacitance is included in the feedback network. Likewise, keeping the source resistances low also takes advantage of the AD8027/AD8028 low input voltage noise of 4.3 nV/√Hz.

With a wide bandwidth of 190 MHz, the AD8027/AD8028 have numerous applications and configurations. The AD8027/AD8028 device shown in Figure 62 is configured as a noninverting amplifier. Table 9 provides an easy selection table of gain, resistor values, bandwidth, and noise performance, and Figure 63 shows the inverting configuration.

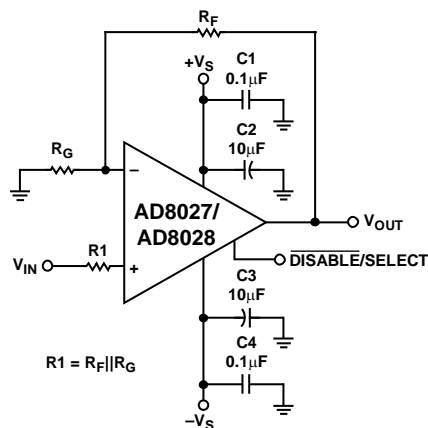


Figure 62. Wideband Noninverting Gain Configuration

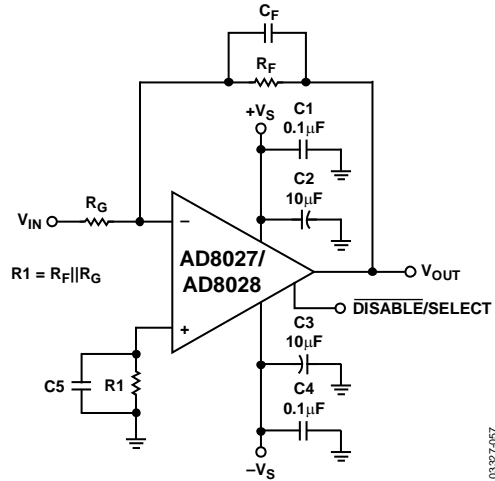


Figure 63. Wideband Inverting Gain Configuration

CIRCUIT CONSIDERATIONS

Balanced Input Impedances

Balanced input impedances can help to improve distortion performance. When the amplifier transitions from PNP pair to NPN pair operation, a change in both the magnitude and direction of the input bias current occurs. When multiplied by imbalanced input impedances, a change in offset can result. The key to minimizing this distortion is to keep the input impedances balanced on both inputs. Figure 64 shows the effect of the imbalance and degradation in SFDR performance for a 50 Ω source impedance, with and without a 50 Ω balanced feedback path.

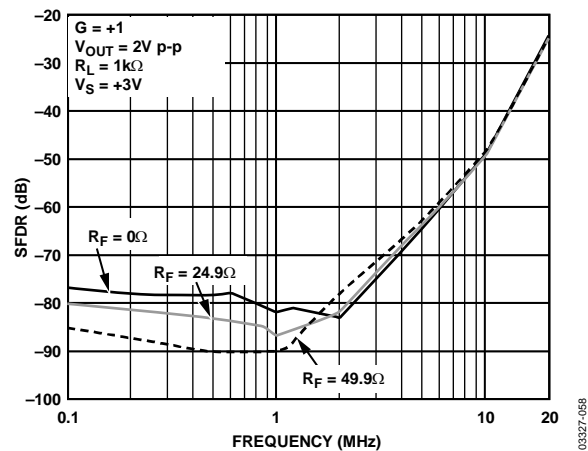


Figure 64. SFDR vs. Frequency and Various R_F

Table 9. Component Values, Bandwidth, and Noise Performance ($V_S = \pm 2.5\text{ V}$)

Noise Gain (Noninverting)	R_{SOURCE} (Ω)	R_F (Ω)	R_G (Ω)	-3 dB Small Signal BW (MHz)	Output Noise with Resistors (nV/√Hz)
1	50	0	Not applicable	190	4.4
2	50	499	499	95	10
10	50	499	54.9	13	45

PCB Layout

As with all high speed op amps, achieving optimum performance from the AD8027/AD8028 requires careful attention to PCB layout. Particular care must be exercised to minimize lead lengths of the bypass capacitors. Excess lead inductance can influence the frequency response and even cause high frequency oscillations. The use of a multilayer board with an internal ground plane can reduce ground noise and enable a tighter layout.

To achieve the shortest possible lead length at the inverting input, position the feedback resistor, R_F , beneath the board so that it spans the distance from the output, to the inverting input. Situate the return node of the resistor, R_G , as closely as possible to the return node of the negative supply bypass capacitor.

On multilayer boards, clear all layers underneath the op amp of metal to avoid creating parasitic capacitive elements. This is especially true at the summing junction (the negative input). Extra capacitance at the summing junction can cause increased peaking in the frequency response and lower phase margin.

Grounding

To minimize parasitic inductances and ground loops in high speed, densely populated boards, a ground plane layer is critical. Understanding where the current flows in a circuit is critical in the implementation of high speed circuit design. The length of the current path is directly proportional to the magnitude of the parasitic inductances and, therefore, the high frequency impedance of the path. Fast current changes in an inductive ground return can create unwanted noise and ringing.

The length of the high frequency bypass capacitor pads and traces is critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Because load currents flow from supplies as well as ground, place the load at the same physical location as the bypass capacitor ground. For large values of capacitors, which are intended to be effective at lower frequencies, the current return path length is less critical.

Power Supply Bypassing

Power supply pins are actually inputs, and care must be taken to provide a clean, low noise, dc voltage source to these inputs. The bypass capacitors have two functions.

- Provide a low impedance path for unwanted frequencies from the supply inputs to ground, thereby reducing the effect of noise on the supply lines.
- Provide sufficient localized charge storage, for fast switching conditions and minimizing the voltage drop at the supply pins and the output of the amplifier. This is usually accomplished with larger electrolytic capacitors.

Decoupling methods are designed to minimize the bypassing impedance at all frequencies. This can be accomplished with a combination of capacitors in parallel to ground.

Use high quality ceramic chip capacitors and always keep them as close as possible to the amplifier package. A parallel combination of a 0.01 μF ceramic and a 10 μF electrolytic covers a wide range of rejection for unwanted noise. The 10 μF capacitor is less critical for high frequency bypassing, and, in most cases, one per supply line is sufficient.

APPLICATIONS INFORMATION

USING THE $\overline{\text{DISABLE/SELECT}}$ PIN

The AD8027/AD8028 unique $\overline{\text{DISABLE/SELECT}}$ pin has two functions:

- The power-down function places the AD8027/AD8028 into low power consumption mode. In power-down mode, the amplifiers draw 500 μA maximum of supply current.
- The second function, as described in the Crossover Selection section, shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail. This selectable crossover point allows the user to minimize distortion based on the input signal and environment. The default state is -1.2 V from the positive power supply, with the $\overline{\text{DISABLE/SELECT}}$ pin left floating or in tristate mode. In tristate mode, it is important that current to the pin is limited to $\pm 20\ \mu\text{A}$ maximum.

Table 10 lists the voltage levels and modes of operation for the $\overline{\text{DISABLE/SELECT}}$ pin over the full temperature range.

Table 10. $\overline{\text{DISABLE/SELECT}}$ Pin Mode Control

Mode	$\overline{\text{DISABLE/SELECT}}$ Pin Voltage (V)
Disable	$-V_S$ to $-V_S + 0.4$
Crossover Referenced -1.2 V to Positive Supply	$-V_S + 1.1$ to $-V_S + 1.3$
Crossover Referenced $+1.2\text{ V}$ to Negative Supply	$-V_S + 2.0$ to $+V_S$

When the input stage transitions from one input differential pair to the other, there is virtually no noticeable change in the output waveform.

The disable time of the AD8027/AD8028 amplifiers is load dependent. Table 11 lists typical enable/disable times. See Figure 56 and Figure 57 for the actual switching measurements.

Table 11. $\overline{\text{DISABLE/SELECT}}$ Switching Speeds

Time	Supply Voltages ($R_L = 1\text{ k}\Omega$)		
	$\pm 5\text{ V}$	+5 V	+3 V
t_{ON}	45 ns	50 ns	50 ns
t_{OFF}	980 ns	1100 ns	1150 ns

DRIVING A 16-BIT ADC

With the adjustable crossover distortion selection point and low noise, the AD8028 is an ideal amplifier for driving or buffering input signals into high resolution ADCs such as the AD7677, a 16-bit, 1 LSB INL, 1 MSPS differential ADC. Figure 65 shows the typical schematic for driving the ADC. The AD8028 driving the AD7677 offers performance close to nonrail-to-rail amplifiers and avoids the need for an additional supply other than the single 5 V supply already used by the ADC.

In this application, the $\overline{\text{DISABLE/SELECT}}$ pins are biased to avoid the crossover region of the AD8028 for low distortion operation.

Table 12 lists summary test data for the schematic shown in Figure 65.

Table 12. ADC Driver Performance, $f_C = 100\text{ kHz}$, $V_{\text{OUT}} = 4.7\text{ V p-p}$

Parameter	Measurement
Second Harmonic Distortion	-105 dB
Third Harmonic Distortion	-102 dB
Total Harmonic Distortion	-102 dB
SFDR	105 dBc

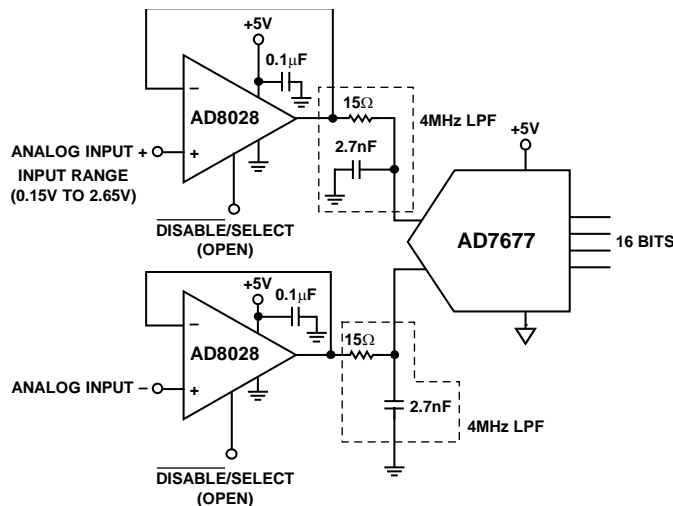


Figure 65. Unity-Gain Differential Drive

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As shown in Figure 66, the AD8028 and AD7677 combination offers excellent integral nonlinearity (INL).

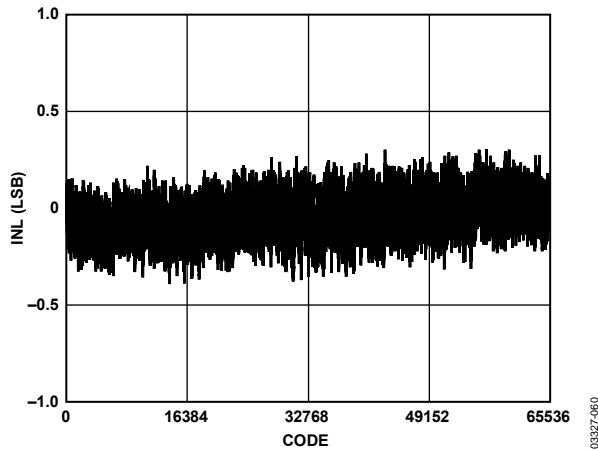


Figure 66. Integral Nonlinearity

BAND-PASS FILTER

In communication systems, active filters are used extensively in signal processing. The AD8027/AD8028 are excellent choices for active filter applications. In realizing this filter, it is important that the amplifier have a large signal bandwidth of at least 10× the center frequency, f_0 . Otherwise, a phase shift can occur in the amplifier, causing instability and oscillations.

In Figure 67, the AD8027/AD8028 device is configured as a 1 MHz band-pass filter. The target specifications are $f_0 = 1$ MHz and a -3 dB pass band of 500 kHz. To start the design, select f_0 , Q, C1, and R4. Then use the following equations to calculate the remaining variables:

$$Q = \frac{f_0 \text{ (MHz)}}{\text{Band Pass (MHz)}}$$

$$k = 2\pi f_0 C1$$

$$C2 = 0.5C1$$

$$R1 = 2/k, R2 = 2/(3k), R3 = 4/k$$

$$H = 1/3(6.5 - 1/Q)$$

$$R5 = R4/(H - 1)$$

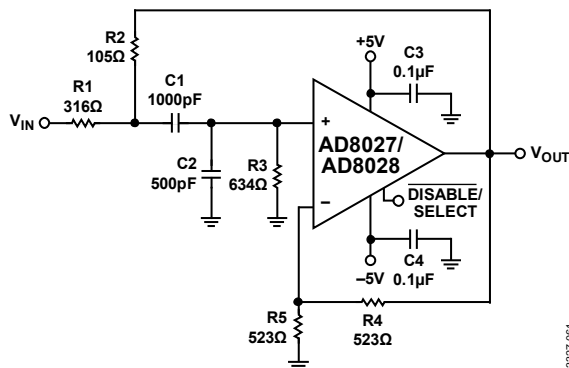


Figure 67. Band-Pass Filter Schematic

The test data shown in Figure 68 indicates that this design yields a filter response with a center frequency of $f_0 = 1$ MHz, and a bandwidth of 450 kHz.

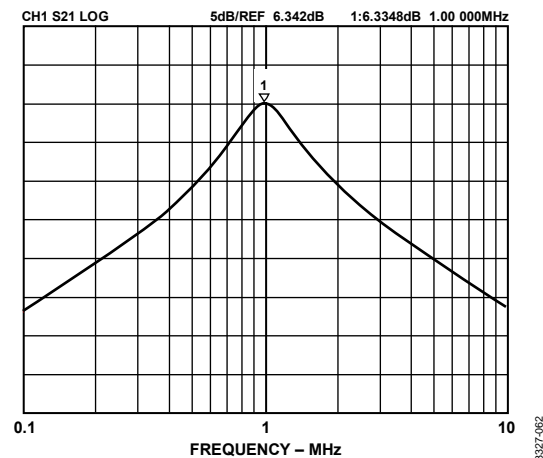
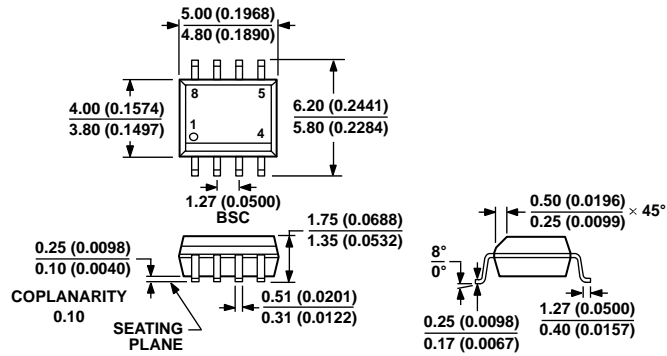


Figure 68. Band-Pass Filter Response

DESIGN TOOLS AND TECHNICAL SUPPORT

Analog Devices is committed to simplifying the design process by providing technical support and online design tools. Analog Devices offers technical support via evaluation boards, sample ICs, interactive evaluation tools, data sheets, SPICE models, application notes, and phone and email support available at www.analog.com.

OUTLINE DIMENSIONS

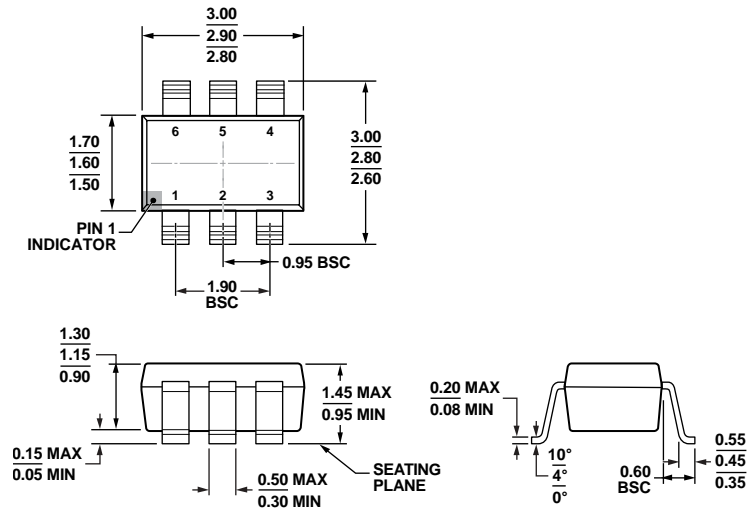


COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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Figure 69. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 70. 6-Lead Small Outline Transistor Package [SOT-23]
 (RJ-6)

Dimensions shown in millimeters

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