Low Cost, 300 MHz Voltage Feedback Amplifiers

AD8055/AD8056

FEATURES

- Low cost single (AD8055) and dual (AD8056)
- Easy-to-use voltage feedback architecture
- High speed
  - 300 MHz, −3 dB bandwidth (G = +1)
  - 1400 V/µs slew rate
  - 20 ns settling to 0.1%
  - Low distortion: −72 dBc @ 10 MHz
  - Low noise: 6 nV/√Hz
  - Low dc errors: 5 mV max V_{OS}, 1.2 µA max I_B
- Small packaging
  - AD8055 available in 5-lead SOT-23
  - AD8056 available in 8-lead MSOP
- Excellent video specifications (R_L = 150 Ω, G = +2)
  - Gain flatness 0.1 dB to 40 MHz
  - 0.01% differential gain error
  - 0.02° differential phase error
  - Drives 4 video loads (37.5 V) with 0.02% differential
  - Gain and 0.1° differential phase
- Low power, ±5 V supplies 5 mA typ/amplifier power supply current
- High output drive current: over 60 mA

APPLICATIONS

- Imaging
- Photodiode preamps
- Video line drivers
- Differential line drivers
- Professional cameras
- Video switchers
- Special effects
- A-to-D drivers
- Active filters

GENERAL DESCRIPTION

The AD8055 (single) and AD8056 (dual) voltage feedback amplifiers offer bandwidth and slew rate typically found in current feedback amplifiers. Additionally, these amplifiers are easy to use and available at a very low cost.

Despite their low cost, the AD8055 and AD8056 provide excellent overall performance. For video applications, their differential gain and phase error are 0.01% and 0.02° into a 150 Ω load and 0.02% and 0.1° while driving four video loads (37.50 Ω).

CONNECTION DIAGRAMS

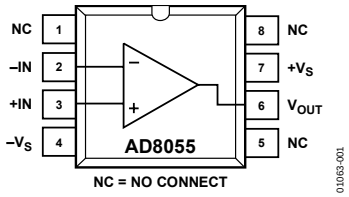

Figure 1. N-8 and R-8

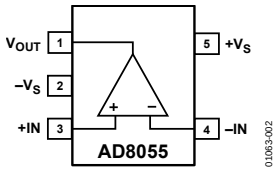

Figure 2. RJ-5

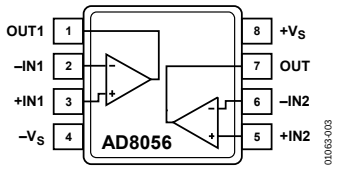

Figure 3. N-8, R-8, and RM-8

Their 0.1 dB flatness out to 40 MHz, wide bandwidth out to 300 MHz, along with 1400 V/µs slew rate and 20 ns settling time, make them useful for a variety of high speed applications.

The AD8055 and AD8056 require only 5 mA typ/amplifier of supply current and operate on a dual ±5 V or a single +12 V power supply, while capable of delivering over 60 mA of load current. The AD8055 is available in a small 8-lead PDIP, an 8-lead SOIC, and a 5-lead SOT-23, while the AD8056 is available in an 8-lead MSOP. These features make the AD8055/AD8056 ideal for portable and battery-powered applications where size and power are critical. These amplifiers in the R-8, N-8, and RM-8 packages are available in the extended temperature range of −40°C to +125°C.

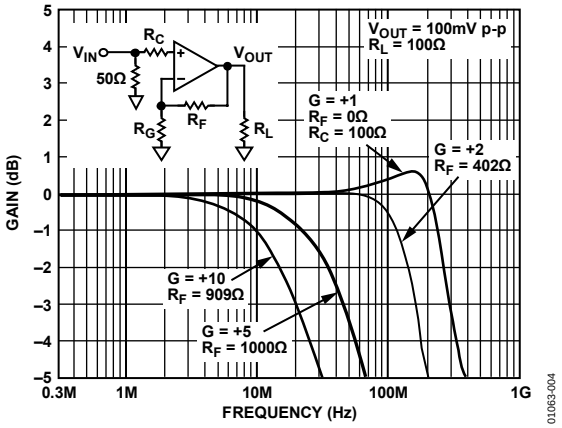

Figure 4. Frequency Response

Rev. J

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SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, Gain = +2, unless otherwise noted.

Table 1.

		AD8055A/AD8056A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.1 V p-p	220	300		MHz
	G=+1, V_O = 2 V p-p	125	150		MHz
	G=+2, V_O = 0.1 V p-p	120	160		MHz
	G=+2, V_O = 2 V p-p	125	150		MHz
Bandwidth for 0.1 dB Flatness	V_O = 100 mV p-p	25	40		MHz
Slew Rate	G = +1, V_O = 4 V step	1000	1400		V/µs
	G = +2, V_O = 4 V step	750	840		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		20		ns
Rise and Fall Time, 10% to 90%	G = +1, V_O = 0.5 V step		2		ns
	G = +1, V_O = 4 V step		2.7		ns
	G = +2, V_O = 0.5 V step		2.8		ns
	G = +2, V_O = 4 V step		4		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 10 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−72		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−57		dBc
Crosstalk, Output-to-Output (AD8056)	f = 5 MHz, G = +2		−60		dB
Input Voltage Noise	f = 100 kHz		6		nV/√Hz
Input Current Noise	f = 100 kHz		1		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
	NTSC, G = +2, R_L = 37.5 Ω		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.02		Degree
	NTSC, G = +2, R_L = 37.5 Ω		0.1		Degree
DC PERFORMANCE					
Input Offset Voltage			3	5	mV
	T_{MIN} to T_{MAX}			10	mV
Offset Drift		6			µV/°C
Input Bias Current			0.4	1.2	µA
	T_{MIN} to T_{MAX}	1			µA
Open-Loop Gain	V_O = ±2.5 V	66	71		dB
	T_{MIN} to T_{MAX}	64			dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V		82		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	2.9	3.1		±V
Output Current[1]	V_O = ±2.0 V	55	60		mA
Short-Circuit Current[1]			110		mA

Parameter	Conditions	AD8055A/AD8056A Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		±4.0	±5.0	±6.0	V
Quiescent Current	AD8055		5.4	6.5	mA
	T_{MIN} to 125°C		7.6		mA
	T_{MIN} to 85°C			7.3	mA
	AD8056		10	12	mA
	T_{MIN} to 125°C		13.9		mA
	T_{MIN} to 85°C			13.3	mA
Power Supply Rejection Ratio	$+V_S$ = +5 V to +6 V, $-V_S$ = −5 V	66	72		dB
	$-V_S$ = −5 V to −6 V, $+V_S$ = +5 V	69	86		dB
OPERATING TEMPERATURE RANGE	AD8055ART	−40		+85	°C
	AD8055AR, AD8055AN, AD8056AR, AD8056AN, AD8056ARM	−40		+125	°C

[1] Output current is limited by the maximum power dissipation in the package. See Figure 5.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Supply Voltage	13.2 V
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±2.5 V
Output Short-Circuit Duration	Observe Power Derating Curves
Storage Temperature Range N, R	−65°C to +150°C
Operating Temperature Range (A Grade)	−40°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8055/AD8056 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8055/AD8056 are internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

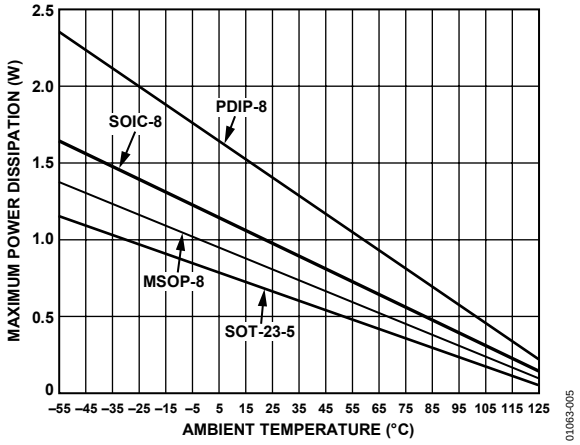


Figure 5. Plot of Maximum Power Dissipation vs. Temperature for AD8055/AD8056

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

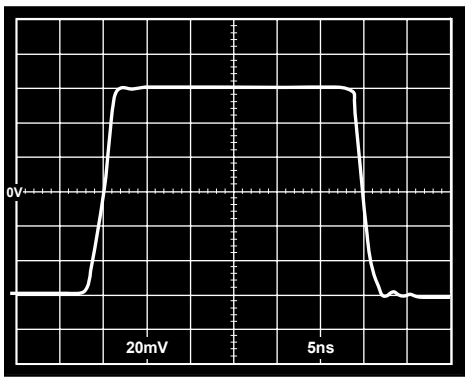


Figure 6. Small Step Response, G = +1 (See Figure 34)

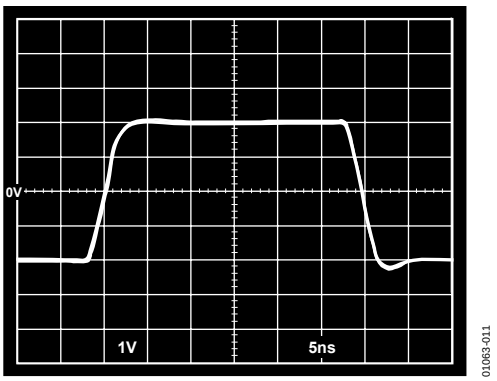


Figure 9. Large Step Response, G = −1 (See Figure 35)

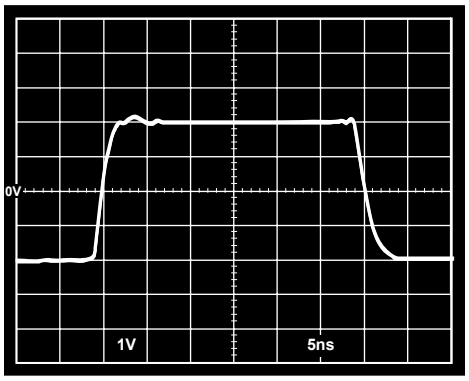


Figure 7. Large Step Response, G = +1 (See Figure 34)

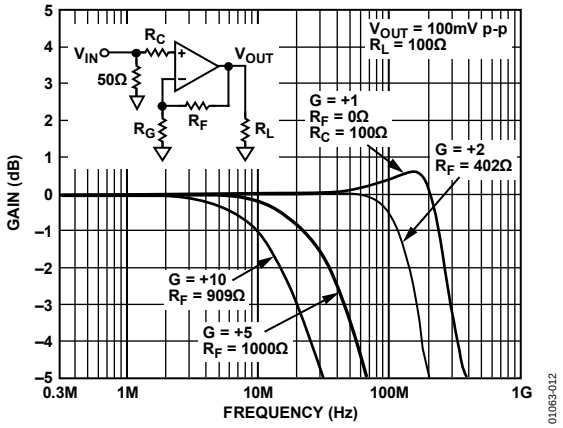


Figure 10. Small Signal Frequency Response, G = +1, G = +2, G = +5, G = +10

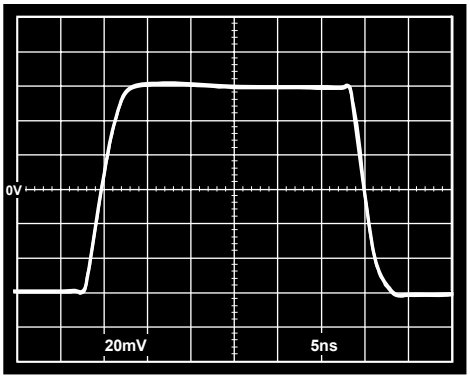


Figure 8. Small Step Response, G = −1 (See Figure 35)

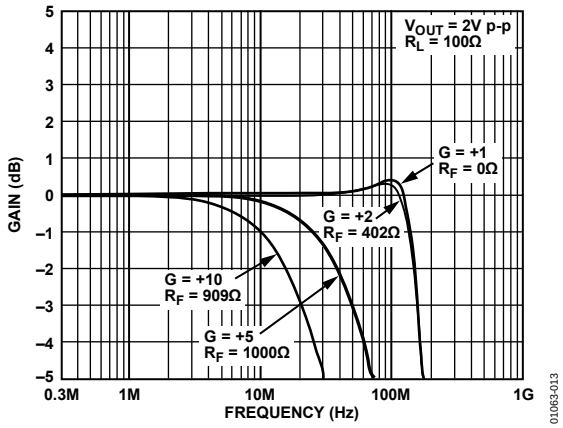


Figure 11. Large Signal Frequency Response, G = +1, G = +2, G = +5, G = +10

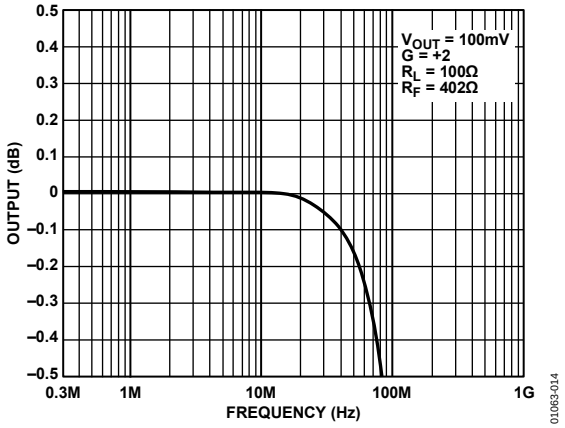


Figure 12. 0.1 dB Flatness

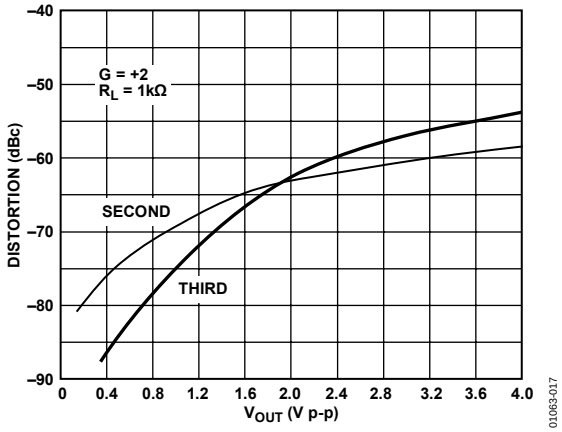


Figure 15. Distortion vs. V_{OUT} @ 20 MHz

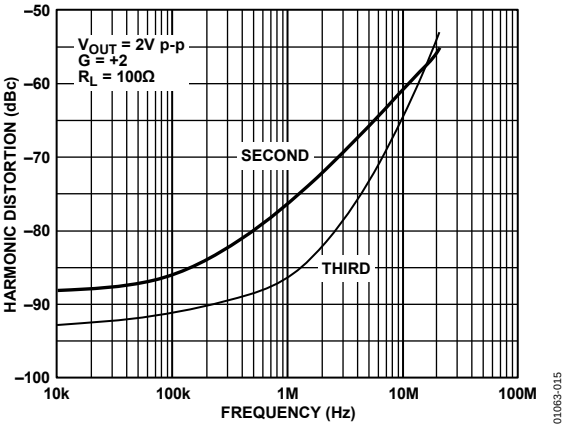


Figure 13. Harmonic Distortion vs. Frequency

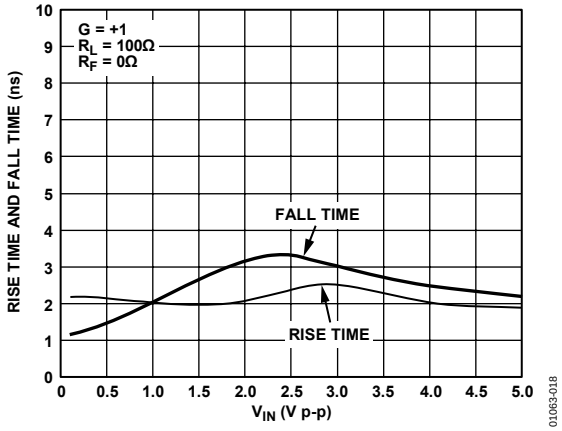


Figure 16. Rise Time and Fall Time vs. V_{IN}

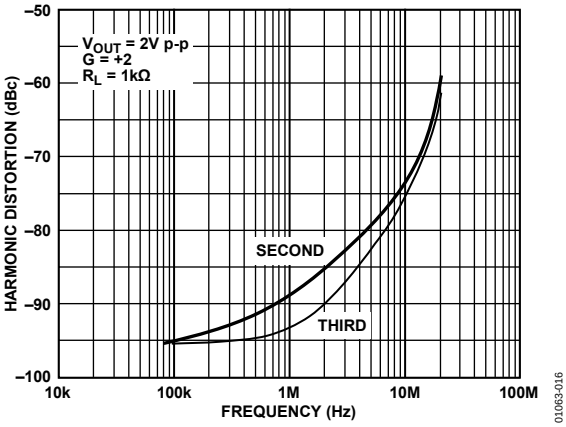


Figure 14. Harmonic Distortion vs. Frequency

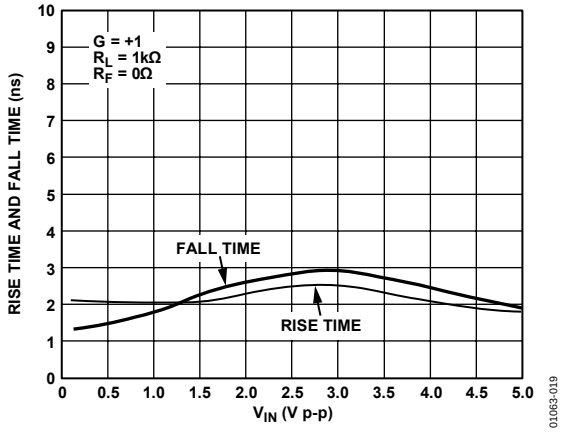


Figure 17. Rise Time and Fall Time vs. V_{IN}

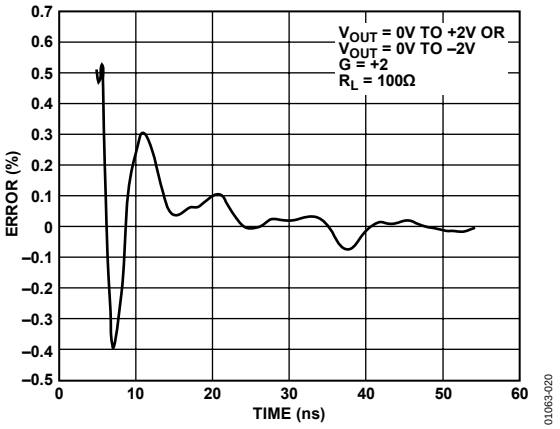


Figure 18. Settling Time

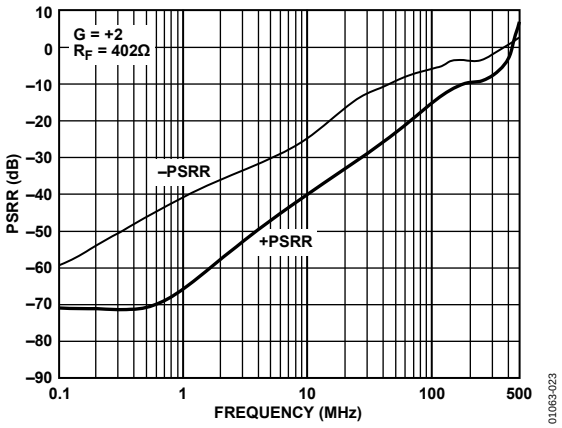


Figure 21. PSRR vs. Frequency

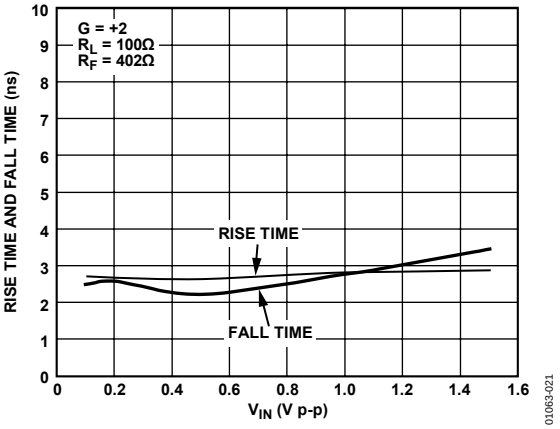


Figure 19. Rise Time and Fall Time vs. V_{IN}

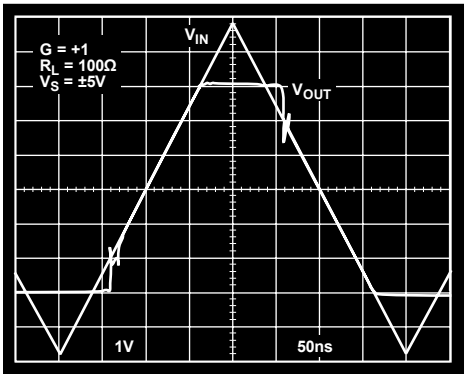


Figure 22. Overload Recovery

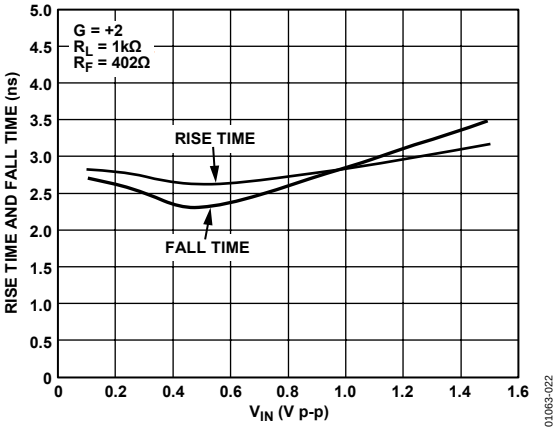


Figure 20. Rise Time and Fall Time vs. V_{IN}

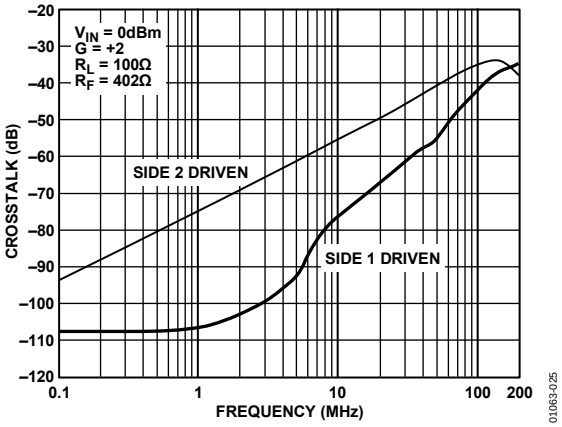


Figure 23. Crosstalk (Output-to-Output) vs. Frequency

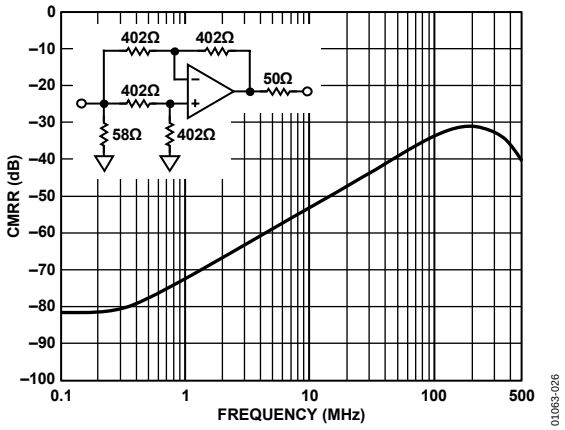


Figure 24. CMRR vs. Frequency

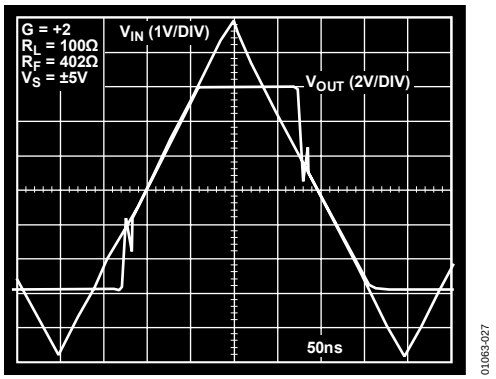


Figure 25. Overload Recovery

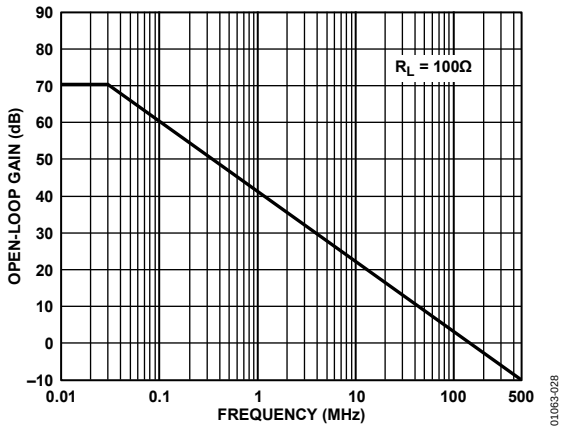


Figure 26. Open-Loop Gain vs. Frequency

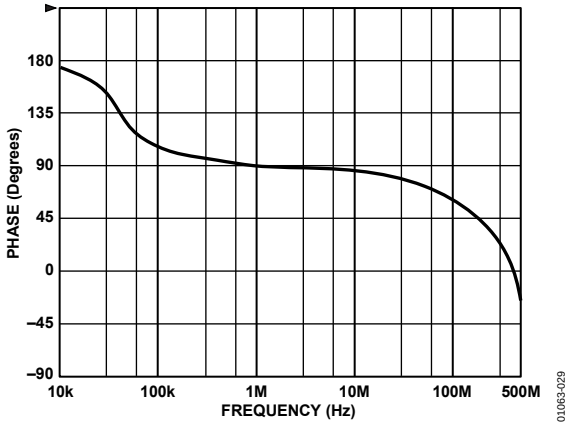


Figure 27. Phase vs. Frequency

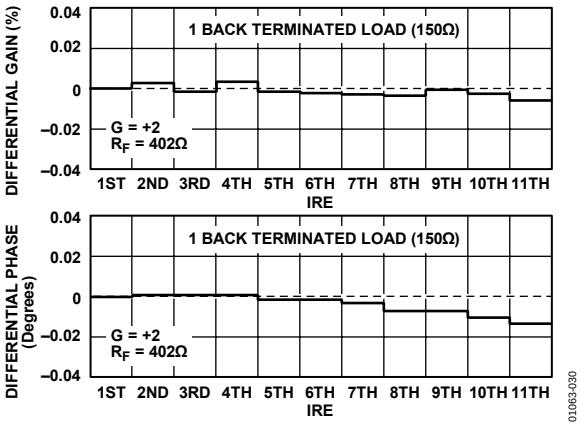


Figure 28. Differential Gain and Differential Phase

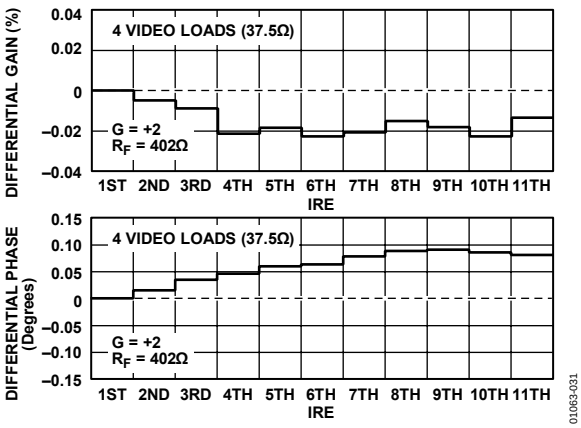


Figure 29. Differential Gain and Differential Phase

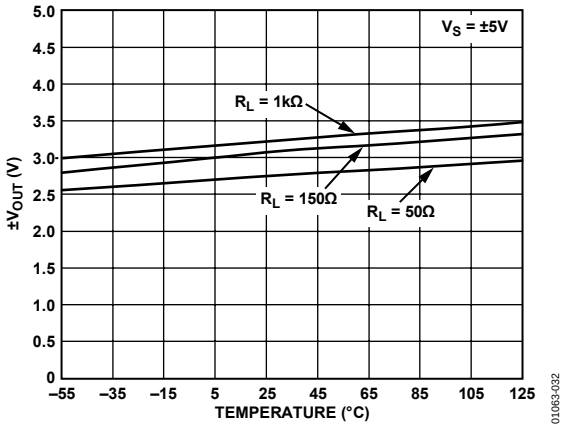


Figure 30. Output Swing vs. Temperature

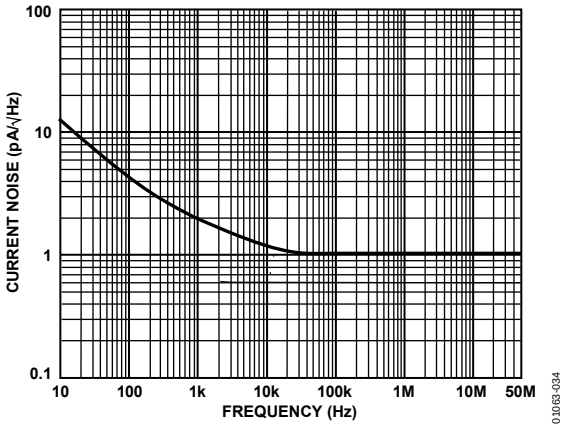


Figure 32. Current Noise vs. Frequency

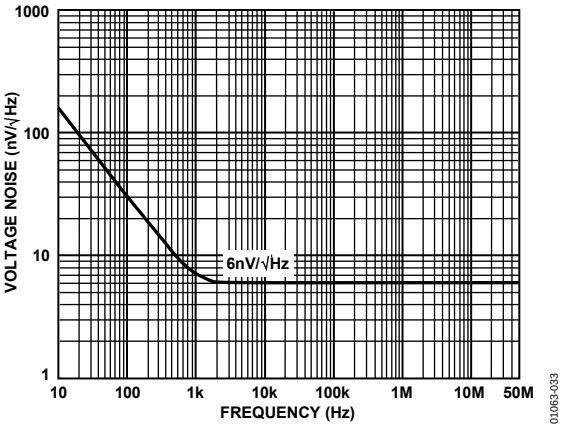


Figure 31. Voltage Noise vs. Frequency

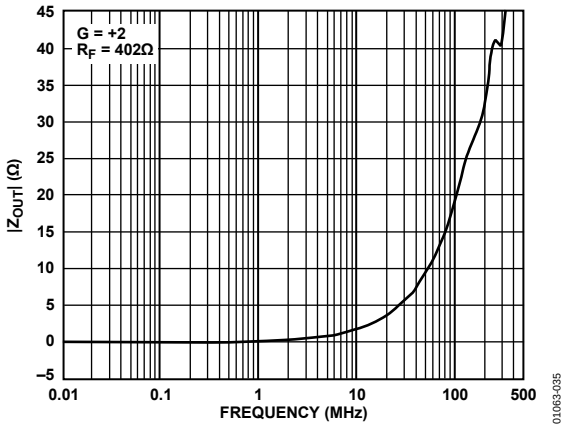


Figure 33. Output Impedance vs. Frequency

TEST CIRCUITS

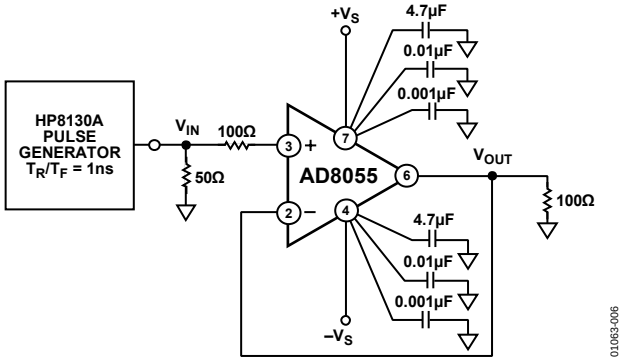


Figure 34. G = +1, R_L = 100 Ω

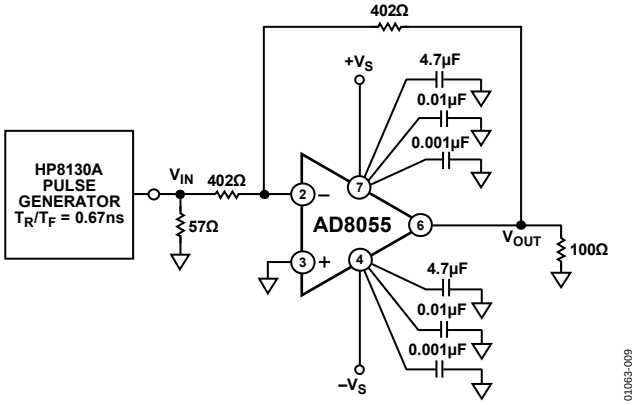


Figure 35. G = −1, R_L = 100 Ω

APPLICATIONS

FOUR-LINE VIDEO DRIVER

The AD8055 is a useful low cost circuit for driving up to four video lines. For such an application, the amplifier is configured for a noninverting gain of 2, as shown in Figure 36. The input video source is terminated in 75 Ω and is applied to the high impedance noninverting input.

Each output cable is connected to the op amp output via a 75 Ω series back termination resistor for proper cable termination. The terminating resistors at the other ends of the lines divide the output signal by 2, which is compensated for by the gain of 2 of the op amp stage.

For a single load, the differential gain error of this circuit was measured as 0.01%, with a differential phase error of 0.02°. The two load measurements were 0.02% and 0.03°, respectively. For four loads, the differential gain error is 0.02%, while the differential phase increases to 0.1°.

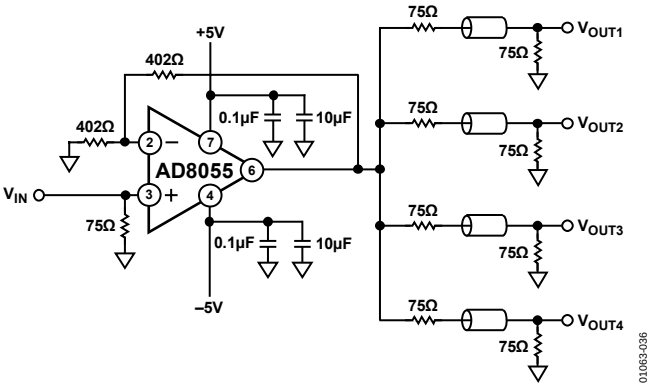


Figure 36. Four-Line Video Driver

SINGLE-ENDED-TO-DIFFERENTIAL LINE DRIVER

Creating differential signals from single-ended signals is required for driving balanced, twisted pair cables, differential input ADCs, and other applications that require differential signals. This can be accomplished by using an inverting and a noninverting amplifier stage to create the complementary signals.

The circuit shown in Figure 37 shows how an AD8056 can be used to make a single-ended-to-differential converter that offers some advantages over the architecture previously mentioned. Each op amp is configured for unity gain by the feedback resistors from the outputs to the inverting inputs. In addition, each output drives the opposite op amp with a gain of −1 by means of the crossed resistors. The result of this is that the outputs are complementary and there is high gain in the overall configuration.

Feedback techniques similar to a conventional op amp are used to control the gain of the circuit. From the noninverting input of AMP1 to the output of AMP2 is an inverting gain. Between these points, a feedback resistor can be used to close the loop. As in the case of a conventional op amp inverting gain stage, an input resistor is added to vary the gain.

The gain of this circuit from the input to AMP1 output is R_F/R_I, while the gain to the output of AMP2 is $-R_F/R_I$. The circuit therefore creates a balanced differential output signal from a single-ended input. The advantage of this circuit is that the gain can be changed by changing a single resistor, while still maintaining the balanced differential outputs.

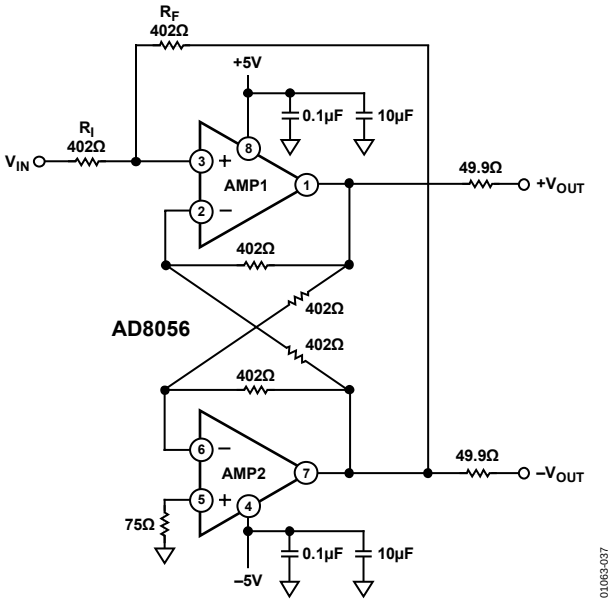


Figure 37. Single-Ended-to-Differential Line Driver

LOW NOISE, LOW POWER PREAMP

The AD8055 makes a good, low cost, low noise, low power preamp. A gain-of-10 preamp can be made with a feedback resistor of 909 Ω and a gain resistor of 100 Ω, as shown in Figure 38. The circuit has a −3 dB bandwidth of 20 MHz.

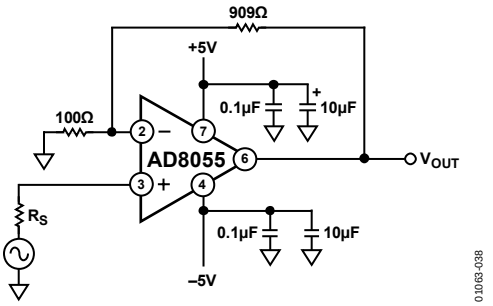


Figure 38. Low Noise, Low Power Preamp with G = +10 and BW = 20 MHz

With a low source resistance (< approximately 100 Ω), the major contributors to the input-referred noise of this circuit are the input voltage noise of the amplifier and the noise of the 100 Ω resistor. These are 6 nV/√Hz and 1.2 nV/√Hz, respectively. These values yield a total input referred noise of 6.1 nV/√Hz.

POWER DISSIPATION LIMITS

With a 10 V supply (total $V_{CC} - V_{EE}$), the quiescent power dissipation of the AD8055 in the SOT-23-5 package is 65 mW, while the quiescent power dissipation of the AD8056 in the MSOP-8 is 120 mW. This translates into a 15.6°C rise above the ambient for the SOT-23-5 package and a 24°C rise for the MSOP-8 package.

The power dissipated under heavy load conditions is approximately equal to the supply voltage minus the output voltage, times the load current, plus the quiescent power previously computed. The total power dissipation is then multiplied by the thermal resistance of the package to find the temperature rise, above ambient, of the part. The junction temperature should be kept below 150°C.

The AD8055 in the SOT-23-5 package can dissipate 270 mW, while the AD8056 in the MSOP-8 package can dissipate 325 mW (at 85°C ambient) without exceeding the maximum die temperature. In the case of the AD8056, this is greater than 1.5 V rms into 50 Ω, enough to accommodate a 4 V p-p sine wave signal on both outputs simultaneously. However, because each output of the AD8055 or AD8056 is capable of supplying as much as 110 mA into a short circuit, a continuous short-circuit condition will exceed the maximum safe junction temperature.

RESISTOR SELECTION

Table 3 is a guide for resistor selection for maintaining gain flatness vs. frequency for various values of gain.

Table 3.

Gain	R_F (Ω)	R_G (Ω)	−3 dB Bandwidth (MHz)
+1	0		300
+2	402	402	160
+5	1 k	249	45
+10	909	100	20

DRIVING CAPACITIVE LOADS

When driving a capacitive load, most op amps exhibit peaking in the frequency response just before the frequency rolls off. Figure 39 shows the responses for an AD8056 running at a gain of +2, with an 100 Ω load that is shunted by various values of capacitance. It can be seen that under these conditions the part is still stable with capacitive loads of up to 30 pF.

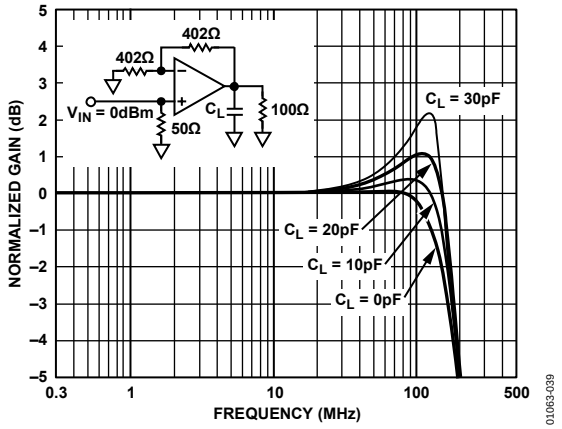


Figure 39. Capacitive Load Drive

In general, to minimize peaking or to ensure the stability for larger values of capacitive loads, a small series resistor, R_S, can be added between the op amp output and the capacitor, C_L. For the setup depicted in Figure 40, the relationship between R_S and C_L was empirically derived and is shown in Figure 41. R_S was chosen to produce less than 1 dB of peaking in the frequency response. Note also that after a sharp rise, R_S quickly settles to approximately 25 Ω.

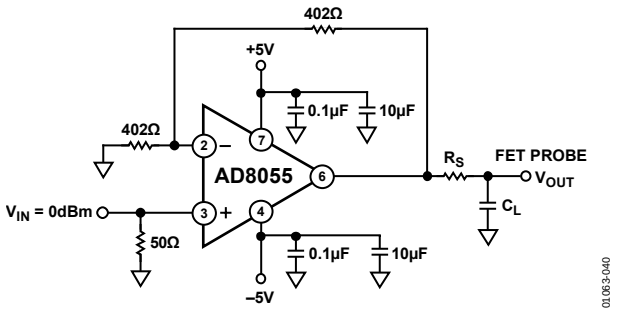


Figure 40. Setup for R_S vs. C_L

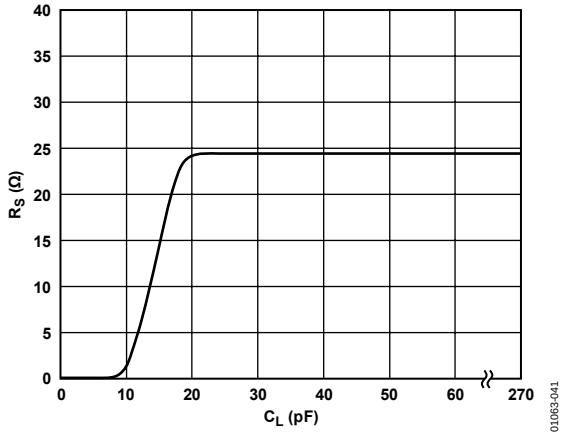
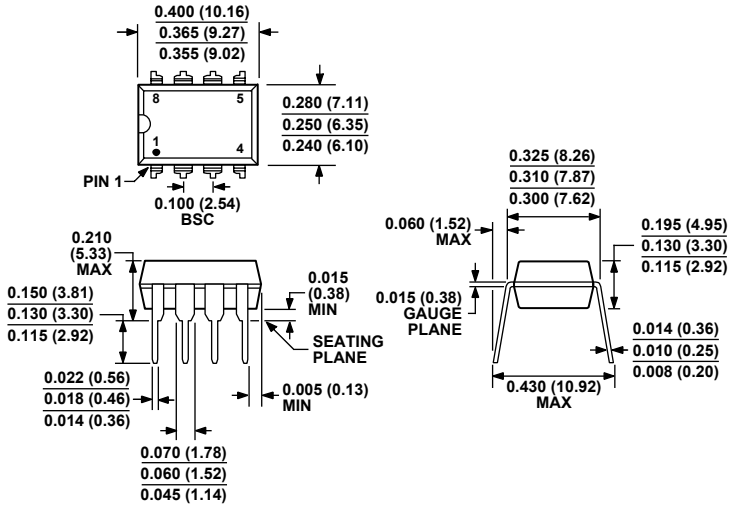


Figure 41. R_S vs. C_L

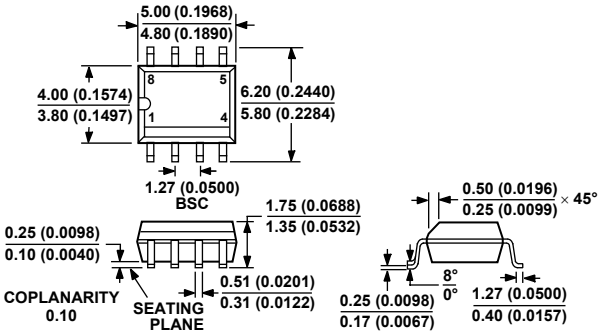
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

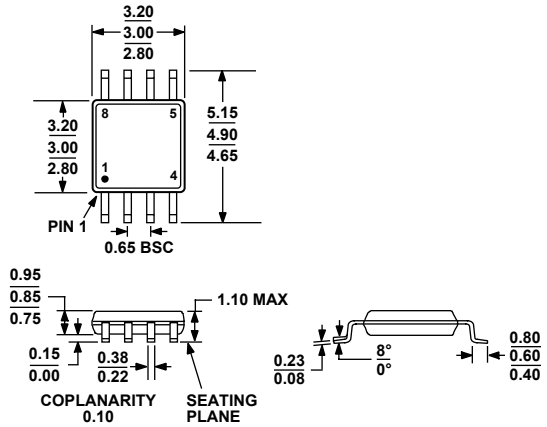
Figure 42. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

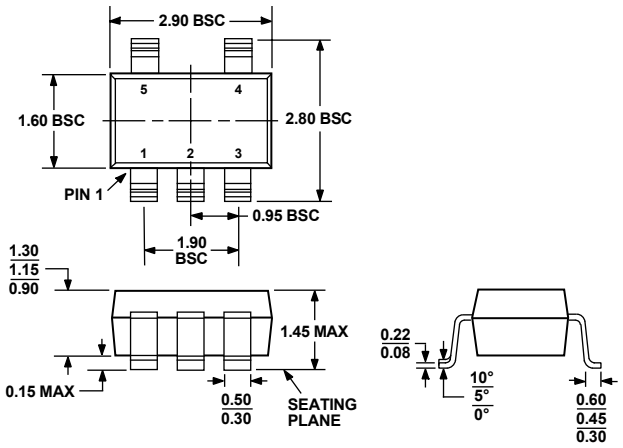
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 45. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters