Precision Instrumentation Amplifier with Signal Processing Amplifiers

AD8295

FEATURES

Saves board space
Includes precision in-amp, 2 op amps, and 2 matched resistors
4 mm × 4 mm LFCSP
- **No heat slug for more routing room**

Differential output fully specified
In-amp specifications
- **Gain set with 1 external resistor (gain range: 1 to 1000)**
- **Input voltage noise: 8 nV/√Hz maximum at 1 kHz**
- **CMRR (G = 1): 90 dB minimum**
- **Input bias current: 0.8 nA maximum**
- **−3 dB bandwidth (G = 1): 1.2 MHz**
- **Slew rate: 2 V/µs**

Wide power supply range: ±2.3 V to ±18 V
1 ppm/°C, 0.03% resistor matching

APPLICATIONS

Industrial process controls
Wheatstone bridges
Precision data acquisition systems
Medical instrumentation
Strain gages
Transducer interfaces
Differential output

CONNECTION DIAGRAM

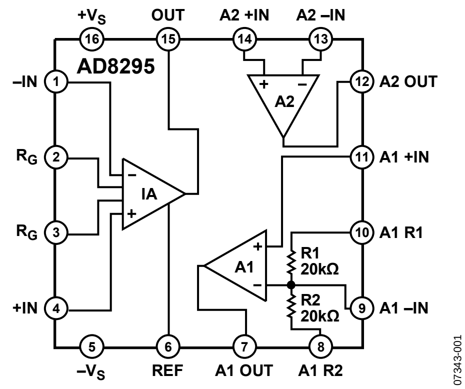

Figure 1.

Table 1. Instrumentation Amplifiers by Category[1]

General-Purpose	Zero Drift	Military Grade	Low Power	High Speed PGA
AD8220	AD8231	AD620	AD8236	AD8250
AD8221	AD8553	AD621	AD627	AD8251
AD8222	AD8555	AD524	AD623	AD8253
AD8224	AD8556	AD526	AD8223	
AD8228	AD8557	AD624	AD8226	
AD8295	AD8293		AD8227	

[1] See www.analog.com for the latest selection of instrumentation amplifiers.

GENERAL DESCRIPTION

The AD8295 contains all the components necessary for a precision instrumentation amplifier front end in one small 4 mm × 4 mm package. It contains a high performance instrumentation amplifier, two general-purpose operational amplifiers, and two precisely matched 20 kΩ resistors.

The AD8295 is designed to make PCB routing easy and efficient. The AD8295 components are arranged in a logical way so that typical application circuits have short routes and few vias. Unlike most chip scale packages, the AD8295 does not have an exposed metal pad on the back of the part, which frees additional space for routing and vias. The logical pin arrangement and routing freedom enable the AD8295 to offer simple pin-strapped solutions for complex systems in the equivalent board space of a typical MSOP package.

The AD8295 includes a high performance, programmable gain instrumentation amplifier. Gain is set from 1 to 1000 with a single resistor. The low noise and excellent common-mode rejection of the AD8295 enable the part to easily detect small signals even in the presence of large common-mode interference. For a similar instrumentation amplifier without the associated signal conditioning circuitry, see the AD8221 or AD8222 data sheet.

The AD8295 operates on both single and dual supplies and is well suited for applications where ±10 V input voltages are encountered. Performance is specified over the entire industrial temperature range of −40°C to +85°C for all grades. The AD8295 is operational from −40°C to +125°C; see the Typical Performance Characteristics section for expected operation up to 125°C.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

6/09—Rev. 0 to Rev. A

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Changes to Table 1 ... 1
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Added Figure 49 ... 17
Changes to Figure 51 and Figure 52 ... 17
Added Figure 53 and Figure 54 ... 18
Changes to Figure 59 ... 19
Added Routing and Vias Section ... 20
Updated Outline Dimensions ... 26

10/08—Revision 0: Initial Version

SPECIFICATIONS

INSTRUMENTATION AMPLIFIER SPECIFICATIONS, SINGLE-ENDED AND DIFFERENTIAL OUTPUT CONFIGURATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted. The differential configuration is shown in Figure 65.

Table 2.

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = −10 V to +10 V							
CMRR, DC to 60 Hz	1 kΩ source imbalance							
G = 1		80			90			dB
G = 10		100			110			dB
G = 100		120			130			dB
G = 1000		130			140			dB
CMRR at 8 kHz								
G = 1		80			80			dB
G = 10		90			100			dB
G = 100		100			120			dB
G = 1000		110			120			dB
NOISE								
Voltage Noise, 1 kHz	RTI noise = $\sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0 V			8			8	nV/√Hz
Output Voltage Noise, e_{NO}	V_{IN+}, V_{IN-}, V_{REF} = 0 V			75			75	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2		μV p-p
G = 10			0.5			0.5		μV p-p
G = 100 to 1000			0.25			0.25		μV p-p
Current Noise	f = 1 kHz		40			40		fA/√Hz
	f = 0.1 Hz to 10 Hz		6			6		pA p-p
VOLTAGE OFFSET	RTI V_{OS} = V_{OSI} + (V_{OSO}/G)							
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			120			60	μV
Over Temperature	T_A = −40°C to +85°C			150			80	μV
Average TC				0.4			0.3	μV/°C
Output Offset Voltage, V_{OSO}	V_S = ±5 V to ±15 V			500			350	μV
Over Temperature	T_A = −40°C to +85°C			0.8			0.5	mV
Average TC				9			5	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.3 V to ±18 V							
G = 1		90	110		94	110		dB
G = 10		110	120		114	130		dB
G = 100		124	130		130	140		dB
G = 1000		130	140		140	150		dB
INPUT CURRENT								
Input Bias Current			0.5	2.0		0.2	0.8	nA
Over Temperature	T_A = −40°C to +85°C			3.0			1.5	nA
Average TC			1			1		pA/°C
Input Offset Current			0.2	1		0.1	0.5	nA
Over Temperature	T_A = −40°C to +85°C			1.5			0.6	nA
Average TC			1			0.5	2	pA/°C

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
GAIN	G = 1 + (49.4 kΩ/R_G)							
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} ± 10 V							
G = 1				0.05			0.02	%
G = 10				0.3			0.1	%
G = 100				0.3			0.1	%
G = 1000				0.3			0.1	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1			3	10		1	5	ppm
G = 10			7	20		7	20	ppm
G = 100			7	20		7	20	ppm
Gain vs. Temperature								
G = 1				5			1	ppm/°C
G > 1				−50			−50	ppm/°C
DYNAMIC RESPONSE (SINGLE-ENDED CONFIGURATION)								
Small Signal −3 dB Bandwidth								
G = 1			1200			1200		kHz
G = 10			750			750		kHz
G = 100			140			140		kHz
G = 1000			15			15		kHz
Settling Time 0.01%	10 V step							
G = 1 to 100			10			10		µs
G = 1000			80			80		µs
Settling Time 0.001%	10 V step							
G = 1 to 100			13			13		µs
G = 1000			110			110		µs
Slew Rate								
G = 1		1.5	2		1.5	2		V/µs
G = 5 to 1000		2	2.5		2	2.5		V/µs
DYNAMIC RESPONSE (DIFFERENTIAL OUTPUT CONFIGURATION)								
Small Signal −3 dB Bandwidth								
G = 1			1200			1200		kHz
G = 10			1000			1000		kHz
G = 100			140			140		kHz
G = 1000			15			15		kHz
Settling Time 0.01%	10 V step							
G = 1 to 100			10			10		µs
G = 1000			80			80		µs
Settling Time 0.001%	10 V step							
G = 1 to 100			13			13		µs
G = 1000			110			110		µs
Slew Rate								
G = 1		1.5	2		1.5	2		V/µs
G = 5 to 1000		2	2.5		2	2.5		V/µs
REFERENCE INPUT								
R_{IN}			20			20		kΩ
I_{IN}	V_{IN+}, V_{IN-}, V_{REF} = 0 V		50	60		50	60	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Gain to Output		1 ± 0.0001			1 ± 0.0001			V/V

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
INPUT								
Input Impedance								
Differential			100‖2			100‖2		GΩ‖pF
Common Mode			100‖2			100‖2		GΩ‖pF
Input Operating Voltage Range[1]	V_S = ±2.3 V to ±5 V	$-V_S + 1.9$		$+V_S - 1.1$	$-V_S + 1.9$		$+V_S - 1.1$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 2.0$		$+V_S - 1.2$	$-V_S + 2.0$		$+V_S - 1.2$	V
Input Operating Voltage Range[1]	V_S = ±5 V to ±18 V	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 2.0$		$+V_S - 1.2$	$-V_S + 2.0$		$+V_S - 1.2$	V
OUTPUT	R_L = 10 kΩ							
Output Swing	V_S = ±2.3 V to ±5 V	$-V_S + 1.1$		$+V_S - 1.2$	$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 1.4$		$+V_S - 1.3$	$-V_S + 1.4$		$+V_S - 1.3$	V
Output Swing	V_S = ±5 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.4$	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 1.6$		$+V_S - 1.5$	$-V_S + 1.6$		$+V_S - 1.5$	V
Short-Circuit Current			18			18		mA

[1] One input grounded; G = 1.

OP AMP SPECIFICATIONS

V_S = ±15 V, T_A = 25°C, R_L = 2 kΩ, unless otherwise noted.

Table 3.

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
INPUT CHARACTERISTICS								
Offset Voltage, V_{OS}			40	150		20	100	µV
Average TC	T_A = −40°C to +85°C			5			5	µV/°C
Input Bias Current[1]			6	10		6	10	nA
	T_A = −40°C		10	13		10	13	nA
	T_A = +85°C		4	8		4	8	nA
Input Offset Current				0.6			0.6	nA
Over Temperature	T_A = −40°C to +85°C			0.6			0.6	nA
Input Voltage Range		$-V_S + 1.2$		$+V_S - 1.2$	$-V_S + 1.2$		$+V_S - 1.2$	V
Open-Loop Gain		100	125		116	125		dB
Common-Mode Rejection Ratio (CMRR)		100			100			dB
Power Supply Rejection Ratio (PSRR)		90	110		94	110		dB
Voltage Noise Density			40			40		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		2.2			2.2		µV p-p
DYNAMIC PERFORMANCE								
Gain Bandwidth Product			1			1		MHz
Slew Rate		2	2.6		2	2.6		V/µs
OUTPUT CHARACTERISTICS								
Output Swing	V_S = ±2.3 V to ±5 V	$-V_S + 1.1$		$+V_S - 1.2$	$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 1.4$		$+V_S - 1.3$	$-V_S + 1.4$		$+V_S - 1.3$	V
Output Swing	V_S = ±5 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.4$	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 1.6$		$+V_S - 1.5$	$-V_S + 1.6$		$+V_S - 1.5$	V
Short-Circuit Current			18			18		mA

[1] Op amp uses an npn input stage, so input bias current always flows into the inputs.

INTERNAL RESISTOR NETWORK

When used with internal Op Amp A1, T_A = 25°C, unless otherwise noted. Use in external op amp feedback loops is not recommended.

Table 4.

		A Grade			B Grade			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Nominal Resistor Value			20			20		kΩ
Resistor Matching				0.1			0.03	%
Matching Temperature Coefficient	T_A = −40°C to +85°C			5			1	ppm/°C
Absolute Resistor Accuracy				0.2			0.1	%
Absolute Temperature Coefficient	T_A = −40°C to +85°C			−50			−50	ppm/°C

POWER AND TEMPERATURE SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, unless otherwise noted.

Table 5.

		A Grade			B Grade			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY								
Operating Range		±2.3		±18	±2.3		±18	V
Quiescent Current	In-amp + two op amps		2	2.3		2	2.3	mA
Over Temperature	T_A = −40°C to +85°C			2.5			2.5	mA
TEMPERATURE RANGE								
Specified Performance		−40		+85	−40		+85	°C
Operational Performance[1]		−40		+125	−40		+125	°C

[1] See the Typical Performance Characteristics section for expected operation from 85°C to 125°C.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current	Indefinite
Input Voltage	
Common-Mode	$\pm V_S$
Differential	$\pm V_S$
Storage Temperature Range	−65°C to +130°C
Operating Temperature Range[1]	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	130°C
ESD (Human Body Model)	2000 V
ESD (Charged Device Model)	500 V
ESD (Machine Model)	200 V

[1] Temperature range for specified performance is −40°C to +85°C. See the Typical Performance Characteristics section for expected operation from 85°C to 125°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Specifications are provided for a device in free air.

Table 7.

Package	θ_{JA}	Unit
16-Lead LFCSP_VQ	86	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

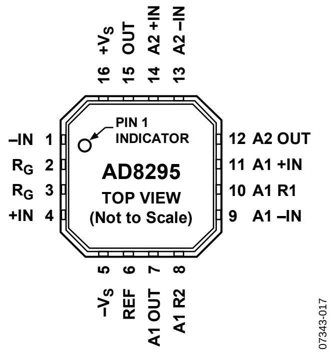

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	In-Amp Negative Input.
2, 3	R_G	In-Amp Gain-Setting Resistor Terminals.
4	+IN	In-Amp Positive Input.
5	$-V_S$	Negative Supply.
6	REF	In-Amp Reference Terminal. Drive with a low impedance source. Output is referred to this pin.
7	A1 OUT	Op Amp A1 Output.
8	A1 R2	Resistor R2 Terminal. Connected internally to Op Amp A1 inverting input.
9	A1 –IN	Op Amp A1 Inverting Input. Midpoint of resistor divider.
10	A1 R1	Resistor R1 Terminal. Connected internally to Op Amp A1 inverting input.
11	A1 +IN	Op Amp A1 Noninverting Input.
12	A2 OUT	Op Amp A2 Output.
13	A2 –IN	Op Amp A2 Inverting Input.
14	A2 +IN	Op Amp A2 Noninverting Input.
15	OUT	In-Amp Output.
16	$+V_S$	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

IN-AMP

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, R_L = 10 kΩ, unless otherwise noted.

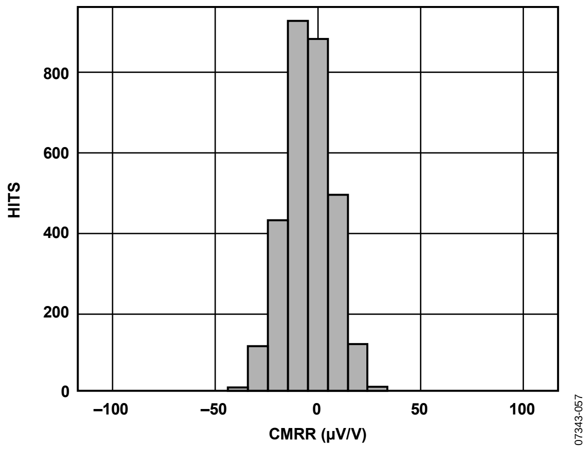

Figure 3. Typical Distribution for CMRR, G = 1

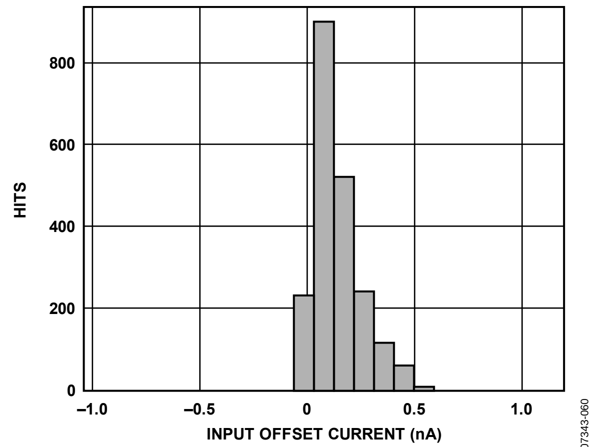

Figure 6. Typical Distribution of Input Offset Current

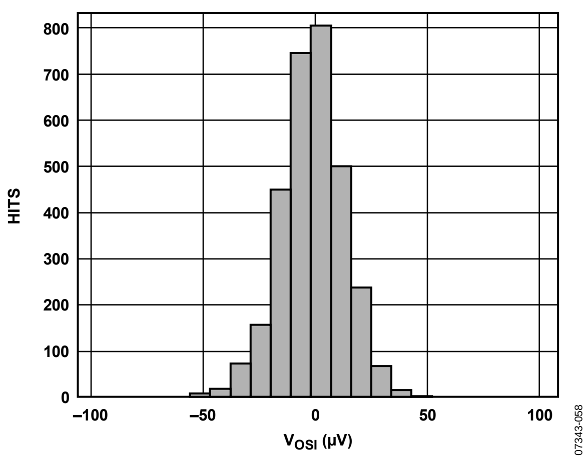

Figure 4. Typical Distribution of Input Offset Voltage

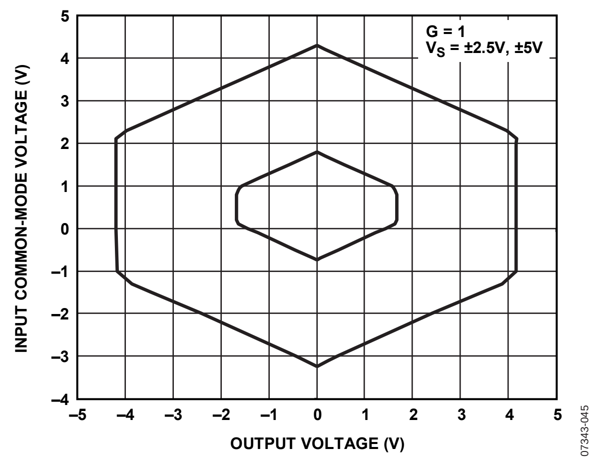

Figure 7. Input Common-Mode Voltage Range vs. Output Voltage, G = 1, V_S = ±2.5 V, ±5 V, V_{REF} = 0 V

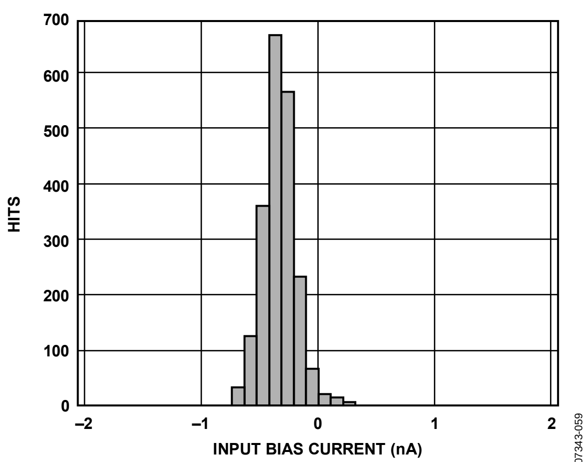

Figure 5. Typical Distribution of Input Bias Current

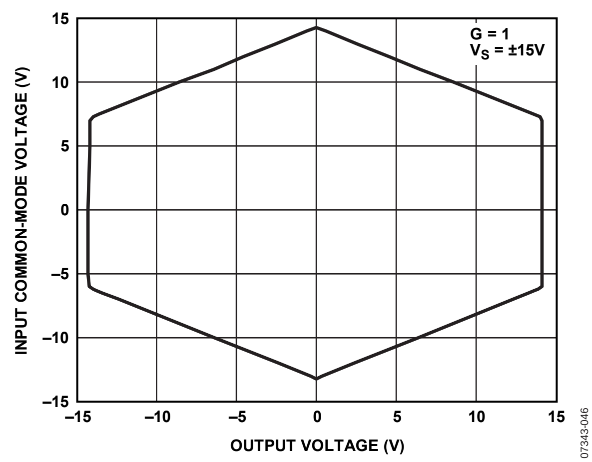

Figure 8. Input Common-Mode Voltage Range vs. Output Voltage, G = 1, V_S = ±15 V, V_{REF} = 0 V

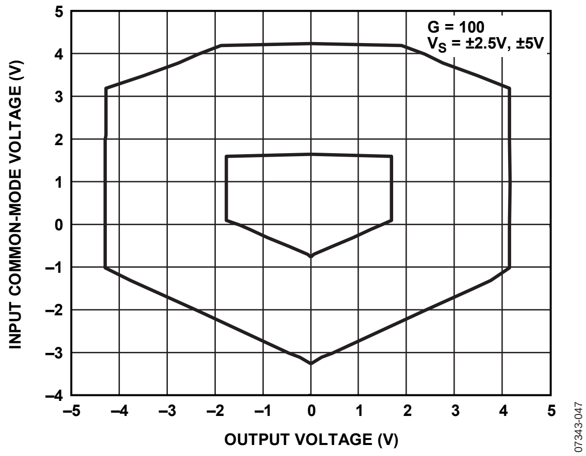

Figure 9. Input Common-Mode Voltage Range vs. Output Voltage, G = 100, V_S = ±2.5 V, ±5 V, V_{REF} = 0 V

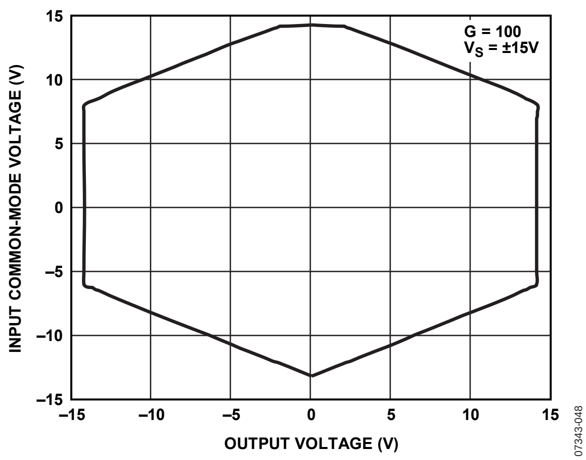

Figure 10. Input Common-Mode Voltage Range vs. Output Voltage, G = 100, V_S = ±15 V, V_{REF} = 0 V

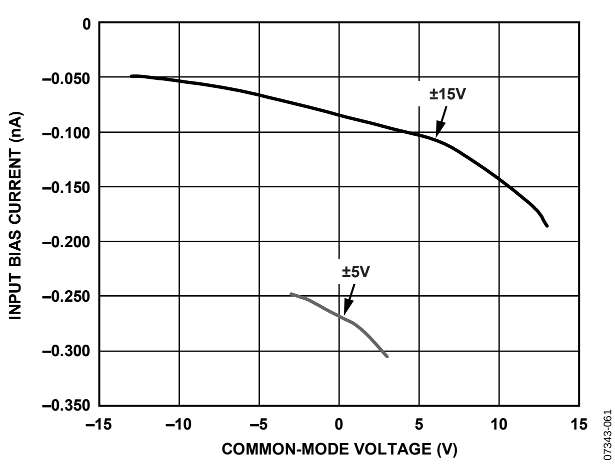

Figure 11. Input Bias Current vs. Common-Mode Voltage

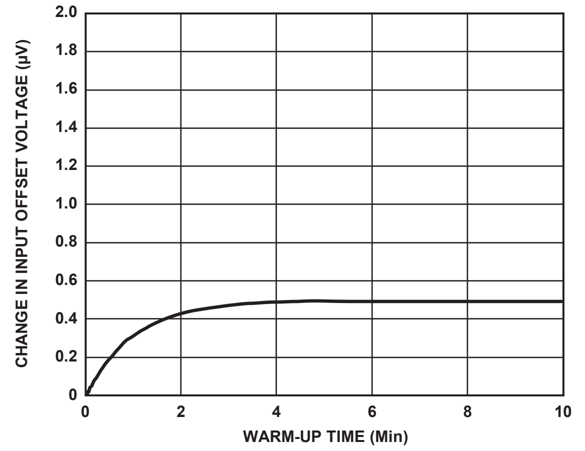

Figure 12. Change in Input Offset Voltage vs. Warm-Up Time

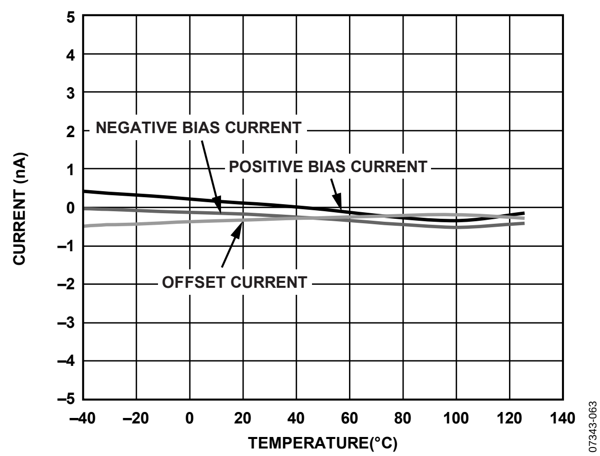

Figure 13. Input Bias Current and Input Offset Current vs. Temperature

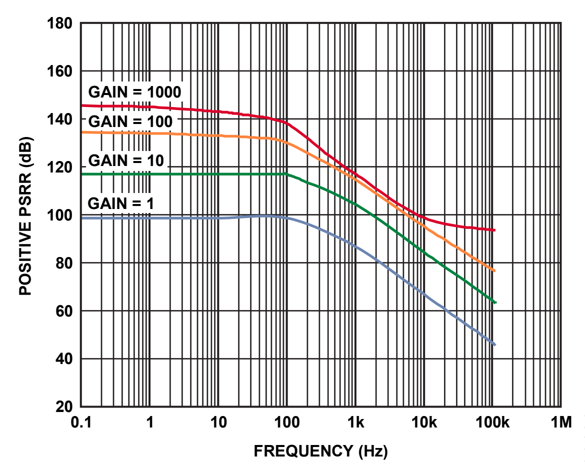

Figure 14. Positive PSRR vs. Frequency, RTI, G = 1 to 1000

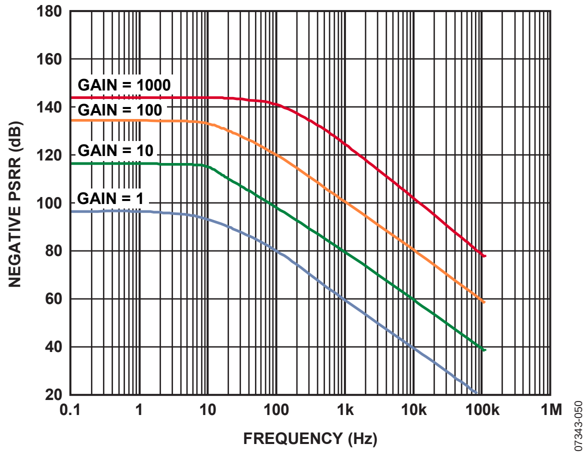

Figure 15. Negative PSRR vs. Frequency, RTI, G = 1 to 1000

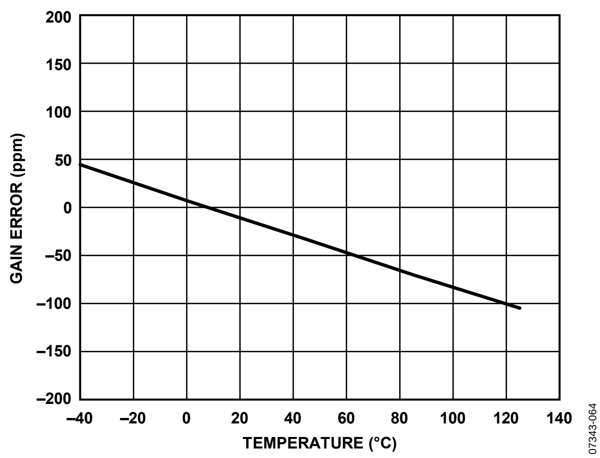

Figure 16. Gain Error vs. Temperature, G = 1

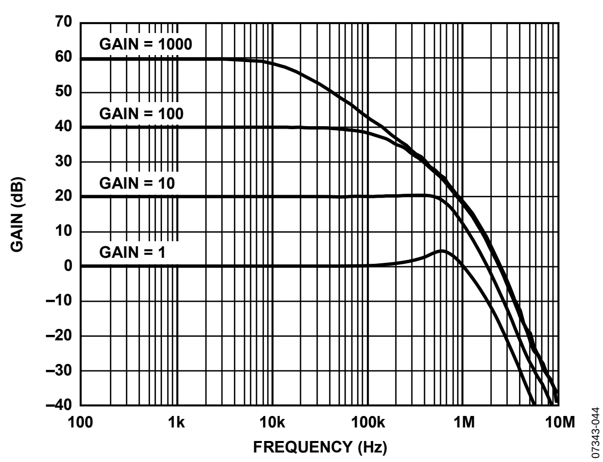

Figure 17. Gain vs. Frequency, G = 1 to 1000

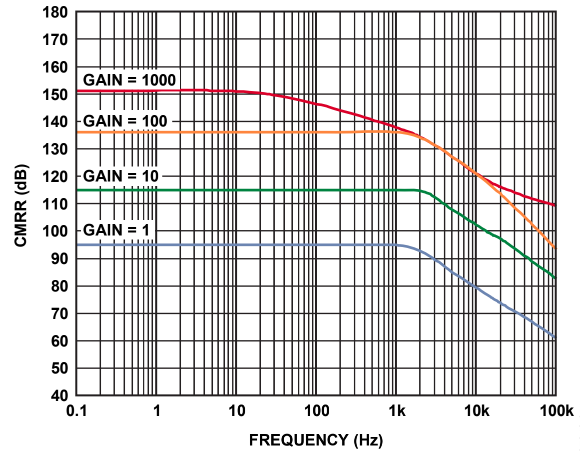

Figure 18. CMRR vs. Frequency, RTI, G = 1 to 1000

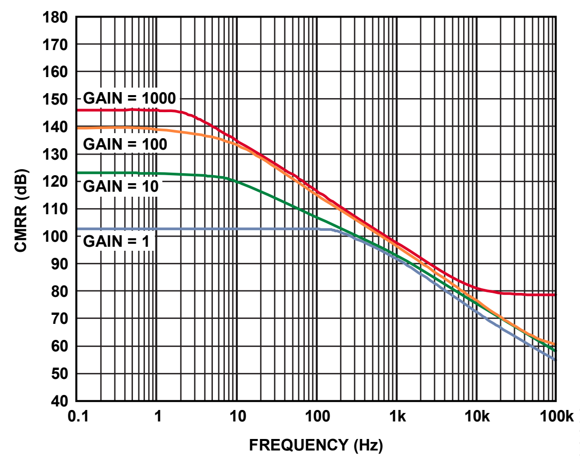

Figure 19. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance, G = 1 to 1000

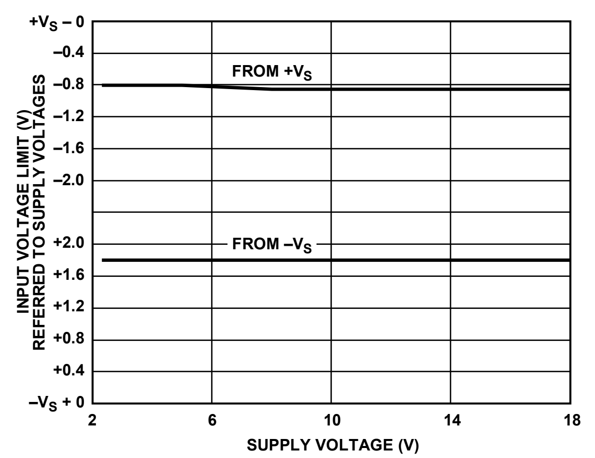

Figure 20. Input Voltage Limit vs. Supply Voltage, G = 1

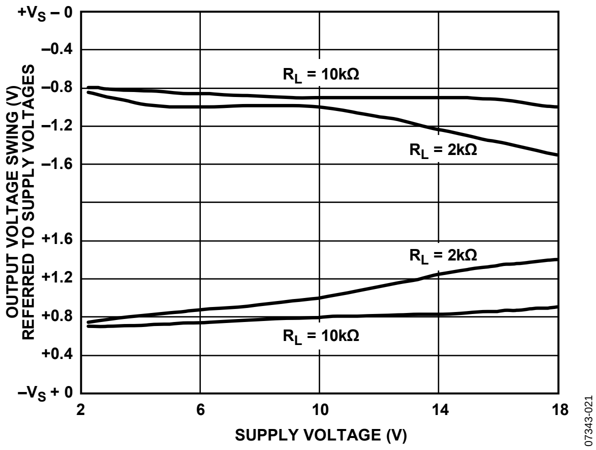

Figure 21. Output Voltage Swing vs. Supply Voltage, G = 1

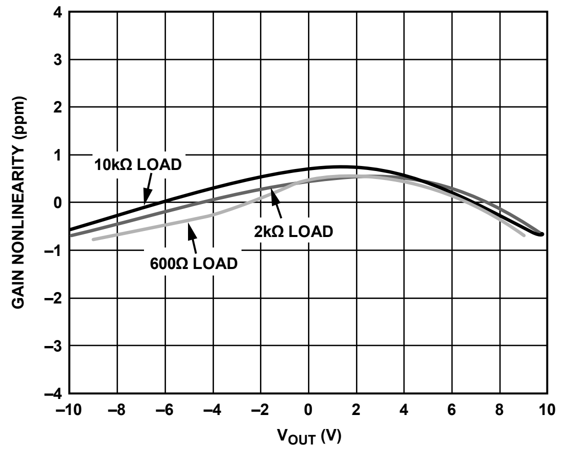

Figure 24. Gain Nonlinearity, G = 1

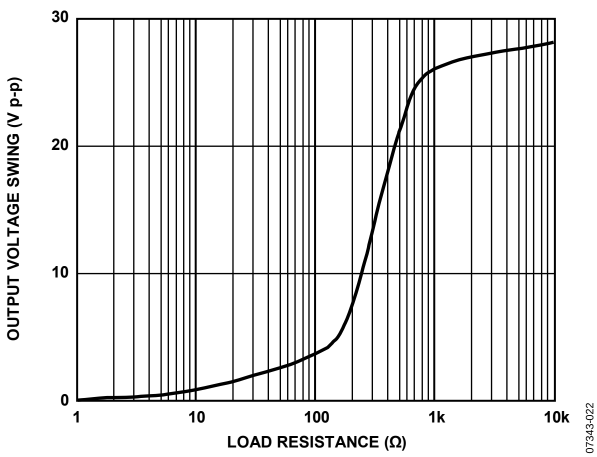

Figure 22. Output Voltage Swing vs. Load Resistance

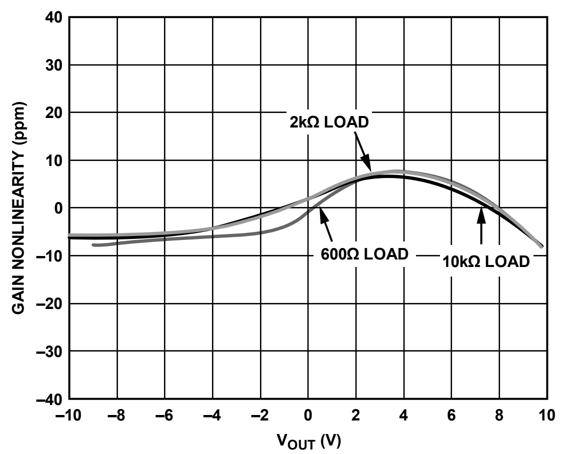

Figure 25. Gain Nonlinearity, G = 100

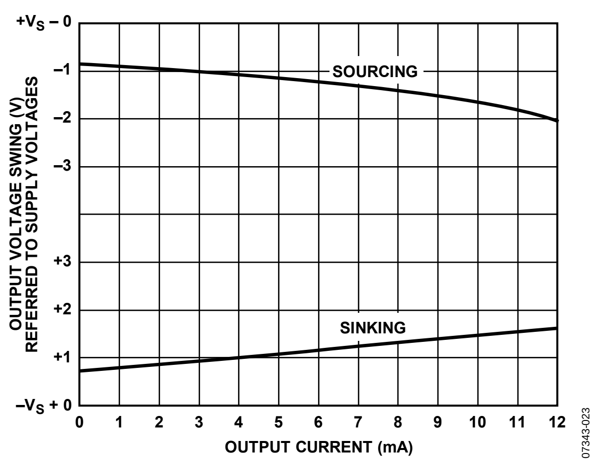

Figure 23. Output Voltage Swing vs. Output Current, G = 1

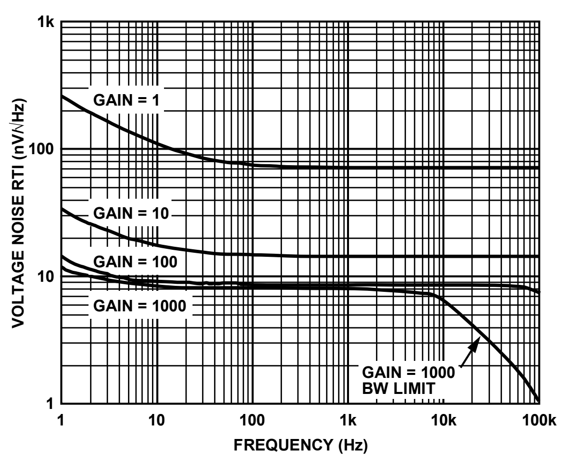

Figure 26. Voltage Noise Spectral Density vs. Frequency, G = 1 to 1000

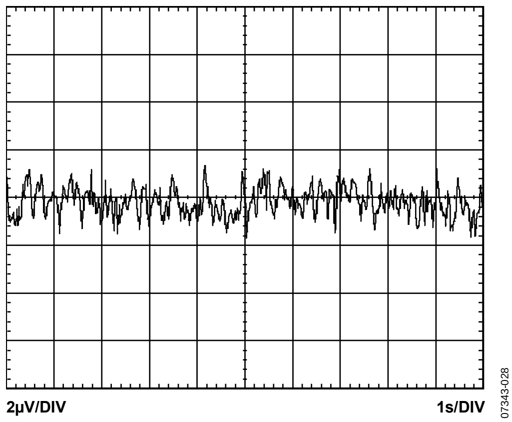

Figure 27. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1

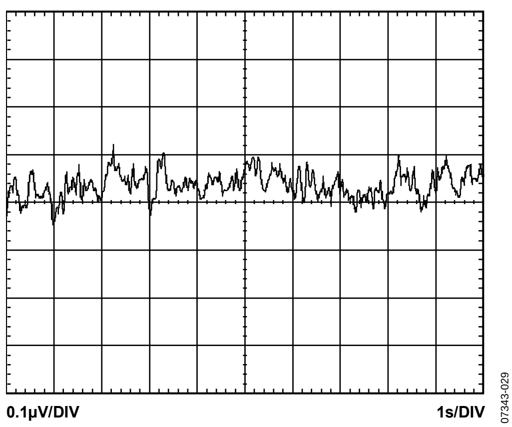

Figure 28. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1000

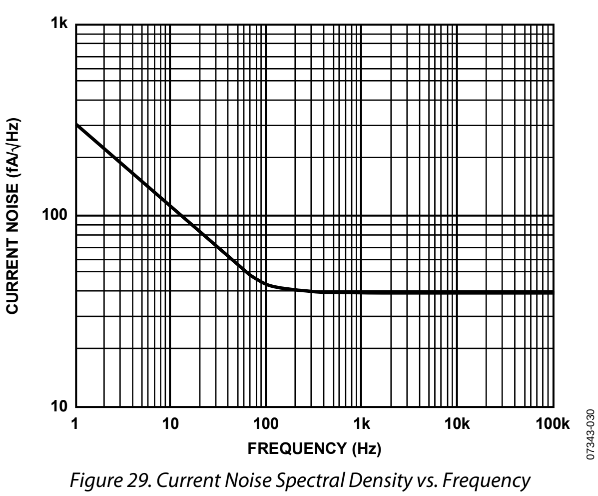

Figure 29. Current Noise Spectral Density vs. Frequency

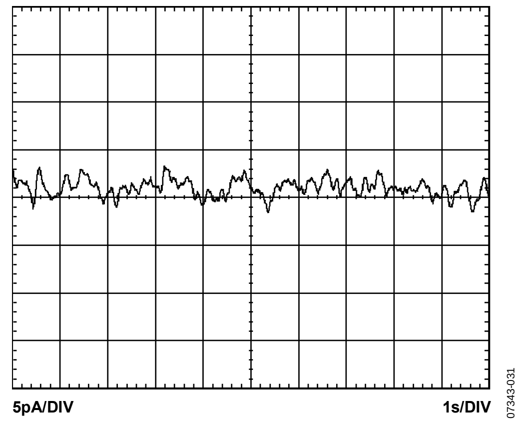

Figure 30. 0.1 Hz to 10 Hz Current Noise

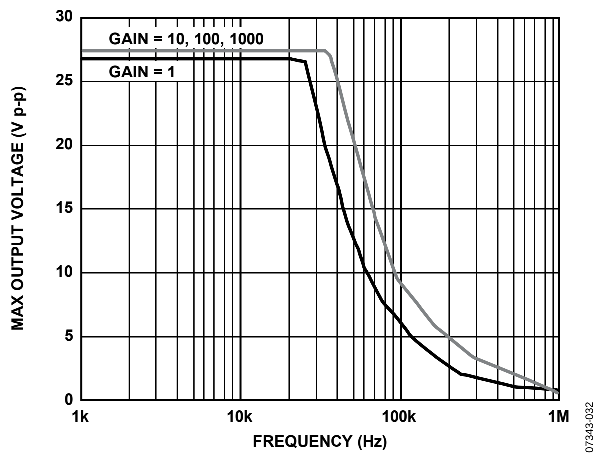

Figure 31. Large Signal Frequency Response

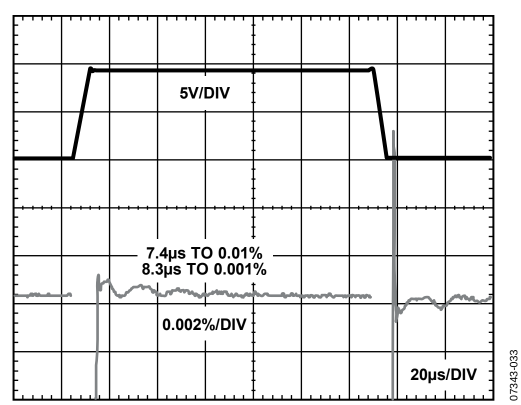

Figure 32. Large Signal Pulse Response and Settling Time, G = 1

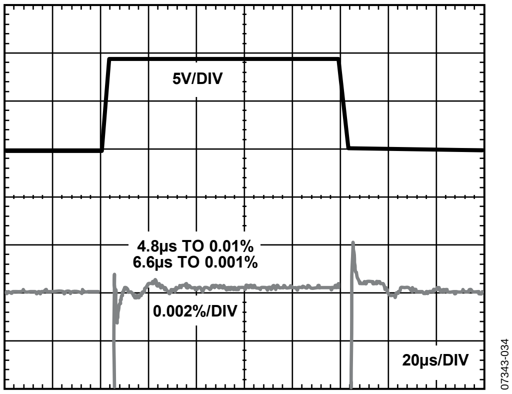

Figure 33. Large Signal Pulse Response and Settling Time, G = 10

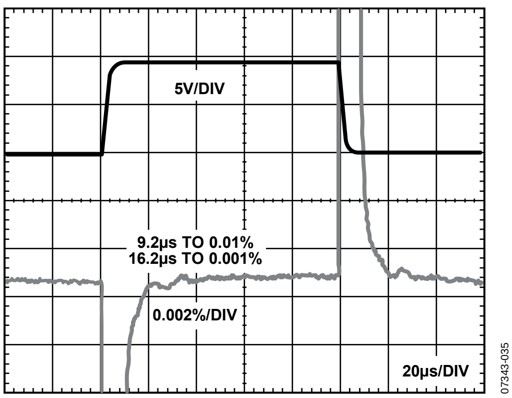

Figure 34. Large Signal Pulse Response and Settling Time, G = 100

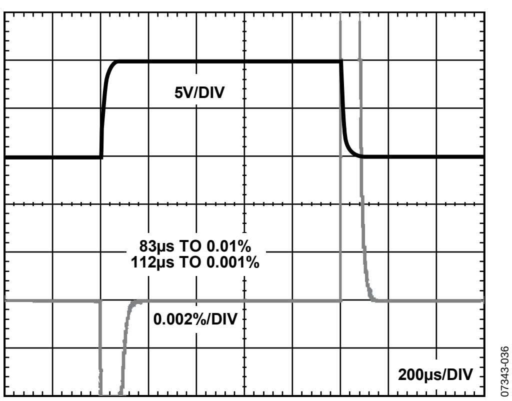

Figure 35. Large Signal Pulse Response and Settling Time, G = 1000

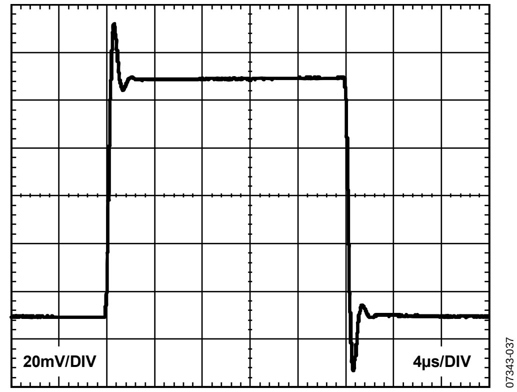

Figure 36. Small Signal Pulse Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

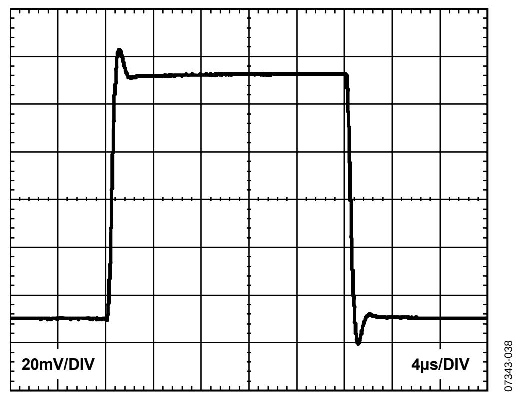

Figure 37. Small Signal Pulse Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

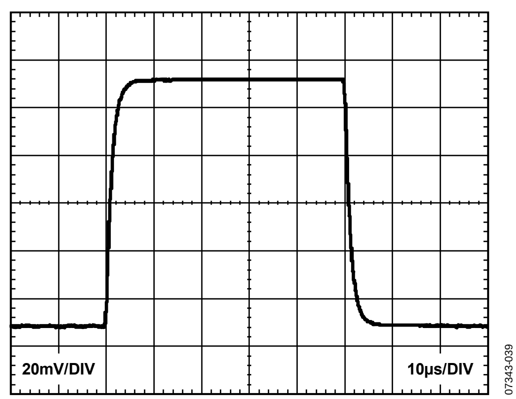

Figure 38. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

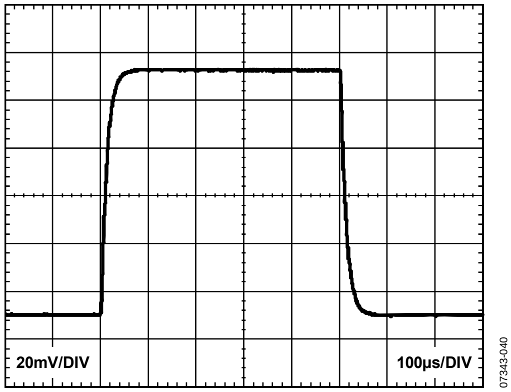

Figure 39. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

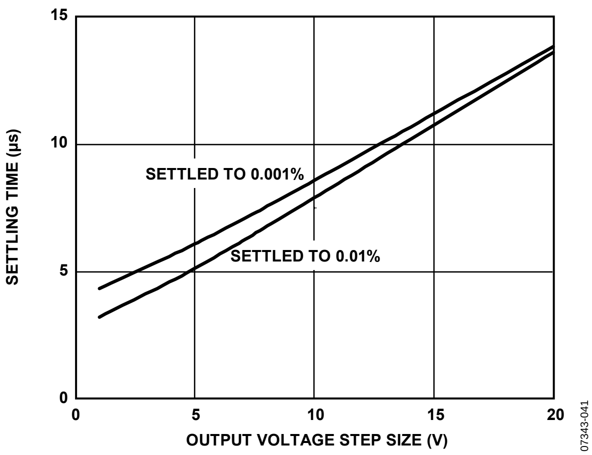

Figure 40. Settling Time vs. Output Voltage Step Size, G = 1

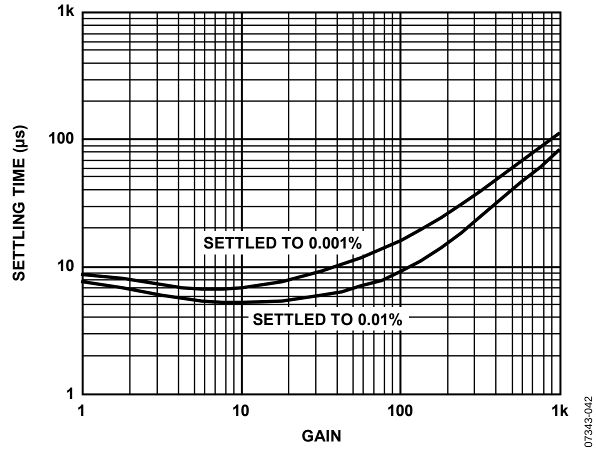

Figure 41. Settling Time vs. Gain for a 10 V Step

OP AMPS

$V_S = \pm15$ V, $T_A = 25°C$, $R_L = 10$ kΩ, Op Amp A1 and Op Amp A2, unless otherwise noted.

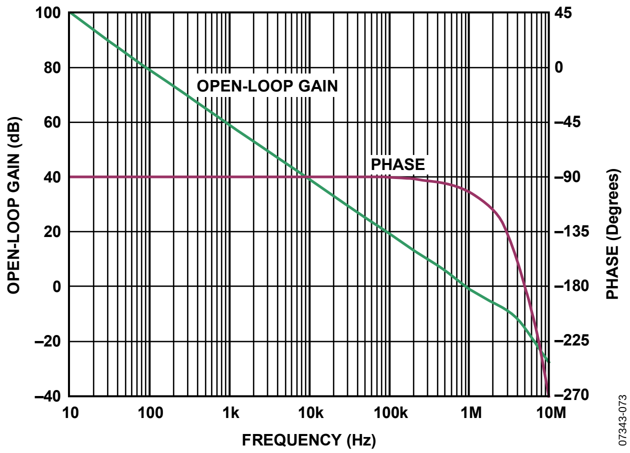

Figure 42. Open-Loop Gain and Phase vs. Frequency, $C_L = 5$ pF

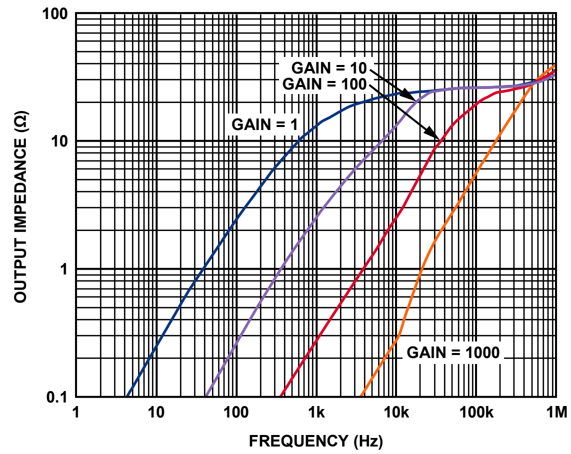

Figure 45. Output Impedance vs. Frequency, G = 1 to 1000

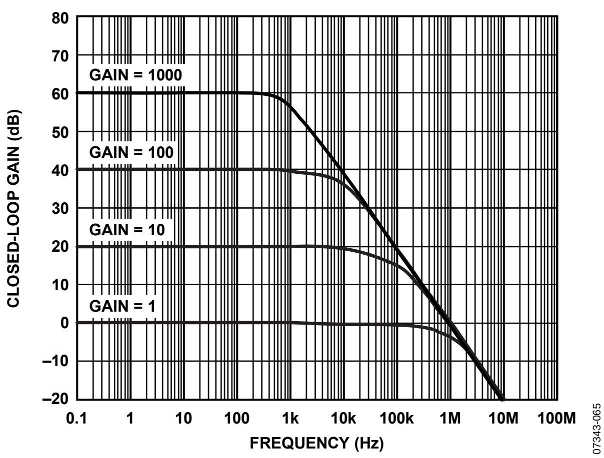

Figure 43. Closed-Loop Gain vs. Frequency, G = 1 to 1000

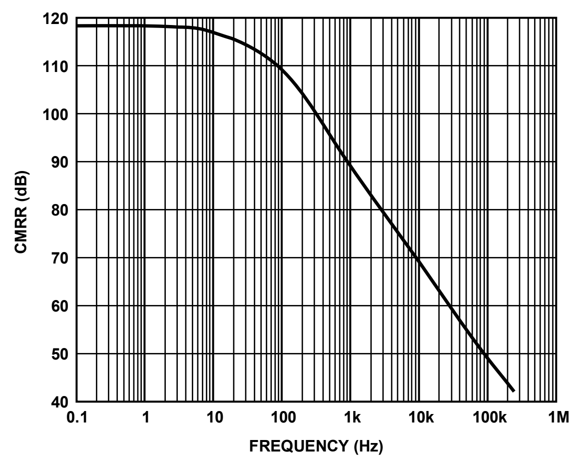

Figure 46. CMRR vs. Frequency

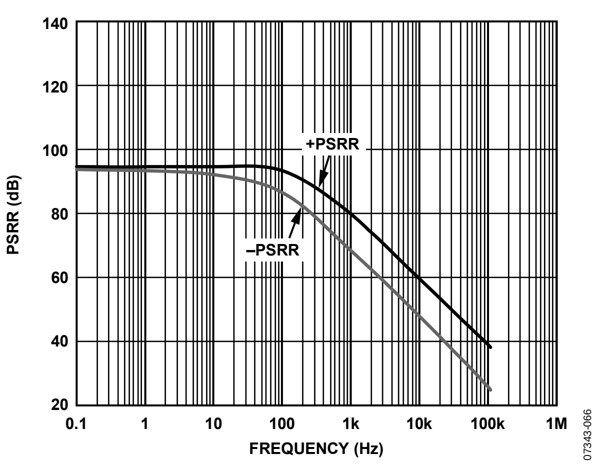

Figure 44. PSRR vs. Frequency

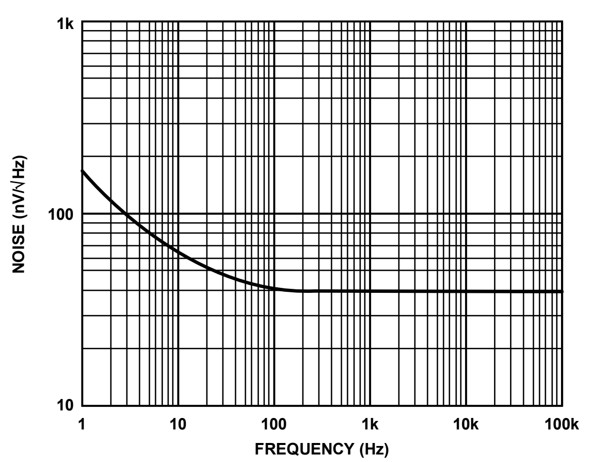

Figure 47. Voltage Noise Density vs. Frequency

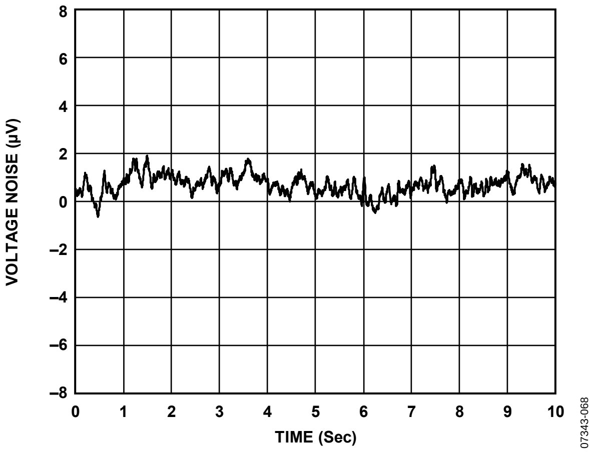

Figure 48. 0.1 Hz to 10 Hz Noise

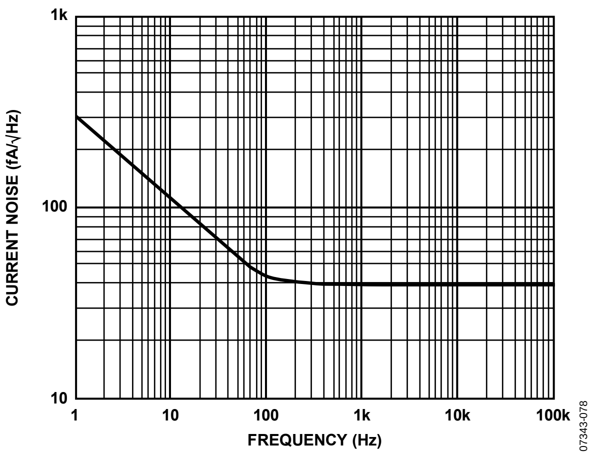

Figure 49. Current Noise Density vs. Frequency

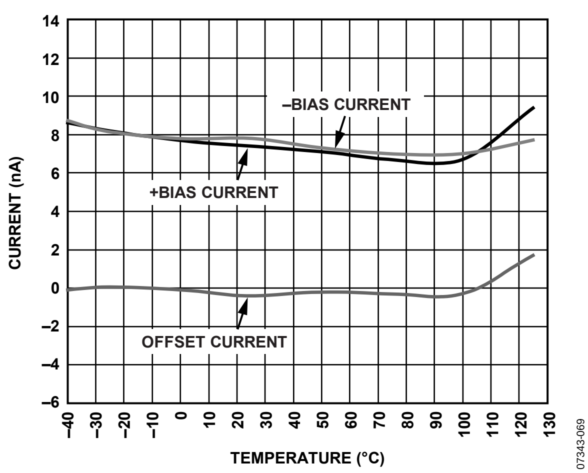

Figure 50. Input Bias Current and Input Offset Current vs. Temperature

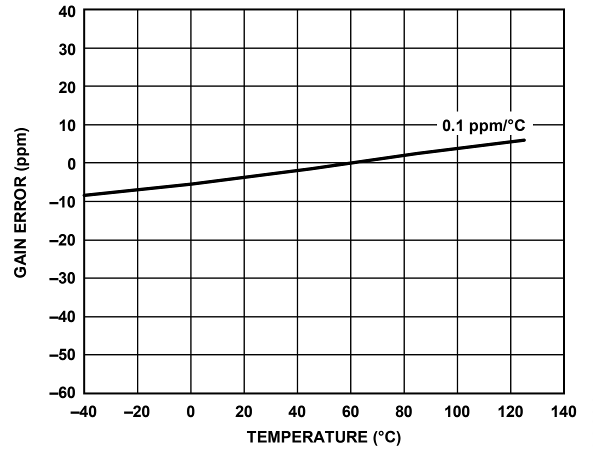

Figure 51. Gain Error vs. Temperature Using On-Chip Resistor Divider, G = −1

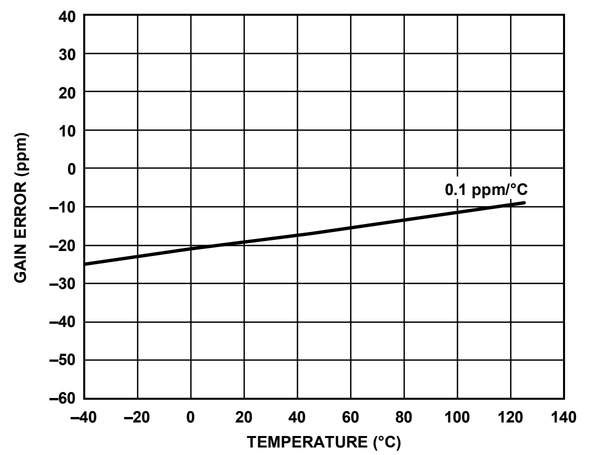

Figure 52. Gain Error vs. Temperature Using On-Chip Resistor Divider, G = 2

SYSTEM

$V_S = \pm 15$ V, $V_{REF} = 0$ V, $T_A = 25°C$, unless otherwise noted.

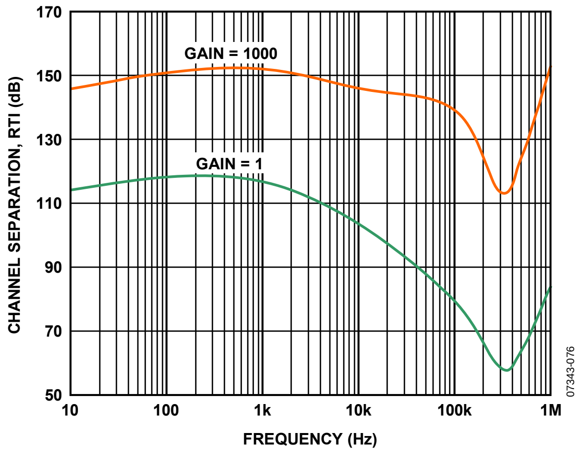

Figure 53. Channel Separation vs. Frequency (Source Channel: Op Amp with $R_L = 2$ kΩ; Receive Channel: In-Amp at G = 1 and G = 1000)

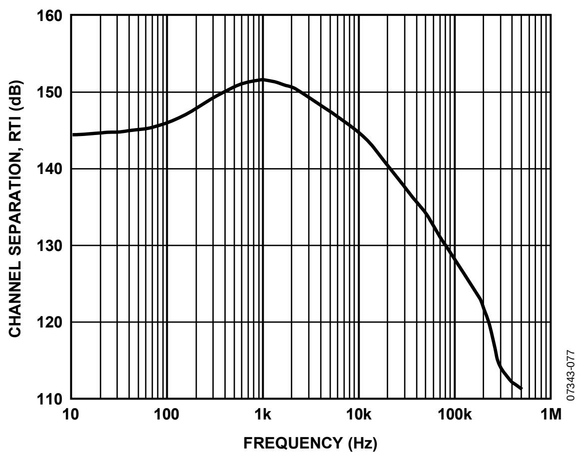

Figure 54. Channel Separation vs. Frequency (Source Channel: In-Amp with $R_L = 2$ kΩ, G = 1; Receive Channel: Op Amp at G = 1000)

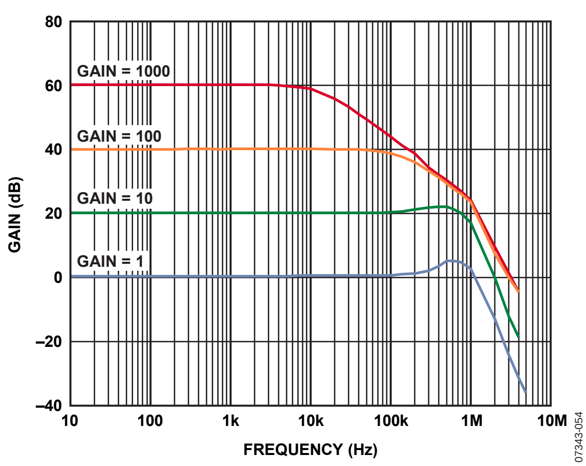

Figure 55. Differential Output Configuration, Gain vs. Frequency, G = 1 to 1000

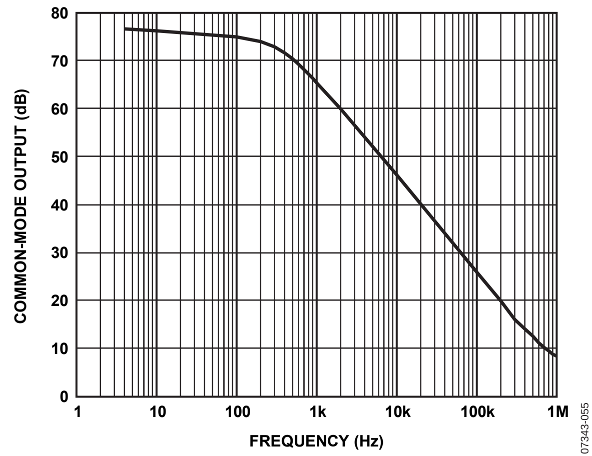

Figure 56. Differential Output Configuration, Common-Mode Output vs. Frequency

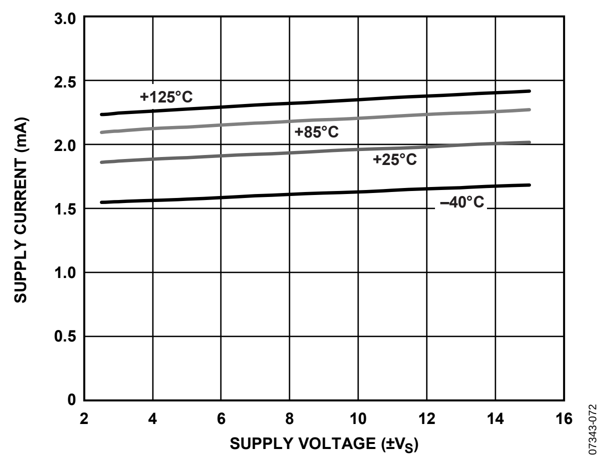

Figure 57. Supply Current vs. Supply Voltage

THEORY OF OPERATION

As shown in Figure 58, the AD8295 contains a precision instrumentation amplifier, two uncommitted op amps, and a precision resistor array. These components allow many common applications to be wired using simple pin-strapping, directly at the IC. This not only saves printed circuit board (PCB) space but also improves circuit performance because both temperature drift and resistor tolerance errors are reduced.

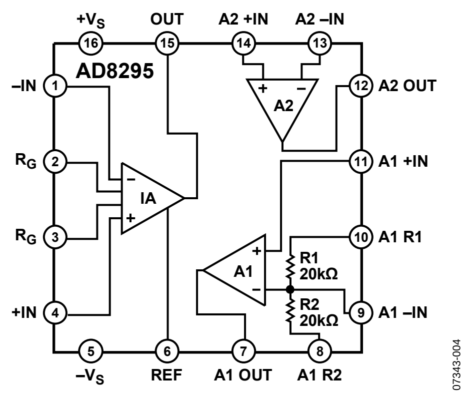

Figure 58. Functional Block Diagram

UNCOMMITTED OP AMPS

The AD8295 has two uncommitted op amps that can be used independently. These op amps allow simple pin-strapping for many common applications circuits.

Op Amp A1 has its inverting input connected to a precision 2:1 voltage divider resistor network. Because this network is internal to the IC, these resistors are closely matched and also track each other, with temperature variations. Op Amp A1 and the associated resistor network can be used to create either a noninverting gain stage of 2 or an inverting gain stage of −1 with excellent gain accuracy and gain drift.

Op Amp A2 is a more conventional op amp, with standard inverting and noninverting inputs and an output.

INSTRUMENTATION AMPLIFIER

Gain Selection

The transfer function of the AD8295 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

where placing a resistor across the R_G terminals sets the gain of the AD8295 according to the following equation:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

Resistor values can be obtained by referring to Table 9 or by using the following gain equation:

$$R_G = \frac{49.4\ \text{k}\Omega}{G - 1}$$

Table 9. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G	Calculated Gain
49.9 kΩ	1.990
12.4 kΩ	4.984
5.49 kΩ	9.998
2.61 kΩ	19.93
1.00 kΩ	50.40
499 Ω	100
249 Ω	199.4
100 Ω	495
49.9 Ω	991

The AD8295 defaults to G = 1 when no gain resistor is used. Gain accuracy is a combination of both the R_G accuracy and the accuracy listed in the specifications in Table 2, including accuracy over temperature. Gain error and gain drift are kept to a minimum when the gain resistor is not used.

Common-Mode Input Voltage Range

The AD8295 in-amp architecture applies gain internally and then removes the common-mode voltage. Therefore, internal nodes in the AD8295 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. Figure 7 through Figure 10 show the allowable common-mode input voltage ranges for various output voltages and supply voltages.

If Figure 7 through Figure 10 indicate that internal voltage limiting may be an issue, the common-mode range can be significantly improved by lowering the gain in the instrumentation amplifier by one half and applying a second G = 2 stage. Figure 59 shows how to do this amplification with the internal circuitry of the AD8295, requiring no additional external components.

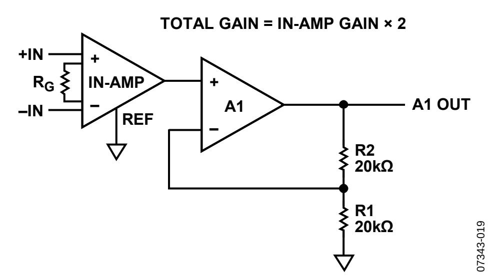

Figure 59. Applying Gain in a Later Stage Allows Wider Input Common-Mode Range

Reference Terminal

The output voltage of the AD8295 instrumentation amplifier is developed with respect to the potential on the reference terminal (REF). This is useful when the output signal needs to be offset to a precise dc level.

The reference pin input can be driven slightly beyond the rails. The REF pin is protected with ESD diodes, and the REF voltage should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, the source impedance to the REF terminal should be kept below 1 Ω. Additional impedance at the REF terminal can significantly degrade the CMRR of the amplifier. When the reference source has significant output impedance (for example, a resistive voltage divider), buffer the signal before driving the REF pin. Internal Op Amp A1 or A2 can be used for this purpose, as shown in Figure 60.

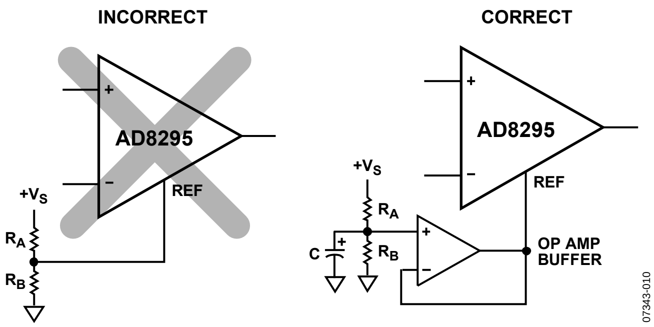

Figure 60. Driving the Reference Pin

Noise at the reference feeds directly to the output. Therefore, in Figure 60, Capacitor C is added to filter out any high frequency noise on the positive power supply line. For very clean supplies, the capacitor may not be needed. The filter frequency is a trade-off between noise rejection and start-up time, and is given by the following equation:

$$f_{LOW-PASS} = \frac{1}{2\pi C \dfrac{R_A R_B}{R_A + R_B}}$$

LAYOUT

The AD8295 is a high precision device. To ensure optimum performance at the PCB level, care must be taken in the board layout. The AD8295 pins are arranged in a logical manner to aid in this task.

Routing and Vias

Unlike most LFCSP packages, the AD8295 package was designed without the thermal pad to allow routes and vias directly beneath the chip. However, the manufacturing process leaves a very small section of exposed metal at each of the package corners. This metal is connected to $-V_S$ through the part. Because of the possibility of a short, vias should not be placed under this exposed metal.

Careful board layout maximizes system performance. Traces from the gain setting resistor to the R_G pins should be kept as short as possible to minimize parasitic inductance. To ensure the most accurate output, the trace from the REF pin should either be connected to the local ground of the AD8295 or to a voltage that is referenced to the local ground of the AD8295.

Common-Mode Rejection over Frequency

The AD8295 has a higher CMRR over frequency than typical in-amps, which gives it greater immunity to disturbances such as line noise and its associated harmonics. The AD8295 pinout and hidden paddle package were designed so that the board designer can take full advantage of this performance with a well-implemented layout.

Poor layout can cause some of the common-mode signal to be converted to a differential signal before it reaches the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR across frequency high, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs to minimize their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. The traces to the R_G resistor should be kept as short as possible. If the board design has a component at the gain setting pins (for example, a switch or jumper), the part should be chosen so that the parasitic capacitance is as small as possible.

Unused Op Amps

When not in use, the internal op amps should be connected in a unity-gain configuration, with the noninverting input connected to a bias point in the input range of the op amp. These connections ensure that the AD8295 op amp uses minimum power and does not disturb the internal power supplies of the AD8295. These connections are shown as dotted lines in several of the applications figures.

Reference

The output voltage of the instrumentation amplifier section of the AD8295 is developed with respect to the potential on the reference terminal (REF); care should be taken to tie the REF pin to the appropriate local ground (see Figure 61).

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 14 and Figure 15 for more information.

A 0.1 μF capacitor should be placed as close as possible to each supply pin. An additional capacitor, a 10 μF tantalum for the lower frequencies, can be used farther away from the IC. In most cases, the 10 μF bypass capacitor can be shared by other integrated circuits on the same PCB.

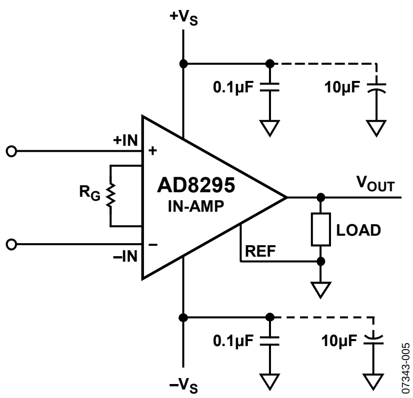

Figure 61. Supply Decoupling, REF, and Output Referred to Local Ground

INPUT PROTECTION

All terminals of the AD8295 are protected against ESD by diodes at the inputs. If voltages beyond the supplies are anticipated, resistors should be placed in series with the inputs to limit the current. Resistors should be chosen so that current does not exceed 6 mA into the internal ESD diodes in the overload condition. These resistors can be the same as those used for RFI protection. (See the RF Interference section for more information.)

For applications where the AD8295 encounters extreme overload voltages, as in cardiac defibrillators, external series resistors and low leakage diode clamps, such as BAV199Ls, FJH1100s, or SP720s can be used.

INPUT BIAS CURRENT RETURN PATH

The input bias currents of the AD8295 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 62. Otherwise, the input currents charge up the input capacitance until the in-amp is turned off or saturated.

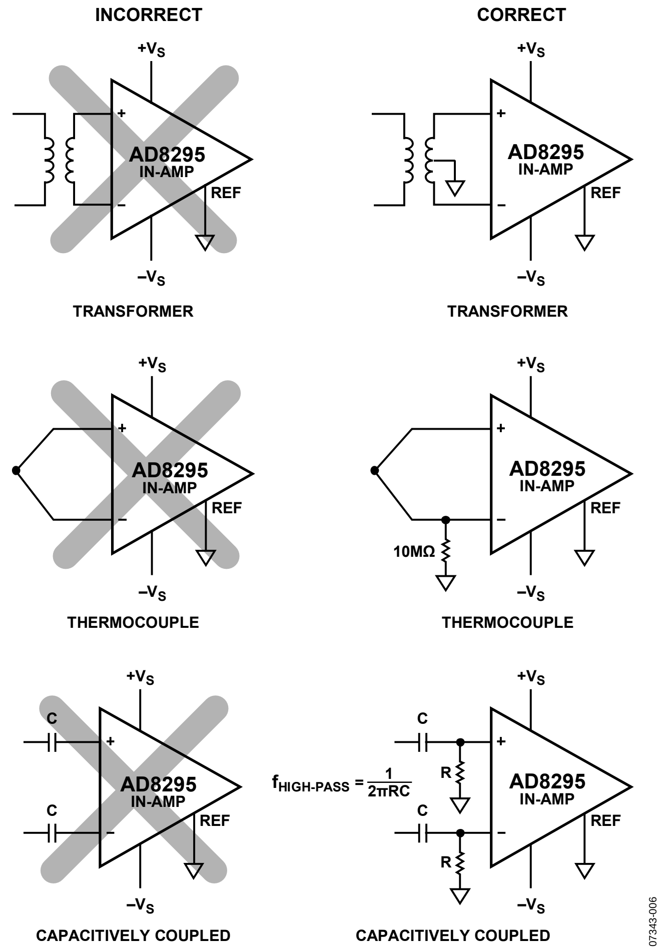

Figure 62. Creating an Input Bias Current Return Path

RF INTERFERENCE

RF interference is often a problem when amplifiers are used in applications where there are strong RF signals. The precision circuits in the AD8295 can rectify the RF signals so that they appear as a dc offset voltage error. To avoid this rectification, place a low-pass filter before the input. Figure 63 shows such a network in front of the instrumentation amplifier. The filter limits both the differential and common-mode bandwidth, as shown in the following equations:

$$f_{FILTER}(Diff) = \frac{1}{2\pi R(2C_D + C_C)}$$

$$f_{FILTER}(CM) = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

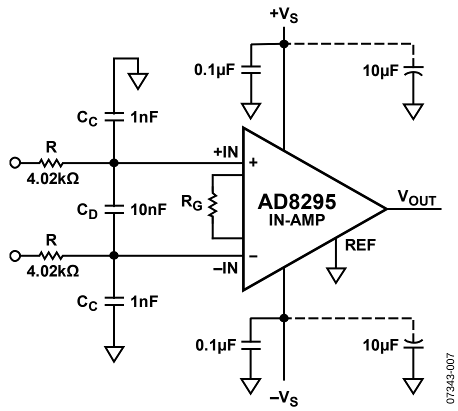

Figure 63. RFI Suppression

Lower cutoff frequencies improve RFI robustness. Accuracy of the C_C capacitors is important, because any mismatch between the R × C_C at the positive input and the R × C_C at the negative input degrades the CMRR of the AD8295. Keeping C_D at least 10 times larger than C_C is recommended.

DIFFERENTIAL OUTPUT

The AD8295 can be pin-strapped to provide a differential output; the simplified schematic is shown in Figure 64 and the full pin connection is shown in Figure 65. This configuration uses the instrumentation amplifier to maintain the differential voltage, while the op amp maintains the common-mode voltage. Because the in-amp precisely controls the output relative to its reference pin, this circuit has the same excellent dc performance as the single-ended output configuration. The transfer function for the differential and common-mode outputs are as follows:

$$V_{DIFF\_OUT} = V_{OUT+} - V_{OUT-} = G \times (V_{IN+} - V_{IN-})$$

$$V_{CM\_OUT} = (V_{OUT+} + V_{OUT-})/2 = V_{REF}$$

where:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

This configuration is fully specified (see Table 2, Figure 55, and Figure 56). DC performance is the same as for the single-ended configuration; ac performance is slightly different.

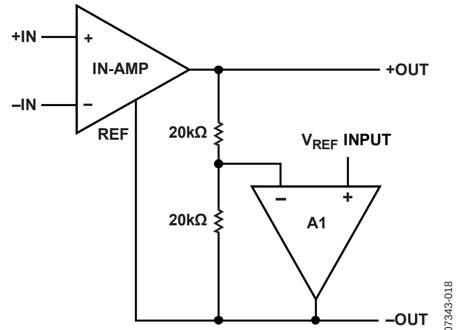

Figure 64. Differential Output Configuration Using an Op Amp

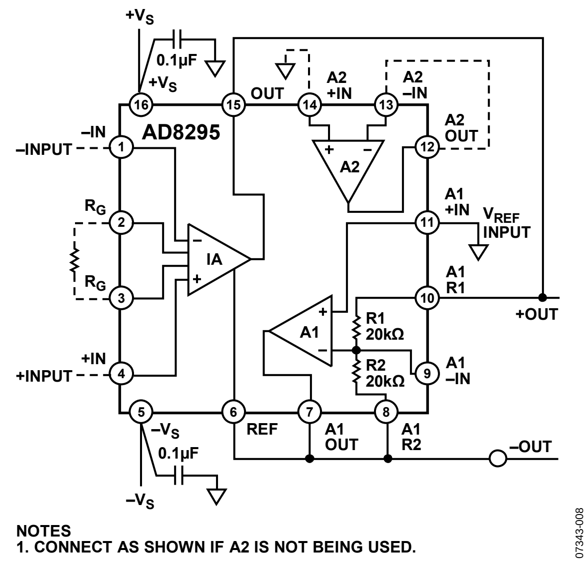

Figure 65. Minimum Component Connections for Differential Output

An alternative differential output configuration, which also requires no external components, is shown in Figure 66. Unlike the circuits shown in Figure 64 and Figure 65, this configuration uses an inverting op amp configuration to double the gain from the instrumentation amplifier. Because this configuration requires less gain from the instrumentation amplifier, it can have a wider frequency response and a wider input common-mode range vs. output voltage. However, because it does not take advantage of feedback at the reference pin of the instrumentation amplifier, dc performance includes the errors from the op amp and the resistor network. When using the internal precision components of the AD8295, these errors have a minimal effect on overall accuracy. This configuration is not specified in this data sheet.

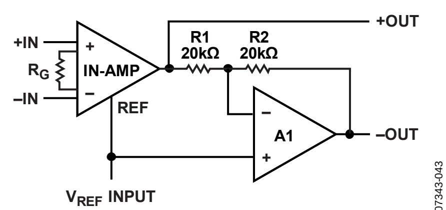

Figure 66. Alternative Differential Output Configuration

APPLICATIONS INFORMATION

CREATING A REFERENCE VOLTAGE AT MIDSCALE

A reference voltage other than ground is often useful, for example, when driving a single-supply ADC. Creating a reference voltage derived from a voltage divider is straightforward with the AD8295 (see Figure 67). In this configuration, Op Amp A2 is used to provide a buffered $V_S/2$ reference for the in-amp section. This configuration is very similar to the one described in the Reference Terminal section.

Note that the internal resistors of Op Amp A1 are not used to provide $V_S/2$. Instead, external 1% (or better) resistors are used. Because the negative input of Op Amp A1 is permanently connected to the junction of internal resistors R1 and R2, Op Amp A1 operates as a low voltage clamp, preventing the resistor string from providing a convenient $V_S/2$ voltage.

Noise at the reference feeds directly to the output, so if the reference voltage is derived from a noisy source, filtering is required. In Figure 67, Capacitor C1 has been added to filter out high frequency noise on the positive power supply line. The 10 µF capacitor and the 100 kΩ resistors shown in Figure 67 roll off noise starting at 0.3 Hz. The filter frequency is a trade-off between noise rejection and start-up time.

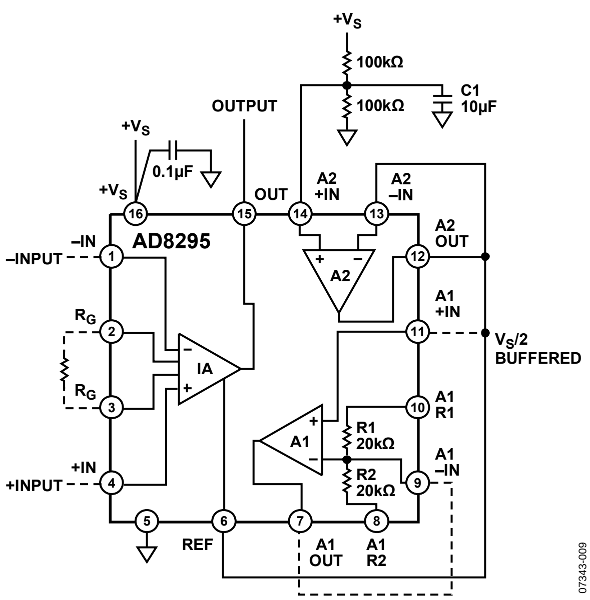

Figure 67. Single-Supply Connection with Buffered Reference

HIGH ACCURACY G = −1 CONFIGURATION WITH LOW-PASS FILTER

The circuit in Figure 68 uses Op Amp A1 and the resistor string to provide a precise G = −1 configuration. Because no external resistors are used to set the gain, gain accuracy and gain drift depend only on the internally matched resistors, yielding excellent performance.

Adding a capacitor across Resistor R2 is a simple way to provide a single-pole low-pass filter that rolls off at 20 dB per decade. This capacitor is shown as C1 in Figure 68.

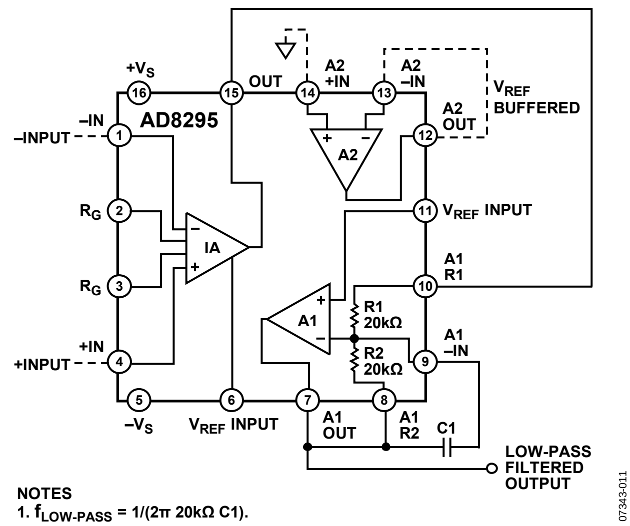

Figure 68. Single-Pole Output Filter Using a Single External Capacitor

If the connections to Pin 10 and Pin 11 in Figure 68 are changed so that Pin 10 connects to ground and Pin 11 connects to the in-amp output, the result is a G = 2 circuit, also with excellent gain accuracy and drift. In the G = 2 configuration, Capacitor C1 lowers the gain from 2 to 1 at higher frequencies.

TWO-POLE SALLEN-KEY FILTER

Figure 69 shows the in-amp output section of the AD8295 being low-pass filtered using a two-pole Sallen-Key filter. The filter section consists of Op Amp A2, External Resistors R1 and R2, as well as Capacitors C1 and C2. Resistor R3 compensates for input offset current errors and is equal to the parallel combination of R1 and R2. The ratio of capacitance between C1 and C2 sets the filter quality factor, Q. For most applications, a filter Q of 0.5 to 0.7 provides a good trade-off between performance and stability. High Q, nonpolarized capacitors, such as NPO ceramic, should be used. The exact pole frequencies are dependent on the tolerance of the resistors and capacitors used.

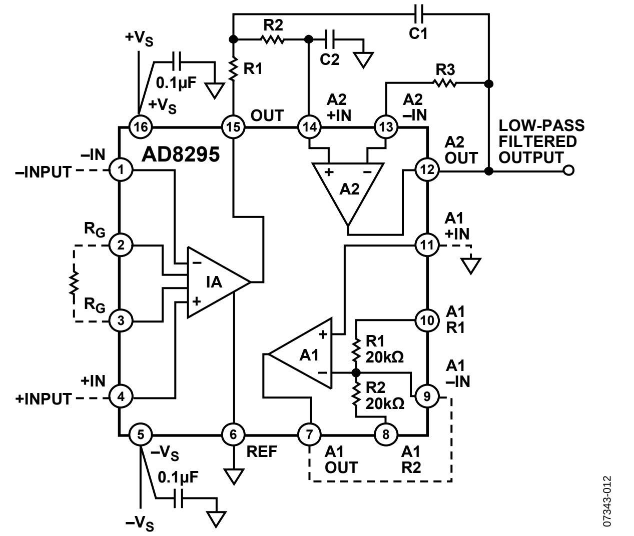

Figure 69. Two-Pole Sallen-Key Filter

The design equations for a Sallen-Key filter can be greatly simplified if the resistors and capacitors are made equal. When C1 = C2 and R1 = R2, Q is 0.5 and the design equation simplifies to

$$f = 1/(2\pi RC)$$

where R is in ohms and C is in farads.

For example, with R1 = R2 = 10 kΩ, and C1 = C2 = 2.2 nF,

$$f = 7.2 \text{ kHz}$$

When C1 is not equal to C2 and R1 is not equal to R2, the values of Q and the cutoff frequency are calculated as follows:

$$Q = \frac{\sqrt{R1\,R2\,C1\,C2}}{C2(R1 + R2)}$$

$$f = \frac{1}{2\pi\sqrt{R1\,R2\,C1\,C2}}$$

AC-COUPLED INSTRUMENTATION AMPLIFIER

The circuit in Figure 70 provides a single-pole high-pass filter, using only one external capacitor.

At low frequencies, Capacitor C1 has a high impedance, thus operating Op Amp A1 at high gain ($G = X_C/20\text{ k}\Omega$). Because of its high gain, Op Amp A1 is able to drive the in-amp reference pin until it forces the output of the in-amp to 0 V. Therefore, no signal appears at the circuit output.

At higher frequencies, the gain of Op Amp A1 drops and the op amp is no longer able to maintain the in-amp output at 0 V. Therefore, at frequencies above the RC filter bandwidth, the in-amp operates in a normal manner, and the signal appears at the output.

The 3 dB corner frequency is set by Internal Resistor R1 and External Capacitor C1 as follows:

$$f = 1/((2\pi \times 20\text{ k}\Omega) \times C1)$$

The precision of R1 (better than 0.2%) means that the filter bandwidth depends mainly on the tolerance of Capacitor C1.

At low frequencies, Op Amp A1 drives the appropriate voltage on the reference pin to null out the original signal. Voltage supplies should be chosen so that Op Amp A1 has enough output headroom to produce the nulling voltage.

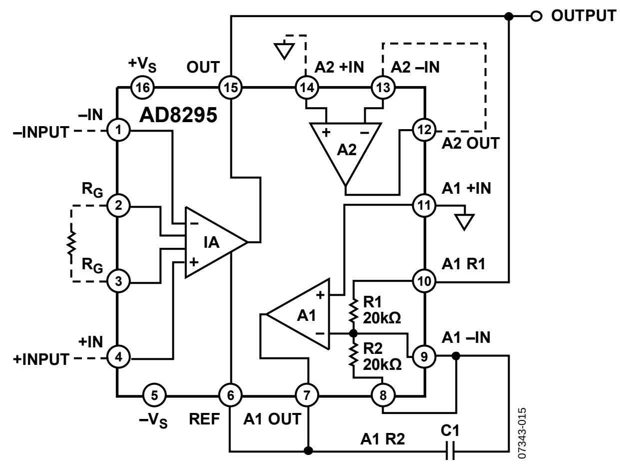

Figure 70. AC-Coupled Connection

DRIVING DIFFERENTIAL ADCs

Figure 71 shows how to configure the AD8295 to drive a differential ADC. The circuit shown uses very little board space and consumes little power. With the AD7690, this configuration gives excellent dc performance and a THD of 83 dB (10 kHz input). For applications that need better distortion performance, a dedicated ADC driver, such as the ADA4941-1 or ADA4922-1 is recommended.

The 500 Ω resistors and the 2.2 nF capacitors form a low-pass, antialiasing filter at 144 kHz. The four elements of the filter also prevent the switching transients produced by a typical SAR ADC from destabilizing the AD8295. The capacitors provide charge to the switched-capacitor front end of the ADC, and the resistors shield the AD8295 from driving any sharp current changes.

If the application requires a lower frequency antialiasing filter than the one shown, increasing the capacitor values produces much better distortion results than increasing the resistor values.

The 500 Ω resistors also protect the ADC against overvoltage. Because the AD8295 runs on wider supply voltages than a typical ADC, there is a possibility of overdriving some converters. This is not an issue with a PulSAR® ADC, such as the AD7690, because its input can handle a 130 mA overdrive, which is much higher than the short-circuit limit of the AD8295. However, other converters have less robust inputs and may benefit from the resistive protection.

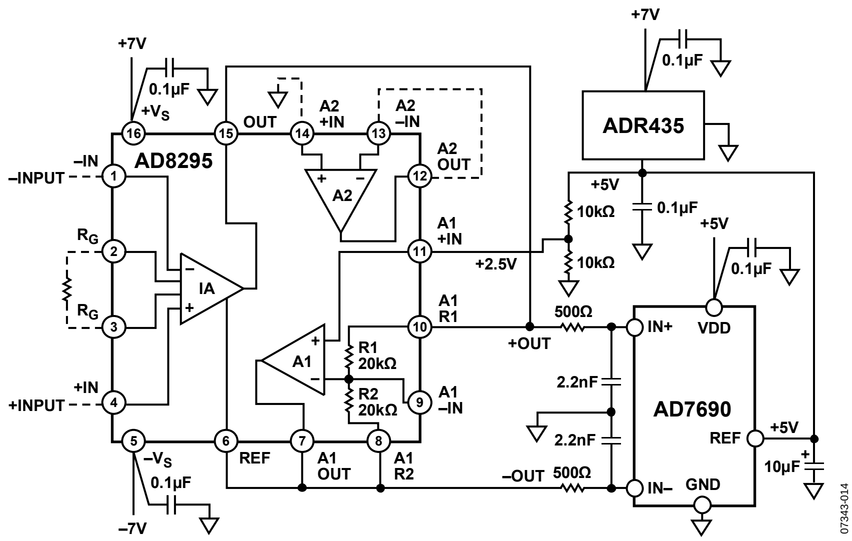

Figure 71. Driving a Differential ADC

OUTLINE DIMENSIONS

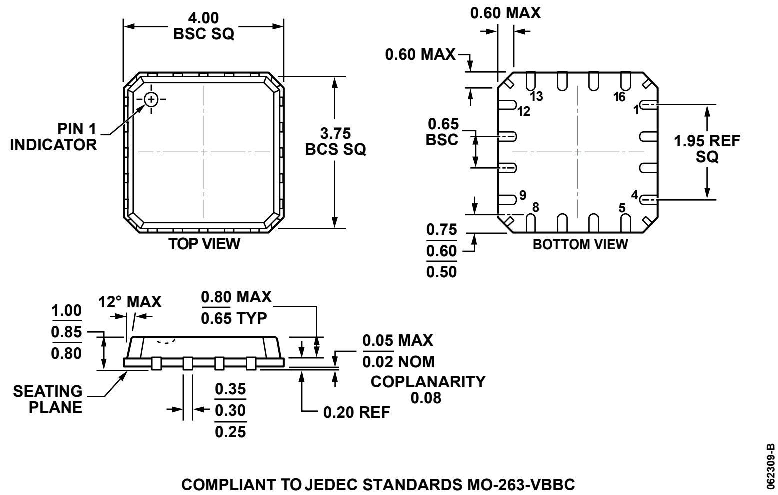

Figure 72. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad, with Hidden Paddle
(CP-16-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8295ACPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ, 7-Inch Tape and Reel	CP-16-19
AD8295ACPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ, 13-Inch Tape and Reel	CP-16-19
AD8295ACPZ-WP[1]	−40°C to +85°C	16-Lead LFCSP_VQ, Waffle Pack	CP-16-19
AD8295BCPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ, 7-Inch Tape and Reel	CP-16-19
AD8295BCPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ, 13-Inch Tape and Reel	CP-16-19
AD8295BCPZ-WP[1]	−40°C to +85°C	16-Lead LFCSP_VQ, Waffle Pack	CP-16-19

[1] Z = RoHS Compliant Part.

NOTES