LF to 2.5 GHz TruPwr™ Detector

Data Sheet

AD8361

FEATURES

Calibrated rms response
Excellent temperature stability
Up to 30 dB input range at 2.5 GHz
700 mV rms, 10 dBm, re 50 Ω maximum input
±0.25 dB linear response up to 2.5 GHz
Single-supply operation: 2.7 V to 5.5 V
Low power: 3.3 mW at 3 V supply
Rapid power-down to less than 1 µA

APPLICATIONS

Measurement of CDMA, W-CDMA, QAM, other complex modulation waveforms
RF transmitter or receiver power measurement

GENERAL DESCRIPTION

The AD8361 is a mean-responding power detector for use in high frequency receiver and transmitter signal chains, up to 2.5 GHz. It is very easy to apply. It requires a single supply only between 2.7 V and 5.5 V, a power supply decoupling capacitor, and an input coupling capacitor in most applications. The output is a linear-responding dc voltage with a conversion gain of 7.5 V/V rms. An external filter capacitor can be added to increase the averaging time constant.

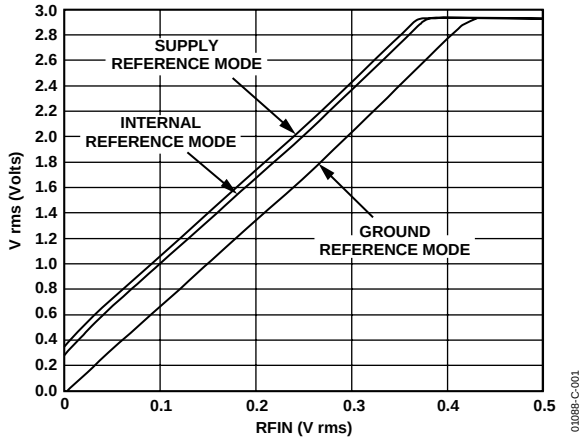

Figure 1. Output in the Three Reference Modes, Supply 3 V, Frequency 1.9 GHz (6-Lead SOT-23 Package Ground Reference Mode Only)

FUNCTIONAL BLOCK DIAGRAMS

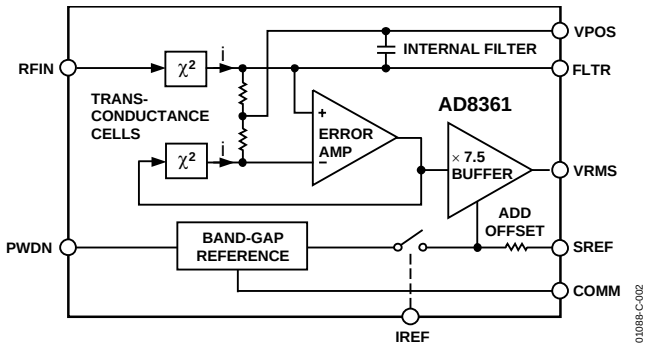

Figure 2. 8-Lead MSOP

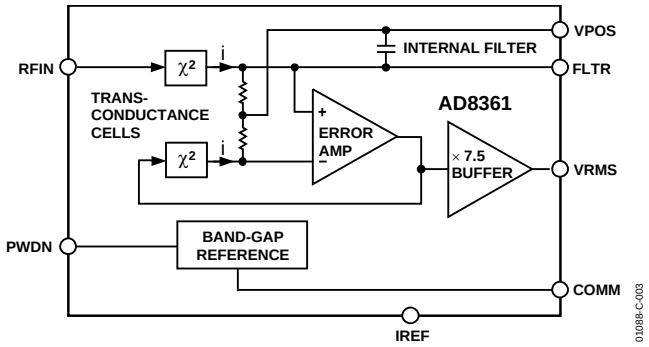

Figure 3. 6-Lead SOT-23

The AD8361 is intended for true power measurement of simple and complex waveforms. The device is particularly useful for measuring high crest-factor (high peak-to-rms ratio) signals, such as CDMA and W-CDMA.

The AD8361 has three operating modes to accommodate a variety of analog-to-digital converter requirements:

1. Ground reference mode, in which the origin is zero.
2. Internal reference mode, which offsets the output 350 mV above ground.
3. Supply reference mode, which offsets the output to $V_S/7.5$.

The AD8361 is specified for operation from −40°C to +85°C and is available in 8-lead MSOP and 6-lead SOT-23 packages. It is fabricated on a proprietary high f_T silicon bipolar process.

Rev. F **Document Feedback**
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REVISION HISTORY

7/15—Rev. E to Rev. F

Change to Ordering Guide ... 22

5/15—Rev. D to Rev. E

Deleted Dynamic Range Extension for the AD8361 Section, Figure 60, Renumbered Sequentially ... 19
Deleted Figure 61, Figure 62, Figure 63, and Figure 64 ... 20

3/14—Rev. C to Rev. D

Changes to Ordering Guide ... 24
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8/04—Rev. B to Rev. C

Changed Trimpots to Trimmable Potentiometers ... Universal
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SPECIFICATIONS

T_A = 25°C, V_S = 3 V, f_{RF} = 900 MHz, ground reference output mode, unless otherwise noted.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	(Input RFIN)				
Frequency Range[1]				2.5	GHz
Linear Response Upper Limit	V_S = 3 V		390		mV rms
	Equivalent dBm, re 50 Ω		4.9		dBm
	V_S = 5 V		660		mV rms
	Equivalent dBm, re 50 Ω		9.4		dBm
Input Impedance[2]			225||1		Ω||pF
RMS CONVERSION	(Input RFIN to Output V rms)				
Conversion Gain			7.5		V/V rms
	f_{RF} = 100 MHz, V_S = 5 V	6.5		8.5	V/V rms
Dynamic Range	Error Referred to Best Fit Line[3]				
±0.25 dB Error[4]	CW Input, −40°C < T_A < +85°C		14		dB
±1 dB Error	CW Input, −40°C < T_A < +85°C		23		dB
±2 dB Error	CW Input, −40°C < T_A < +85°C		26		dB
	CW Input, V_S = 5 V, −40°C < T_A < +85°C		30		dB
Intercept-Induced Dynamic Range Reduction[5, 6]	Internal Reference Mode		1		dB
	Supply Reference Mode, V_S = 3.0 V		1		dB
	Supply Reference Mode, V_S = 5.0 V		1.5		dB
Deviation from CW Response	5.5 dB Peak-to-Average Ratio (IS95 Reverse Link)		0.2		dB
	12 dB Peak-to-Average Ratio (W-CDMA 4 Channels)		1.0		dB
	18 dB Peak-to-Average Ratio (W-CDMA 15 Channels)		1.2		dB
OUTPUT INTERCEPT[5]	Inferred from Best Fit Line[3]				
Ground Reference Mode (GRM)	0 V at SREF, V_S at IREF		0		V
	f_{RF} = 100 MHz, V_S = 5 V	−50		+150	mV
Internal Reference Mode (IRM)	0 V at SREF, IREF Open		350		mV
	f_{RF} = 100 MHz, V_S = 5 V	300		500	mV
Supply Reference Mode (SRM)	3 V at IREF, 3 V at SREF		400		mV
	V_S at IREF, V_S at SREF		V_S/7.5		V
	f_{RF} = 100 MHz, V_S = 5 V	590		750	mV
POWER-DOWN INTERFACE					
PWDN HI Threshold	2.7 ≤ V_S ≤ 5.5 V, −40°C < T_A < +85°C	V_S − 0.5			V
PWDN LO Threshold	2.7 ≤ V_S ≤ 5.5 V, −40°C < T_A < +85°C			0.1	V
Power-Up Response Time	2 pF at FLTR Pin, 224 mV rms at RFIN		5		µs
	100 nF at FLTR Pin, 224 mV rms at RFIN		320		µs
PWDN Bias Current			<1		µA
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.7		5.5	V
Quiescent Current	0 mV rms at RFIN, PWDN Input LO[7]		1.1		mA
Power-Down Current	GRM or IRM, 0 mV rms at RFIN, PWDN Input HI		<1		µA
	SRM, 0 mV rms at RFIN, PWDN Input HI		10 × V_S		µA

[1] Operation at arbitrarily low frequencies is possible; see Application Information section.
[2] Figure 17 and Figure 47 show impedance versus frequency for the MSOP and SOT-23, respectively.
[3] Calculated using linear regression.
[4] Compensated for output reference temperature drift; see Application Information section.
[5] SOT-23-6L operates in ground reference mode only.
[6] The available output swing, and hence the dynamic range, is altered by both supply voltage and reference mode; see Figure 39 and Figure 40.
[7] Supply current is input level dependent; see Figure 16.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage V_S	5.5 V
SREF, PWDN	0 V, V_S
IREF	V_S − 0.3 V, V_S
RFIN	1 V rms
Equivalent Power, re 50 Ω	13 dBm
Internal Power Dissipation[1]	200 mW
6-Lead SOT-23	170 mW
8-Lead MSOP	200 mW
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] Specification is for the device in free air.
6-Lead SOT-23: θ_{JA} = 230°C/W; θ_{JC} = 92°C/W.
8-Lead MSOP: θ_{JA} = 200°C/W; θ_{JC} = 44°C/W.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

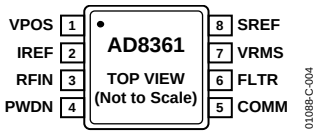

Figure 4. 8-Lead MSOP

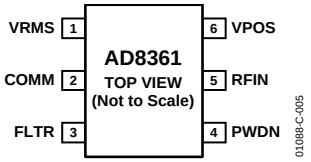

Figure 5. 6-Lead SOT-23

Table 3. Pin Function Descriptions

Pin No. MSOP	Pin No. SOT-23	Mnemonic	Description
1	6	VPOS	Supply Voltage Pin. Operational range 2.7 V to 5.5 V.
2	N/A	IREF	Output Reference Control Pin. Internal reference mode enabled when pin is left open; otherwise, this pin should be tied to VPOS. Do not ground this pin.
3	5	RFIN	Signal Input Pin. Must be driven from an ac-coupled source. The low frequency real input impedance is 225 Ω.
4	4	PWDN	Power-Down Pin. For the device to operate as a detector, it needs a logical low input (less than 100 mV). When a logic high (greater than V_S − 0.5 V) is applied, the device is turned off and the supply current goes to nearly zero (ground and internal reference mode less than 1 µA, supply reference mode V_S divided by 100 kΩ).
5	2	COMM	Device Ground Pin.
6	3	FLTR	By placing a capacitor between this pin and VPOS, the corner frequency of the modulation filter is lowered. The on-chip filter is formed with 27 pF‖2 kΩ for small input signals.
7	1	VRMS	Output Pin. Near rail-to-rail voltage output with limited current drive capabilities. Expected load >10 kΩ to ground.
8	N/A	SREF	Supply Reference Control Pin. To enable supply reference mode, this pin must be connected to VPOS; otherwise, it should be connected to COMM (ground).

TYPICAL PERFORMANCE CHARACTERISTICS

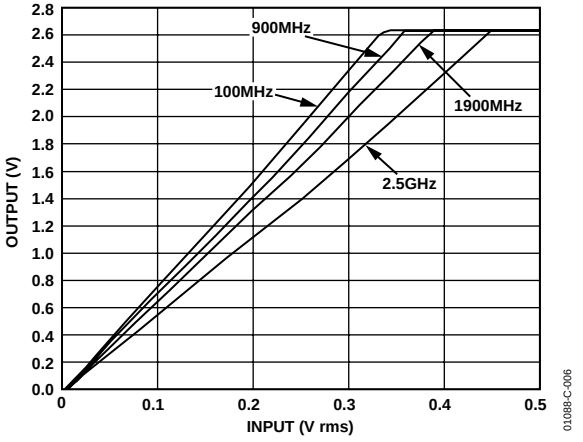

Figure 6. Output vs. Input Level, Frequencies 100 MHz, 900 MHz, 1900 MHz, and 2500 MHz, Supply 2.7 V, Ground Reference Mode, MSOP

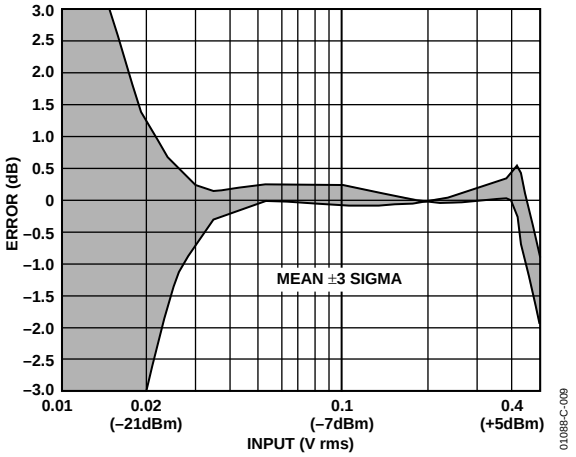

Figure 9. Error from Linear Reference vs. Input Level, 3 Sigma to Either Side of Mean, Sine Wave, Supply 3.0 V, Frequency 900 MHz

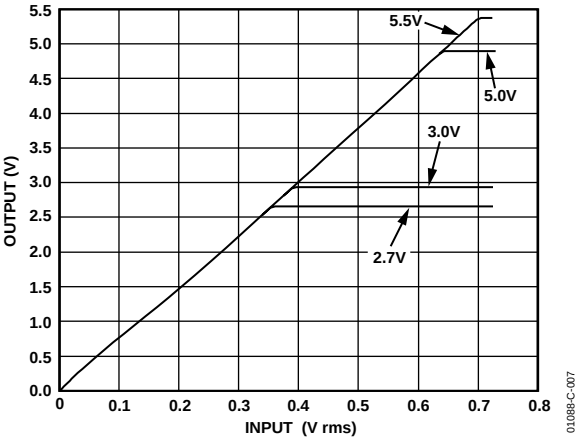

Figure 7. Output vs. Input Level, Supply 2.7 V, 3.0 V, 5.0 V, and 5.5 V, Frequency 900 MHz

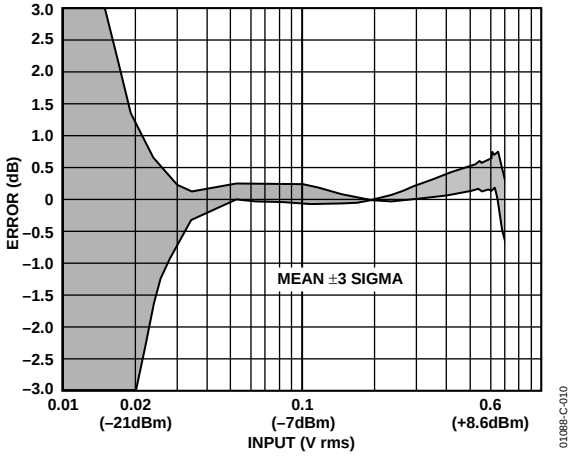

Figure 10. Error from Linear Reference vs. Input Level, 3 Sigma to Either Side of Mean, Sine Wave, Supply 5.0 V, Frequency 900 MHz

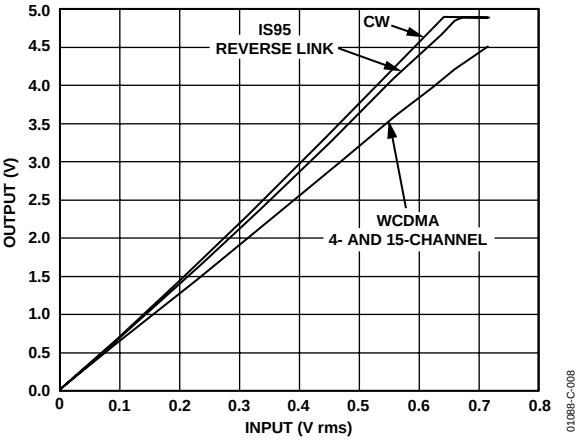

Figure 8. Output vs. Input Level with Different Waveforms Sine Wave (CW), IS95 Reverse Link, W-CDMA 4-Channel and W-CDMA 15-Channel, Supply 5.0 V

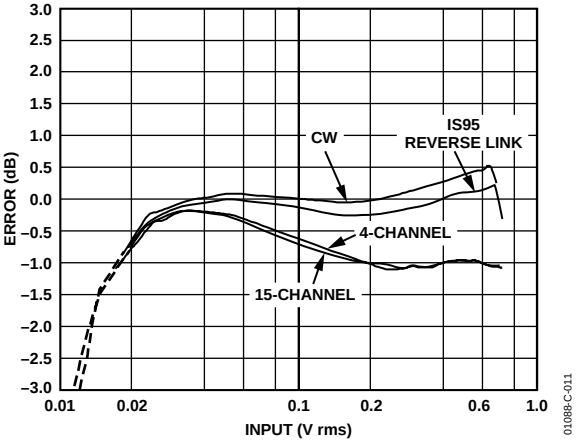

Figure 11. Error from CW Linear Reference vs. Input with Different Waveforms Sine Wave (CW), IS95 Reverse Link, W-CDMA 4-Channel and W-CDMA 15-Channel, Supply 3.0 V, Frequency 900 MHz

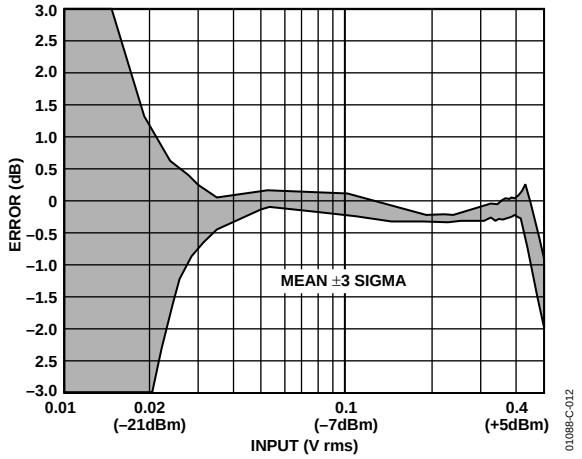

Figure 12. Error from CW Linear Reference vs. Input, 3 Sigma to Either Side of Mean, IS95 Reverse Link Signal, Supply 3.0 V, Frequency 900 MHz

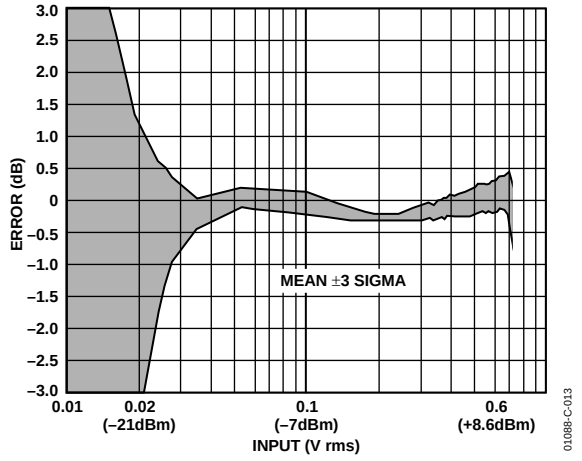

Figure 13. Error from CW Linear Reference vs. Input Level, 3 Sigma to Either Side of Mean, IS95 Reverse Link Signal, Supply 5.0 V, Frequency 900 MHz

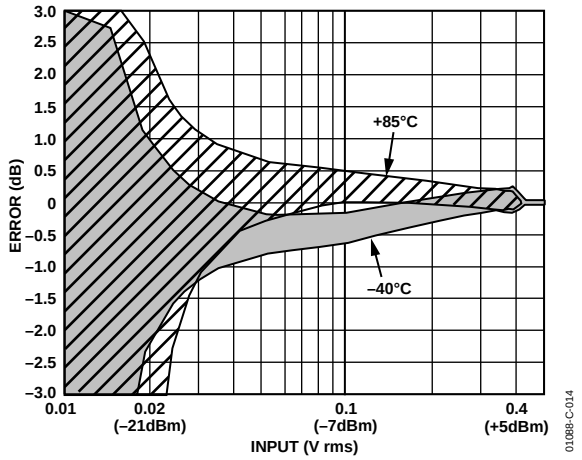

Figure 14. Output Delta from +25°C vs. Input Level, 3 Sigma to Either Side of Mean Sine Wave, Supply 3.0 V, Frequency 900 MHz, Temperature –40°C to +85°C

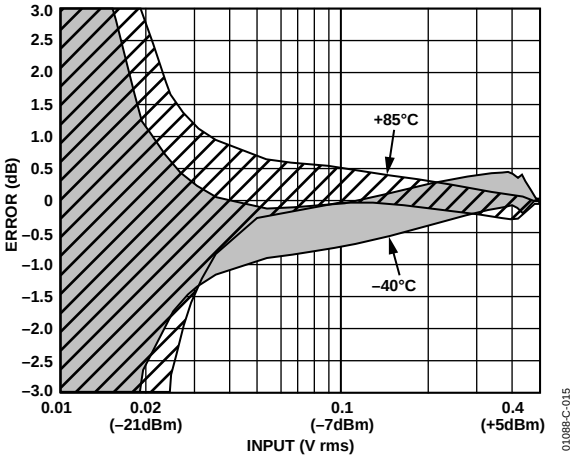

Figure 15. Output Delta from +25°C vs. Input Level, 3 Sigma to Either Side of Mean Sine Wave, Supply 3.0 V, Frequency 1900 MHz, Temperature –40°C to +85°C

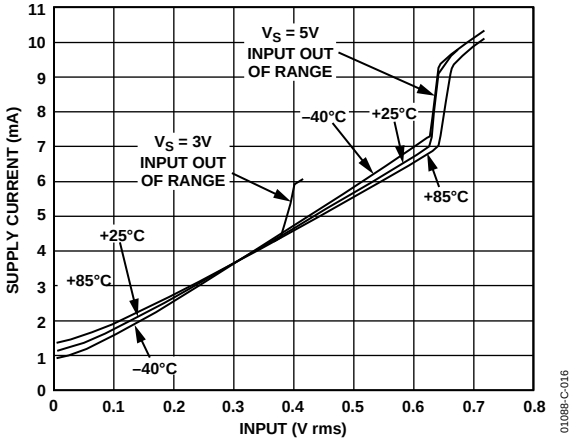

Figure 16. Supply Current vs. Input Level, Supplies 3.0 V, and 5.0 V, Temperatures –40°C, +25°C, and +85°C

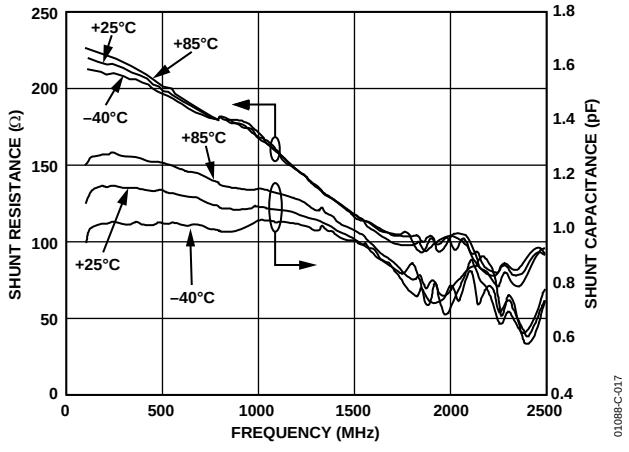

Figure 17. Input Impedance vs. Frequency, Supply 3 V, Temperatures –40°C, +25°C, and +85°C, MSOP (See the Application Information Section for SOT-23 Data)

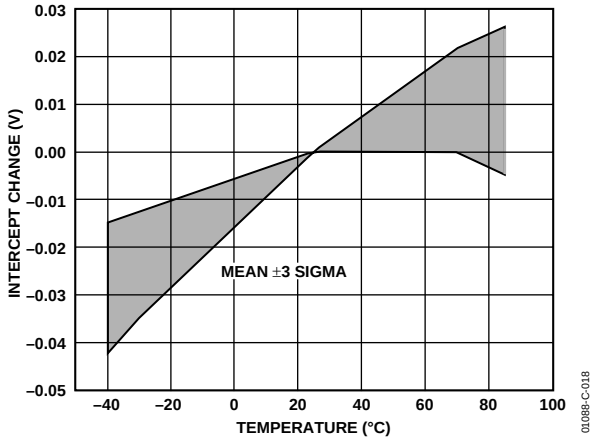

Figure 18. Output Reference Change vs. Temperature, Supply 3 V, Ground Reference Mode

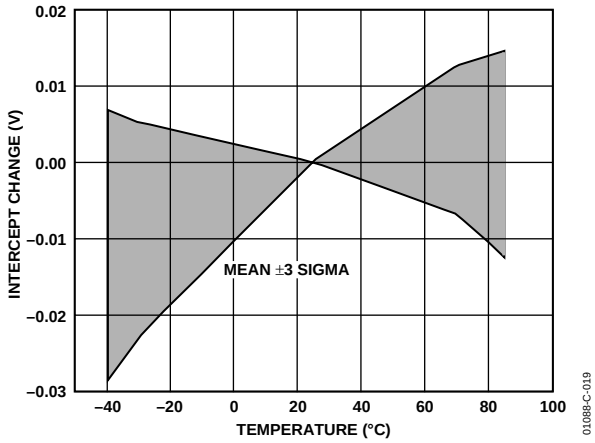

Figure 19. Output Reference Change vs. Temperature, Supply 3 V, Internal Reference Mode (MSOP Only)

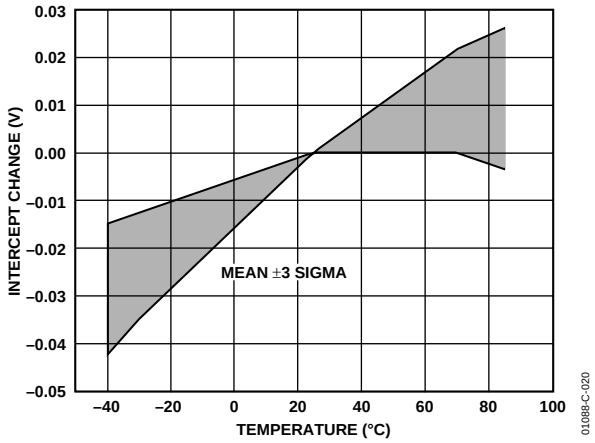

Figure 20. Output Reference Change vs. Temperature, Supply 3 V, Supply Reference Mode (MSOP Only)

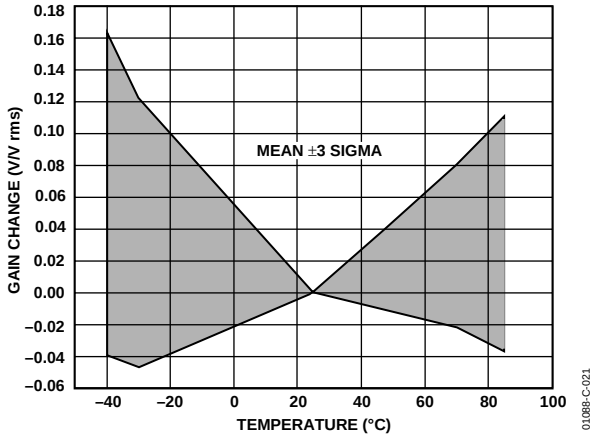

Figure 21. Conversion Gain Change vs. Temperature, Supply 3 V, Ground Reference Mode, Frequency 900 MHz

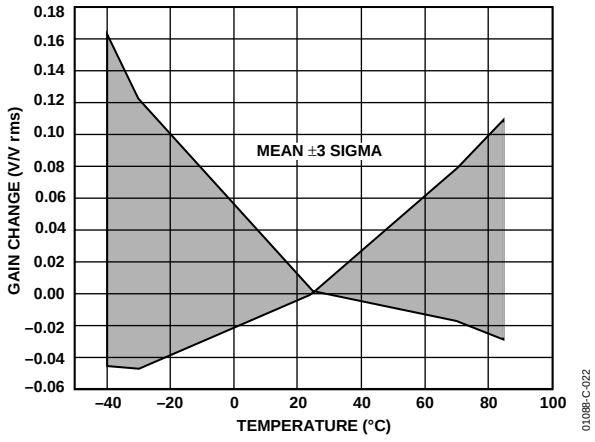

Figure 22. Conversion Gain Change vs. Temperature, Supply 3 V, Internal Reference Mode, Frequency 900 MHz (MSOP Only)

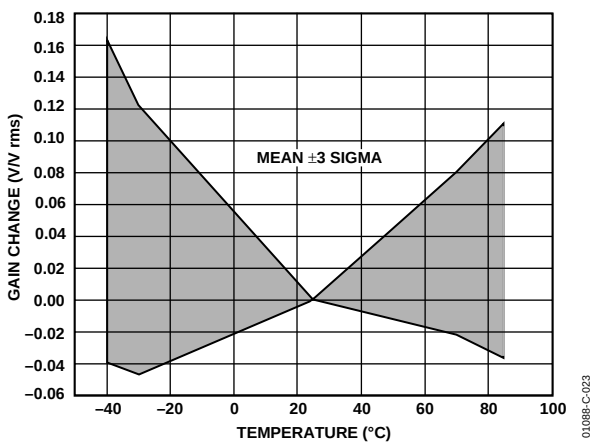

Figure 23. Conversion Gain Change vs. Temperature, Supply 3 V, Supply Reference Mode, Frequency 900 MHz (MSOP Only)

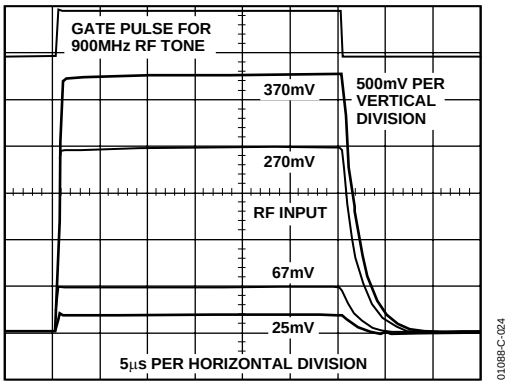

Figure 24. Output Response to Modulated Pulse Input for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, No Filter Capacitor

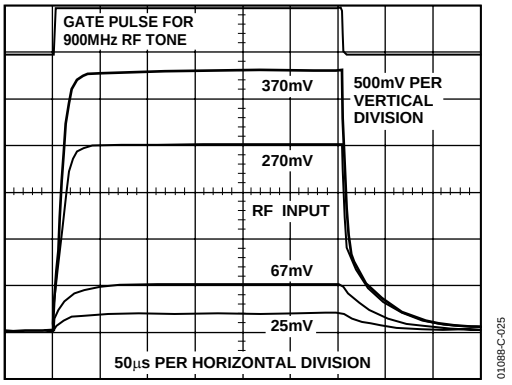

Figure 25. Output Response to Modulated Pulse Input for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, 0.01 µF Filter Capacitor

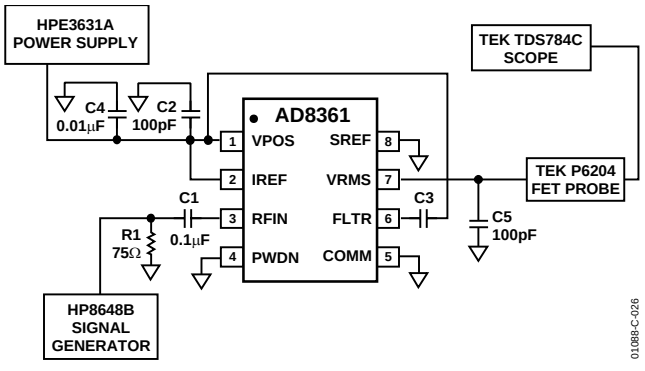

Figure 26. Hardware Configuration for Output Response to Modulated Pulse Input

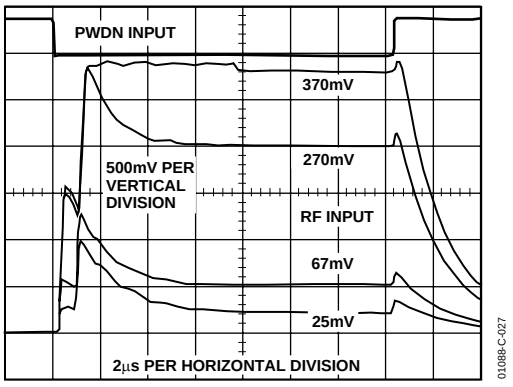

Figure 27. Output Response Using Power-Down Mode for Various RF Input Levels, Supply 3 V, Frequency 900 MHz, No Filter Capacitor

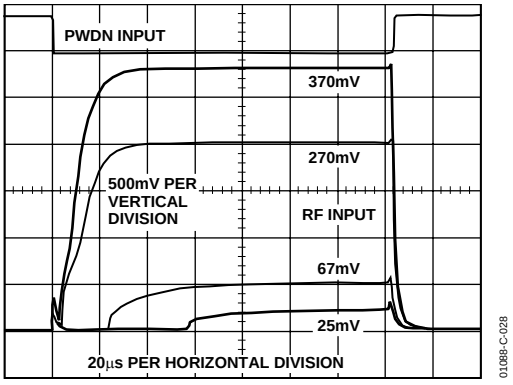

Figure 28. Output Response Using Power-Down Mode for Various RF Input Levels, Supply 3 V, Frequency 900 MHz, 0.01 µF Filter Capacitor

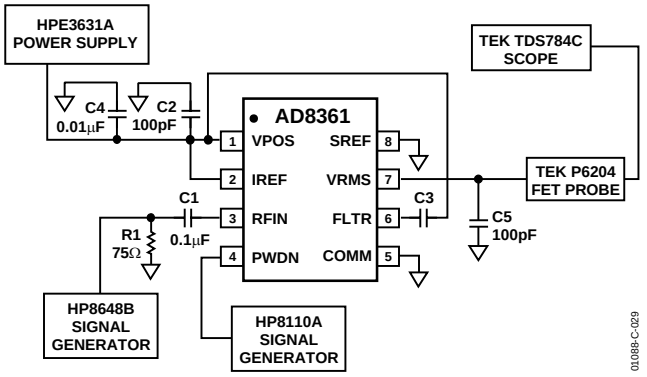

Figure 29. Hardware Configuration for Output Response Using Power-Down Mode

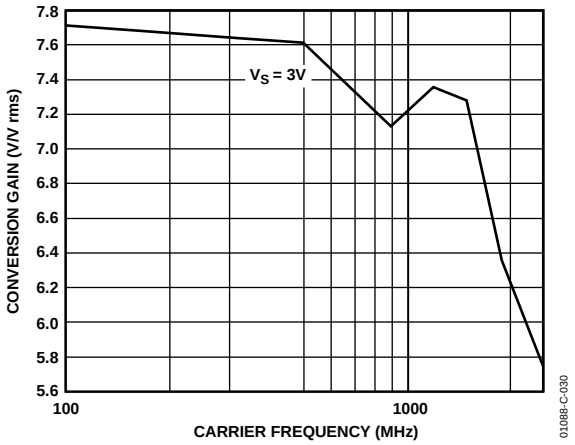

Figure 30. Conversion Gain Change vs. Frequency, Supply 3 V, Ground Reference Mode, Frequency 100 MHz to 2500 MHz, Representative Device

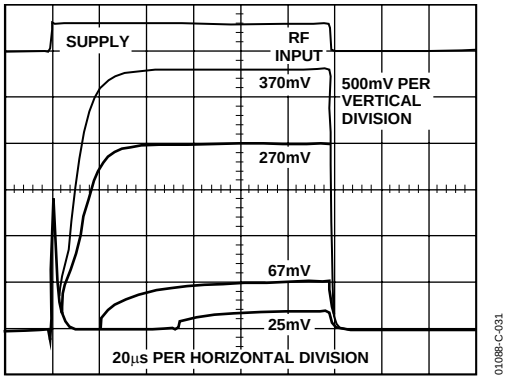

Figure 31. Output Response to Gating on Power Supply, for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, 0.01 µF Filter Capacitor

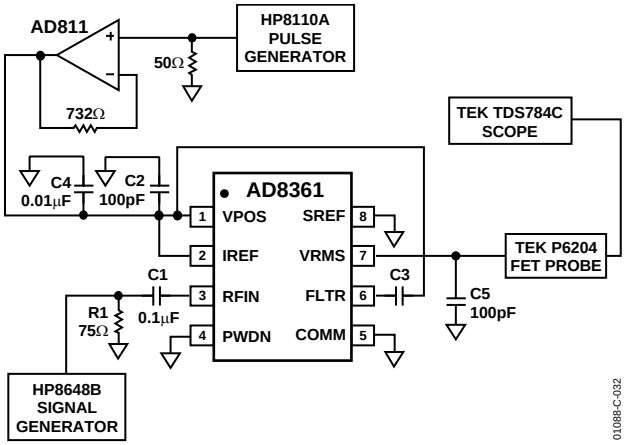

Figure 32. Hardware Configuration for Output Response to Power Supply Gating Measurements

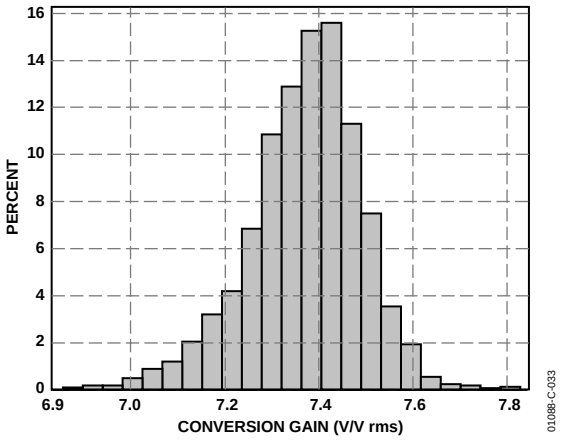

Figure 33. Conversion Gain Distribution Frequency 100 MHz, Supply 5 V, Sample Size 3000

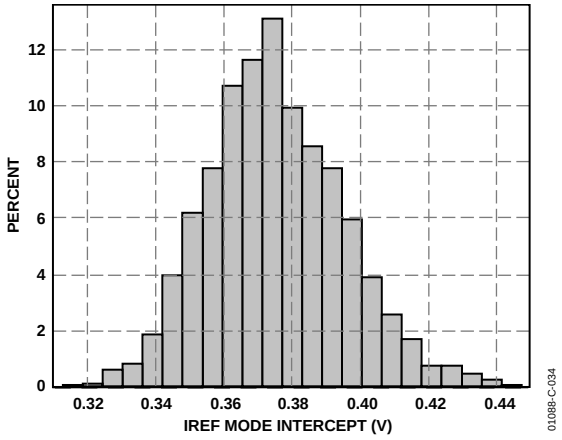

Figure 34. Output Reference, Internal Reference Mode, Supply 5 V, Sample Size 3000 (MSOP Only)

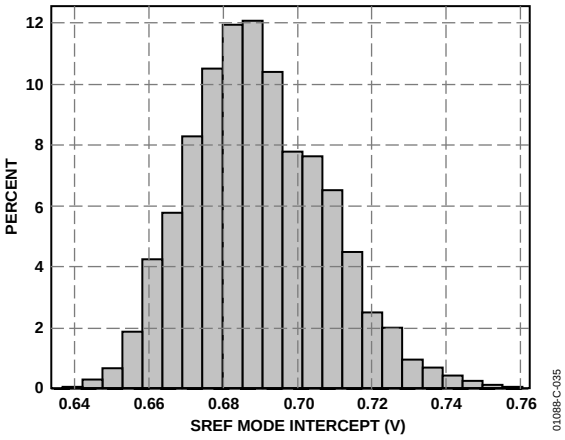

Figure 35. Output Reference, Supply Reference Mode, Supply 5 V, Sample Size 3000 (MSOP Only)

CIRCUIT DESCRIPTION

The AD8361 is an rms-responding (mean power) detector that provides an approach to the exact measurement of RF power that is basically independent of waveform. It achieves this function through the use of a proprietary technique in which the outputs of two identical squaring cells are balanced by the action of a high-gain error amplifier.

The signal to be measured is applied to the input of the first squaring cell, which presents a nominal (LF) resistance of 225 Ω between the RFIN and COMM pins (connected to the ground plane). Because the input pin is at a bias voltage of about 0.8 V above ground, a coupling capacitor is required. By making this an external component, the measurement range may be extended to arbitrarily low frequencies.

The AD8361 responds to the voltage, V_{IN}, at its input by squaring this voltage to generate a current proportional to V_{IN} squared. This is applied to an internal load resistor, across which a capacitor is connected. These form a low-pass filter, which extracts the mean of V_{IN} squared. Although essentially voltage-responding, the associated input impedance calibrates this port in terms of equivalent power. Therefore, 1 mW corresponds to a voltage input of 447 mV rms. The Application Information section shows how to match this input to 50 Ω.

The voltage across the low-pass filter, whose frequency may be arbitrarily low, is applied to one input of an error-sensing amplifier. A second identical voltage-squaring cell is used to close a negative feedback loop around this error amplifier. This second cell is driven by a fraction of the quasi-dc output voltage of the AD8361. When the voltage at the input of the second squaring cell is equal to the rms value of V_{IN}, the loop is in a stable state, and the output then represents the rms value of the input. The feedback ratio is nominally 0.133, making the rms-dc conversion gain ×7.5, that is

$$V_{OUT} = 7.5 \times V_{IN}\, rms$$

By completing the feedback path through a second squaring cell, identical to the one receiving the signal to be measured, several benefits arise. First, scaling effects in these cells cancel; thus, the overall calibration may be accurate, even though the open-loop response of the squaring cells taken separately need not be. Note that in implementing rms-dc conversion, no reference voltage enters into the closed-loop scaling. Second, the tracking in the responses of the dual cells remains very close over temperature, leading to excellent stability of calibration.

The squaring cells have very wide bandwidth with an intrinsic response from dc to microwave. However, the dynamic range of such a system is fairly small, due in part to the much larger dynamic range at the output of the squaring cells. There are practical limitations to the accuracy of sensing very small error signals at the bottom end of the dynamic range, arising from small random offsets that limit the attainable accuracy at small inputs.

On the other hand, the squaring cells in the AD8361 have a Class-AB aspect; the peak input is not limited by their quiescent bias condition but is determined mainly by the eventual loss of square-law conformance. Consequently, the top end of their response range occurs at a fairly large input level (approximately 700 mV rms) while preserving a reasonably accurate square-law response. The maximum usable range is, in practice, limited by the output swing. The rail-to-rail output stage can swing from a few millivolts above ground to less than 100 mV below the supply. An example of the output induced limit: given a gain of 7.5 and assuming a maximum output of 2.9 V with a 3 V supply, the maximum input is (2.9 V rms)/7.5 or 390 mV rms.

Filtering

An important aspect of rms-dc conversion is the need for averaging (the function is *root-MEAN-square*). For complex RF waveforms, such as those that occur in CDMA, the filtering provided by the on-chip, low-pass filter, although satisfactory for CW signals above 100 MHz, is inadequate when the signal has modulation components that extend down into the kilohertz region. For this reason, the FLTR pin is provided: a capacitor attached between this pin and VPOS can extend the averaging time to very low frequencies.

Offset

An offset voltage can be added to the output (when using the MSOP version) to allow the use of ADCs whose range does not extend down to ground. However, accuracy at the low end degrades because of the inherent error in this added voltage. This requires that the IREF (*internal reference*) pin be tied to VPOS and SREF (*supply reference*) to ground.

In the IREF mode, the intercept is generated by an internal reference cell and is a fixed 350 mV, independent of the supply voltage. To enable this intercept, IREF should be open-circuited, and SREF should be grounded.

In the SREF mode, the voltage is provided by the supply. To implement this mode, tie IREF to VPOS and SREF to VPOS. The offset is then proportional to the supply voltage and is 400 mV for a 3 V supply and 667 mV for a 5 V supply.

APPLICATION INFORMATION

Basic Connections

Figure 36 through Figure 38 show the basic connections for the AD8361's MSOP version in its three operating modes. In all modes, the device is powered by a single supply of between 2.7 V and 5.5 V. The VPOS pin is decoupled using 100 pF and 0.01 µF capacitors. The quiescent current of 1.1 mA in operating mode can be reduced to 1 µA by pulling the PWDN pin up to VPOS.

A 75 Ω external shunt resistance combines with the ac-coupled input to give an overall broadband input impedance near 50 Ω. Note that the coupling capacitor must be placed between the input and the shunt impedance. Input impedance and input coupling are discussed in more detail below.

The input coupling capacitor combines with the internal input resistance (Figure 37) to provide a high-pass corner frequency given by the equation

$$f_{3\ dB} = \frac{1}{2\pi \times C_C \times R_{IN}}$$

With the 100 pF capacitor shown in Figure 36 through Figure 38, the high-pass corner frequency is about 8 MHz.

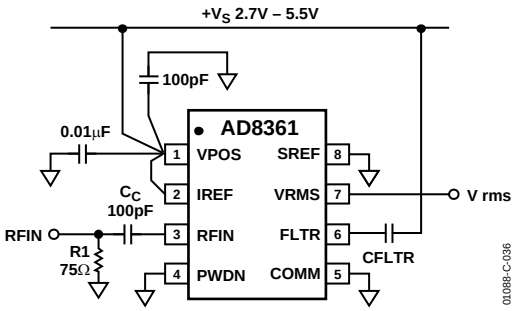

Figure 36. Basic Connections for Ground Reference Mode

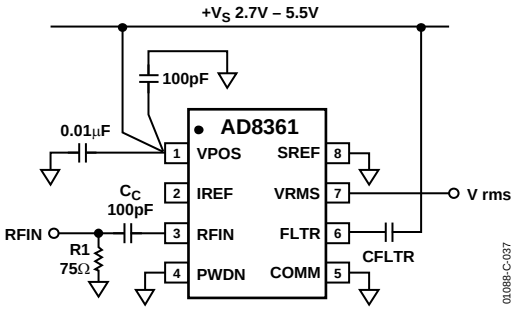

Figure 37. Basic Connections for Internal Reference Mode

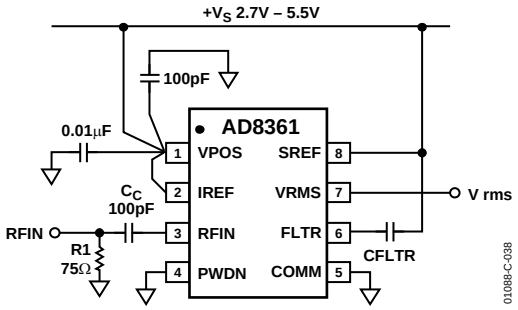

Figure 38. Basic Connections for Supply Referenced Mode

The output voltage is nominally 7.5 times the input rms voltage (a conversion gain of 7.5 V/V rms). Three modes of operation are set by the SREF and IREF pins. In addition to the ground reference mode shown in Figure 36, where the output voltage swings from around near ground to 4.9 V on a 5.0 V supply, two additional modes allow an offset voltage to be added to the output. In the internal reference mode (Figure 37), the output voltage swing is shifted upward by an internal reference voltage of 350 mV. In supply referenced mode (Figure 38), an offset voltage of $V_S/7.5$ is added to the output voltage. Table 4 summarizes the connections, output transfer function, and minimum output voltage (i.e., zero signal) for each mode.

Output Swing

Figure 39 shows the output swing of the AD8361 for a 5 V supply voltage for each of the three modes. It is clear from Figure 39 that operating the device in either internal reference mode or supply referenced mode reduces the effective dynamic range as the output headroom decreases. The response for lower supply voltages is similar (in the supply referenced mode, the offset is smaller), but the dynamic range reduces further as headroom decreases. Figure 40 shows the response of the AD8361 to a CW input for various supply voltages.

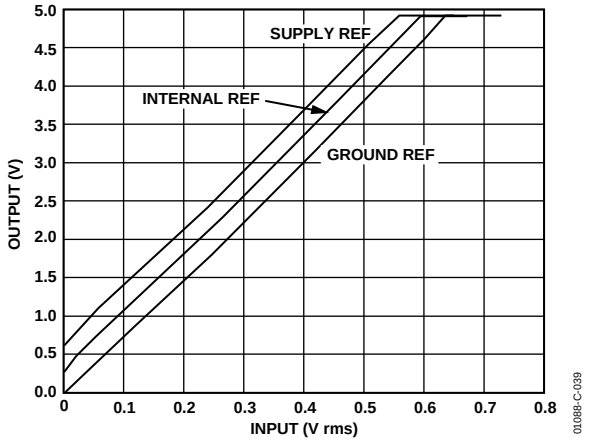

Figure 39. Output Swing for Ground, Internal, and Supply Referenced Mode, VPOS = 5 V (MSOP Only)

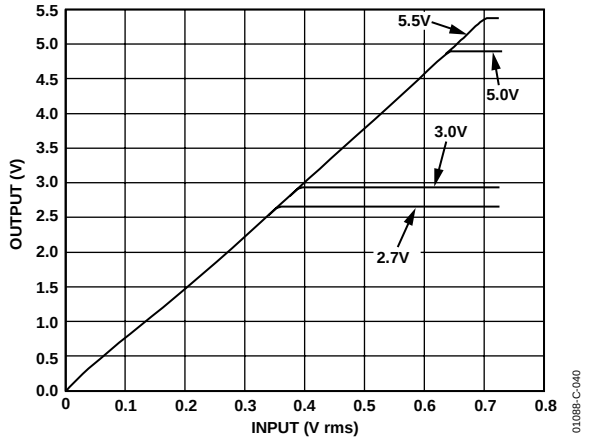

Figure 40. Output Swing for Supply Voltages of 2.7 V, 3.0 V, 5.0 V and 5.5 V (MSOP Only)

Dynamic Range

Because the AD8361 is a linear-responding device with a nominal transfer function of 7.5 V/V rms, the dynamic range in dB is not clear from plots such as Figure 39. As the input level is increased in constant dB steps, the output *step size* (per dB) also increases. Figure 41 shows the relationship between the output step size (i.e., mV/dB) and input voltage for a nominal transfer function of 7.5 V/V rms.

Table 4. Connections and Nominal Transfer Function for Ground, Internal, and Supply Reference Modes

Reference Mode	IREF	SREF	Output Intercept (No Signal)	Output
Ground	VPOS	COMM	Zero	7.5 V_{IN}
Internal	OPEN	COMM	0.350 V	7.5 V_{IN} + 0.350 V
Supply	VPOS	VPOS	V_S/7.5	7.5 V_{IN} + V_S/7.5

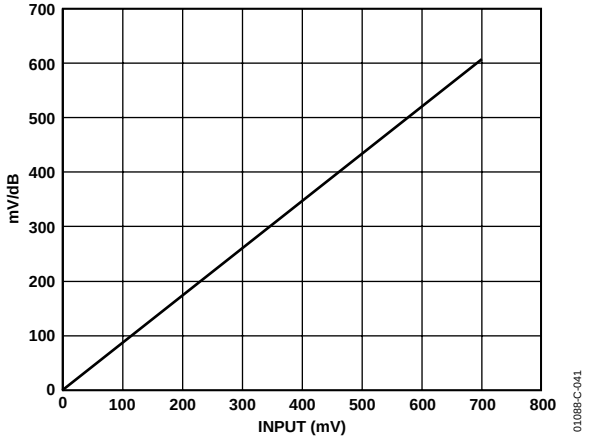

Figure 41. Idealized Output Step Size as a Function of Input Voltage

Plots of output voltage versus input voltage result in a straight line. It may sometimes be more useful to plot the error on a logarithmic scale, as shown in Figure 42. The deviation of the plot for the ideal straight line characteristic is caused by output clipping at the high end and by signal offsets at the low end. It should however be noted that offsets at the low end can be either positive or negative, so this plot could also trend upwards at the low end. Figure 9, Figure 10, Figure 12, and Figure 13 show a ±3 sigma distribution of the device error for a large population of devices.

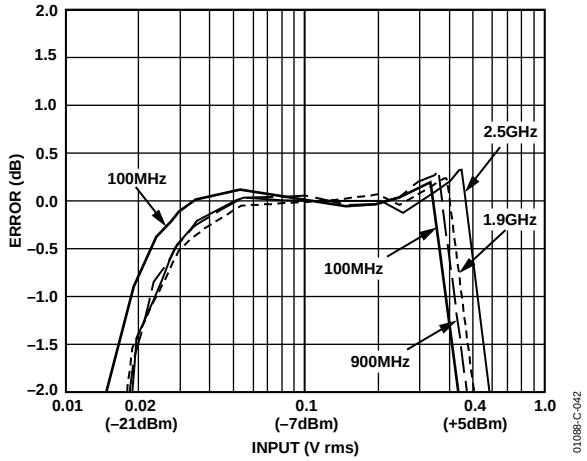

Figure 42. Representative Unit, Error in dB vs. Input Level, V_S = 2.7 V

It is also apparent in Figure 42 that the error plot tends to shift to the right with increasing frequency. Because the input impedance decreases with frequency, the voltage actually applied to the input also tends to decrease (assuming a constant source impedance over frequency). The dynamic range is almost constant over frequency, but with a small decrease in conversion gain at high frequency.

Input Coupling and Matching

The input impedance of the AD8361 decreases with increasing frequency in both its resistive and capacitive components (Figure 17). The resistive component varies from 225 Ω at 100 MHz down to about 95 Ω at 2.5 GHz.

A number of options exist for input matching. For operation at multiple frequencies, a 75 Ω shunt to ground, as shown in Figure 43, provides the best overall match. For use at a single frequency, a resistive or a reactive match can be used. By plotting the input impedance on a Smith Chart, the best value for a resistive match can be calculated. The VSWR can be held below 1.5 at frequencies up to 1 GHz, even as the input impedance varies from part to part. (Both input impedance and input capacitance can vary by up to ±20% around their nominal values.) At very high frequencies (i.e., 1.8 GHz to 2.5 GHz), a shunt resistor is not sufficient to reduce the VSWR below 1.5. Where VSWR is critical, remove the shunt component and insert an inductor in series with the coupling capacitor as shown in Figure 44.

Table 5 gives recommended shunt resistor values for various frequencies and series inductor values for high frequencies. The coupling capacitor, C_C, essentially acts as an ac-short and plays no intentional part in the matching.

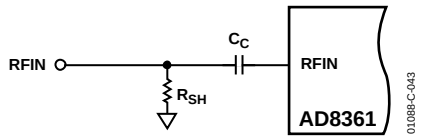

Figure 43. Input Coupling/Matching Options, Broadband Resistor Match

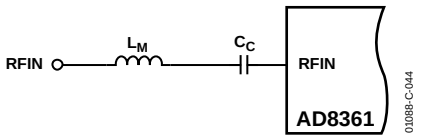

Figure 44. Input Coupling/Matching Options, Series Inductor Match

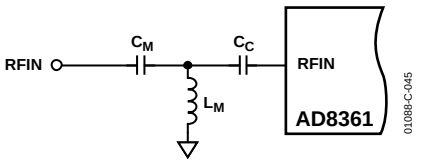

Figure 45. Input Coupling/Matching Options, Narrowband Reactive Match

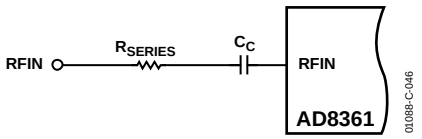

Figure 46. Input Coupling/Matching Options, Attenuating the Input Signal

Table 5. Recommended Component Values for Resistive or Inductive Input Matching (Figure 43 and Figure 44)

Frequency	Matching Component
100 MHz	63.4 Ω Shunt
800 MHz	75 Ω Shunt
900 MHz	75 Ω Shunt
1800 MHz	150 Ω Shunt or 4.7 nH Series
1900 MHz	150 Ω Shunt or 4.7 nH Series
2500 MHz	150 Ω Shunt or 2.7 nH Series

Alternatively, a reactive match can be implemented using a shunt inductor to ground and a series capacitor, as shown in Figure 45. A method for hand calculating the appropriate matching components is shown on page 12 of the AD8306 data sheet.

Matching in this manner results in very small values for C_M, especially at high frequencies. As a result, a stray capacitance as small as 1 pF can significantly degrade the quality of the match. The main advantage of a reactive match is the increase in sensitivity that results from the input voltage being gained up (by the square root of the impedance ratio) by the matching network. Table 6 shows the recommended values for reactive matching.

Table 6. Recommended Values for a Reactive Input Matching (Figure 45)

Frequency (MHz)	C_M (pF)	L_M (nH)
100	16	180
800	2	15
900	2	12
1800	1.5	4.7
1900	1.5	4.7
2500	1.5	3.3

Input Coupling Using a Series Resistor

Figure 46 shows a technique for coupling the input signal into the AD8361 that may be applicable where the input signal is much larger than the input range of the AD8361. A series resistor combines with the input impedance of the AD8361 to attenuate the input signal. Because this series resistor forms a divider with the frequency dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being tapped off in RF power transmission applications. If the resistor is large compared to the transmission line's impedance, then the VSWR of the system is relatively unaffected.

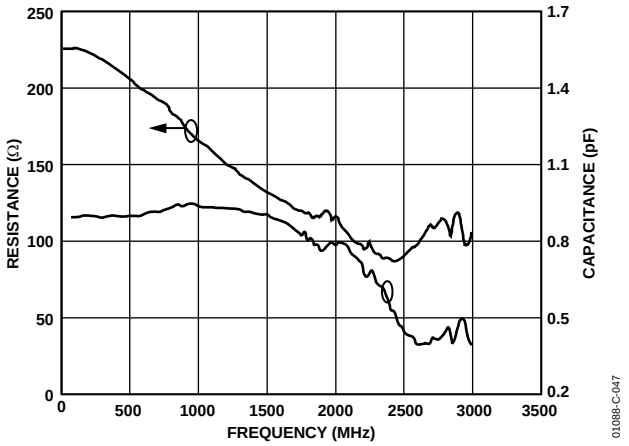

Figure 47. Input Impedance vs. Frequency, Supply 3 V, SOT-23

Selecting the Filter Capacitor

The AD8361's internal 27 pF filter capacitor is connected in parallel with an internal resistance that varies with signal level from 2 kΩ for small signals to 500 Ω for large signals. The resulting low-pass corner frequency between 3 MHz and 12 MHz provides adequate filtering for all frequencies above 240 MHz (i.e., 10 times the frequency at the output of the squarer, which is twice the input frequency). However, signals with high peak-to-average ratios, such as CDMA or W-CDMA signals, and low frequency components require additional filtering. TDMA signals, such as GSM, PDC, or PHS, have a peak-to average ratio that is close to that of a sinusoid, and the internal filter is adequate.

The filter capacitance of the AD8361 can be augmented by connecting a capacitor between Pin 6 (FLTR) and VPOS. Table 7 shows the effect of several capacitor values for various communications standards with high peak-to-average ratios along with the residual ripple at the output, in peak-to-peak and rms volts. Note that large filter capacitors increase the enable and pulse response times, as discussed below.

Table 7. Effect of Waveform and CFILT on Residual AC

Waveform	C_{FILT}	Output V dc	Residual AC mV p-p	Residual AC mV rms
IS95 Reverse Link	Open	0.5	550	100
		1.0	1000	180
		2.0	2000	360
	0.01 µF	0.5	40	6
		1.0	160	20
		2.0	430	60
	0.1 µF	0.5	20	3
		1.0	40	6
		2.0	110	18
IS95 8-Channel Forward Link	0.01 µF	0.5	290	40
		1.0	975	150
		2.0	2600	430
	0.1 µF	0.5	50	7
		1.0	190	30
		2.0	670	95
W-CDMA 15 Channel	0.01 µF	0.5	225	35
		1.0	940	135
		2.0	2500	390
	0.1 µF	0.5	45	6
		1.0	165	25
		2.0	550	80

Operation at Low Frequencies

Although the AD8361 is specified for operation up to 2.5 GHz, there is no lower limit on the operating frequency. It is only necessary to increase the input coupling capacitor to reduce the corner frequency of the input high-pass filter (use an input resistance of 225 Ω for frequencies below 100 MHz). It is also necessary to increase the filter capacitor so that the signal at the output of the squaring circuit is free of ripple. The corner frequency is set by the combination of the internal resistance of 2 kΩ and the external filter capacitance.

Power Consumption, Enable and Power-On

The quiescent current consumption of the AD8361 varies with the size of the input signal from about 1 mA for no signal up to 7 mA at an input level of 0.66 V rms (9.4 dBm, re 50 Ω). If the input is driven beyond this point, the supply current increases steeply (see Figure 16). There is little variation in quiescent current with power supply voltage.

The AD8361 can be disabled either by pulling the PWDN (Pin 4) to VPOS or by simply turning off the power to the device. While turning off the device obviously eliminates the current consumption, disabling the device reduces the leakage current to less than 1 µA. Figure 27 and Figure 28 show the response of the output of the AD8361 to a pulse on the PWDN pin, with no capacitance and with a filter capacitance of 0.01 µF, respectively; the turn-on time is a function of the filter capacitor. Figure 31 shows a plot of the output response to the supply being turned on (i.e., PWDN is grounded and VPOS is pulsed) with a filter capacitor of 0.01 µF. Again, the turn-on time is strongly influenced by the size of the filter capacitor.

If the input of the AD8361 is driven while the device is disabled (PWDN = VPOS), the leakage current of less than 1 µA increases as a function of input level. When the device is disabled, the output impedance increases to approximately 16 kΩ.

Volts to dBm Conversion

In many of the plots, the horizontal axis is scaled in both rms volts and dBm. In all cases, dBm are calculated relative to an impedance of 50 Ω. To convert between dBm and volts in a 50 Ω system, the following equations can be used. Figure 48 shows this conversion in graphical form.

$$Power\,(\text{dBm}) = 10\log\left[\frac{\frac{(V\,rms)^2}{50\,\Omega}}{0.001\,\text{W}}\right] = 10\log\left(20\,(V\,rms)^2\right)$$

$$V\,rms = \sqrt{0.001\,\text{W}\times 50\,\Omega\times\log^{-1}\left(\frac{dBm}{10}\right)} = \sqrt{\frac{\log^{-1}(dBm/10)}{20}}$$

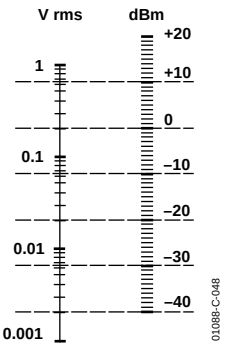

Figure 48. Conversion from dBm to rms Volts

Output Drive Capability and Buffering

The AD8361 is capable of sourcing an output current of approximately 3 mA. If additional current is required, a simple buffering circuit can be used as shown in Figure 51. Similar circuits can be used to increase or decrease the nominal conversion gain of 7.5 V/V rms (Figure 49 and Figure 50). In Figure 50, the AD8031 buffers a resistive divider to give a slope of 3.75 V/V rms. In Figure 49, the op amp's gain of two increases the slope to 15 V/V rms. Using other resistor values, the slope can be changed to an arbitrary value. The AD8031 rail-to-rail op amp, used in these example, can swing from 50 mV to 4.95 V on a single 5 V supply and operate at supply voltages down to 2.7 V. If high output current is required (>10 mA), the AD8051, which also has rail-to- rail capability, can be used down to a supply voltage of 3 V. It can deliver up to 45 mA of output current.

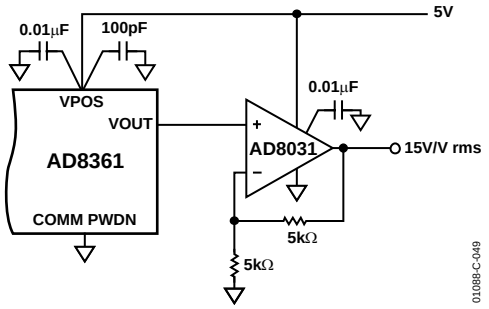

Figure 49. Output Buffering Options, Slope of 15 V/V rms

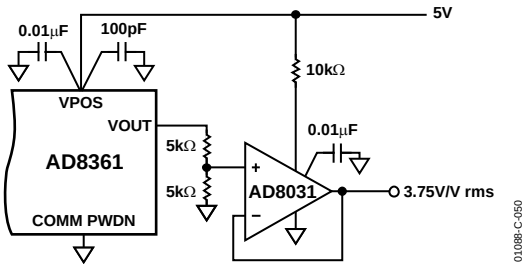

Figure 50. Output Buffering Options, Slope of 3.75 V/V rms

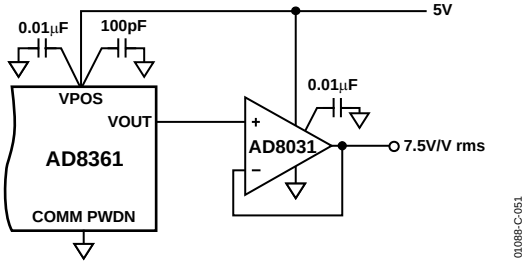

Figure 51. Output Buffering Options, Slope of 7.5 V/V rms

OUTPUT REFERENCE TEMPERATURE DRIFT COMPENSATION

The error due to low temperature drift of the AD8361 can be reduced if the temperature is known. Many systems incorporate a temperature sensor; the output of the sensor is typically digitized, facilitating a software correction. Using this information, only a two-point calibration at ambient is required.

The output voltage of the AD8361 at ambient (25°C) can be expressed by the equation

$$V_{OUT} = (GAIN \times V_{IN}) + \varsigma_{O\Sigma}$$

where *GAIN* is the conversion gain in V/V rms and V_{OS} is the extrapolated output voltage for an input level of 0 V. *GAIN* and V_{OS} (also referred to as intercept and output reference) can be calculated at ambient using a simple two-point calibration by measuring the output voltages for two specific input levels. Calibration at roughly 35 mV rms (−16 dBm) and 250 mV rms (+1 dBm) is recommended for maximum linear dynamic range. However, alternative levels and ranges can be chosen to suit the application. *GAIN* and V_{OS} are then calculated using the equations

$$GAIN = \frac{(V_{OUT2} - V_{OUT1})}{V_{IN2} - V_{IN1}}$$

$$V_{OS} = V_{OUT1} - (GAIN \times V_{IN1})$$

Both *GAIN* and V_{OS} drift over temperature. However, the drift of V_{OS} has a bigger influence on the error relative to the output. This can be seen by inserting data from Figure 18 and Figure 21 (intercept drift and conversion gain) into the equation for V_{OUT}. These plots are consistent with Figure 14 and Figure 15, which show that the error due to temperature drift decreases with increasing input level. This results from the offset error having a diminishing influence with increasing level on the overall measurement error.

From Figure 18, the average intercept drift is 0.43 mV/°C from −40°C to +25°C and 0.17 mV/°C from +25°C to +85°C. For a less rigorous compensation scheme, the average drift over the complete temperature range can be calculated as

$$DRIFT_{VOS}(\text{V/°C}) = \left(\frac{0.010\text{ V} - (-0.028\text{ V})}{+85°\text{C} - (-40°\text{C})}\right) = 0.000304\text{ V/°C}$$

With the drift of V_{OS} included, the equation for V_{OUT} becomes

$$V_{OUT} = (GAIN \times V_{IN}) + V_{OS} + DRIFT_{VOS} \times (TEMP - 25°\text{C})$$

The equation can be rewritten to yield a temperature compensated value for V_{IN}:

$$V_{IN} = \frac{\left(V_{OUT} - V_{OS} - DRIFT_{VOS} \times (TEMP - 25°C)\right)}{GAIN}$$

Figure 52 shows the output voltage and error (in dB) as a function of input level for a typical device (note that output voltage is plotted on a logarithmic scale). Figure 53 shows the error in the calculated input level after the temperature compensation algorithm has been applied. For a supply voltage of 5 V, the part exhibits a worst-case linearity error over temperature of approximately ±0.3 dB over a dynamic range of 35 dB.

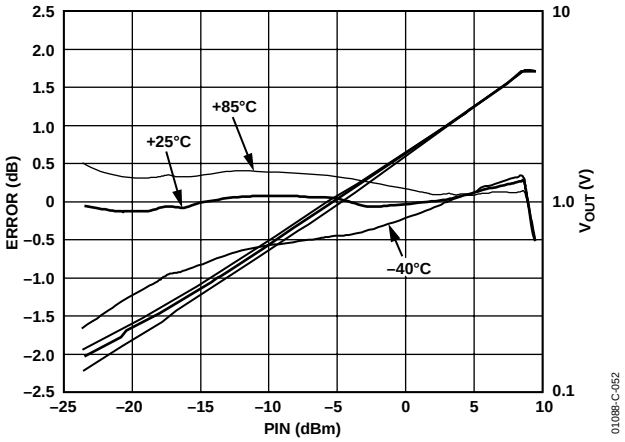

Figure 52. Typical Output Voltage and Error vs. Input Level, 800 MHz, VPOS = 5 V

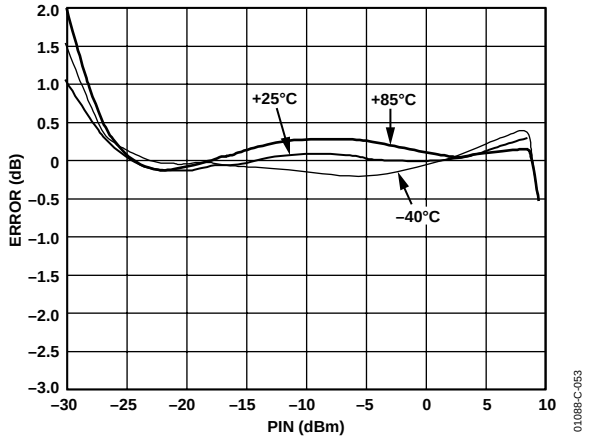

Figure 53. Error after Temperature Compensation of Output Reference,800 MHz, VPOS = 5 V

Extended Frequency Characterization

Although the AD8361 was originally intended as a power measurement and control device for cellular wireless applications, the AD8361 has useful performance at higher frequencies. Typical applications may include MMDS, LMDS, WLAN, and other noncellular activities.

In order to characterize the AD8361 at frequencies greater than 2.5 GHz, a small collection of devices were tested. Dynamic range, conversion gain, and output intercept were measured at several frequencies over a temperature range of −30°C to +80°C. Both CW and 64 QAM modulated input wave forms were used in the characterization process in order to access varying peak-to-average waveform performance.

The dynamic range of the device is calculated as the input power range over which the device remains within a permissible error margin to the ideal transfer function. Devices were tested over frequency and temperature. After identifying an acceptable error margin for a given application, the usable dynamic measurement range can be identified using the plots in Figure 54 through Figure 57. For instance, for a 1 dB error margin and a modulated carrier at 3 GHz, the usable dynamic range can be found by inspecting the 3 GHz plot of Figure 57. Note that the −30°C curve crosses the −1 dB error limit at −17 dBm. For a 5 V supply, the maximum input power should not exceed 6 dBm in order to avoid compression. The resultant usable dynamic range is therefore

6 dBm − (−17 dBm)

or 23 dBm over a temperature range of −30°C to +80°C.

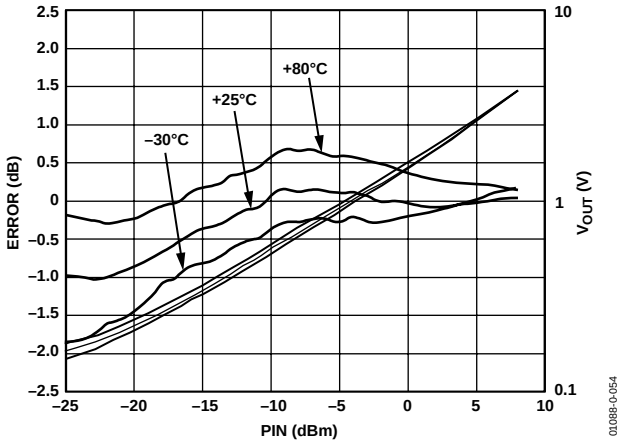

Figure 54. Transfer Function and Error Plots Measured at 1.5 GHz for a 64 QAM Modulated Signal

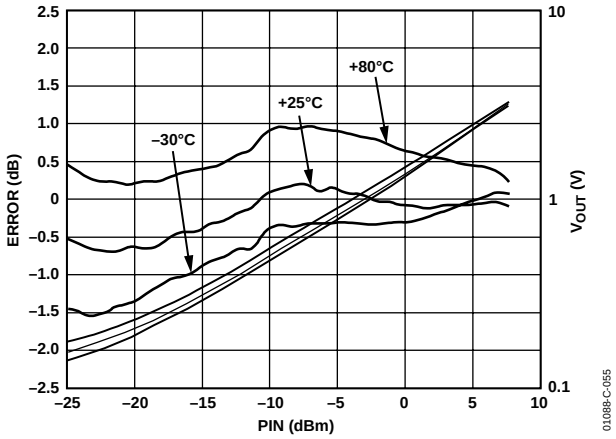

Figure 55. Transfer Function and Error Plots Measured at 2.5 GHz for a 64 QAM Modulated Signal

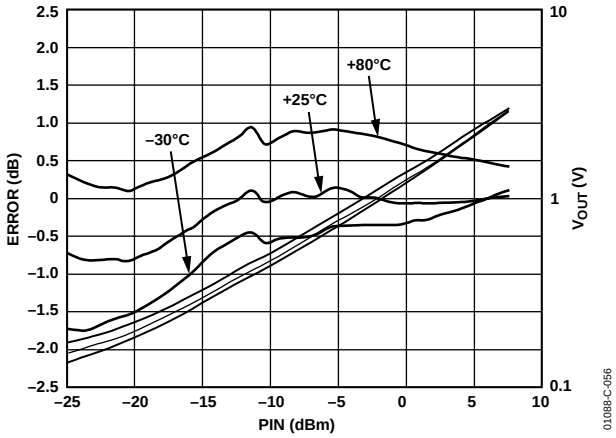

Figure 56. Transfer Function and Error Plots Measured at 2.7 GHz for a 64 QAM Modulated Signal

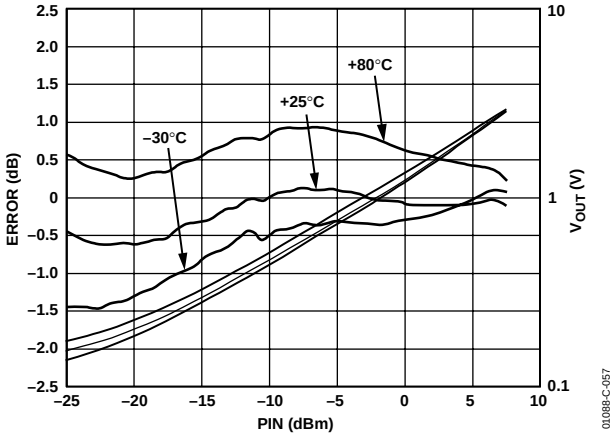

Figure 57. Transfer Function and Error Plots Measured at 3.0 GHz for a 64 QAM Modulated Signal

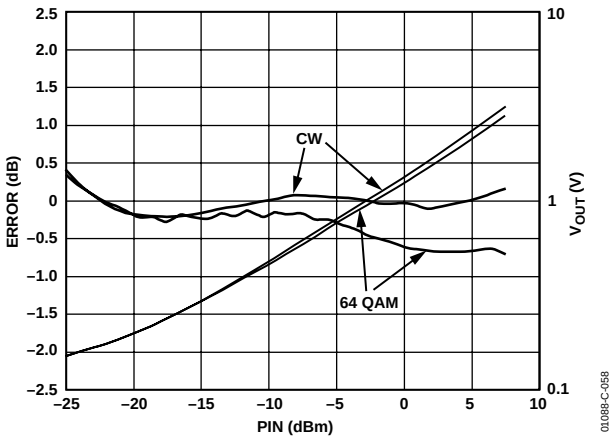

Figure 58. Error from CW Linear Reference vs. Input Drive Level for CW and 64 QAM Modulated Signals at 3.0 GHz

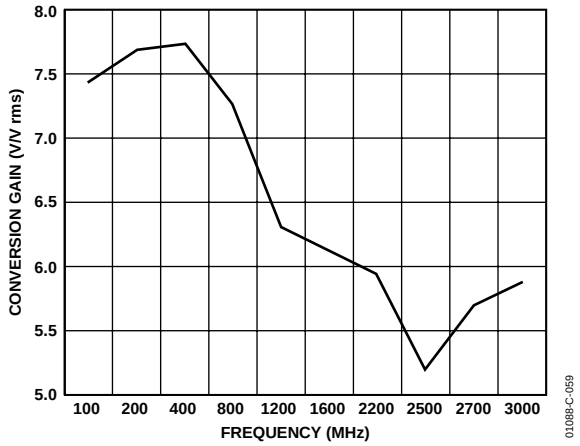

Figure 59. Conversion Gain vs. Frequency for a Typical Device, Supply 3 V, Ground Reference Mode

The transfer functions and error for a CW input and a 64 QAM input waveform is shown in Figure 58. The error curve is generated from a linear reference based on the CW data. The increased crest factor of the 64 QAM modulation results in a decrease in output from the AD8361. This decrease in output is a result of the limited bandwidth and compression of the internal gain stages. This inaccuracy should be accounted for in systems where varying crest factor signals need to be measured. The conversion gain is defined as the slope of the output voltage vs. the input rms voltage. An ideal best fit curve can be found for the measured transfer function at a given supply voltage and temperature. The slope of the ideal curve is identified as the conversion gain for a particular device. The conversion gain relates the measurement sensitivity of the AD8361 to the rms input voltage of the RF waveform. The conversion gain was measured for a number of devices over a temperature range of −30°C to +80°C. The conversion gain for a typical device is shown in Figure 59. Although the conversion gain tends to decrease with increasing frequency, the AD8361 provides measurement capability at frequencies greater than 2.5 GHz. However, it is necessary to calibrate for a given application to accommodate for the change in conversion gain at higher frequencies.

EVALUATION BOARD

Figure 60 and Figure 63 show the schematic of the AD8361 evaluation board. Note that uninstalled components are drawn in as dashed. The layout and silkscreen of the component side are shown in Figure 61, Figure 62, Figure 64, and Figure 65. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by 100 pF and 0.01 µF capacitors. Additional decoupling, in the form of a series resistor or inductor in R6, can also be added. Table 8 details the various configuration options of the evaluation board.

Table 8. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Ground and Supply Vector Pins.	Not Applicable
SW1	Device Enable. When in Position A, the PWDN pin is connected to $+V_S$ and the AD8361 is in power-down mode. In Position B, the PWDN pin is grounded, putting the device in operating mode.	SW1 = B
SW2/SW3	Operating Mode. Selects either ground reference mode, internal reference mode or supply reference mode. See Table 4 for more details.	SW2 = A, SW3 = B (Ground Reference Mode)
C1, R2	Input Coupling. The 75 Ω resistor in Position R2 combines with the AD8361's internal input impedance to give a broadband input impedance of around 50 Ω. For more precise matching at a particular frequency, R2 can be replaced by a different value (see Input Coupling and Matching and Figure 43 through Figure 46). Capacitor C1 ac couples the input signal and creates a high-pass input filter whose corner frequency is equal to approximately 8 MHz. C1 can be increased for operation at lower frequencies. If resistive attenuation is desired at the input, series resistor R1, which is nominally 0 Ω, can be replaced by an appropriate value.	R2 = 75 Ω (Size 0402) C1 = 100 pF (Size 0402)
C2, C3, R6	Power Supply Decoupling. The nominal supply decoupling of 0.01 µF and 100 pF. A series inductor or small resistor can be placed in R6 for additional decoupling.	C2 = 0.01 µF (Size 0402) C3 = 100 pF (Size 0402) R6 = 0 Ω (Size 0402)
C5	Filter Capacitor. The internal 50 pF averaging capacitor can be augmented by placing a capacitance in C5.	C5 = 1 nF (Size 0603)
C4, R5	Output Loading. Resistors and capacitors can be placed in C4 and R5 to load test V rms.	C4 = R5 = Open (Size 0603)

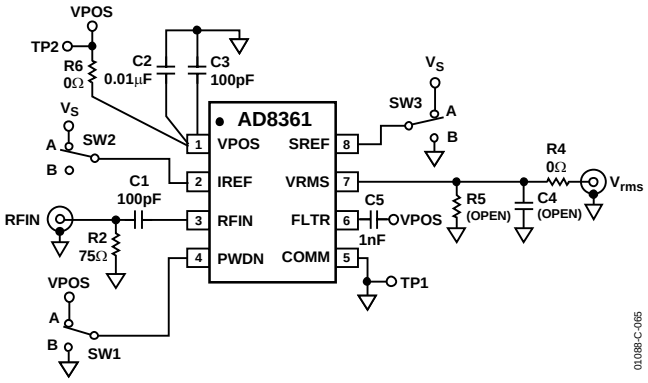

Figure 60. Evaluation Board Schematic, MSOP

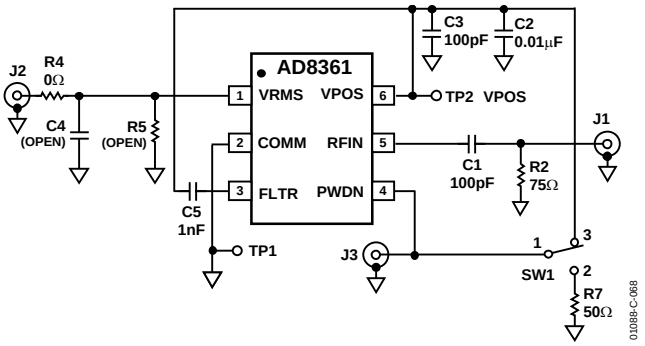

Figure 63. Evaluation Board Schematic, SOT-23

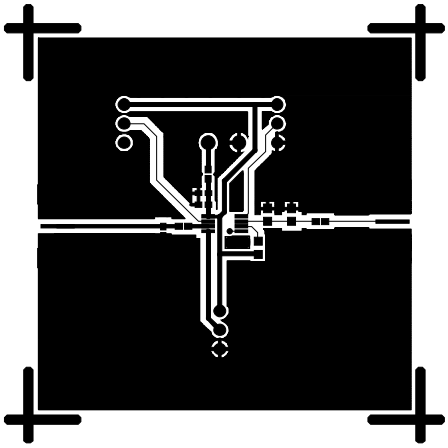

Figure 61. Layout of Component Side, MSOP

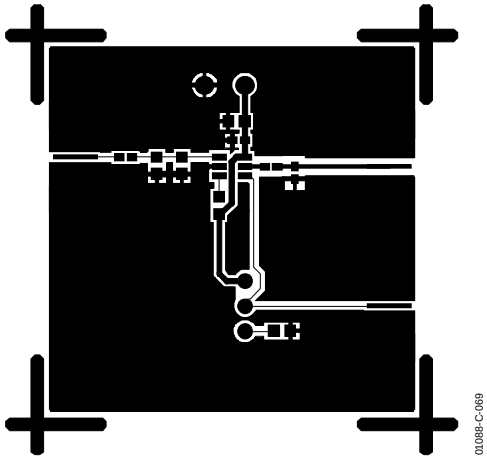

Figure 64. Layout of the Component Side, SOT-23

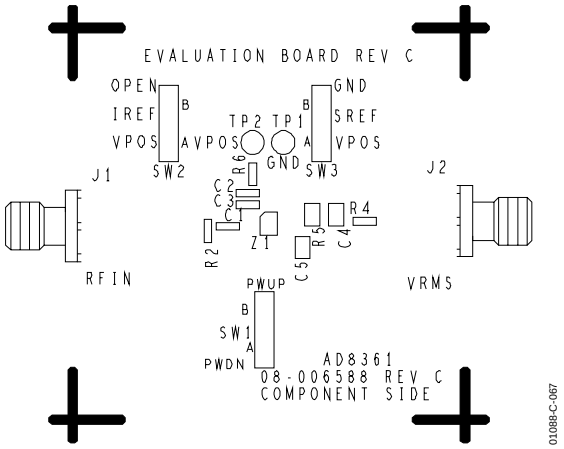

Figure 62. Silkscreen of Component Side, MSOP

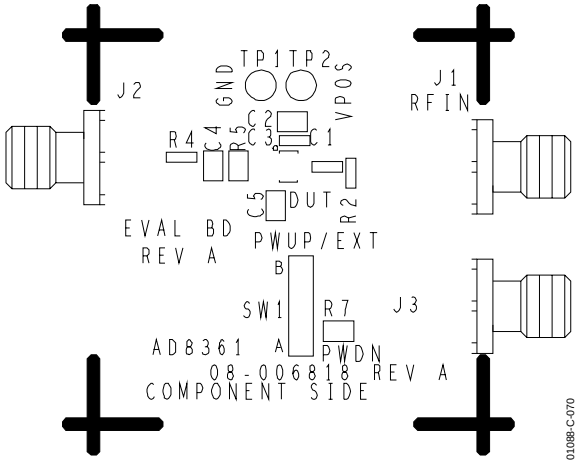

Figure 65. Silkscreen of the Component Side, SOT-23

Problems caused by impedance mismatch may arise using the evaluation board to examine the AD8361 performance. One way to reduce these problems is to put a coaxial 3 dB attenuator on the RFIN SMA connector. Mismatches at the source, cable, and cable interconnection, as well as those occurring on the evaluation board, can cause these problems.

A simple (and common) example of such a problem is triple travel due to mismatch at both the source and the evaluation board. Here the signal from the source reaches the evaluation board and mismatch causes a reflection. When that reflection reaches the source mismatch, it causes a new reflection, which travels back to the evaluation board, adding to the original signal incident at the board. The resultant voltage varies with both cable length and frequency dependence on the relative phase of the initial and reflected signals. Placing the 3 dB pad at the input of the board improves the match at the board and thus reduces the sensitivity to mismatches at the source. When such precautions are taken, measurements are less sensitive to cable length and other fixture issues. In an actual application when the distance between AD8361 and source is short and well defined, this 3 dB attenuator is not needed.

CHARACTERIZATION SETUPS

Equipment

The primary characterization setup is shown in Figure 67. The signal source used was a Rohde & Schwarz SMIQ03B, version 3.90HX. The modulated waveforms used for IS95 reverse link, IS95 nine active channels forward (forward link 18 setting), and W-CDMA 4-channel and 15-channel were generated using the default settings coding and filtering. Signal levels were calibrated into a 50 Ω impedance.

Analysis

The conversion gain and output reference are derived using the coefficients of a linear regression performed on data collected in its central operating range (35 mV rms to 250 mV rms). This range was chosen to avoid areas of operation where offset distorts the linear response. Error is stated in two forms error from linear response to CW waveform and output delta from 2°C performance.

The error from linear response to CW waveform is the difference in output from the ideal output defined by the conversion gain and output reference. This is a measure of both the linearity of the device response to both CW and modulated waveforms. The error in dB uses the conversion gain multiplied by the input as its reference. Error from linear response to CW waveform is not a measure of absolute accuracy, since it is calculated using the gain and output reference of each device. However, it does show the linearity and effect of modulation on the device response. Error from 25°C performance uses the performance of a given device and waveform type as the reference; it is predominantly a measure of output variation with temperature.

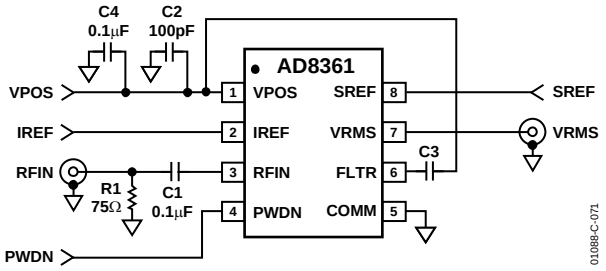

Figure 66. Characterization Board

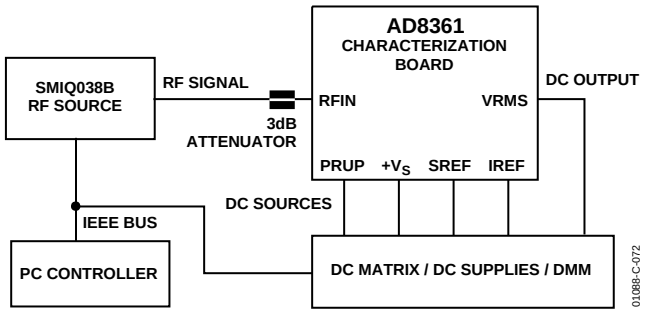

Figure 67. Characterization Setup