DC to 600 MHz, Dual-Digital Variable Gain Amplifiers

Data Sheet **AD8366**

FEATURES

Matched pair of differential, digitally controlled VGAs
Gain range: 4.5 dB to 20.25 dB
0.25 dB gain step size
Operating frequency
- **DC to 150 MHz (2 V p-p)**
- **3 dB bandwidth: 600 MHz**

Noise figure (NF)
- **11.4 dB at 10 MHz at maximum gain**
- **18 dB at 10 MHz at minimum gain**

OIP3: 45 dBm at 10 MHz
HD2/HD3
- **Better than −90 dBc for 2 V p-p output at 10 MHz at maximum gain**

Differential input and output
Adjustable output common-mode
Optional dc output offset correction
Serial/parallel mode gain control
Power-down feature
Single 5 V supply operation

APPLICATIONS

Baseband I/Q receivers
Diversity receivers
Wideband ADC drivers

FUNCTIONAL BLOCK DIAGRAM

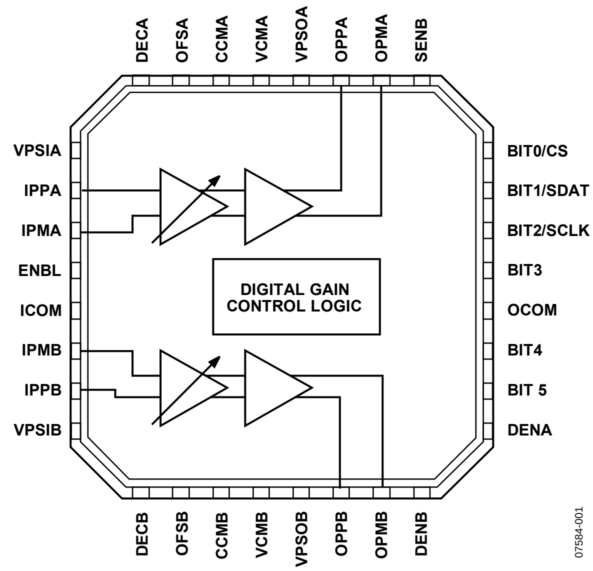

Figure 1.

GENERAL DESCRIPTION

The AD8366 is a matched pair of fully differential, low noise and low distortion, digitally programmable variable gain amplifiers (VGAs). The gain of each amplifier can be programmed separately or simultaneously over a range of 4.5 dB to 20.25 dB in steps of 0.25 dB. The amplifier offers flat frequency performance from dc to 70 MHz, independent of gain code.

The AD8366 offers excellent spurious-free dynamic range, suitable for driving high resolution analog-to-digital converters (ADCs). The NF at maximum gain is 11.4 dB at 10 MHz and increases ~2 dB for every 4 dB decrease in gain. Over the entire gain range, the HD3/HD2 are better than −90 dBc for 2 V p-p at the output at 10 MHz into 200 Ω. The two-tone intermodulation distortion of −90 dBc into 200 Ω translates to an OIP3 of 45 dBm (38 dBVrms). The differential input impedance of 200 Ω provides a well-defined termination. The differential output has a low impedance of ~25 Ω.

The output common-mode voltage defaults to $V_{POS}/2$ but can be programmed via the VCMA and VCMB pins over a range of voltages. The input common-mode voltage also defaults to $V_{POS}/2$ but can be driven down to 1.5 V. A built-in, dc offset compensation loop can be used to eliminate dc offsets from prior stages in the signal chain. This loop can also be disabled if dc-coupled operation is desired.

The digital interface allows for parallel or serial mode gain programming. The AD8366 operates from a 4.75 V to 5.25 V supply and consumes typically 180 mA. When disabled, the part consumes roughly 3 mA. The AD8366 is fabricated using Analog Devices, Inc., advanced silicon-germanium bipolar process, and it is available in a 32-lead exposed paddle LFCSP package. Performance is specified over the −40°C to +85°C temperature range.

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Updated Outline Dimensions ... 28
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3/2011—Rev. 0 to Rev. A

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10/2010—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_S = 200 Ω, Z_L = 200 Ω, f = 10 MHz, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth	3 dB; all gain codes		600		MHz
	1 dB; all gain codes		200		MHz
Slew Rate	Maximum gain		1100		V/µs
	Minimum gain		1500		V/µs
INPUT STAGE	IPPA, IPMA, IPPB, IPMB				
Linear Input Swing	At minimum gain A_V = 4.5 dB, 1 dB gain compression		3.6		V p-p
Differential Input Impedance			217		Ω
Minimum Input Common-Mode Voltage			1.5		V
Maximum Input Common-Mode Voltage			$V_{POS}/2 + 0.075$		V
	Input pins left floating		$V_{POS}/2$		V
GAIN					
Minimum Voltage Gain			4.5		dB
Maximum Voltage Gain			20.25		dB
Gain Step Size	All gain codes		0.25		dB
Gain Step Accuracy	All gain codes		±0.25		dB
Gain Flatness	Maximum gain, DC to 70 MHz		0.1		dB
Gain Mismatch	Channel A/Channel B at minimum/maximum gain code		0.1		dB
Group Delay Flatness	All gain codes, 20% fractional bandwidth, f_C < 100 MHz		<0.5		ns
Mismatch	Channel A and Channel B at same gain code		2		ps
Gain Step Response	Maximum gain to minimum gain		30		ns
	Minimum gain to maximum gain		60		ns
Common-Mode Rejection Ratio			−66.2		dB
OUTPUT STAGE	OPPA, OPMA, OPPB, OPMB, VCMA, VCMB				
Linear Output Swing	1 dB gain compression		6		V p-p
Differential Output Impedance			28		Ω
Output DC Offset	Inputs shorted, offset loop disabled at minimum/maximum gain		−10/−30		mV
	Inputs shorted, offset loop enabled (across all gain codes)		10		mV
Minimum Output Common-Mode Voltage	HD3, HD2 > −90 dBc, 2 V p-p output		1.6		V
Maximum Output Common-Mode Voltage	HD3, HD2 > −90 dBc, 2 V p-p output		3		V
	VCMA and VCMB left floating		$V_{POS}/2$		V
Common-Mode Setpoint Input Impedance			4		kΩ
NOISE/DISTORTION					
3 MHz					
Noise Figure	Maximum gain		11.3		dB
	Minimum gain		18.2		dB
Second Harmonic	2 V p-p output, maximum gain		−82		dBc
	2 V p-p output, minimum gain		−82		dBc
Third Harmonic	2 V p-p output, maximum gain		−87		dBc
	2 V p-p output, minimum gain		−90		dBc
OIP3[1]	2 V p-p composite, maximum gain		34		dBVrms
	2 V p-p composite, minimum gain		35		dBVrms
OIP2[1]	2 V p-p composite, maximum gain		76		dBVrms
	2 V p-p composite, minimum gain		76		dBVrms
Output 1 dB Compression Point[1]	Maximum gain		6.7		dBVrms
	Minimum gain		6.9		dBVrms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
10 MHz					
Noise Figure	Maximum gain		11.4		dB
	Minimum gain		18		dB
Second Harmonic	2 V p-p output, maximum gain		−97		dBc
	2 V p-p output, minimum gain		−96		dBc
Third Harmonic	2 V p-p output, maximum gain		−97		dBc
	2 V p-p output, minimum gain		−90		dBc
OIP3[1]	2 V p-p composite, maximum gain		38		dBVrms
	2 V p-p composite, minimum gain		36		dBVrms
OIP2[1]	2 V p-p composite, maximum gain		72		dBVrms
	2 V p-p composite, minimum gain		76		dBVrms
Output 1 dB Compression Point[1]	Maximum gain		7		dBVrms
	Minimum gain		6.7		dBVrms
50 MHz					
Noise Figure	Maximum gain		11.8		dB
	Minimum gain		18.2		dB
Second Harmonic	2 V p-p output, maximum gain		−82		dBc
	2 V p-p output, minimum gain		−84		dBc
Third Harmonic	2 V p-p output, maximum gain		−80		dBc
	2 V p-p output, minimum gain		−71		dBc
OIP3[1]	2 V p-p composite, maximum gain		32		dBVrms
	2 V p-p composite, minimum gain		26		dBVrms
OIP2[1]	2 V p-p composite, maximum gain		71		dBVrms
	2 V p-p composite, minimum gain		78		dBVrms
Output 1 dB Compression Point[1]	Maximum gain		6.7		dBVrms
	Minimum gain		6.7		dBVrms
DIGITAL LOGIC	SENB, DENA, DENB, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5				
Input High Voltage, V_{INH}			2.2		V
Input Low Voltage, V_{INL}			1.2		V
Input Capacitance, C_{IN}			1		pF
Input Resistance, R_{IN}			50		kΩ
SPI INTERFACE TIMING	SENB = high				
f_{SCLK}	Serial clock frequency (maximum)		44.4		MHz
t_1	CS rising edge to first SCLK rising edge (minimum)		7.5		ns
t_2	SCLK high pulse width (minimum)		7.5		ns
t_3	SCLK low pulse width (minimum)		15		ns
t_4	SCLK falling edge to CS low (minimum)		7.5		ns
t_5	SDAT setup time (minimum)		7.5		ns
t_6	SDAT hold time (minimum)		15		ns
PARALLEL PORT TIMING	SENB = low				
t_7	DENA/DENB high pulse width (minimum)		7.5		ns
t_8	DENA/DENB low pulse width (minimum)		15		ns
t_9	BITx setup time (minimum)		7.5		ns
t_{10}	BITx hold time (minimum)		7.5		ns
POWER AND ENABLE	VPSIA, VPSIB, VPSOA, VPSOB, ICOM, OCOM, ENBL				
Supply Voltage Range		4.75		5.25	V
Total Supply Current	ENBL = 5 V		180		mA
Disable Current	ENBL = 0 V		3.2		mA
Disable Threshold			1.65		V
Enable Response Time	Delay following high-to-low transition until device meets full specifications		150		ns
Disable Response Time	Delay following low-to-high transition until device produces full attenuation		3		µs

[1] To convert to dBm for a 200 Ω load impedance, add 7 dB to the dBVrms value.

PARALLEL AND SERIAL INTERFACE TIMING

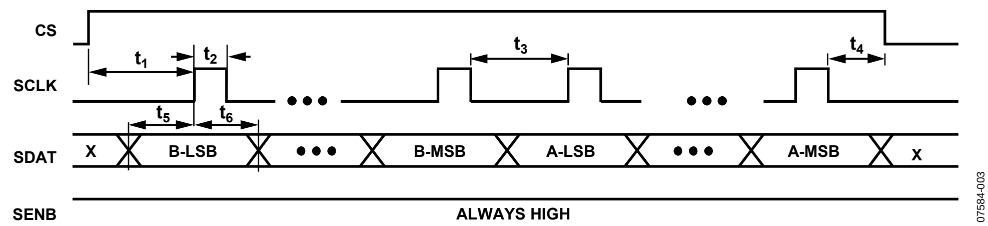

Figure 2. SPI Port Timing Diagram

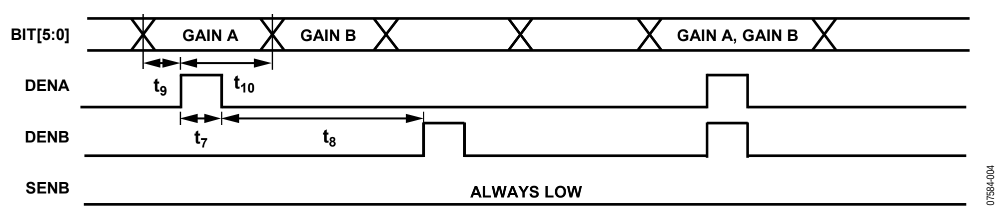

Figure 3. Parallel Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages, VPSIx and VPSOx	5.5 V
ENBL, SENB, DENA, DENB, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5	5.5 V
IPPA, IPMA, IPPB, IPMB	5.5 V
OPPA, OPMA, OPPB, OPMB	5.5 V
OFSA, OFSB	5.5 V
DECA, DECB, VCMA, VCMB, CCMA, CCMB	5.5 V
Internal Power Dissipation	1.4 W
θ_{JA} (With Pad Soldered to Board)	45.4°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

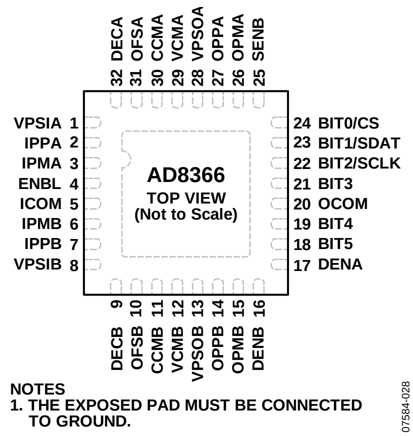

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 13, 28	VPSIA, VPSIB, VPSOB, VPSOA	Input and Output Stage Positive Supply Voltage (4.75 V to 5.25 V).
2, 3, 6, 7	IPPA, IPMA, IPMB, IPPB	Differential Inputs.
4	ENBL	Chip Enable. Pull this pin high to enable.
5, 20	ICOM, OCOM	Input and Output Ground Pins. Connect these pins via the lowest possible impedance to ground.
9, 32	DECB, DECA	$V_{POS}/2$ Reference Decoupling Node. Connect a decoupling capacitor from these nodes to ground.
10, 31	OFSB, OFSA	Output Offset Correction Loop Compensation. Connect a capacitor from these nodes to ground to enable the correction loop. Tie this pin to ground to disable.
11, 30	CCMB, CCMA	Connect These Nodes to Ground.
12, 29	VCMB, VCMA	Output Common-Mode Setpoint. These pins default to $V_{POS}/2$ if left open. Drive these pins from a low impedance source to change the output common-mode voltage.
14, 15, 26, 27	OPPB, OPMB, OPMA, OPPA	Differential Outputs.
16, 17	DENB, DENA	Data Enable. Pull these pins high to address each or both channels for parallel gain programming. These pins are not used in serial mode.
18, 19, 21, 22, 23, 24	BIT5, BIT4, BIT3, BIT2/SCLK, BIT1/SDAT, BIT0/CS	Parallel Data Path (When SENB Is Low). When SENB is high, BIT0 becomes a chip select (CS), BIT1 becomes a serial data input (SDAT), and BIT2 becomes a serial clock (SCLK). BIT3 to BIT5 are not used in serial mode.
25	SENB	Serial Interface Enable. Pull this pin high for serial gain programming mode and pull this pin low for parallel gain programming mode.
	EPAD	The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, Z_S = 200 Ω, Z_L = 200 Ω, f = 10 MHz, unless otherwise noted.

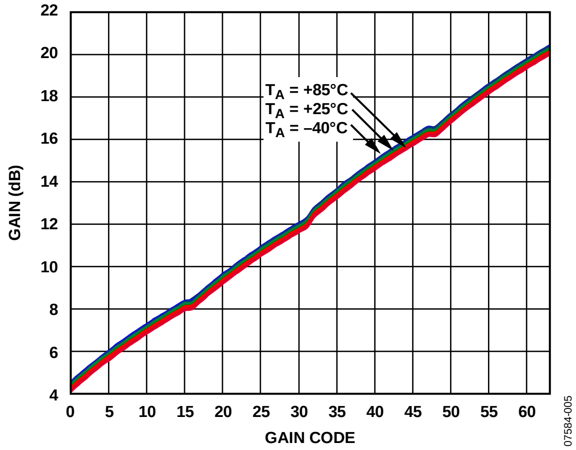

Figure 5. Gain vs. Gain Code at 500 kHz, 3 MHz, 10 MHz, and 50 MHz

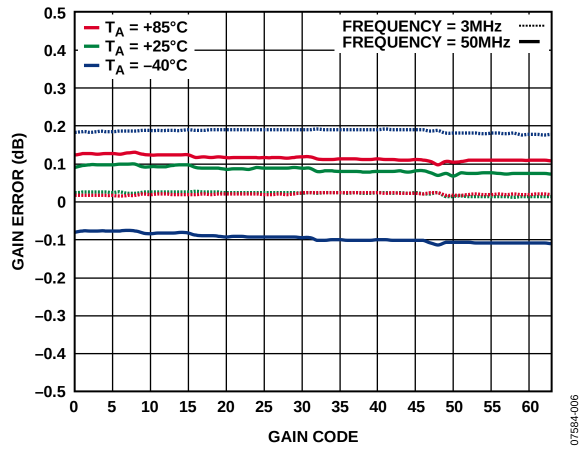

Figure 8. Gain Error vs. Gain Code, Error Normalized to 10 MHz

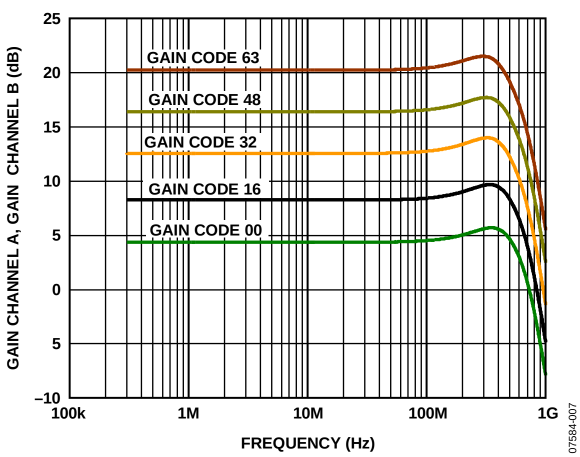

Figure 6. Frequency Response vs. Gain Code

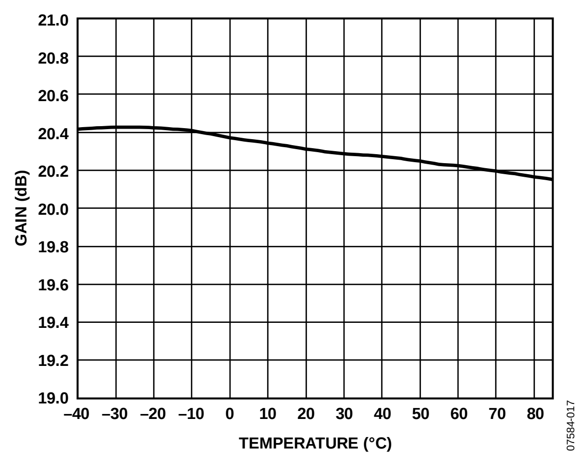

Figure 9. Gain vs. Temperature at Maximum Gain at 10 MHz

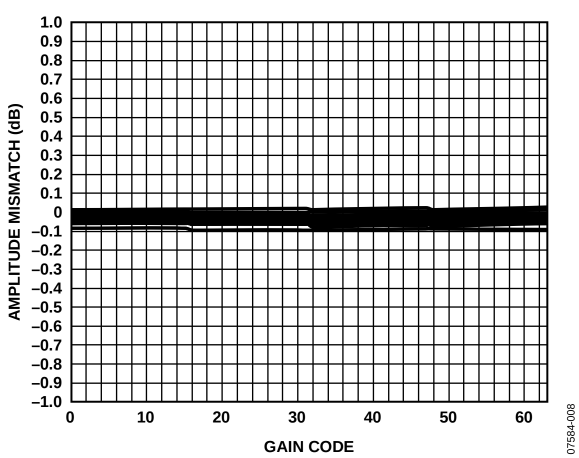

Figure 7. Channel A-to-Channel B Amplitude Mismatch vs. Gain Code, 2 V p-p Output

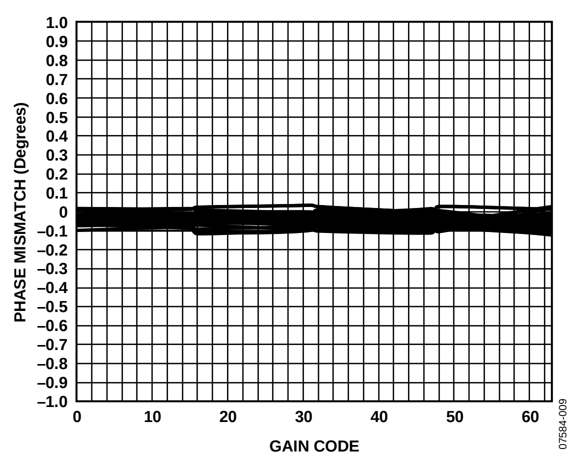

Figure 10. Channel A-to-Channel B Phase Mismatch vs. Gain Code, 2 V p-p Output

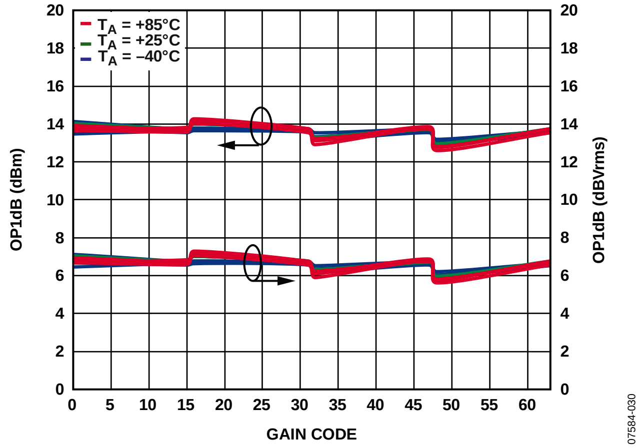

Figure 11. OP1dB vs. Gain Code at 500 kHz, 3 MHz, 10 MHz, and 50 MHz

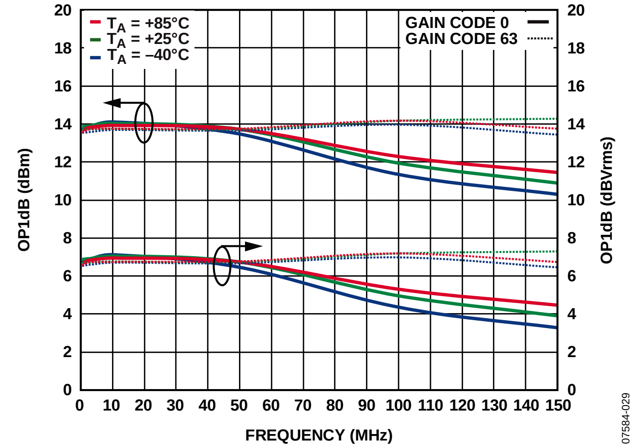

Figure 14. OP1dB vs. Frequency at Gain Code 0 and Gain Code 63

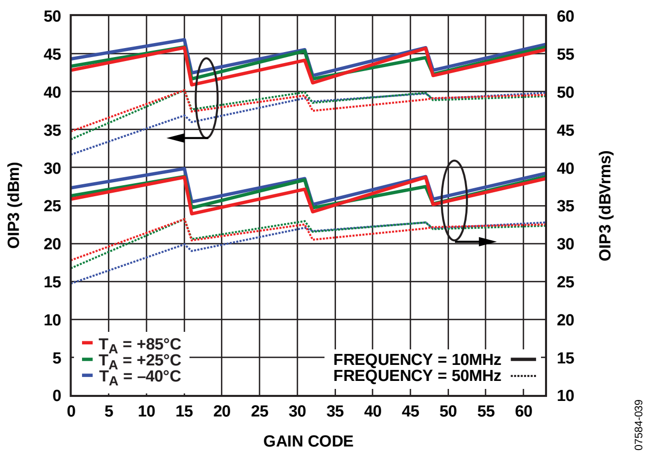

Figure 12. OIP3 vs. Gain Code at 10 MHz and 50 MHz Frequency, 2 V p-p Composite Output

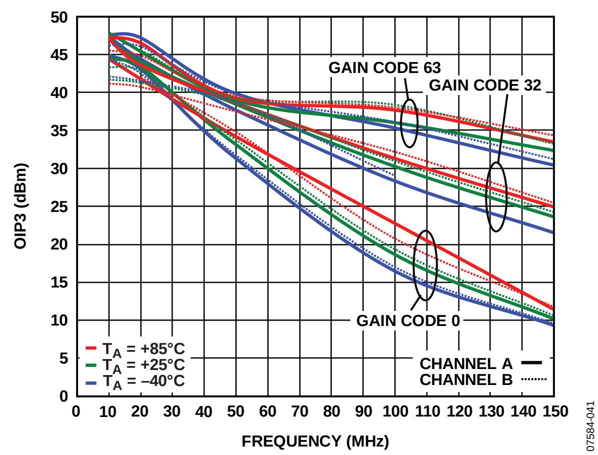

Figure 15. OIP3 vs. Frequency, Gain Code 0, Gain Code 32, and Gain Code 63, 2 V p-p Composite Output

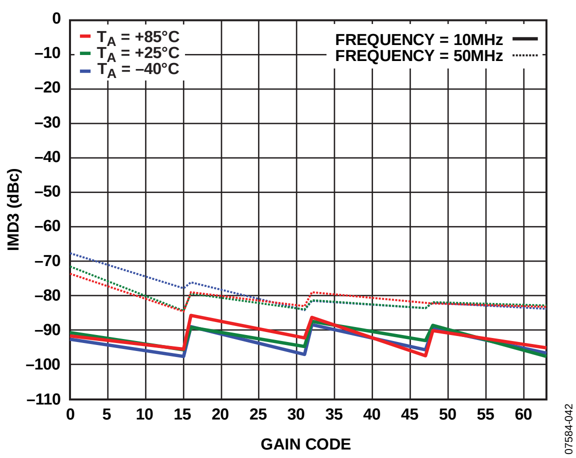

Figure 13. Two-Tone Output IMD3 vs. Gain Code at 10 MHz and 50 MHz Frequency, 2 V p-p Composite Output

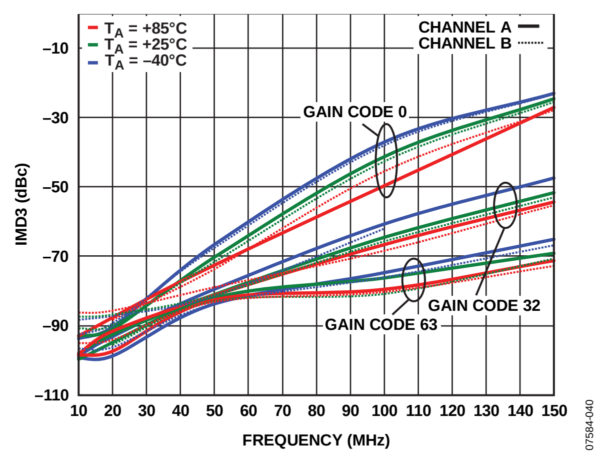

Figure 16. Two-Tone Output IMD3 vs. Frequency at Gain Code 0, Gain Code 32, and Gain Code 63, 2 V p-p Composite Output

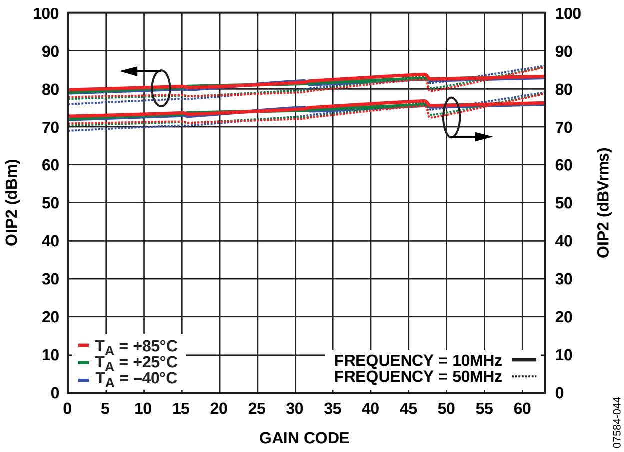

Figure 17. OIP2 vs. Gain Code at 10 MHz and 50 MHz Frequency, 2 V p-p Composite Output

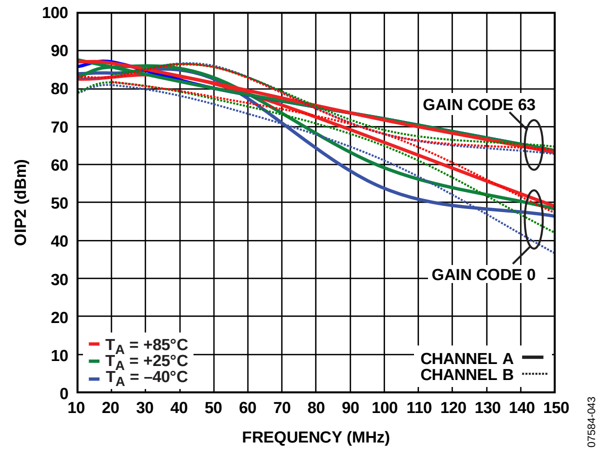

Figure 20. OIP2 vs. Frequency at Gain Code 0 and Gain Code 63, 2 V p-p Composite Output

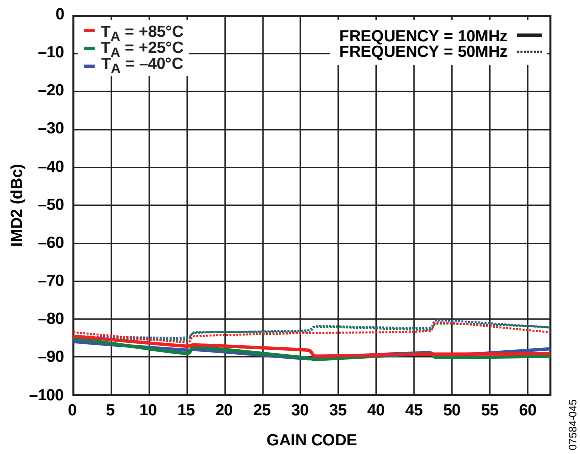

Figure 18. Two-Tone Output IMD2 vs. Gain Code at 10 MHz and 50 MHz Frequency, 2 V p-p Composite Output

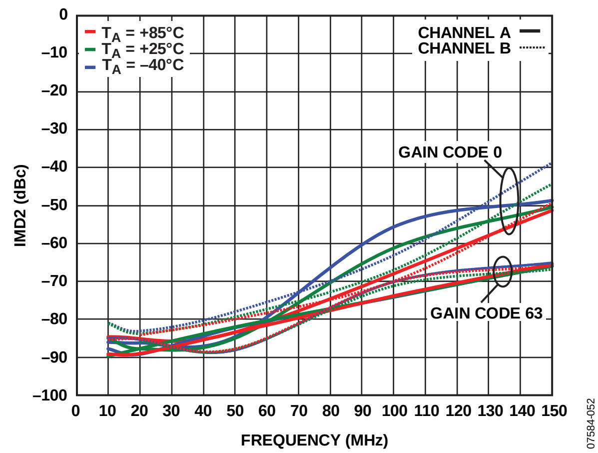

Figure 21. Two-Tone Output IMD2 vs. Frequency, Gain Code 0 and Gain Code 63, 2 V p-p Composite Output

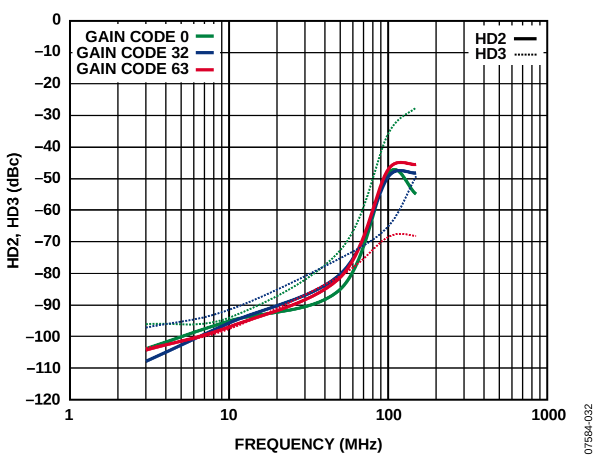

Figure 19. Harmonic Distortion vs. Frequency at Gain Code 0, Gain Code 32, and Gain Code 63, 2 V p-p Output

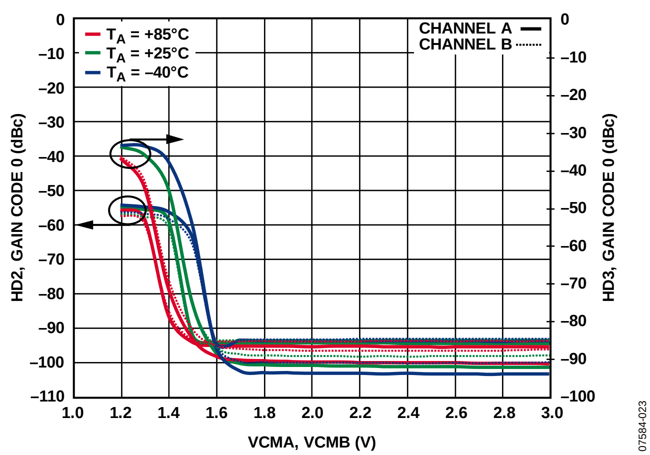

Figure 22. HD3/HD2 vs. V_{OCM} at 10 MHz, Gain Code 0, 2 V p-p Output

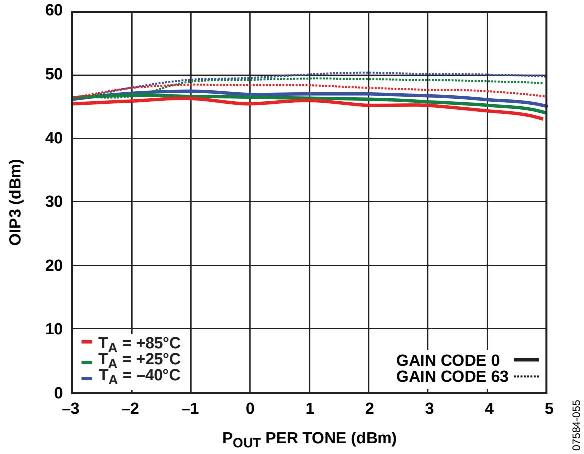

Figure 23. OIP3 vs. Output Power (P_{OUT}) at Minimum and Maximum Gain Codes, 10 MHz Frequency

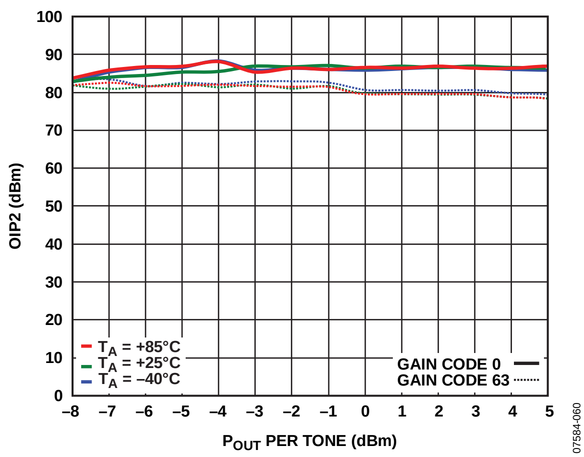

Figure 24. OIP2 vs. Output Power (P_{OUT}) at Minimum and Maximum Gain Codes, 10 MHz Frequency

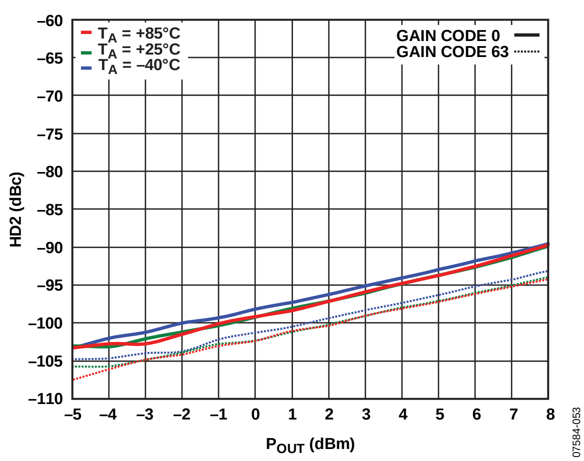

Figure 25. HD2 vs. Output Power (P_{OUT}) at Gain Code 0 and Gain Code 63, 10 MHz Frequency

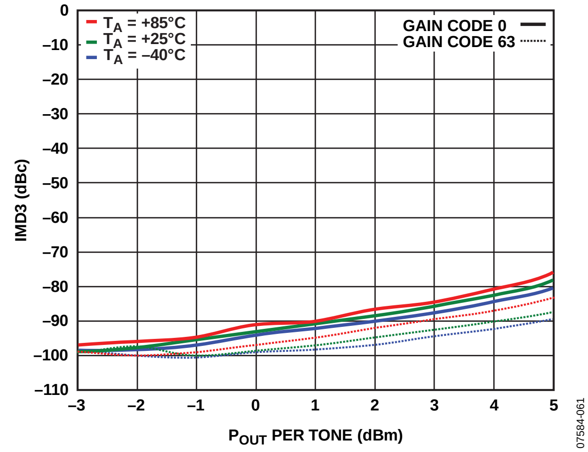

Figure 26. IMD3 vs. Output Power (P_{OUT}) at Minimum-to-Maximum Gain Codes, 10 MHz Frequency

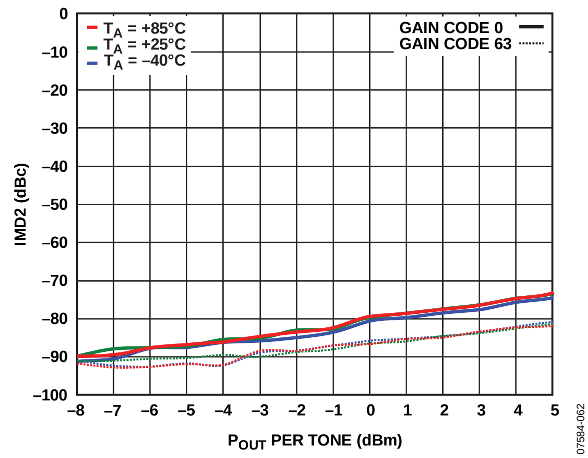

Figure 27. IMD2 vs. Output Power (P_{OUT}) at Minimum and Maximum Gain Codes, 10 MHz Frequency

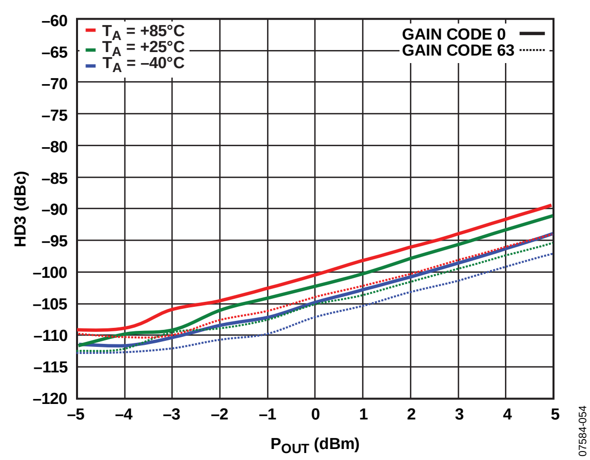

Figure 28. HD3 vs. Output Power (P_{OUT}) for Gain Code 0 and Gain Code 63, 10 MHz Frequency

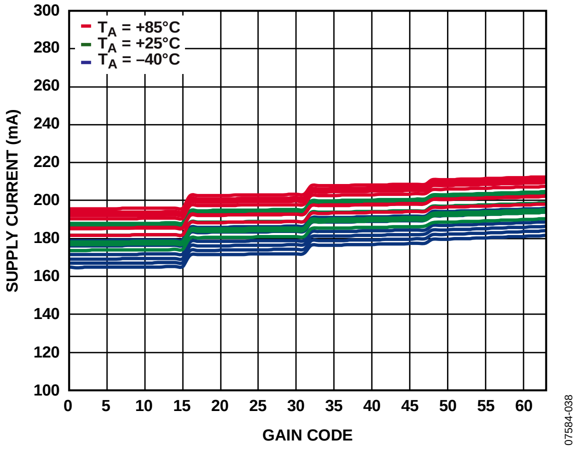

Figure 29. Supply Current vs. Gain Code at 10 MHz

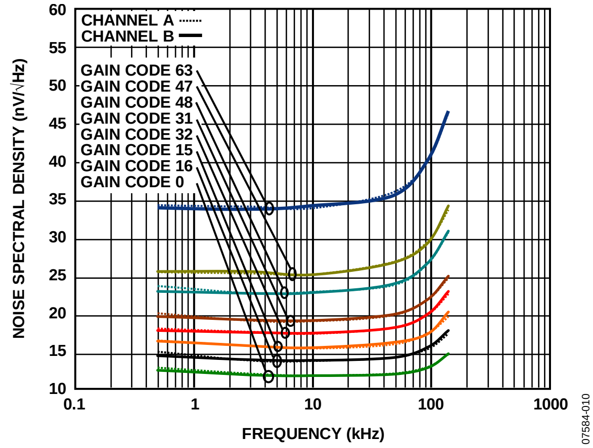

Figure 32. Noise Spectral Density vs. Frequency

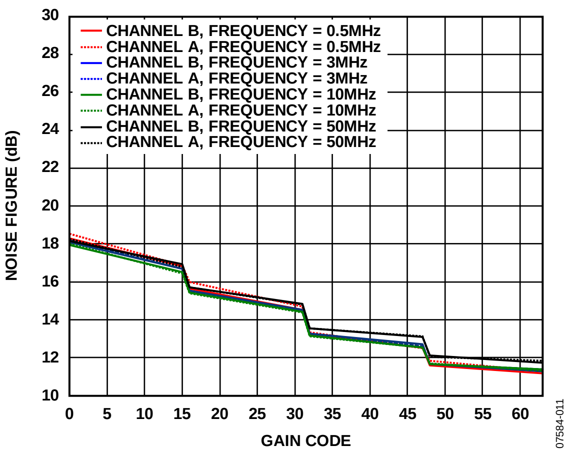

Figure 30. Noise Figure vs. Gain Code at 0.5 MHz, 3 MHz, 10 MHz, and 50 MHz

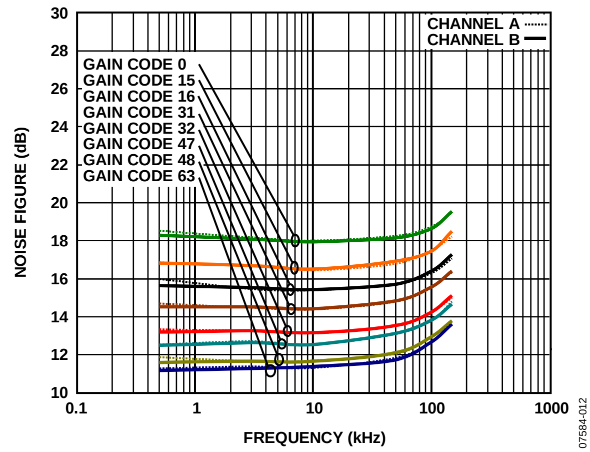

Figure 33. Noise Figure vs. Frequency

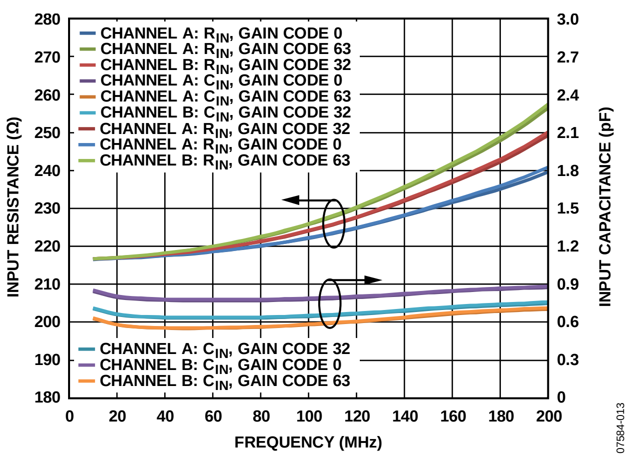

Figure 31. Differential Parallel Input Resistance and Capacitance vs. Frequency

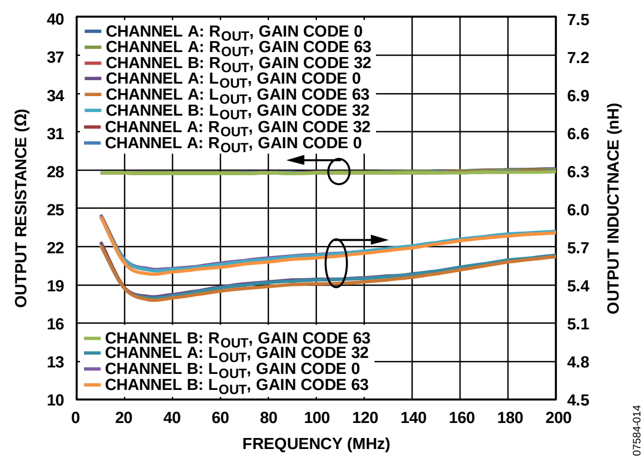

Figure 34. Differential Series Output Resistance and Inductance vs. Frequency

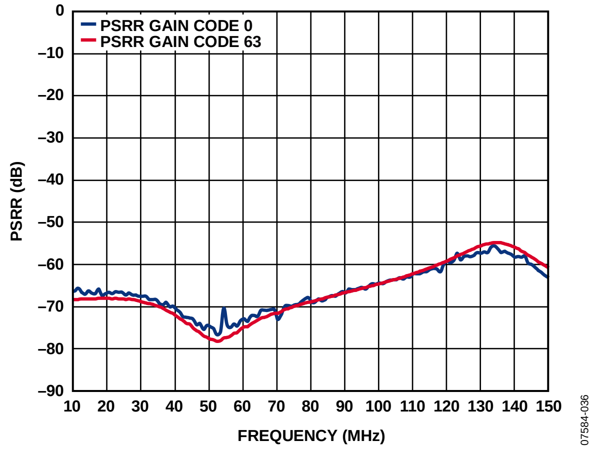

Figure 35. Power Supply Rejection Ratio (PSRR) vs. Frequency

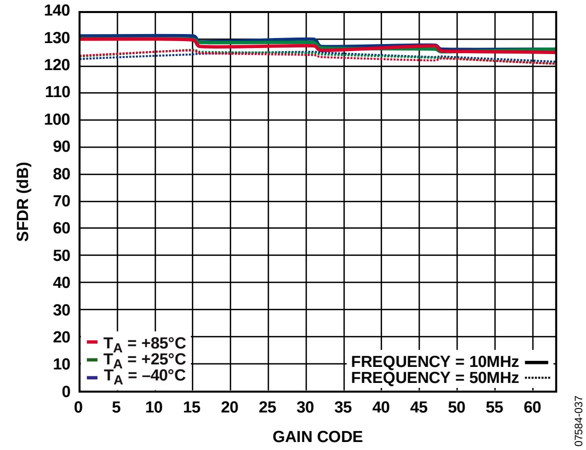

Figure 38. SFDR vs. Gain Code at 10 MHz and 50 MHz, 1 Hz Analysis Bandwidth

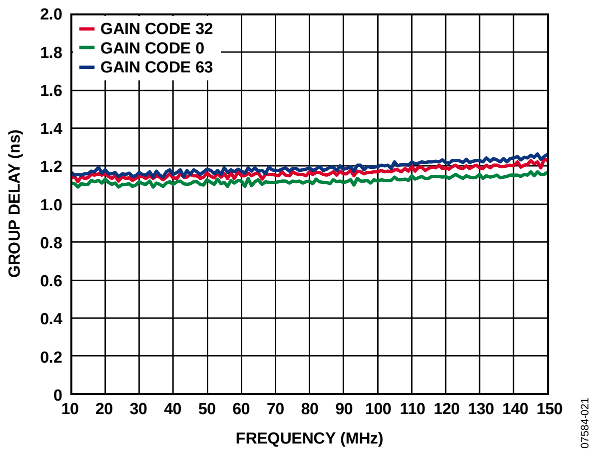

Figure 36. Group Delay vs. Frequency at Gain Code 0, Gain Code 32, and Gain Code 63

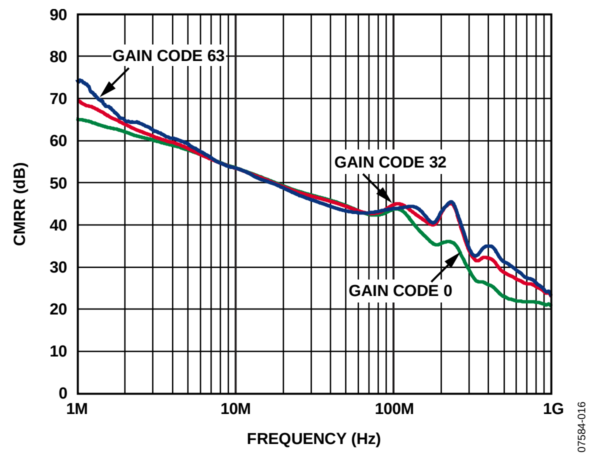

Figure 39. Common-Mode Rejection Ratio (CMRR) vs. Frequency

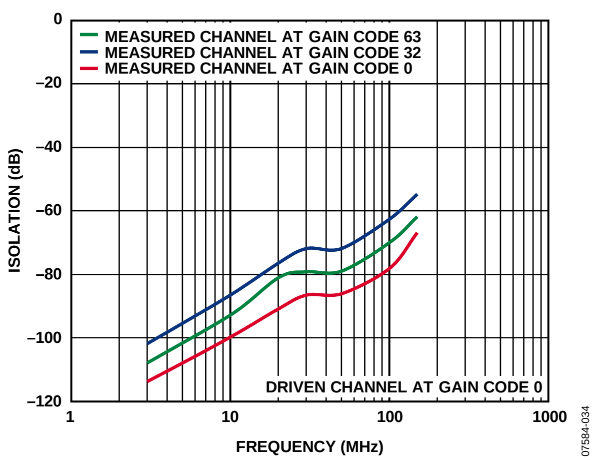

Figure 37. Channel-to-Channel Isolation vs. Frequency, Channel A Driven, Channel B Measured

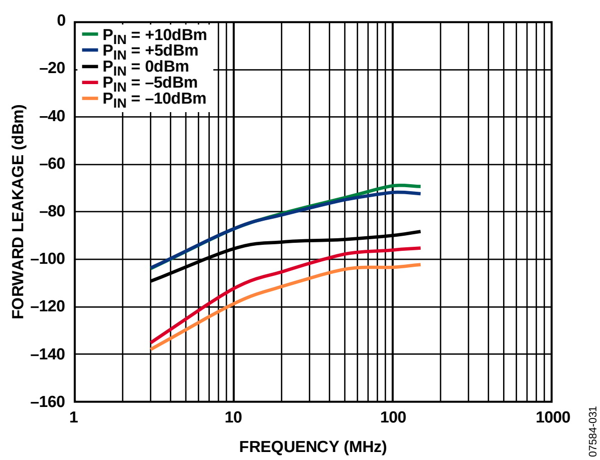

Figure 40. Forward Leakage vs. Frequency, Part Disabled

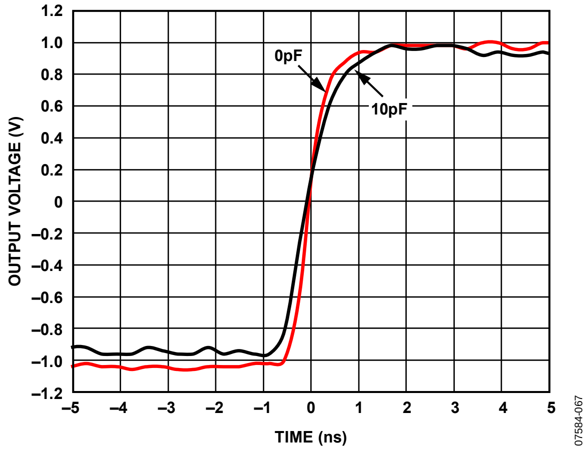

Figure 41. Large Signal Pulse Response, Gain Code 0, Input Signal 1.2 V p-p, 0 pF and 10 pF Capacitive Loading Conditions

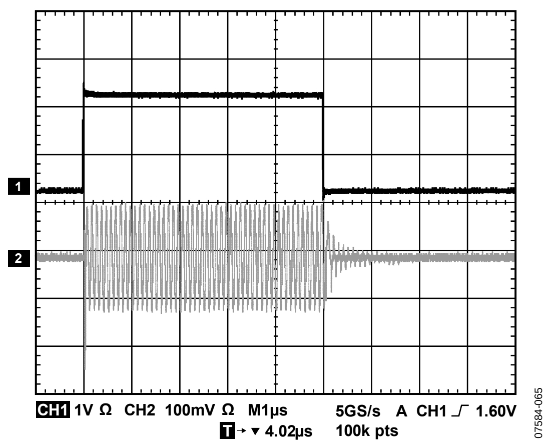

Figure 42. ENBL Time Domain Response

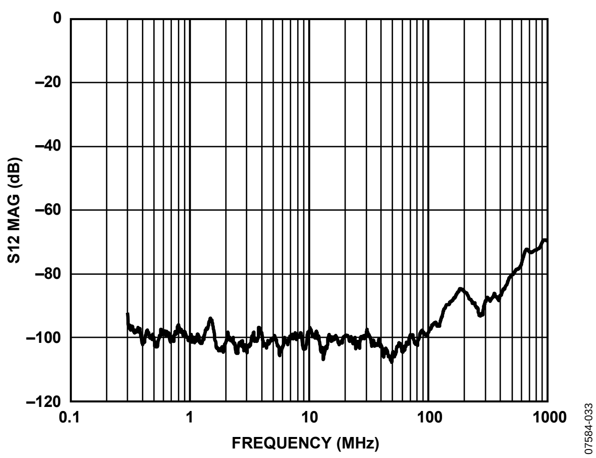

Figure 43. Reverse Isolation (S12) vs. Frequency

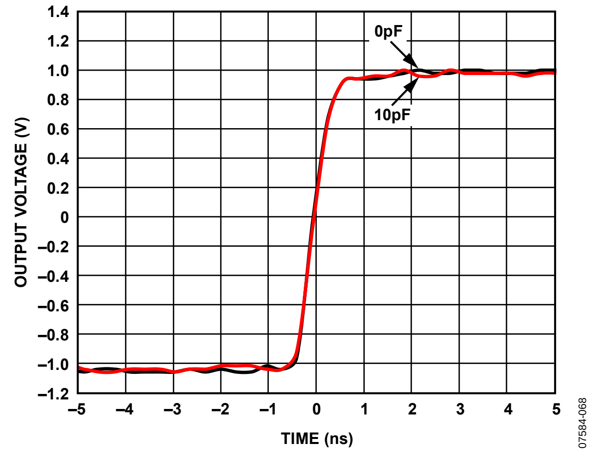

Figure 44. Large Signal Pulse Response, Gain Code 63, Input Signal 240 mV p-p, 0 pF and 10 pF Capacitive Loading Conditions

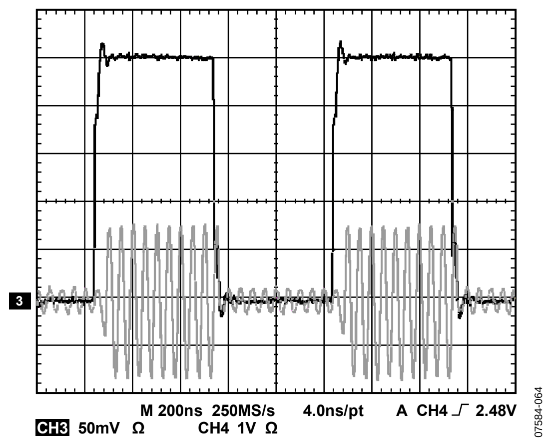

Figure 45. Gain Step Time Domain Response, Minimum-to-Maximum Gain (Time Scale 200 ns/division), CH4 = Digital Control Inputs

CIRCUIT DESCRIPTION

The AD8366 is a dual, differential, digitally controlled VGA with 600 MHz of 3 dB bandwidth and a gain range of 4.5 dB to 20.25 dB adjustable in 0.25 dB steps. Using a proprietary variable gain architecture, the AD8366 is able to achieve excellent linearity (45 dBm) and noise performance (11.7 nV/√Hz) at 10 MHz at minimum gain. Intended for use in direct conversion systems, the part also includes dc offset correction that can be disabled easily by grounding either OFSA or OFSB. In addition, the part offers an adjustable output common-mode range of 1.6 V to 3 V.

The main signal path is shown in Figure 46. It consists of an input transconductance, a variable-gain cell, and an output transimpedance amplifier.

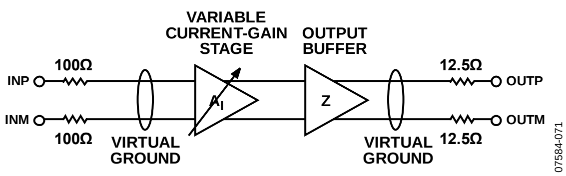

Figure 46. Main Signal Path

The input transconductance provides a broadband 200 Ω differential termination and converts the input voltage to a current. This current is fed into the variable current-gain cell. The output of this cell goes into the transimpedance stage, which generates the output voltage. The transimpedance is fixed at 500 Ω, with a roughly 25 Ω differential output impedance.

INPUTS

The inputs to the digitally-controlled VGAs in the AD8366 are differential and can be either ac- or dc-coupled. The AD8366 synthesizes a 200 Ω (differential) input impedance, with a return loss (re: 200 Ω) of better than 10 dB to 200 MHz. The nominal common-mode input voltage to the part is $V_{POS}/2$, but the AD8366 can be dc-coupled to parts with lower common modes if these parts can sink current. The amount of current sinking required depends on the input common-mode level and is given by

$$I_{SINK}\ (per\ leg) = (V_{POS}/2 - V_{ICM})/100$$

The input common-mode range is 1.5 V to $V_{POS}/2$.

OUTPUTS

The outputs of the digitally-controlled VGAs are differential and can be either ac- or dc-coupled. The AD8366 synthesizes a 25 Ω differential output impedance, with a return loss (re: 25 Ω) of better than 10 dB to 120 MHz. The nominal common-mode output voltage is $V_{POS}/2$; however, it can be lowered or raised by driving the VCMA or VCMB pins.

OUTPUT DIFFERENTIAL OFFSET CORRECTION

To prevent significant levels of offset from appearing at the outputs of the AD8366, each digitally controlled VGA has a differential offset correction loop, as shown in Figure 47. This loop senses any differential offset at the output and corrects for it by injecting an opposing current at the input differential ground. The loop is able to correct for input dc offsets of up to ±20 mV. Because the loop automatically nulls out any dc or low frequency offset, the effect of the loop is to introduce a high-pass corner into the transfer function of the digitally controlled VGA. The location of this high-pass corner depends on both the gain setting and the value of the capacitor connected to the OFSx pin (OFSA for DVGA A and OFSB for DVGA B) and is given by

$$f_{3dB,HP}(\text{kHz}) = \frac{4300(1.037)^{GC} + 4000}{2\pi(C_{OFS} + 10)}$$

where:
GC is the gain code (a value from 0 to 63).
C_{OFS} is the value of the capacitance connected to OFSA or OFSB, in picofarads (pF).

The offset correction loop can be disabled by grounding either OFSA or OFSB.

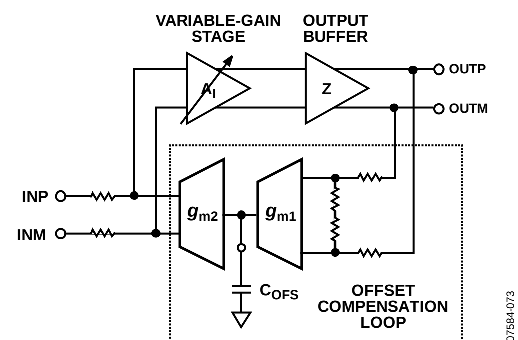

Figure 47. Differential Offset Correction Loop

OUTPUT COMMON-MODE CONTROL

To interface to ADCs that require different input common-mode voltages, the AD8366 has an adjustable output common-mode level. The output common-mode level is normally set to $V_{POS}/2$; however, it can be changed between 1.6 V and 3 V by driving the VCMA pin or the VCMB pin. The input equivalent circuit for the VCMA pin is shown in Figure 48; the VCMB pin has the same input equivalent circuit.

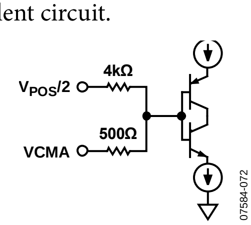

Figure 48. Input Equivalent Circuit for VCMA

GAIN CONTROL INTERFACE

The AD8366 provides two methods of digital gain control: serial or parallel. When the SENB pin is pulled low, the part is in parallel gain control mode. In this mode, the two digitally controlled VGAs can be programmed simultaneously, or one at a time, depending on the levels at DENA and DENB. If the SENB pin is pulled high, the part is in serial gain control mode, with Pin 24, Pin 23, and Pin 22 corresponding to the CS, SDAT, and SCLK signals, respectively.

The voltage gain of the AD8366 is well approximated by

$$Gain\ (\text{dB}) = GainCode \times 0.253 + 4.5$$

Note that at several major transitions (15 to 16, 31 to 32, and 47 to 48), the gain changes significantly less (0 dB step) or significantly more (0.5 dB step) than the desired 0.25 dB step. This is inherent in the design of the part and is related to the partitioning of the variable gain block into a fine-gain and a coarse-gain section.

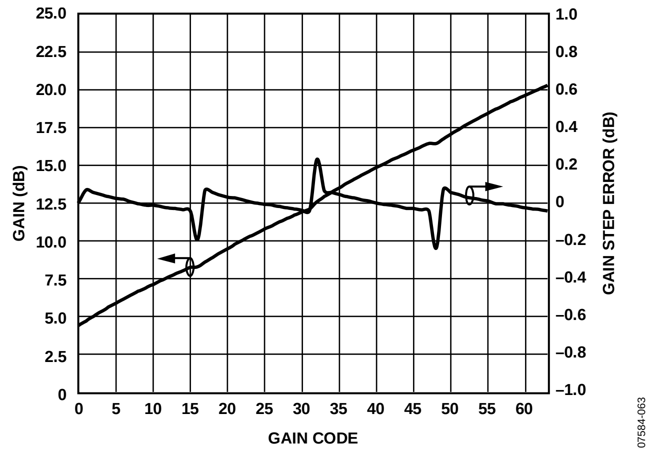

Figure 49. Gain and Gain Step Error vs. Gain Code at 10 MHz

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 50 shows the basic connections for operating the AD8366. A voltage from 4.75 V to 5.25 V must be applied to the supply pins. Each supply pin must be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1 μF placed as close as possible to the device.

The differential input impedance is 200 Ω and sits at a nominal common-mode voltage of $V_{POS}/2$. The inputs can be dc-coupled or ac-coupled. If using direct dc coupling, the common-mode voltage, V_{CM}, can range from 1.5 V to $V_{POS}/2$.

The output buffers of the AD8366 are low impedance around 25 Ω designed to drive ADC inputs. The output common-mode voltage defaults to $V_{POS}/2$; however, it can be adjusted by applying a desired external voltage to VCMA/VCMB. The common-mode voltage can be adjusted from 1.6 V to 3.0 V without significant harmonic distortion degradation.

To enable the AD8366, the ENBL pin must be pulled high. Taking ENBL low disables the device, reducing current consumption to approximately 3 mA at ambient temperature.

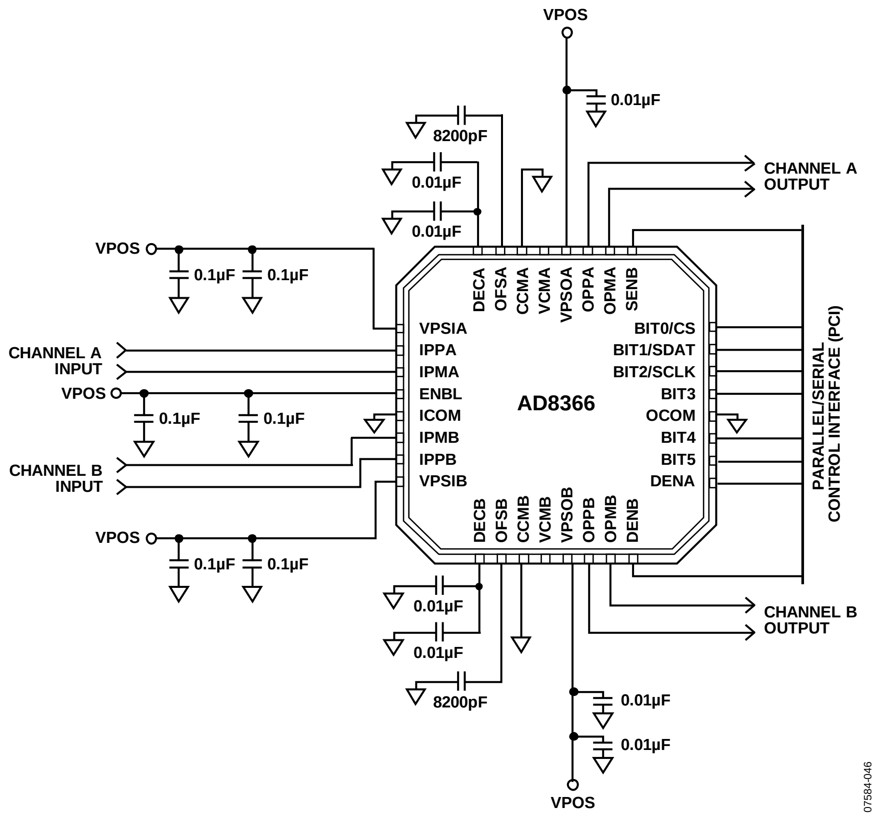

Figure 50. Basic Connections

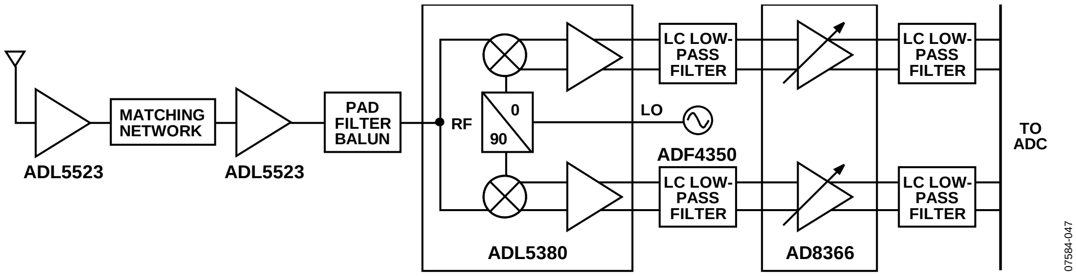

Figure 51. Direct Conversion Receiver Block Diagram

DIRECT CONVERSION RECEIVER DESIGN

A direct conversion receiver directly demodulates an RF modulated carrier to baseband frequencies, where the signals can be detected and the conveyed information recovered. Eliminating the IF stages and directly converting the signal to effectively zero IF results in reduced component count. The image problems associated with the traditional superheterodyne architectures can be ignored as well. However, there are different challenges associated with direct conversion that include LO leakage, dc offsets, quadrature imperfections, and image rejection. LO leakage causes self mixing that results in squaring of the LO waveform which generates a dc offset that falls in band for the direct conversion receiver. Residual dc offsets create a similar interfering signal that falls in band. I/Q amplitude and phase mismatch lead to degraded SNR performance and poor image rejection in the direct conversion system. Figure 51 shows the block diagram for a direct conversion receiver system.

QUADRATURE ERRORS AND IMAGE REJECTION

An overall RF-to-baseband EVM performance was measured with the ADL5380 IQ demodulator preceding the AD8366, as shown in Figure 56. In this setup, no LC low-pass filters were used between the ADL5380 and AD8366. A 1900 MHz W-CDMA RF signal with a 3.84 MHz symbol rate was used. The local oscillator (LO) is set at 1900 MHz to obtain a zero IF baseband signal. The gain of the AD8366 is set to maximum gain (~20.25 dB). Figure 52 shows the SNR vs. the input power of the cascaded system for a 5 MHz analysis bandwidth. The broad input power range over which the system exhibits strong SNR performance reflects the superior dynamic range of the AD8366.

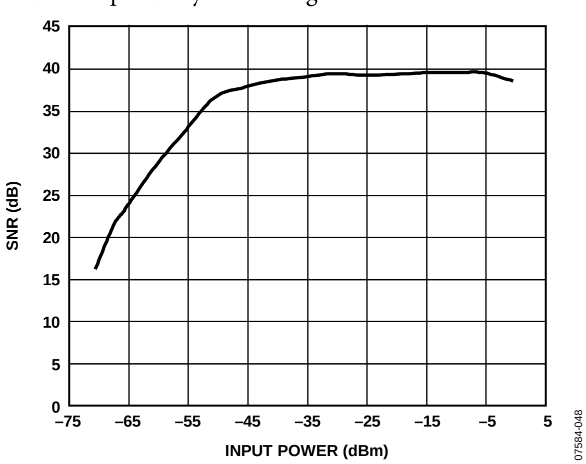

Figure 52. SNR vs. RF Input Power Level

The image rejection ratio is the ratio of the intermediate frequency (IF) signal level produced by the desired input frequency to that produced by the image frequency. The image rejection ratio is expressed in decibels (dB). Appropriate image rejection is critical because the image power can be much higher than that of the desired signal, thereby plaguing the downconversion process. Amplitude and phase balance between the I/Q channels are critical for high levels of image rejection. Image rejection of greater than 47 dB was measured for the combined ADL5380 and the AD8366 for a 5 MHz baseband frequency, as seen in Figure 53. This level of image rejection corresponds to a ±0.5° phase mismatch and a ±0.05 dB of amplitude mismatch for the combined ADL5380 and AD8366. Looking back to Figure 7 and Figure 10, the AD8366 exhibits only ±0.05 dB of amplitude mismatch and ±0.05° of phase mismatch, thus implying that the AD8366 does not introduce additional amplitude and phase imbalance.

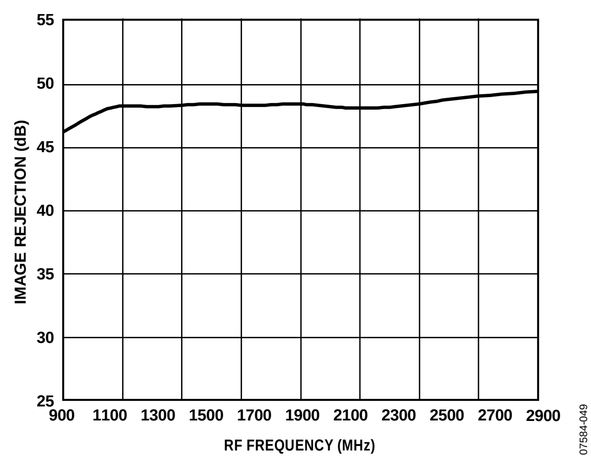

Figure 53. Image Rejection vs. RF Frequency

LOW FREQUENCY IMD3 PERFORMANCE

To measure the IMD3 data at low frequencies, wideband transformer baluns from North Hills Signal Processing Corp. were used, specifically the 0301BB and the 0520BB. Figure 55 shows the IMD3 performance vs. frequency for a 2 V p-p composite output. The IMD3 performance was also measured for the combined ADL5380 and AD8366 system, as shown in Figure 56, with an FFT spectrum analyzer. An FFT spectrum analyzer works very similar to a typical ADC, the input signal is digitized at a high sampling rate that is then passed through an antialiasing filter. The resulting signal is transformed to the frequency domain using fast Fourier transforms (FFT).

The single-ended RF signal from the source generator is converted to a differential signal using a balun that gets demodulated and down converted to differential IF signals through the ADL5380. This differential IF signal drives the AD8366, thus eliminating the need for low frequency baluns. Figure 54 shows the IMD3 performance vs. frequency over the 500 kHz to 5 MHz range for minimum and maximum gain code setting on the AD8366. During the measurements, the output was set to 2 V p-p composite.

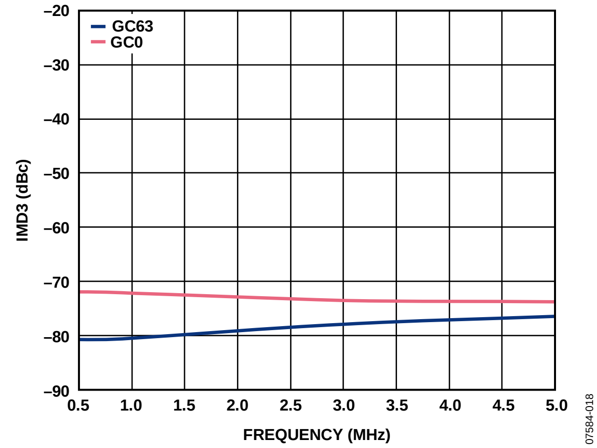

Figure 54. System IMD3 vs. Frequency, 2 V p-p Composite at the Output of the AD8366

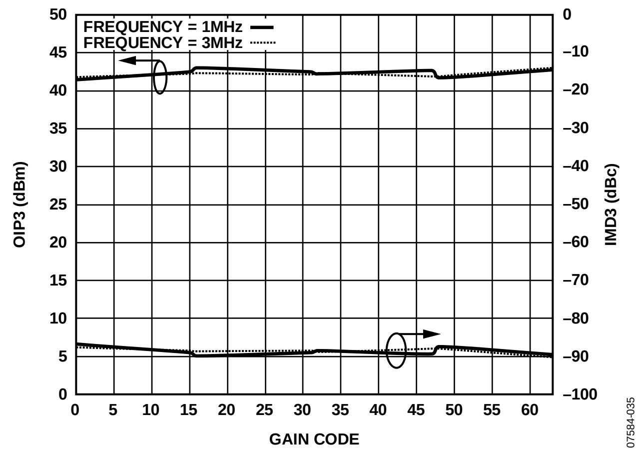

Figure 55. OIP3 on Low Frequency, 2 V p-p Composite

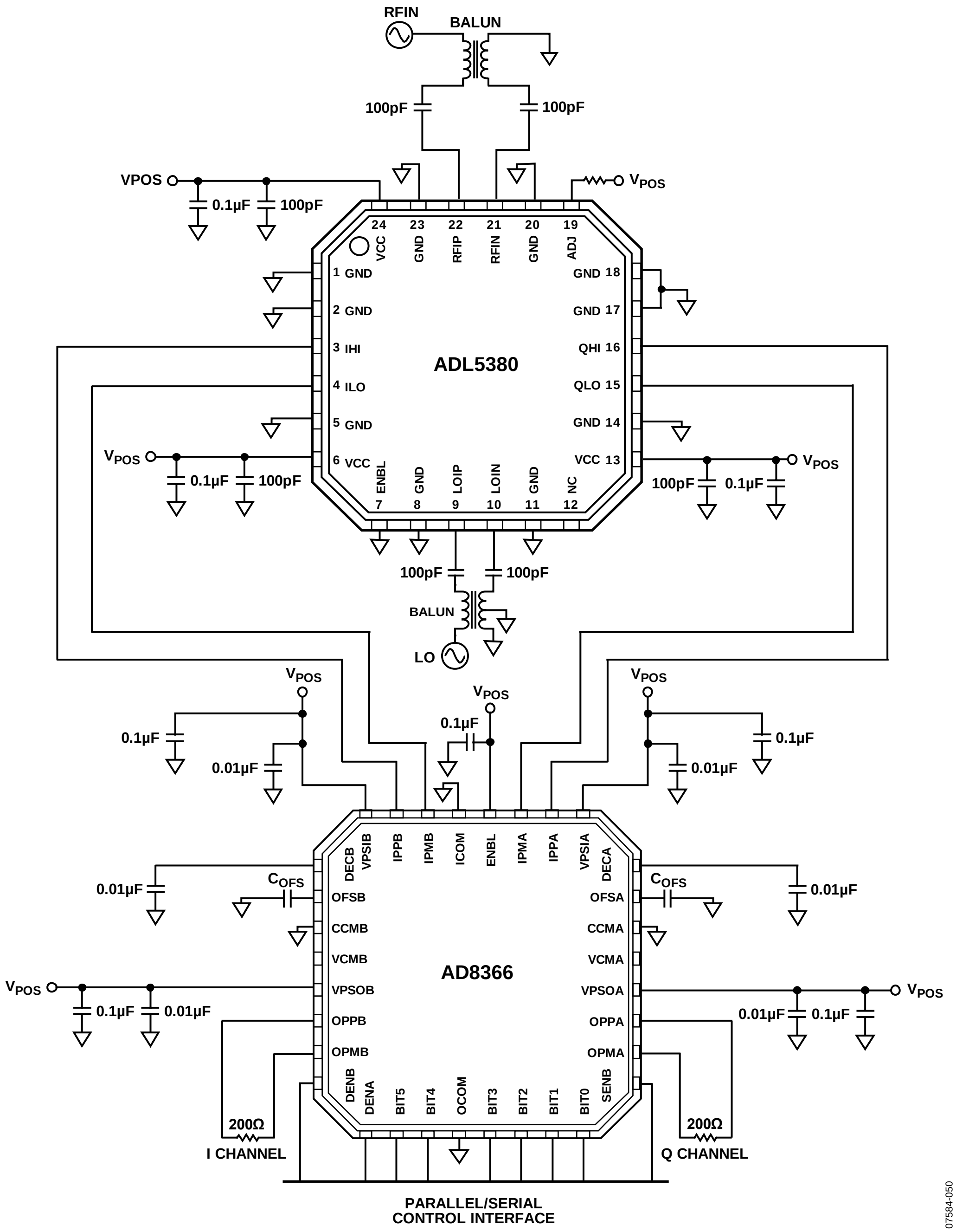

Figure 56. ADL5380 and AD8366 Interface Block Diagram

BASEBAND INTERFACE

In most direct-conversion receiver designs, it is desirable to select a wanted carrier within a specified band. The desired channel can be demodulated by tuning the LO to the appropriate carrier frequency. If the desired RF band contains multiple carriers of interest, the adjacent carriers would also be down converted to a lower IF frequency. These adjacent carriers can be a problem if they are large relative to the desired carrier because they can overdrive the baseband signal detection circuitry. As a result, it is often necessary to insert a filter to provide sufficient rejection of the adjacent carriers.

It is necessary to consider the overall source and load impedance presented by the AD8366 and the ADC input to design the filter network. The differential baseband output impedance of the AD8366 is 25 Ω and is designed to drive a high impedance ADC input. It may be desirable to terminate the ADC input down to the lower impedance by using a terminating resistor, such as 500 Ω. The terminating resistor helps to better define the input impedance at the ADC input at the cost of a slightly reduced gain.

The order and type of filter network depends on the desired high frequency rejection required, pass-band ripple, and group delay.

Figure 57 shows the schematic for a typical fourth-order, Chebyshev, low-pass filter. Table 4 shows the typical values of the filter components for a fourth-order, Chebyshev, low-pass filter with a differential source impedance of 25 Ω and a differential load impedance of 200 Ω.

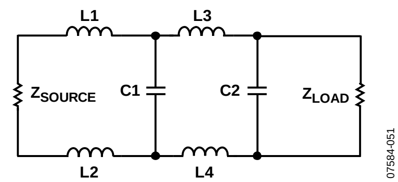

Figure 57. Schematic of a Fourth-Order, Chebyshev, Low-Pass Filter

Table 4. Typical Values for Fourth-Order, Chebyshev, Low-Pass Filter

3 dB Corner (MHz)	Z_{SOURCE} (Ω)	Z_{LOAD} (Ω)	L1 (μH)	L2 (μH)	L3 (μH)	L4 (μH)	C1 (pF)	C2 (pF)
5	25	200	6.6	6.6	6.0	6.0	220	180
10	25	200	3.3	3.3	3	3	110	90
28	25	200	1.2	1.2	1	1	39	33

CHARACTERIZATION SETUPS

Figure 58 and Figure 59 are characterization setups used extensively to characterize the AD8366. Characterization was done on single-ended and differential evaluation boards. The bulk of the characterization was done using an automated VEE program to control the equipment as shown in Figure 58. This setup was used to measure P1dB, OIP3, OIP2, IMD2, IMD3, harmonic distortion, gain, gain error, supply current, and noise density. All measurements were done with a 200 Ω load. All balun, output matching network, and filter losses were de-embedded. Gain error was measured with constant input power. All other measurements were done on 2 V p-p (4 dBm, re: 200 Ω) on the output of the device under test (DUT), and 2 V p-p composite output for two-tone measurements. To measure harmonic distortion, band-pass and band-reject filters were used on the input and output of the DUT.

Figure 59 shows the setup used to make differential measurements. All measurements on this setup were done in a 50 Ω system and post processed to reference the measurements to a 200 Ω system. Gain and phase mismatch were measured with 2 V p-p on the output, and small signal frequency responses were measured with −30 dBm on the input of the DUT.

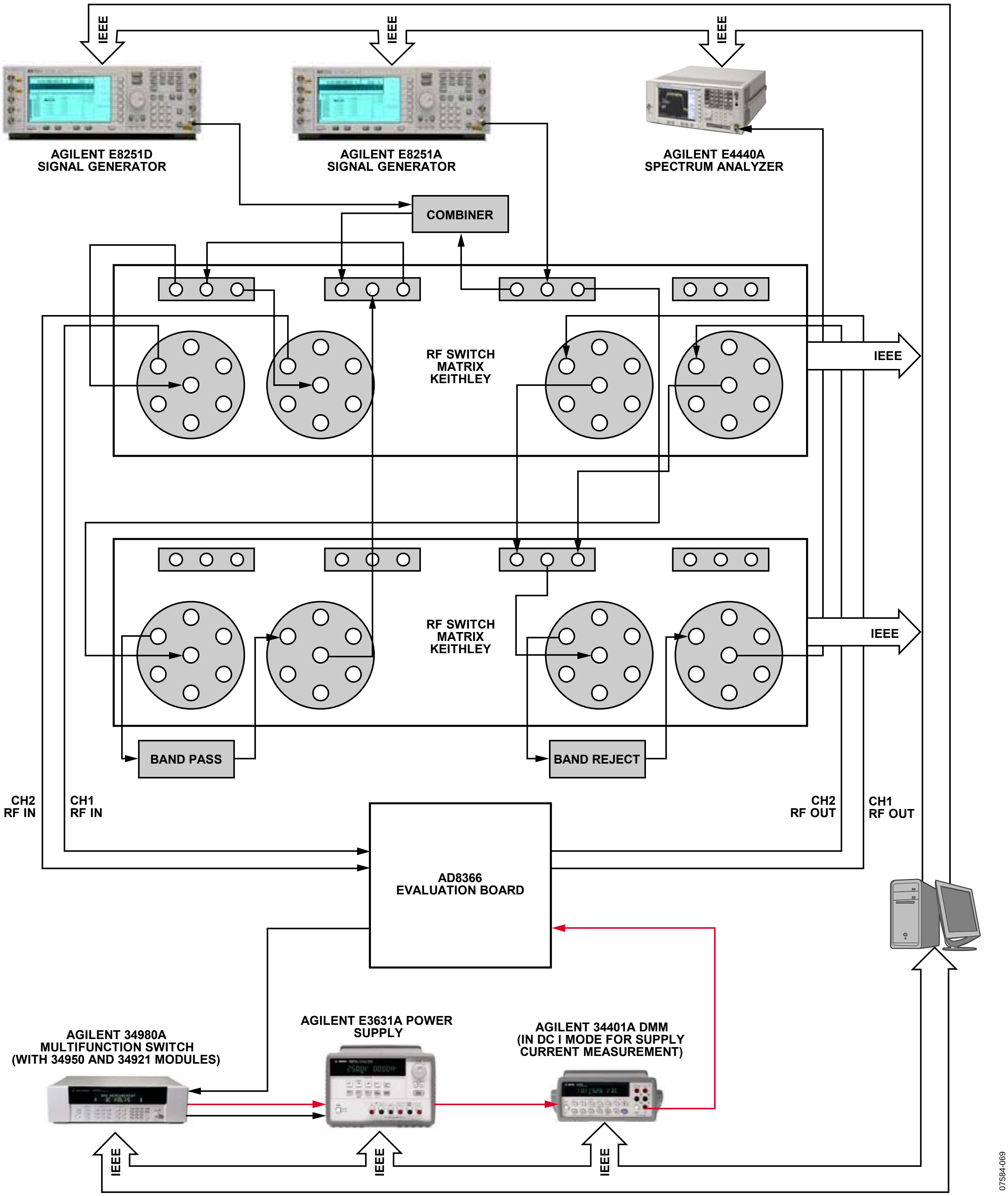

Figure 58. Characterization Setup, Single-Ended Measurements

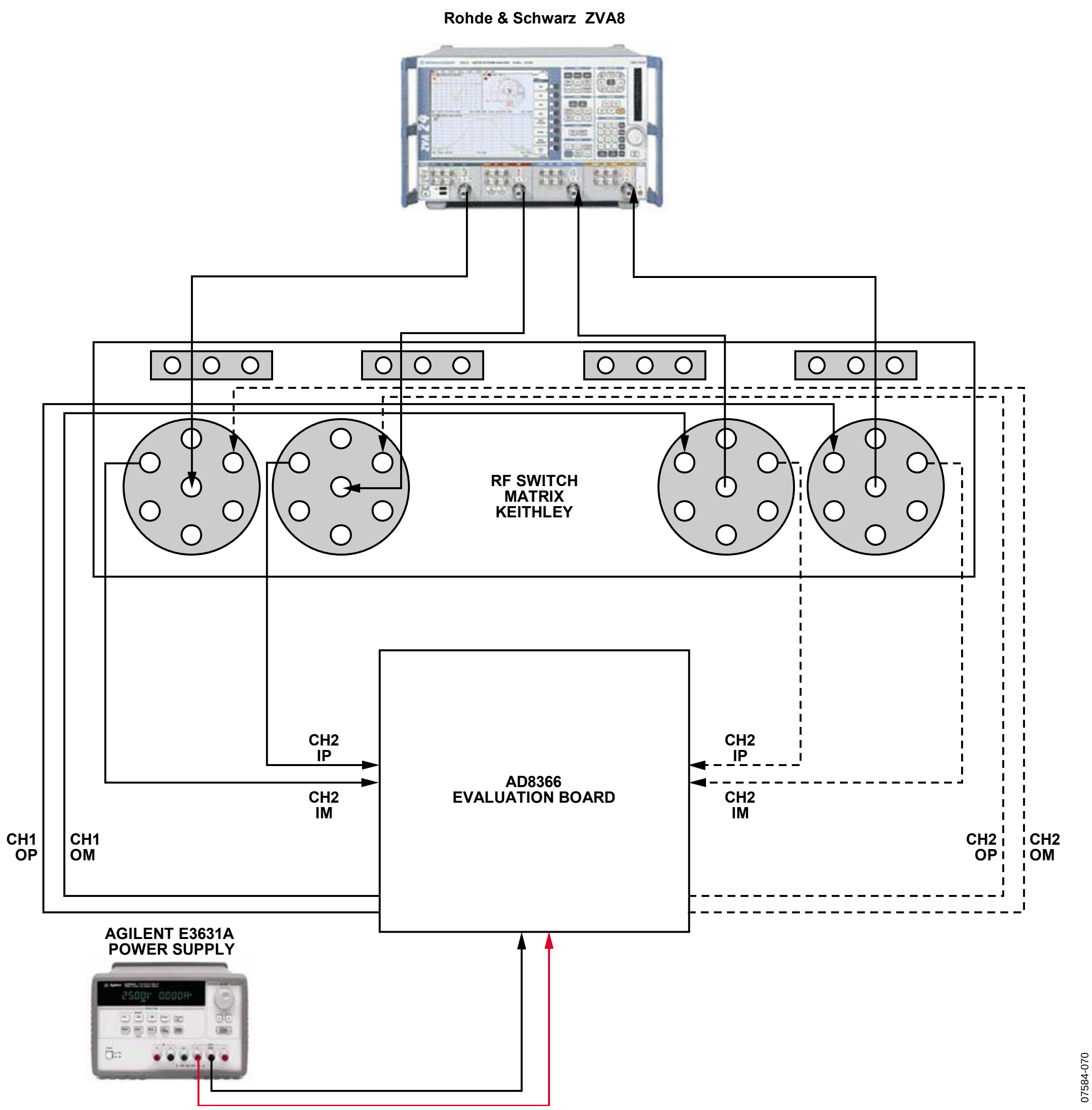

Figure 59. Characterization Setup, Differential Measurements

EVALUATION BOARD

The schematic for the AD8366 evaluation board is shown in Figure 60. The board can be used for single-ended or differential baseband analysis. The default configuration of the board is for single-ended baseband analysis.

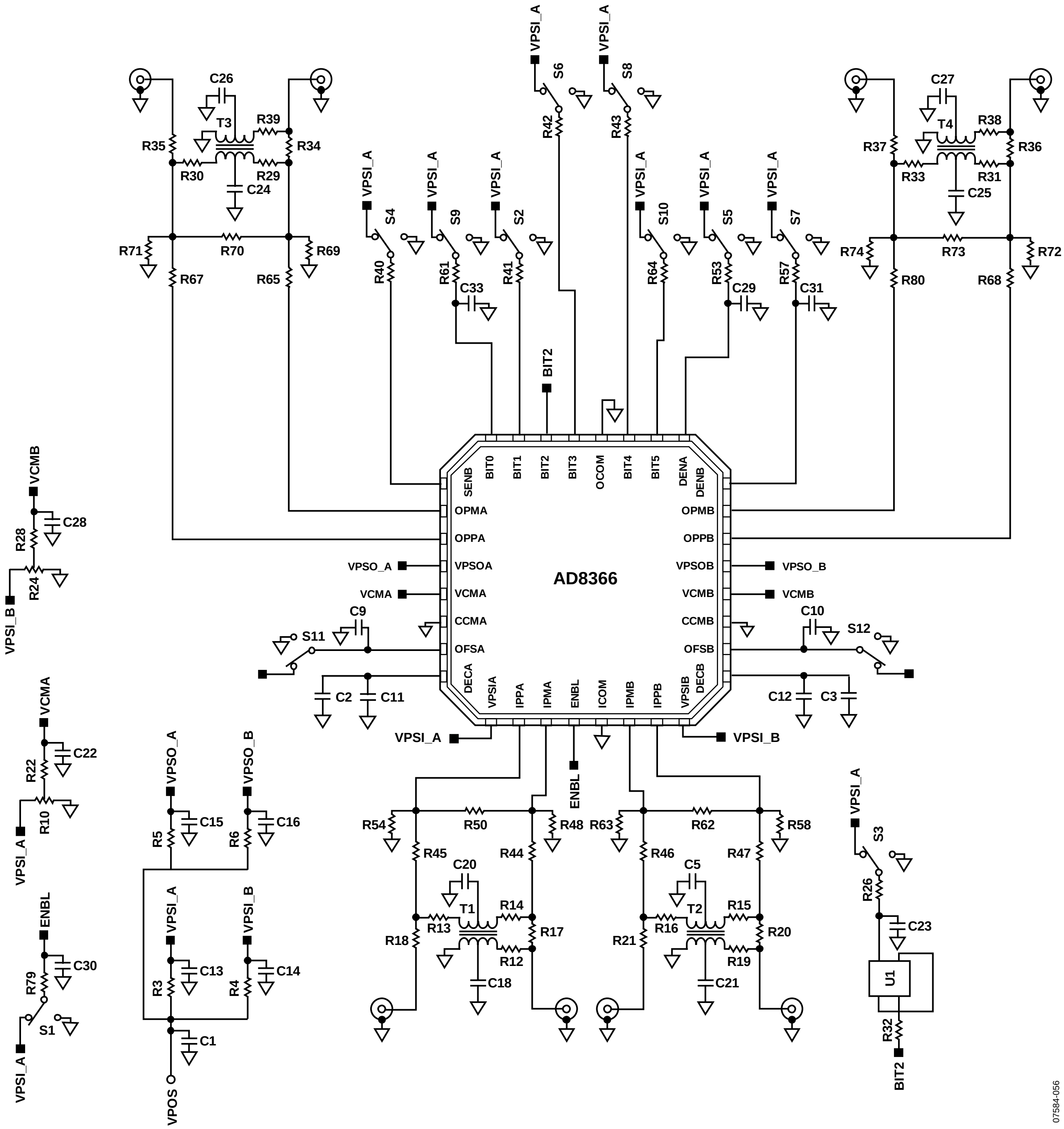

Figure 60. Evaluation Board Schematic

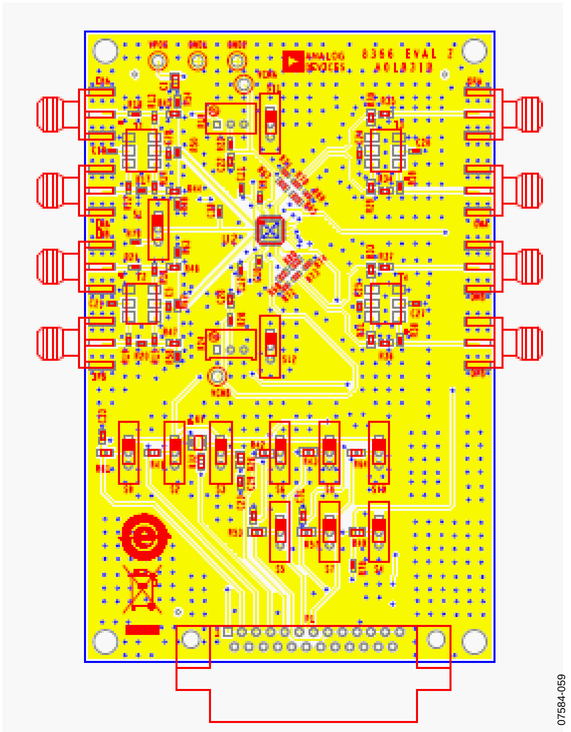

Figure 61. AD8366 Evaluation Board Printed Circuit Board (PCB), Top Side

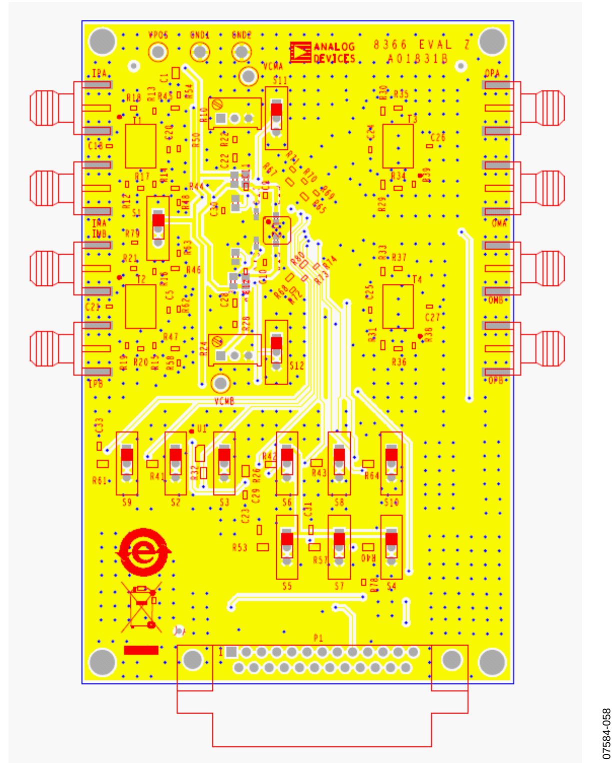

Figure 62. AD8366 Evaluation Board PCB, Bottom Side

Table 5. Evaluation Board Configuration Options

Components	Function	Default Conditions
C1, C13 to C16, R3 to R6	Power supply decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground followed by 0.01 µF capacitors to ground positioned as close to the device as possible.	C1 = 0.1 µF (size 0603), C13 to C16 = 0.01 µF (size 0402), R3 to R6 = 0 Ω (size 0603)
T1, T2, C5, C18, C20, C21, R12 to R21, R44 to R48, R50, R54, R58, R62, R63	Input interface. The default configuration of the evaluation board is for single-ended operation. T1 and T2 are 4:1 impedance ratio baluns to transform a 50 Ω single-ended input into a 200 Ω balanced differential signal. R12 to R14 and R15, R16, and R19 are populated for appropriate balun interface. R44 to R48 and R50, R54, R58, R62, and R63 are provided for generic placement of matching components. C5, C18, C20, and C21 are balun decoupling capacitors. R17, R18, R20, and R21 can be populated with 0 Ω, and the balun interfacing resistors can be removed to bypass T1 and T2 for differential interfacing.	T1, T2 = ADT4-6T+ (Mini-Circuits), C5, C20 = 0.1 µF (size 0402), C18, C21 = do not install, R12 to R16, R19, R44 to R47 = 0 Ω (size 0402), R17, R18, R20, R21,R48, R50, R54, R58, R62, and R63 = open (size 0402)
T3, T4, C24 to C27, R29 to R31, R33 to R39, R65, R67 to R74, R80	Output interface. The default configuration of the evaluation board is for single-ended operation. T3 and T4 are 4:1 impedance ratio baluns to transform a 50 Ω single-ended output into a 200 Ω balanced differential load. R29 to R31, R33, R38, and R39 are populated for appropriate balun interface. R65, R67 to R74, and R80 are provided for generic placement of matching components. C24, C25, C26, and C27 are balun decoupling capacitors. R34 to R37 can be populated with 0 Ω, and the balun interfacing resistors can be removed to bypass T3 and T4 for differential interfacing.	T3, T4 = ADT4-6T+ (Mini-Circuits), C24, C25 = 0.1 µF (size 0402), C26, C27 = do not install, R29 to R31, R33, R38, R39, R65, R67, R68, R80 = 0 Ω (size 0402), R34 to R37, R69 to R74 = open (size 0402)

Components	Function	Default Conditions
S1, S5, S7, R53, R57, R79, C29, C30, C31	Enable interface includes device enable and data enable. Device enable. The AD8366 is enabled by applying a logic high voltage to the ENBL pin. The device is enabled when the S1 switch is set in the down position (high), connecting the ENBL pin to VPSI_A. Data enable. DENA and DENB are used to enable the data path for Channel A and Channel B, respectively. Channel A is enabled when the S5 switch is set in the down position (high), connecting the DENA pin to VPSI_A. Likewise, Channel B is enabled when the S7 switch is set in the down position (high), connecting the DENB pin to VPSI_A. Both channels are disabled by setting the switches to the up position, connecting the DENA and DENB pins to GND.	S1, S5, S7 = installed, R53, R57 = 5.1 kΩ (size 0603), R79 = 10 kΩ (size 0402), C30 = 0.01 μF (size 0402), C29, C31 = 1500 pF (size 0402)
S2, S3, S4, S6, S8, S9, S10 R26, R32, R40 to R43, R61, R64, C23, C33, U1	Serial/parallel interface control. SENB is used to set the data control either in parallel or serial mode. The parallel interface is enabled when S4 is in the up position (low). The serial interface is enabled when S4 is in the down position (high). For SENB pulled low, BIT0 (S9) sets 0.25 dB gain, BIT1 (S2) sets 0.5 dB gain, BIT2 (S3) sets 1 dB gain, BIT3 (S6) sets 2 dB gain, BIT4 (S8) sets 4 dB gain, and BIT5 (S10) sets 8 dB gain. For SENB pulled high, BIT0 becomes a chip select (CS), BIT1 becomes a serial data input (SDAT), and BIT2 becomes serial clock (SCLK). BIT3 to BIT5 are not used in serial mode. U1 is used to deglitch the SCLK signal.	S2, S3, S4, S6, S8, S9, S10 = installed, R26 = 698 kΩ (size 0603), R32, R40 to R43, R61, R64 = 5.1 kΩ (size 0603), C23, C33 = 1500 pF (size 0603), U1 = SN74LVC2G14 inverter chip
S11, S12, C9, C10	DC offset correction loop compensation. The dc offset correction loop is enabled (high) with S11 and S12 for Channel A and Channel B, respectively, when the enabled pins, OFSA/OFSB, are connected to ground through the C9 and C10 capacitors. When disabled (low), OFSA/OFSB are connected to ground directly.	S11, S12 = installed, C9, C10 = 8200 pF (size 0402)
R10, R22, R24, R28, C22, C28	Output common-mode setpoint. The output common mode on Channel A and Channel B can be set externally when applied to VCMA and VCMB. The resistive change through the potentiometer sets a variable VCMA voltage. If left open, the output common mode defaults to $V_{POS}/2$.	R10, R24 = 10 kΩ potentiometers, R22, R28 = 0 Ω, C22, C28 = 0.1 μF (size 0402)
C2, C3, C11, C12	Reference output decoupling capacitor to circuit common.	C2, C3 = 0.1 μF (size 0402), C11, C12 = 0.01 μF (size 0402)