LF to 750 MHz, Digitally Controlled VGA

Data Sheet

AD8370

FEATURES

- Programmable low and high gain (<2 dB resolution)
  - Low range: −11 dB to +17 dB
  - High range: 6 dB to 34 dB
- Differential input and output
  - 200 Ω differential input
  - 100 Ω differential output
- 7 dB noise figure @ maximum gain
- Two-tone IP3 of 35 dBm @ 70 MHz
- −3 dB bandwidth of 750 MHz
- 40 dB precision gain range
- Serial 8-bit digital interface
- Wide input dynamic range
- Power-down feature
- Single 3 V to 5 V supply

APPLICATIONS

- Differential ADC drivers
- IF sampling receivers
- RF/IF gain stages
- Cable and video applications
- SAW filter interfacing
- Single-ended-to-differential conversion

GENERAL DESCRIPTION

The AD8370 is a low cost, digitally controlled, variable gain amplifier (VGA) that provides precision gain control, high IP3, and low noise figure. The excellent distortion performance and wide bandwidth make the AD8370 a suitable gain control device for modern receiver designs.

For wide input, dynamic range applications, the AD8370 provides two input ranges: high gain mode and low gain mode. A vernier, 7-bit, transconductance (g_m) stage provides 28 dB of gain range at better than 2 dB resolution and 22 dB of gain range at better than 1 dB resolution. A second gain range, 17 dB higher than the first, can be selected to provide improved noise performance.

The AD8370 is powered on by applying the appropriate logic level to the PWUP pin. When powered down, the AD8370 consumes less than 4 mA and offers excellent input to output isolation. The gain setting is preserved when operating in a power-down mode.

FUNCTIONAL BLOCK DIAGRAM

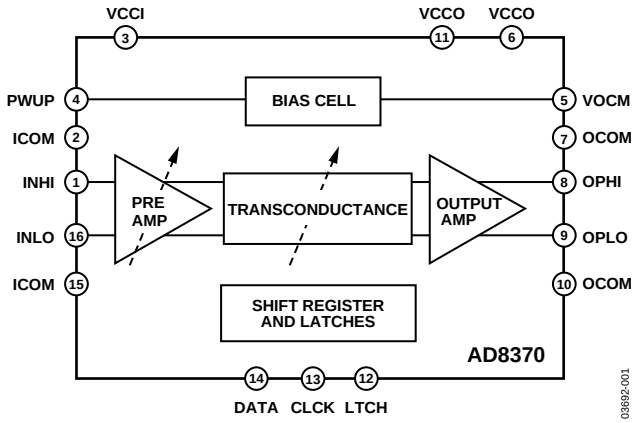

Figure 1.

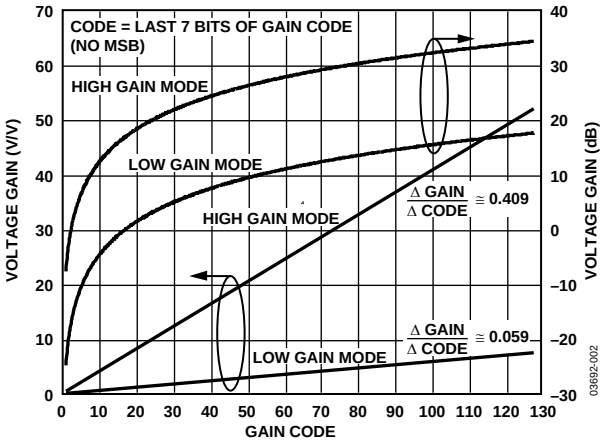

Figure 2. Gain vs. Gain Code at 70 MHz

Gain control of the AD8370 is through a serial 8-bit gain control word. The MSB selects between the two gain ranges, and the remaining 7 bits adjust the overall gain in precise linear gain steps.

Fabricated on the ADI high speed XFCB process, the high bandwidth of the AD8370 provides high frequency and low distortion. The quiescent current of the AD8370 is 78 mA typically. The AD8370 amplifier comes in a compact, thermally enhanced 16-lead TSSOP package and operates over the temperature range of −40°C to +85°C.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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1/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_S = 200 Ω, Z_L = 100 Ω at gain code HG127, 70 MHz, 1 V p-p differential output, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 1 V p-p		750		MHz
Slew Rate	Gain Code HG127, R_L = 1 kΩ, AD8370 in compression		5.75		V/ns
	Gain Code LG127, RL = 1 kΩ, V_{OUT} = 2 V p-p		3.5		V/ns
INPUT STAGE	Pins INHI and IHLO				
Maximum Input	Gain Code LG2, 1 dB compression		3.2		V p-p
Input Resistance	Differential		200		Ω
Common-Mode Input Range			3.2		V p-p
CMRR	Differential, f = 10 MHz, Gain Code LG127		77		dB
Input Noise Spectral Density			1.9		nV/√Hz
GAIN					
Maximum Voltage Gain					
High Gain Mode	Gain Code = HG127		34		dB
			52		V/V
Low Gain Mode	Gain Code = LG127		17		dB
			7.4		V/V
Minimum Voltage Gain					
High Gain Mode	Gain Code = HG1		−8		dB
			0.4		V/V
Low Gain Mode	Gain Code = LG1		−25		dB
			0.06		V/V
Gain Step Size	High Gain Mode		0.408		(V/V)/Code
	Low Gain Mode		0.056		(V/V)/Code
Gain Temperature Sensitivity	Gain Code = HG127		−2		mdB/°C
Step Response	For 6 dB gain step, settled to 10% of final value		20		ns
OUTPUT INTERFACE	Pins OPHI and OPLO				
Output Voltage Swing	R_L ≥ 1 kΩ (1 dB compression)		8.4		V p-p
Output Resistance	Differential		95		Ω
Output Differential Offset	V_{INHI} = V_{INLO}, over all gain codes		±60		mV
NOISE/HARMONIC PERFORMANCE					
10 MHz					
Gain Flatness	Within ±10 MHz of 10 MHz		±0.01		dB
Noise Figure			7.2		dB
Second Harmonic[1]	V_{OUT} = 2 V p-p		−77		dBc
Third Harmonic[1]	V_{OUT} = 2 V p-p		−77		dBc
Output IP3			35		dBm
Output 1 dB Compression Point			17		dBm
70 MHz					
Gain Flatness	Within ±10 MHz of 70 MHz		±0.02		dB
Noise Figure			7.2		dB
Second Harmonic[1]	V_{OUT} = 2 V p-p		−65		dBc
Third Harmonic[1]	V_{OUT} = 2 V p-p		−62		dBc
Output IP3			35		dBm
Output 1 dB Compression Point			17		dBm

Parameter	Conditions	Min	Typ	Max	Unit
140 MHz					
Gain Flatness	Within ±10 MHz of 140 MHz		±0.03		dB
Noise Figure			7.2		dB
Second Harmonic[1]	V_{OUT} = 2 V p-p		−54		dBc
Third Harmonic[1]	V_{OUT} = 2 V p-p		−50		dBc
Output IP3			33		dBm
Output 1 dB Compression Point			17		dBm
190 MHz					
Gain Flatness	Within ±10 MHz of 240 MHz		±0.03		dB
Noise Figure			7.2		dB
Second Harmonic[1]	V_{OUT} = 2 V p-p		−43		dBc
Third Harmonic[1]	V_{OUT} = 2 V p-p		−43		dBc
Output IP3			33		dBm
Output 1 dB Compression Point			17		dBm
240 MHz					
Gain Flatness	Within ±10 MHz of 240 MHz		±0.04		dB
Noise Figure			7.4		dB
Second Harmonic[1]	V_{OUT} = 2 V p-p		−28		dBc
Third Harmonic[1]	V_{OUT} = 2 V p-p		−33		dBc
Output IP3			32		dBm
Output 1 dB Compression Point			17		dBm
380 MHz					
Gain Flatness	Within ±10 MHz of 240 MHz		±0.04		dB
Noise Figure			8.1		dB
Output IP3			27		dBm
Output 1 dB Compression Point			14		dBm
POWER-INTERFACE					
Supply Voltage		3.0[2]		5.5	V
Quiescent Current[3]	PWUP High, GC = LG127, R_L = ∞, 4 seconds after power-on, thermal connection made to exposed paddle under device	72.5	79	85.5	mA
vs. Temperature[4]	−40°C ≤ T_A ≤ +85°C			105	mA
Total Supply Current	PWUP High, V_{OUT} = 1 V p-p, Z_L = 100 Ω reactive, GC = LG127 (includes load current)		82		mA
Power-Down Current	PWUP low		3.7		mA
vs. Temperature[4]	−40°C ≤T_A ≤ +85°C			5	mA
POWER-UP INTERFACE	Pin PWUP				
Power-Up Threshold[4]	Voltage to enable the device	1.8			V
Power-Down Threshold[4]	Voltage to disable the device			0.8	V
PWUP Input Bias Current	PWUP = 0 V		400		nA
GAIN CONTROL INTERFACE	Pins CLCK, DATA, and LTCH				
V_{IH}[4]	Voltage for a logic high	1.8			V
V_{IL}[4]	Voltage for a logic low			0.8	V
Input Bias Current			900		nA

[1] Refer to Figure 22 for performance into a lighter load.
[2] See the 3 V Operation section for more information.
[3] Minimum and maximum specified limits for this parameter are guaranteed by production test.
[4] Minimum or maximum specified limit for this parameter is a 6-sigma value and not guaranteed by production test.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	5.5 V
PWUP, DATA, CLCK, LTCH	V_S + 500 mV
Differential Input Voltage, $V_{INHI} - V_{INLO}$	2 V
Common-Mode Input Voltage, V_{INHI} or V_{INLO}, with Respect to ICOM or OCOM	V_S + 500 mV (max), V_{ICOM} – 500 mV, V_{OCOM} – 500 mV (min)
Internal Power Dissipation	575 mW
θ_{JA} (Exposed Paddle Soldered Down)	30°C/W
θ_{JA} (Exposed Paddle Not Soldered Down)	95°C/W
θ_{JC} (At Exposed Paddle)	9°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	235°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

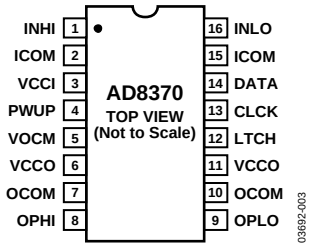

Figure 3.16-Lead TSSOP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INHI	Balanced Differential Input. Internally biased.
2, 15, PADDLE	ICOM	Input Common. Connect to a low impedance ground. This node is also connected to the exposed pad on the bottom of the device.
3	VCCI	Input Positive Supply. 3.0 V to 5.5 V. Should be properly bypassed.
4	PWUP	Power Enable Pin. Device is operational when PWUP is pulled high.
5	VOCM	Common-Mode Output Voltage Pin. The midsupply ((V_{VCCO} – V_{OCOM})/2) common-mode voltage is delivered to this pin for external bypassing for additional common-mode supply decoupling. This can be achieved with a bypass capacitor to ground. This pin is an output only and is not to be driven externally.
6, 11	VCCO	Output Positive Supply. 3.0 V to 5.5 V. Should be properly bypassed.
7, 10	OCOM	Output Common. Connect to a low impedance ground.
8	OPHI	Balanced Differential Output. Biased to midsupply.
9	OPLO	Balanced Differential Output. Biased to midsupply.
12	LTCH	Serial Data Latch Pin. Serial data is clocked into the shift register via the DATA pin when LTCH is low. Data in shift register is latched on the next high-going edge.
13	CLCK	Serial Clock Input Pin.
14	DATA	Serial Data Input Pin.
16	INLO	Balanced Differential Input. Internally biased.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, Z_S = 200 Ω, Z_L = 100 Ω, T = 25°C, unless otherwise noted.

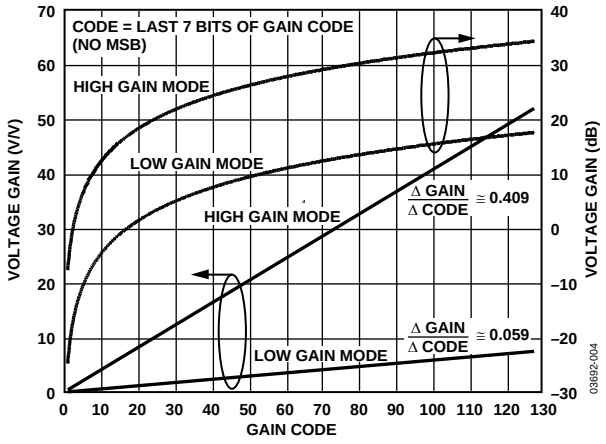

Figure 4. Gain vs. Gain Code at 70 MHz

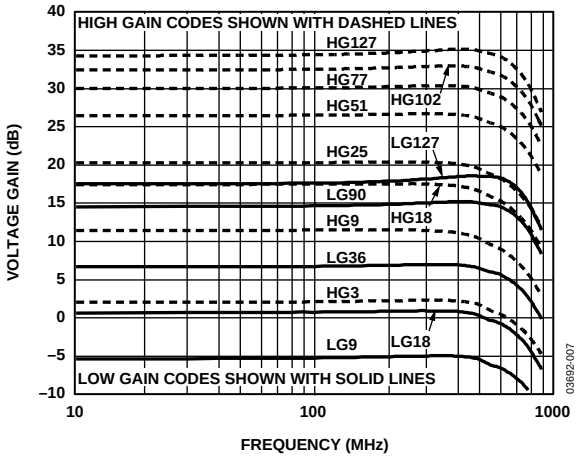

Figure 7. Frequency Response vs. Gain Code

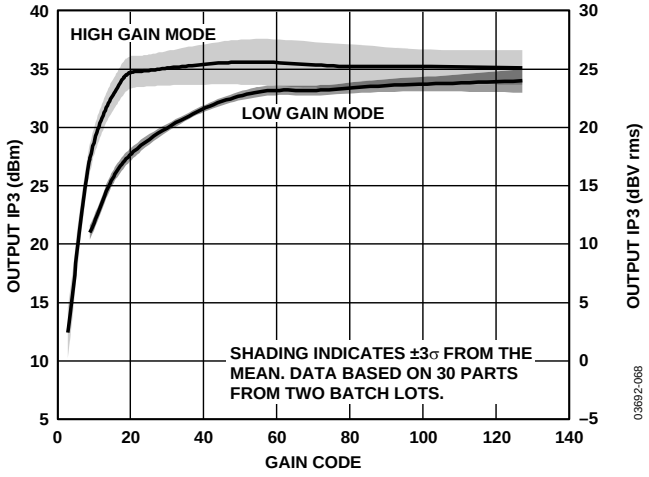

Figure 5. Output Third-Order Intercept vs. Gain Code at 70 MHz

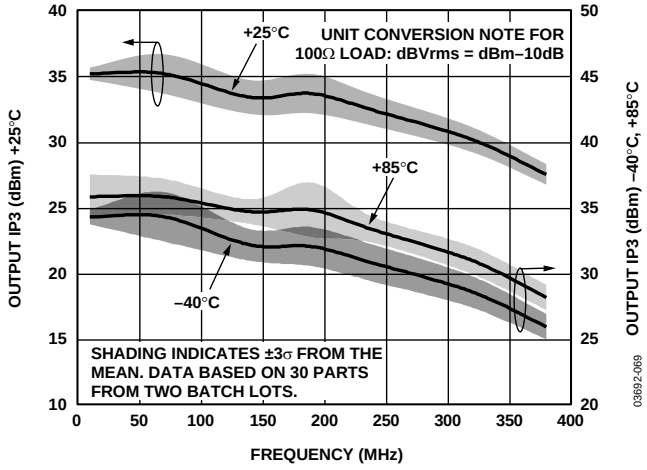

Figure 8. Output Third-Order Intercept vs. Frequency at Maximum Gain

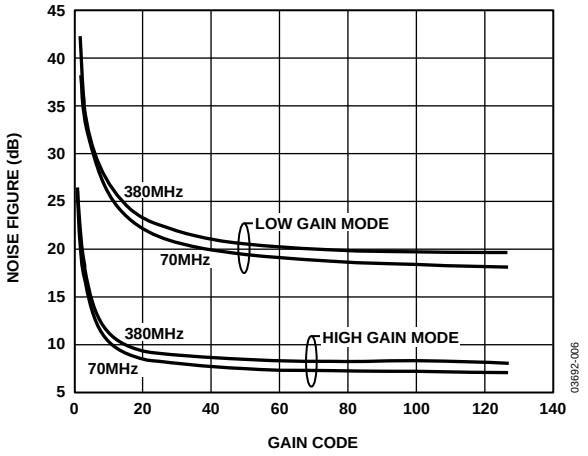

Figure 6. Noise Figure vs. Gain Code at 70 MHz

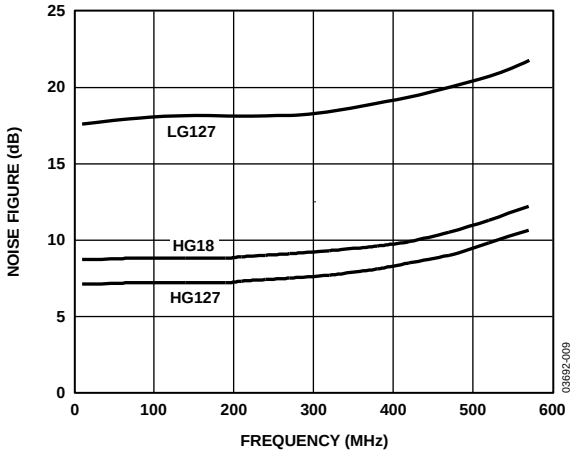

Figure 9. Noise Figure vs. Frequency at Various Gains

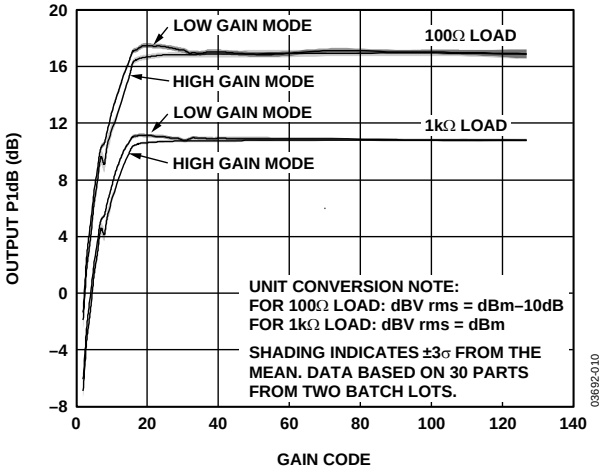

Figure 10. Output P1dB vs. Gain Code at 70 MHz

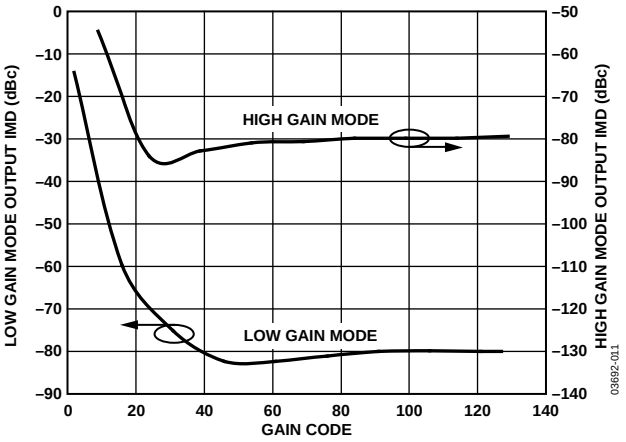

Figure 11. Two-Tone Output IMD3 vs. Gain Code at 70 MHz, $RL = 1\ k\Omega$, $V_{OUT} = 2\ V\ p\text{-}p$ Composite Differential

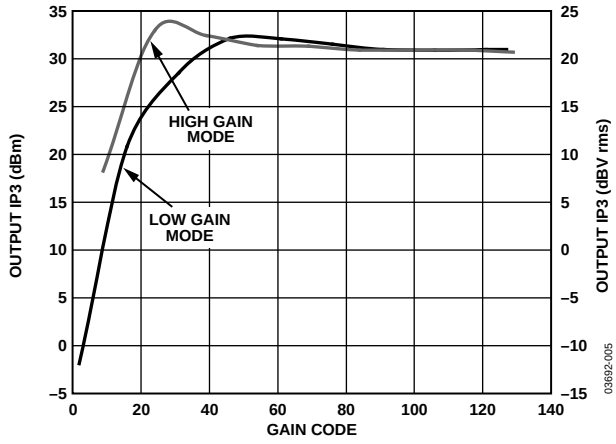

Figure 12. Output Third-Order Intercept vs. Gain Code at 70 MHz, $R_L = 1\ k\Omega$, $V_{OUT} = 2\ V\ p\text{-}p$ Composite Differential

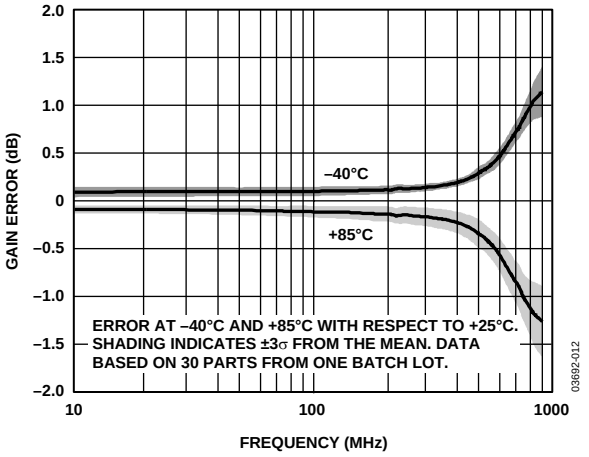

Figure 13. Gain Error over Temperature vs. Frequency, $R_L = 100\ \Omega$

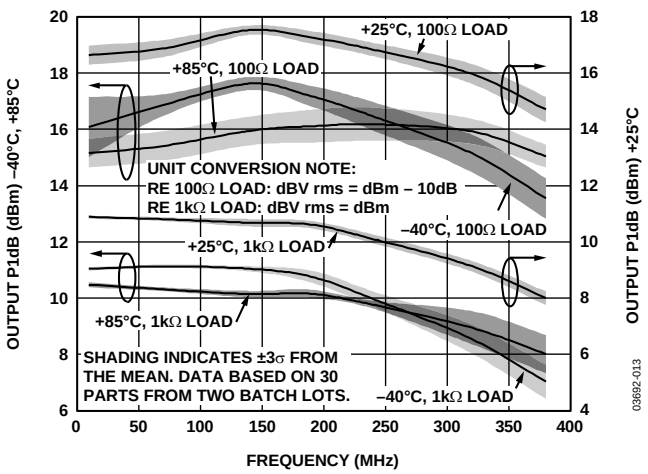

Figure 14. Output P1dB vs. Frequency

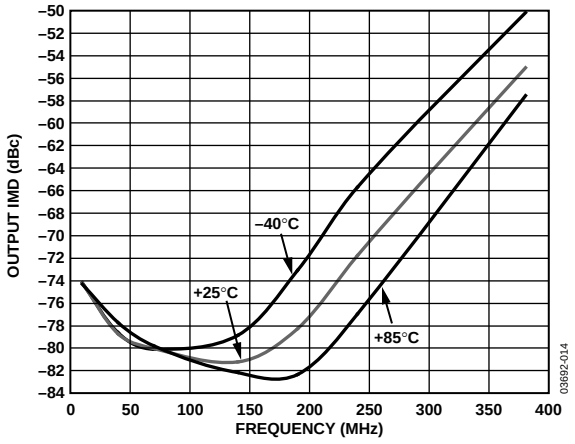

Figure 15. Two-Tone Output IMD3 vs. Frequency at Maximum Gain, $R_L = 1\ k\Omega$, $V_{OUT} = 2\ V\ p\text{-}p$ Composite Differential

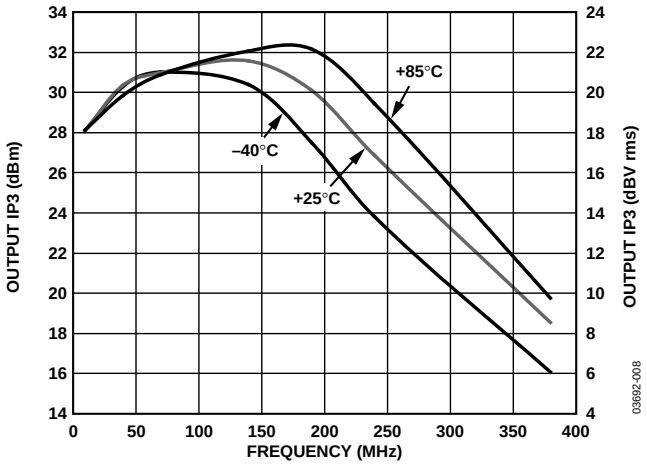

Figure 16. Output Third-Order Intercept vs. Frequency at Maximum Gain, R_L = 1 kΩ, V_{OUT} = 2 V p-p Composite Differential

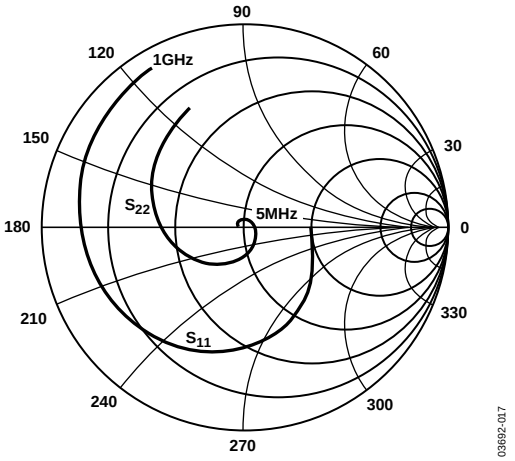

Figure 19. Input and Output Reflection Coefficients, S11 and S22, Z_O = 100 Ω Differential

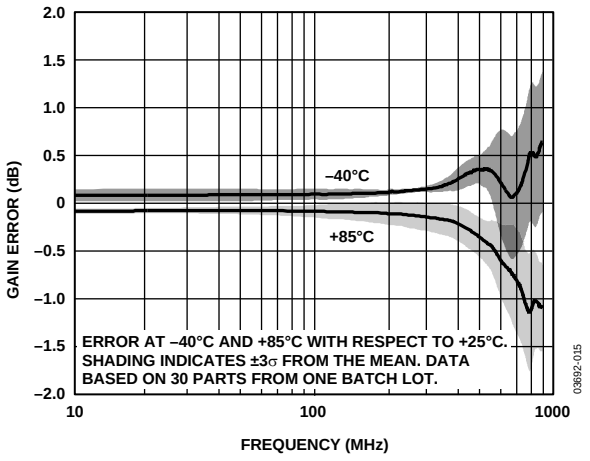

Figure 17. Gain Error over Temperature vs. Frequency, R_L = 1 kΩ

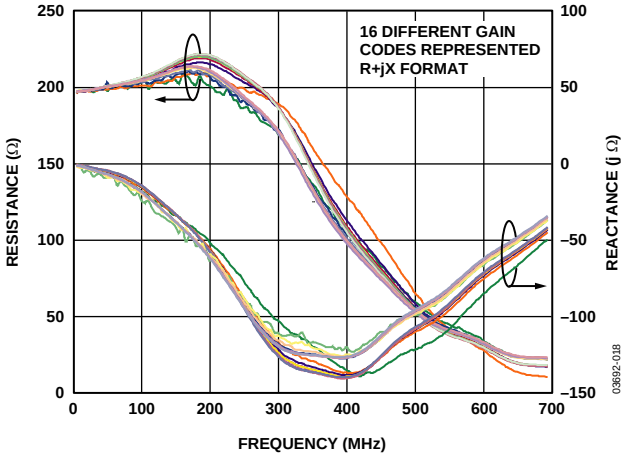

Figure 20. Input Resistance and Reactance vs. Frequency

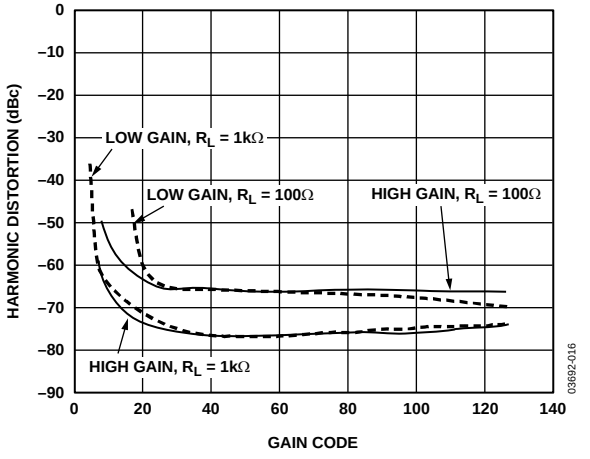

Figure 18. Second-Order Harmonic Distortion vs. Gain Code at 70 MHz, V_{OUT} = 2 V p-p Differential

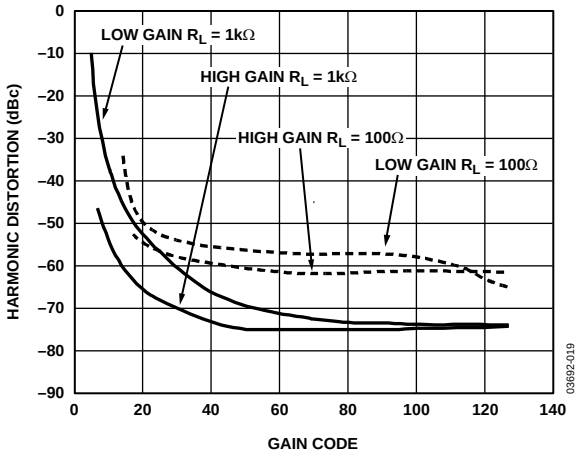

Figure 21. Third-Order Harmonic Distortion vs. Gain Code at 70 MHz, V_{OUT} = 2 V p-p Differential

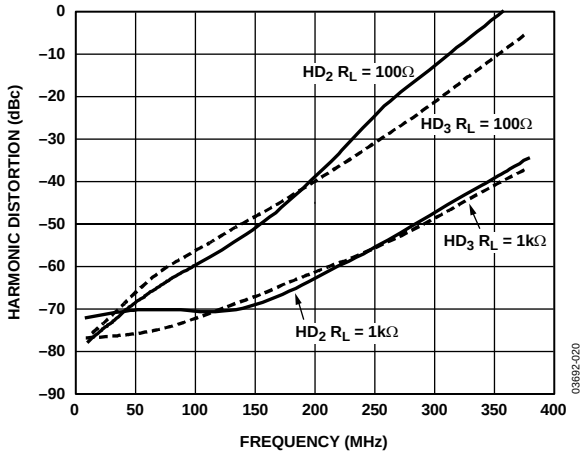

Figure 22. Harmonic Distortion vs. Frequency at Maximum Gain, V_{OUT} = 2 V p-p Composite Differential

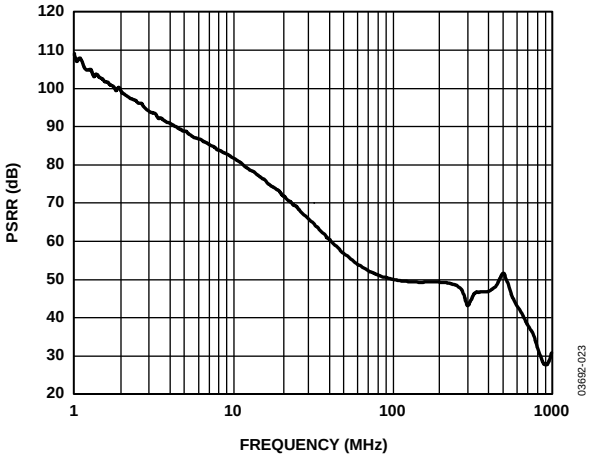

Figure 25. Power Supply Rejection Ratio vs. Frequency at Maximum Gain

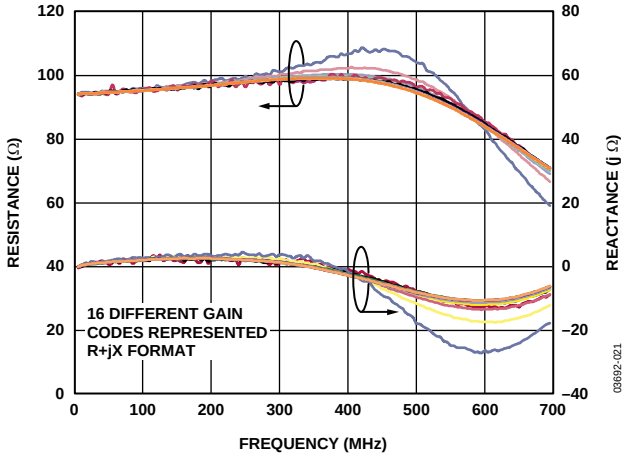

Figure 23. Output Resistance and Reactance vs. Frequency

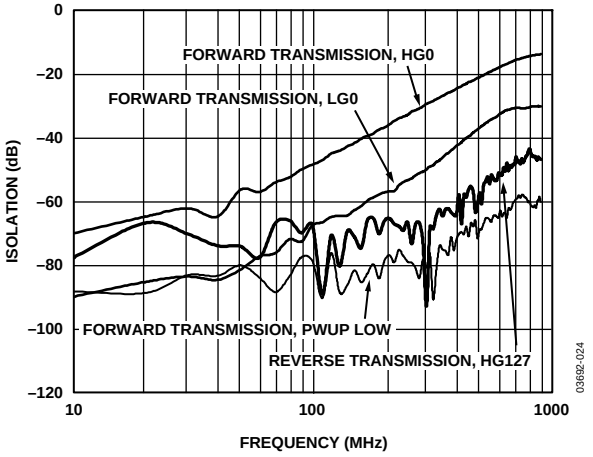

Figure 26. Various Forms of Isolation vs. Frequency

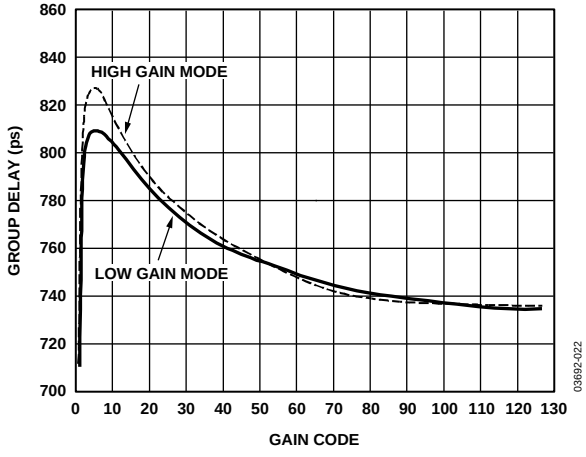

Figure 24. Group Delay vs. Gain Code at 70 MHz

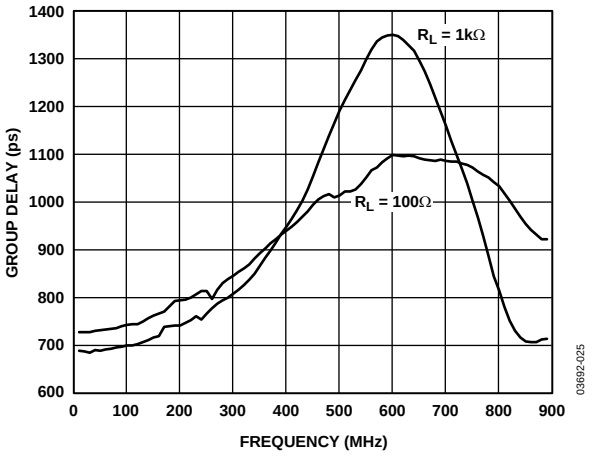

Figure 27. Group Delay vs. Frequency at Maximum Gain

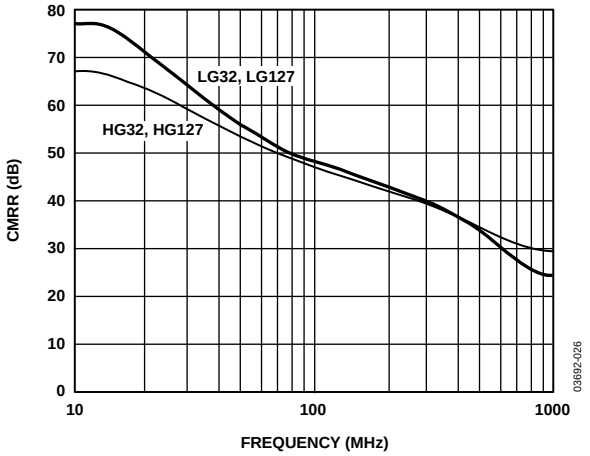

Figure 28. Common-Mode Rejection Ratio vs. Frequency

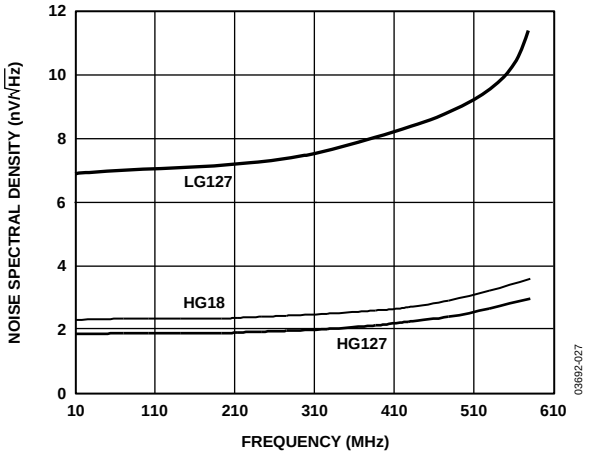

Figure 29. Input Referred Noise Spectral Density vs. Frequency at Various Gains

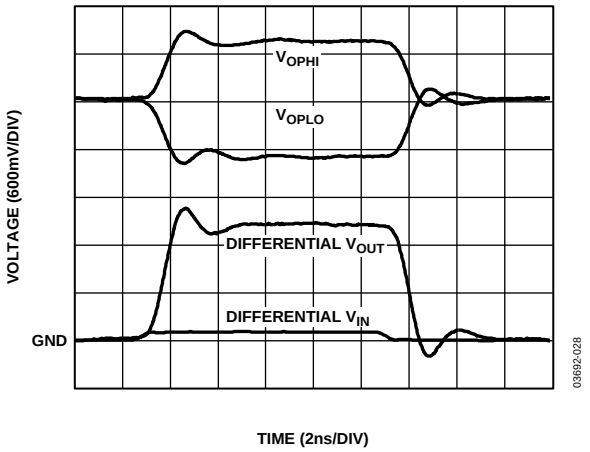

Figure 30. DC-Coupled Large Signal Pulse Response

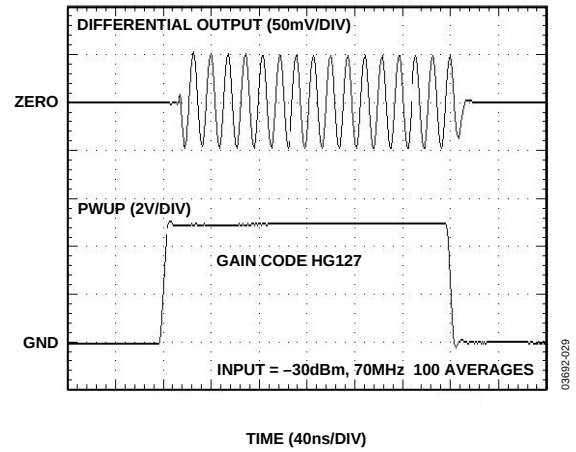

Figure 31. PWUP Time Domain Response

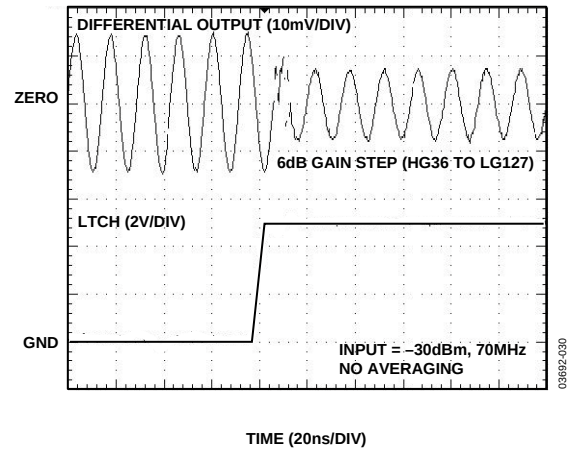

Figure 32. Gain Step Time Domain Response

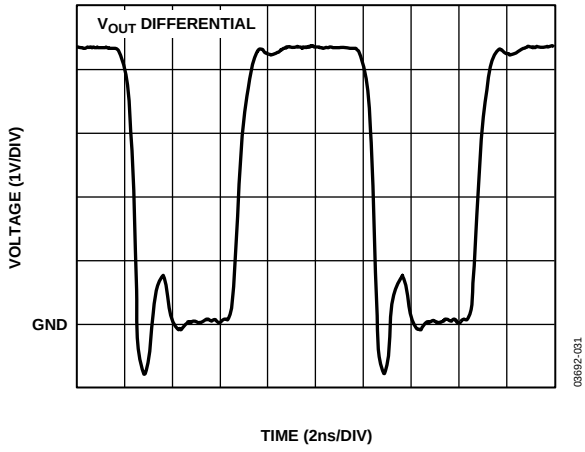

Figure 33. Overdrive Recovery

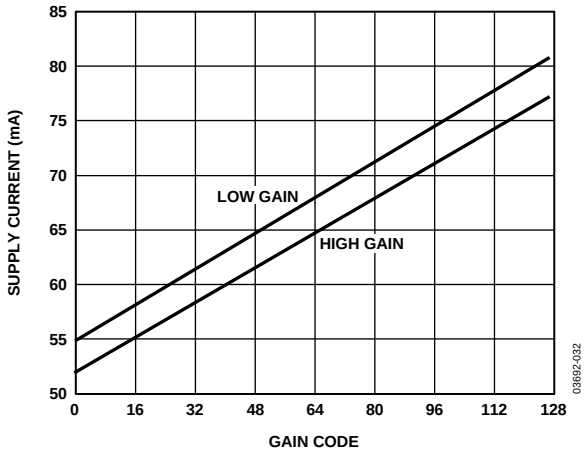

Figure 34. Supply Current vs. Gain Code

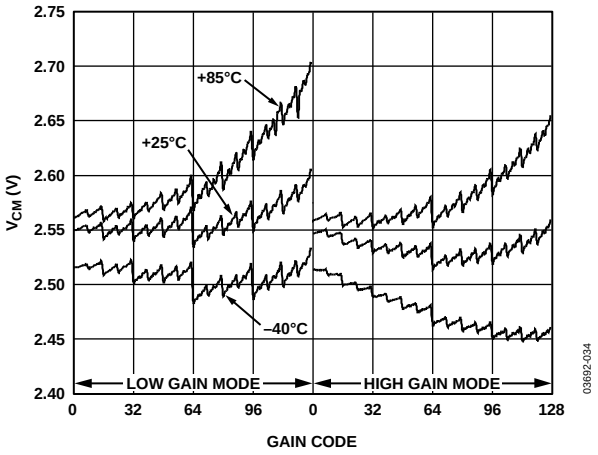

Figure 36. Common-Mode Output Voltage vs. Gain Code at Various Temperatures

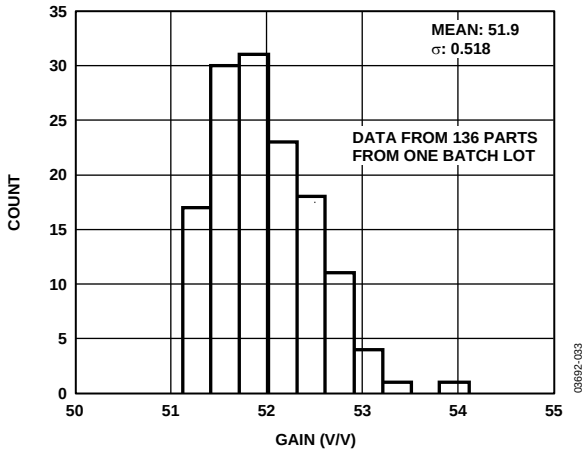

Figure 35. Distribution of Voltage Gain, HG127, 70 MHz, R_L = 100 Ω

THEORY OF OPERATION

The AD8370 is a low cost, digitally controlled, fine adjustment variable gain amplifier (VGA) that provides both high IP3 and low noise figure. The AD8370 is fabricated on an ADI proprietary high performance 25 GHz silicon bipolar process. The −3 dB bandwidth is approximately 750 MHz throughout the variable gain range. The typical quiescent current of the AD8370 is 78 mA. A power-down feature reduces the current to less than 4 mA. The input impedance is approximately 200 Ω differential, and the output impedance is approximately 100 Ω differential to be compatible with saw filters and matching networks used in intermediate frequency (IF) radio applications. Because there is no feedback between the input and output and stages within the amplifier, the input amplifier is isolated from variations in output loading and from subsequent impedance changes, and excellent input to output isolation is realized. Excellent distortion performance and wide bandwidth make the AD8370 a suitable gain control device for modern differential receiver designs. The AD8370 differential input and output configuration is ideally suited to fully differential signal chain circuit designs, although it can be adapted to single-ended system applications, if required.

BLOCK ARCHITECTURE

The three basic building blocks of the AD8370 are a high/low gain selectable input preamplifier, a digitally controlled transconductance (g_m) block, and a fixed gain output stage.

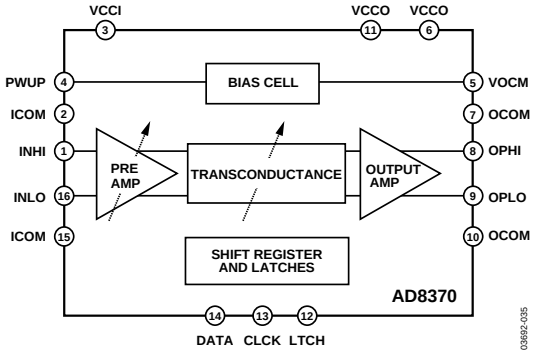

Figure 37. Functional Block Diagram

PREAMPLIFIER

There are two selectable input preamplifiers. Selection is made by the most significant bit (MSB) of the serial gain control data-word. In the high gain mode, the overall device gain is 7.1 V/V (17 dB) above the low gain setting. The two preamplifiers give the AD8370 the ability to accommodate a wide range of input amplitudes. The overlap between the two gain ranges allows the user some flexibility based on noise and distortion demands. See the Choosing Between Gain Ranges section for more information.

The input impedance is approximately 200 Ω differential, regardless of which preamplifier is selected. Note that the input impedance is formed by using active circuit elements and is not set by passive components. See Figure 38 for a simplified schematic of the input interface.

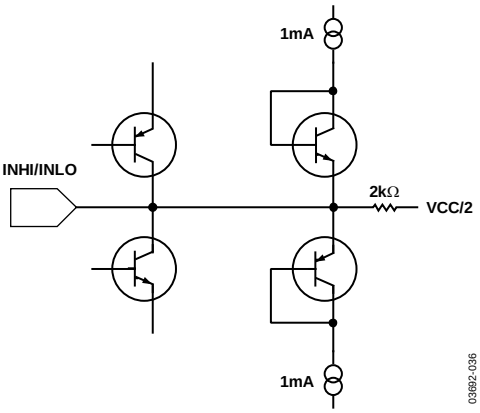

Figure 38. INHI/INLO Simplified Schematic

TRANSCONDUCTANCE STAGE

The digitally controlled g_m section has 42 dB of controllable gain and makes gain adjustments within each gain range. The step size resolution ranges from a fine ~ 0.07 dB up to a coarse 6 dB per bit, depending on the gain code. As shown in Figure 39, of the 42 dB total range, 28 dB has resolution of better than 2 dB, and 22 dB has resolution of better than 1 dB.

Figure 39 shows typical input levels that can be applied to this amplifier at different gain settings. The maximum input was determined by finding the 1 dB compression or expansion point of the V_{OUT}/V_{SOURCE} gain. Note that this is not V_{OUT}/V_{IN}. In this way, the change in the input impedance of the device is also taken into account.

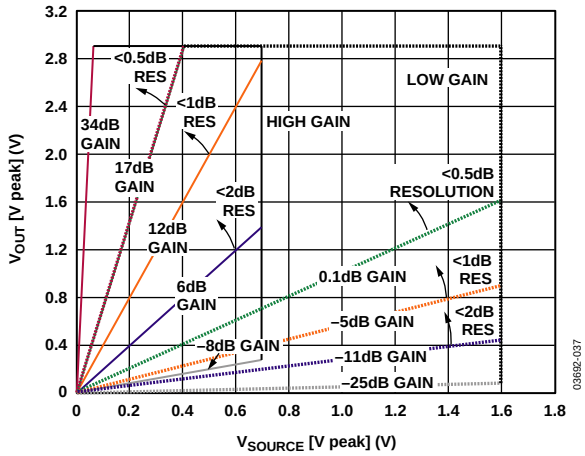

Figure 39. Gain Resolution and Nominal Input and Output Range over the Gain Range

OUTPUT AMPLIFIER

The output impedance is approximately 100 Ω differential and, like the input preamplifier, this impedance is formed using active circuit elements. See Figure 40 for a simplified schematic of the output interface.

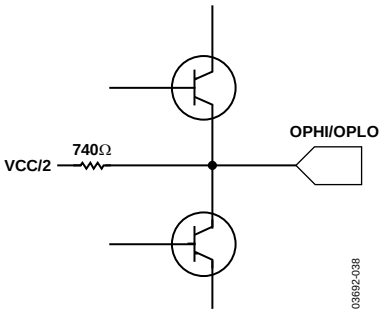

Figure 40. OPHI/OPLO Simplified Circuit

The gain of the output amplifier, and thus the AD8370 as a whole, is load dependent. The following equation can be used to predict the gain deviation of the AD8370 from that at 100 Ω as the load is varied.

$$GainDeviation = \frac{1.98}{1+\frac{98}{R_{LOAD}}}$$

For example, if R_{LOAD} is 1 kΩ, the gain is a factor of 1.80 (5.12 dB) *above* that at 100 Ω, all other things being equal. If R_{LOAD} is 50 Ω, the gain is a factor of 0.669 (3.49 dB) *below* that at 100 Ω.

DIGITAL INTERFACE AND TIMING

The digital control port uses a standard TTL interface. The 8-bit control word is read in a serial fashion when the LTCH pin is held low. The levels presented to the DATA pin are read on each rising edge of the CLCK signal. Figure 41 illustrates the timing diagram for the control interface. Minimum values for timing parameters are presented in Table 4. Figure 42 is a simplified schematic of the digital input pins.

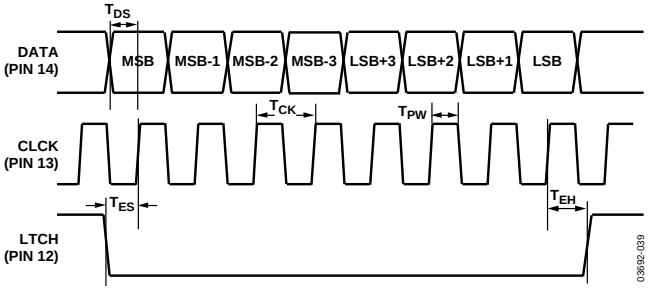

Figure 41. Digital Timing Diagram

Table 4. Serial Programming Timing Parameters

Parameter	Min	Unit
Clock Pulse Width (T_{PW})	25	ns
Clock Period (T_{CK})	50	ns
Setup Time Data vs. Clock (T_{DS})	10	ns
Setup Time Latch vs. Clock (T_{ES})	20	ns
Hold Time Latch vs. Clock (T_{EH})	10	ns

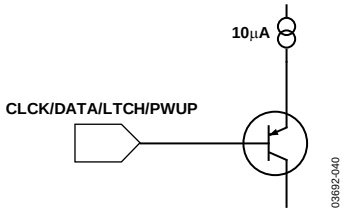

Figure 42. Simplified Circuit for Digital Inputs

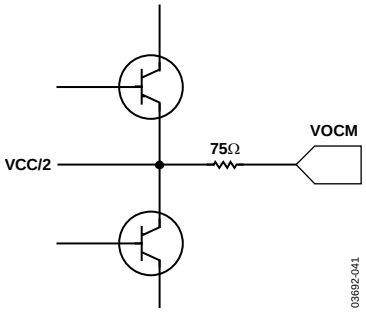

Figure 43. Simplified Circuit for VOCM Output

APPLICATIONS

BASIC CONNECTIONS

Figure 44 shows the minimum connections required for basic operation of the AD8370. Supply voltages between 3.0 V and 5.5 V are allowed. The supply to the VCCO and VCCI pins should be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the device.

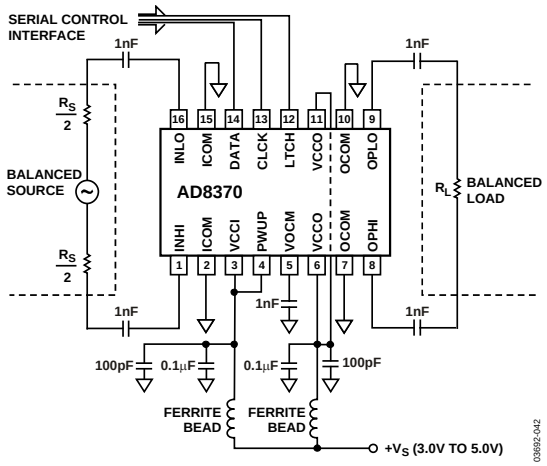

Figure 44. Basic Connections

The AD8370 is designed to be used in differential signal chains. Differential signaling allows improved even-order harmonic cancellation and better common-mode immunity than can be achieved using a single-ended design. To fully exploit these benefits, it is necessary to drive and load the device in a balanced manner. This requires some care to ensure that the common-mode impedance values presented to each set of inputs and outputs are balanced. Driving the device with an unbalanced source can degrade the common-mode rejection ratio. Loading the device with an unbalanced load can cause degradation to even-order harmonic distortion and premature output compression. In general, optimum designs are fully balanced, although the AD8370 still provides impressive performance when used in an unbalanced environment.

The AD8370 is a fine adjustment, VGA. The gain control transfer function is linear in voltage gain. On a decibel scale, this results in the logarithmic transfer functions shown in Figure 4. At the low end of the gain transfer function, the slope is steep, providing a rather coarse control function. At the high end of the gain control range, the decibel step size decreases, allowing precise gain adjustment.

GAIN CODES

The AD8370's two gain ranges are referred to as high gain (HG) and low gain (LG). Within each range, there are 128 possible gain codes. Therefore, the minimum gain in the low gain range is given by the nomenclature LG0 whereas the maximum gain in that range is given by LG127. The same is true for the high gain range. Both LG0 and HG0 essentially turn off the variable transconductance stage, and thus no output is available with these codes (see Figure 26).

The theoretical linear voltage gain can be expressed with respect to the gain code as

$$A_V = GainCode\ Vernier\ (1 + (PreGain - 1)\ MSB)$$

where:

A_V is the linear voltage gain.

GainCode is the digital gain control word minus the MSB (the final 7 bits).

Vernier = 0.055744 V/V

PreGain = 7.079458 V/V

MSB is the most significant bit of the 8-bit gain control word. The MSB sets the device in either high gain mode (MSB = 1) or low gain mode (MSB = 0).

For example, a gain control word of HG45 (or 10101101 binary) results in a theoretical linear voltage gain of 17.76 V/V, calculated as

$$45 \times 0.055744 \times (1 + (7.079458 - 1) \times 1)$$

Increments or decrements in gain within either gain range are simply a matter of operating on the GainCode. Six –dB gain steps, which are equivalent to doubling or halving the linear voltage gain, are accomplished by doubling or halving the GainCode.

When power is first applied to the AD8370, the device is programmed to code LG0 to avoid overdriving the circuitry following it.

POWER-UP FEATURE

The power-up feature does not affect the GainCode, and the gain setting is preserved when in power-down mode. Powering down the AD8370 (bringing PWUP low while power is still applied to the device) does not erase or change the GainCode from the AD8370, and the same gain code is in place when the device is powered up, that is, when PWUP is brought high again. Removing power from the device all together and reapplying, however, reprograms to LG0.

CHOOSING BETWEEN GAIN RANGES

There is some overlap between the two gain ranges; users can choose which one is most appropriate for their needs. When deciding which preamp to use, consider resolution, noise, linearity, and spurious-free dynamic range (SFDR). The most important points to keep in mind are

- The low gain range has better gain resolution.
- The high gain range has a better noise figure.
- The high gain range has better linearity and SFDR at higher gains.
- Conversely, the low gain range has higher SFDR at lower gains.

Figure 45 provides a summary of noise, OIP3, IIP3, and SFDR as a function of device power gain. SFDR is defined as

$$SFDR = \frac{2}{3}(IIP3 - NF - N_S)$$

where:

IIP3 is the input third-order intercept point, the output intercept point in dBm minus the gain in dB.

NF is the noise figure in dB.

N_S is source resistor noise, −174 dBm for a 1 Hz bandwidth at 300°K (27°C).

In general, $N_S = 10 \log_{10}(kTB)$, where $k = 1.374 \times 10^{-23}$, T is the temperature in degrees Kelvin, and B is the noise bandwidth in Hertz.

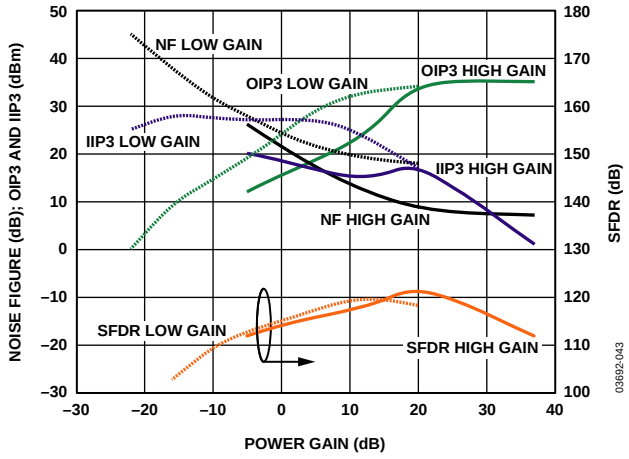

Figure 45. OIP3, IIP3, NF, and SFDR Variation with Gain

As the gain increases, the input amplitude required to deliver the same output amplitude is reduced. This results in less distortion at the input stage, and therefore the OIP3 increases. At some point, the distortion of the input stage becomes small enough such that the nonlinearity of the output stage becomes dominant. The OIP3 does not improve significantly because the gain is increased beyond this point, which explains the knee in the OIP3 curve. The IIP3 curve has a knee for the same reason; however, as the gain is increased beyond the knee, the IIP3 starts to decrease rather than increase. This is because in this region OIP3 is constant, therefore the higher the gain, the lower the IIP3. The two gain ranges have equal SFDR at approximately 13 dB power gain.

LAYOUT AND OPERATING CONSIDERATIONS

Each input and output pin of the AD8370 presents either a 100 Ω or 50 Ω impedance relative to their respective ac grounds. To ensure that signal integrity is not seriously impaired by the printed circuit board, the relevant connection traces should provide an appropriate characteristic impedance to the ground plane. This can be achieved through proper layout.

When laying out an RF trace with a controlled impedance, consider the following:

- Space the ground plane to either side of the signal trace at least three line-widths away to ensure that a microstrip (vertical dielectric) line is formed, rather than a coplanar (lateral dielectric) waveguide.
- Ensure that the width of the microstrip line is constant and that there are as few discontinuities as possible, such as component pads, along the length of the line. Width variations cause impedance discontinuities in the line and may result in unwanted reflections.
- Do not use silkscreen over the signal line because it alters the line impedance.

Keep the length of the input and output connection lines as short as possible.

Figure 46 shows the cross section of a PC board, and Table 5 show the dimensions that provide a 100 Ω line impedance for FR-4 board material with εr = 4.6.

Table 5.

	100 Ω	50 Ω
W	22 mils	13 mils
H	53 mils	8 mils
T	2 mils	2 mils

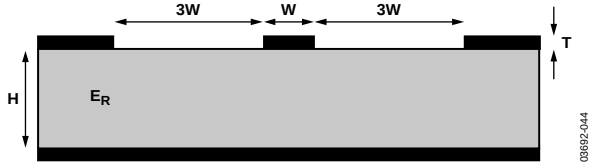

Figure 46. Cross-Sectional View of a PC Board

It possible to approximate a 100 Ω trace on a board designed with the 50 Ω dimensions above by removing the ground plane within 3 line-widths of the area directly below the trace.

The AD8370 contains both digital and analog sections. Care should be taken to ensure that the digital and analog sections are adequately isolated on the PC board. The use of separate ground planes for each section connected at only one point via a ferrite bead inductor ensures that the digital pulses do not adversely affect the analog section of the AD8370.

Due to the nature of the AD8370's circuit design, care must be taken to minimize parasitic capacitance on the input and output. The AD8370 could become unstable with more than a few pF of shunt capacitance on each input. Using resistors in series with input pins is recommended under conditions of high source capacitance.

High transient and noise levels on the power supply, ground, and digital inputs can, under some circumstances, reprogram the AD8370 to an unintended gain code. This further reinforces the need for proper supply bypassing and decoupling. The user should also be aware that probing the AD8370 and associated circuitry during circuit debug may also induce the same effect.

PACKAGE CONSIDERATIONS

The package of the AD8370 is a compact, thermally enhanced TSSOP 16-lead design. A large exposed paddle on the bottom of the device provides both a thermal benefit and a low inductance path to ground for the circuit. To make proper use of this packaging feature, the PCB needs to make contact directly under the device, connected to an ac/dc common ground reference with as many vias as possible to lower the inductance and thermal impedance.

SINGLE-ENDED-TO-DIFFERENTIAL CONVERSION

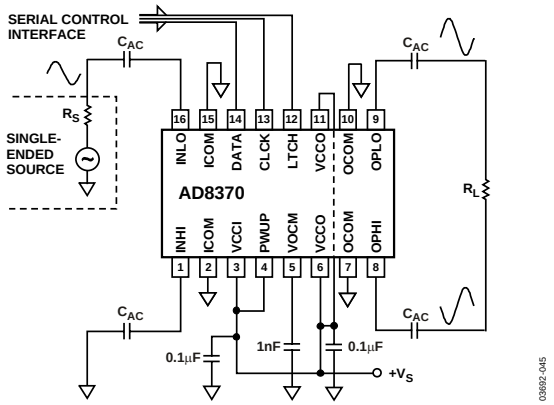

Figure 47. Single-Ended-to-Differential Conversion

The AD8370 is primarily designed for differential signal interfacing. The device can be used for single-ended-to-differential conversion simply by terminating the unused input to ground using a capacitor as depicted in Figure 47. The ac coupling capacitors should be selected such that their reactance is negligible at the frequency of operation. For example, using 1 nF capacitors for C_{AC} presents a capacitive reactance of −j1.6 Ω on each input node at 100 MHz. This attenuates the applied input voltage by 0.003 dB. If 10 pF capacitors had been selected, the voltage delivered to the input would be reduced by 2.1 dB when operating with a 200 Ω source impedance.

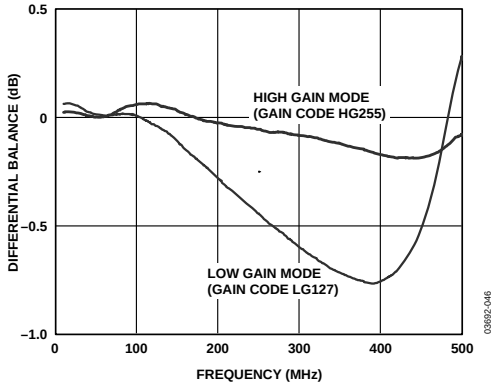

Figure 48. Differential Output Balance for a Single-Ended Input Drive at Maximum Gain (R_L = 1 kΩ, C_{AC} = 10 nF)

Figure 48 illustrates the differential balance at the output for a single-ended input drive for multiple gain codes. The differential balance is better than 0.5 dB for signal frequencies less than 250 MHz. Figure 49 depicts the differential balance over the entire gain range at 10 MHz. The balance is degraded for lower gain settings because the finite common gain allows some of the input signal applied to INHI to pass directly through to the OPLO pin. At higher gain settings, the differential gain dominates and balance is restored.

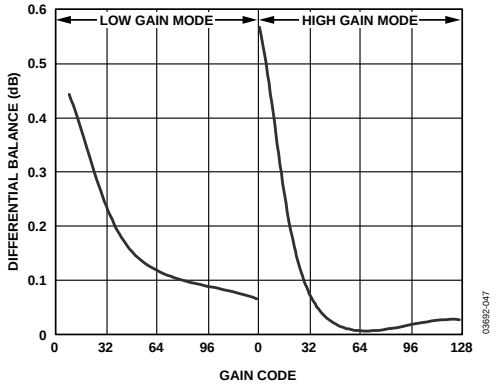

Figure 49. Differential Output Balance at 10 MHz for a Single-Ended Drive vs. Gain Code (R_L = 1 kΩ, C_{AC} = 10 nF)

Even though the amplifier is no longer being driven in a balanced manner, the distortion performance remains adequate for most applications. Figure 50 illustrates the harmonic distortion performance of the circuit in Figure 47 over the entire gain range.

If the amplifier is driven in single-ended mode, the input impedance varies depending on the value of the resistor used to terminate the other input as

$$Rin_{SE} = Rin_{DIFF} + R_{TERM}$$

where R_{TERM} is the termination resistor connected to the other input.

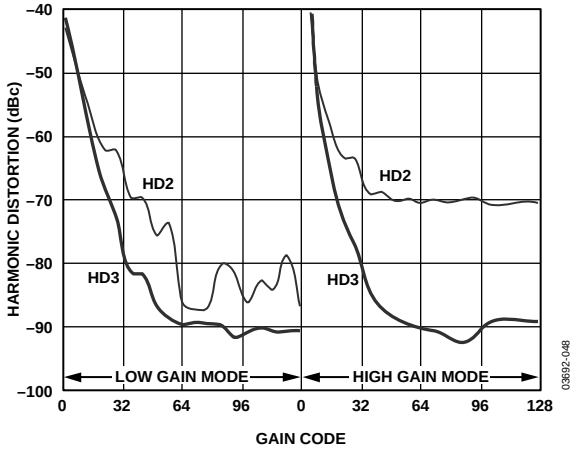

Figure 50. Harmonic Distortion of the Circuit in Figure 47

DC-COUPLED OPERATION

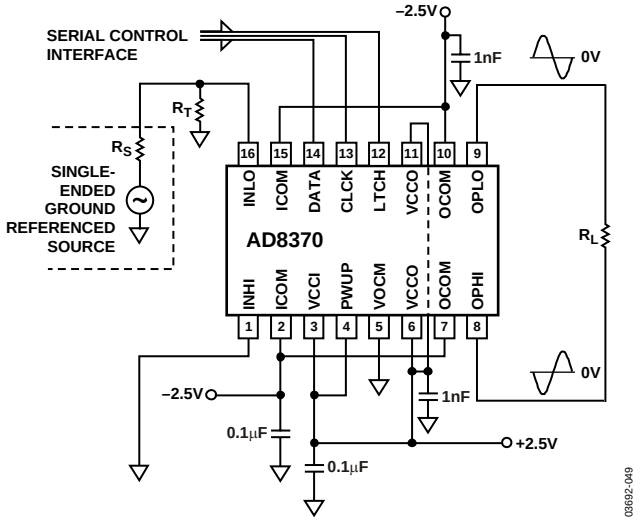

Figure 51. DC Coupling the AD8370. Dual supplies are used to set the input and output common-mode levels to 0 V.

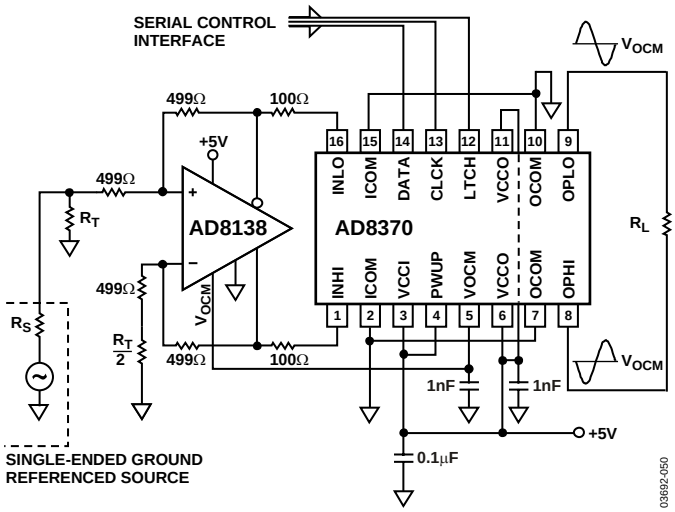

Figure 52. DC Coupling the AD8370. The AD8138 is used as a unity-gain level shifting amplifier to lift the common-mode level of the source to midsupply.

The AD8370 is also a dc accurate VGA. The common-mode dc voltage present at the output pins is internally set to midsupply using what is essentially a buffered resistive divider network connected between the positive supply rail and the common (ground) pins. The input pins are at a slightly higher dc potential, typically 250 mV to 550 mV above the output pins, depending on gain setting. In a typical single-supply application, it is necessary to raise the common-mode reference level of the source and load to roughly midsupply to maintain symmetric swing and to avoid sinking or sourcing strong bias currents from the input and output pins. It is possible to use balanced dual supplies to allow ground referenced source and load, as shown in Figure 51. By connecting the VOCM pin and unused input to ground, the input and output common-mode potentials are forced to virtual ground. This allows direct coupling of ground referenced source and loads. The initial differential input offset is typically only a few 100 µV. Over temperature, the input offset could be as high as a few tens of mVs. If precise dc accuracy is needed over temperature and time, it may be necessary to periodically measure the input offset and to apply the necessary opposing offset to the unused differential input, canceling the resulting output offset.

To address situations where dual supplies are not convenient, a second option is presented in Figure 52. The AD8138 differential amplifier is used to translate the common-mode level of the driving source to midsupply, which allows dc accurate performance with a ground-referenced source without the need for dual supplies. The bandwidth of the solution in Figure 52 is limited by the gain-bandwidth product of the AD8138. The normalized frequency response of both implementations is shown in Figure 53.

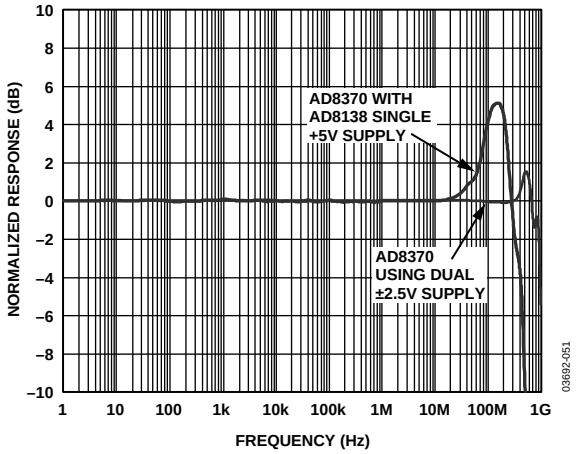

Figure 53. Normalized Frequency Response of the Two Solutions in Figure 51 and Figure 52

ADC INTERFACING

Although the AD8370 is designed to provide a 100 Ω output source impedance, the device is capable of driving a variety of loads while maintaining reasonable gain and distortion performance. A common application for the AD8370 is ADC driving in IF sampling receivers and broadband wide dynamic range digitizers. The wide gain adjustment range allows the use of lower resolution ADCs. Figure 54 illustrates a typical ADC interface network.

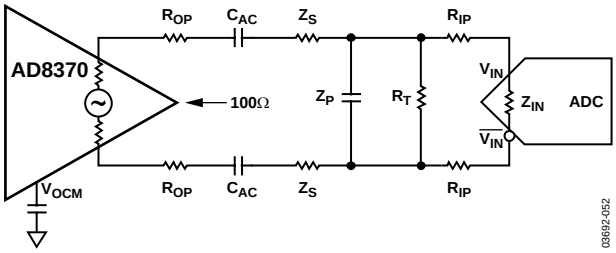

Figure 54. Generic ADC Interface

Many factors need to be considered before defining component values used in the interface network, such as the desired frequency range of operation, the input swing, and input impedance of the ADC. AC coupling capacitors, C_{AC}, should be used to block any potential dc offsets present at the AD8370 outputs, which would otherwise consume the available low-end range of the ADC. The C_{AC} capacitors should be large enough so that they present negligible reactance over the intended frequency range of operation. The VOCM pin may serve as an external reference for ADCs that do not include an on-board reference. In either case, it is suggested that the VOCM pin be decoupled to ground through a moderately large bypassing capacitor (1 nF to 10 nF) to help minimize wideband noise pick-up.

Often it is wise to include input and output parasitic suppression resistors, R_{IP} and R_{OP}. Parasitic suppressing resistors help to prevent resonant effects that occur as a result of internal bond-wire inductance, pad to substrate capacitance, and stray capacitance of the printed circuit board trace artwork. If omitted, undesirable settling characteristics may be observed. Typically, only 10 Ω to 25 Ω of series resistance is all that is needed to help dampen resonant effects. Considering that most ADCs present a relatively high input impedance, very little signal is lost across the R_{IP} and R_{OP} series resistors.

Depending on the input impedance presented by the input system of the ADC, it may be desirable to terminate the ADC input down to a lower impedance by using a terminating resistor, R_T. The high frequency response of the AD8370 exhibits greater peaking when driving very light loads. In addition, the terminating resistor helps to better define the input impedance at the ADC input. Any part-to-part variability of ADC input impedance is reduced when shunting down the ADC inputs by using a moderate tolerance terminating resistor (typically a 1% value is acceptable).

After defining reasonable values for coupling capacitors, suppressing resistors, and the terminating resistor, it is time to design the intermediate filter network. The example in Figure 54 suggests a second-order, low-pass filter network comprised of series inductors and a shunt capacitor. The order and type of filter network used depends on the desired high frequency rejection required for the ADC interface, as well as on pass-band ripple and group delay. In some situations, the signal spectra may already be sufficiently band-limited such that no additional filter network is necessary, in which case ZS would simply be a short and ZP would be an open. In other situations, it may be necessary to have a rather high-order antialiasing filter to help minimize unwanted high frequency spectra from being aliased down into the first Nyquist zone of the ADC.

To properly design the filter network, it is necessary to consider the overall source and load impedance presented by the AD8370 and ADC input, including the additional resistive contribution of suppression and terminating resistors. The filter design can then be handled by using a single-ended equivalent circuit, as shown in Figure 55. A variety of references that address filter synthesis are available. Most provide tables for various filter types and orders, indicating the normalized inductor and capacitor values for a 1 Hz cutoff frequency and 1 Ω load. After scaling the normalized prototype element values by the actual desired cut-off frequency and load impedance, it is simply a matter of splitting series element reactances in half to realize the final balanced filter network component values.

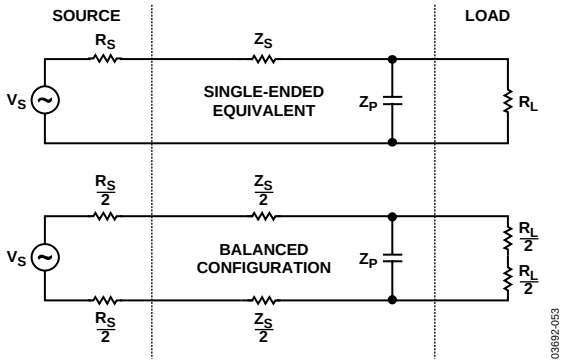

Figure 55. Single-Ended-to-Differential Network Conversion

As an example, a second-order, Butterworth, low-pass filter design is presented where the differential load impedance is 1200 Ω, and the padded source impedance of the AD8370 is assumed to be 120 Ω. The normalized series inductor value for the 10-to-1, load-to-source impedance ratio is 0.074 H, and the normalized shunt capacitor is 14.814 F. For a 70 MHz cutoff frequency, the single-ended equivalent circuit consists of a 200 nH series inductor followed by a 27 pF capacitor. To realize the balanced equivalent, simply split the 200 nH inductor in half to realize the network shown in Figure 56.

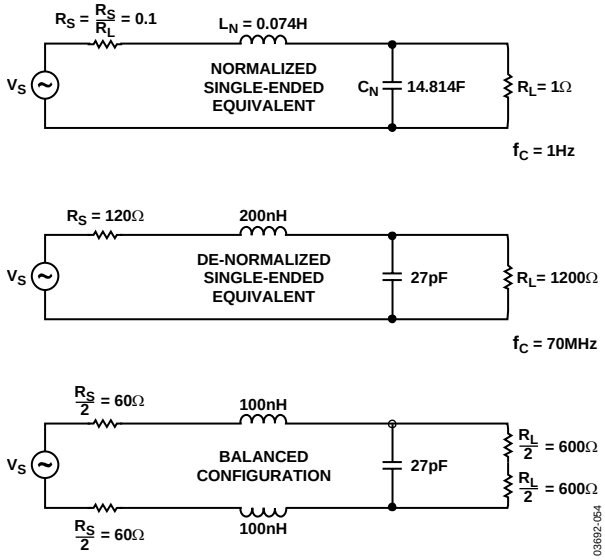

Figure 56. Second-Order, Butterworth, Low-Pass Filter Design Example

A complete design example is shown in Figure 58. The AD8370 is configured for single-ended-to-differential conversion with the input terminated down to present a single-ended 75 Ω input. A sixth-order Chebyshev differential filter is used to interface the output of the AD8370 to the input of the AD9430 170 MSPS, 12-bit ADC. The filter minimizes aliasing effects and improves harmonic distortion performance.

The input of the AD9430 is terminated with a 1.5 kΩ resistor so that the overall load presented to the filter network is ~1 kΩ. The variable gain of the AD8370 extends the useable dynamic range of the ADC. The measured intermodulation distortion of the combination is presented in Figure 57 at 42 MHz.

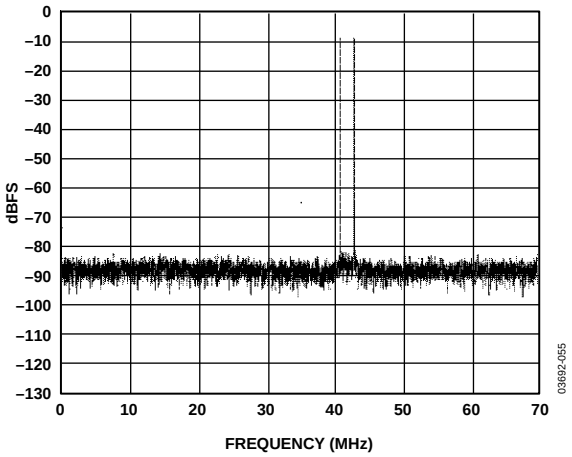

Figure 57. FFT Plot of Two-Tone Intermodulation Distortion at 42 MHz for the Circuit in Figure 58

In Figure 57, the intermodulation products are comparable to the noise floor of the ADC. The spurious-free dynamic range of the combination is better than 66 dB for a 70 MHz measurement bandwidth.

3 V OPERATION

It is possible to operate the AD8370 at voltages as low as 3 V with only minor performance degradation. Table 6 gives typical specifications for operation at 3 V.

Table 6.

Parameter	Typical (70 MHz, R_L = 100 Ω)
Output IP3	+23.5 dBm
P1dB	+12.7 dBm
−3 dB Bandwidth	650 MHz (HG 127)
IMD3	−82 dBc (R_L = 1 kΩ)

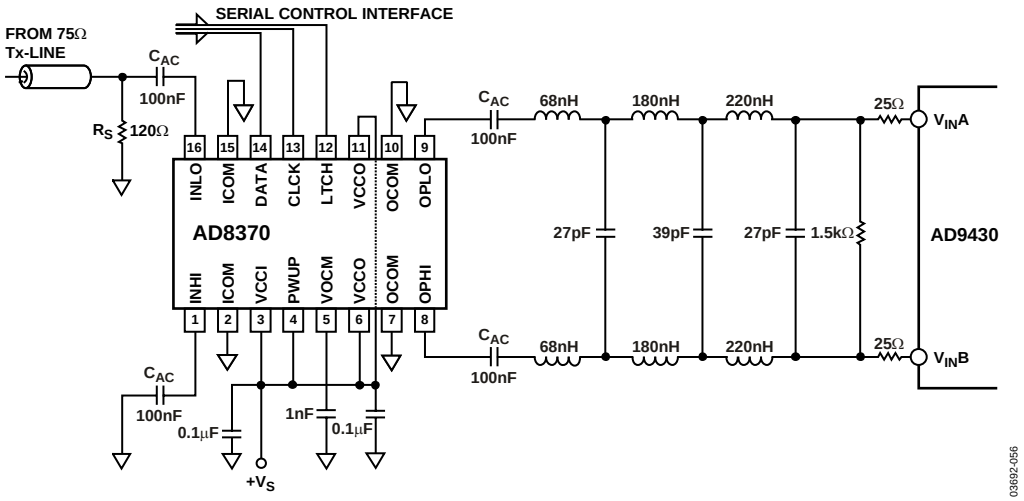

Figure 58. ADC Interface Example

EVALUATION BOARD AND SOFTWARE

The evaluation board allows quick testing of the AD8370 by using standard 50 Ω test equipment. The schematic is shown in Figure 59. Transformers T1 and T2 are used to transform 50 Ω source and load impedances to the desired input and output reference levels. The top and bottom layers are shown in Figure 63 and Figure 64. The ground plane was removed under the traces between T1 and Pins INHI and INLO to approximate a 100 Ω characteristic impedance.

The evaluation board comes with the AD8370 control software that allows serial gain control from most computers. The evaluation board is connected via a cable to the parallel port of the computer. Adjusting the appropriate slider bar in the control software automatically updates the gain code of the AD8370 in either a linear or linear-in-dB fashion.

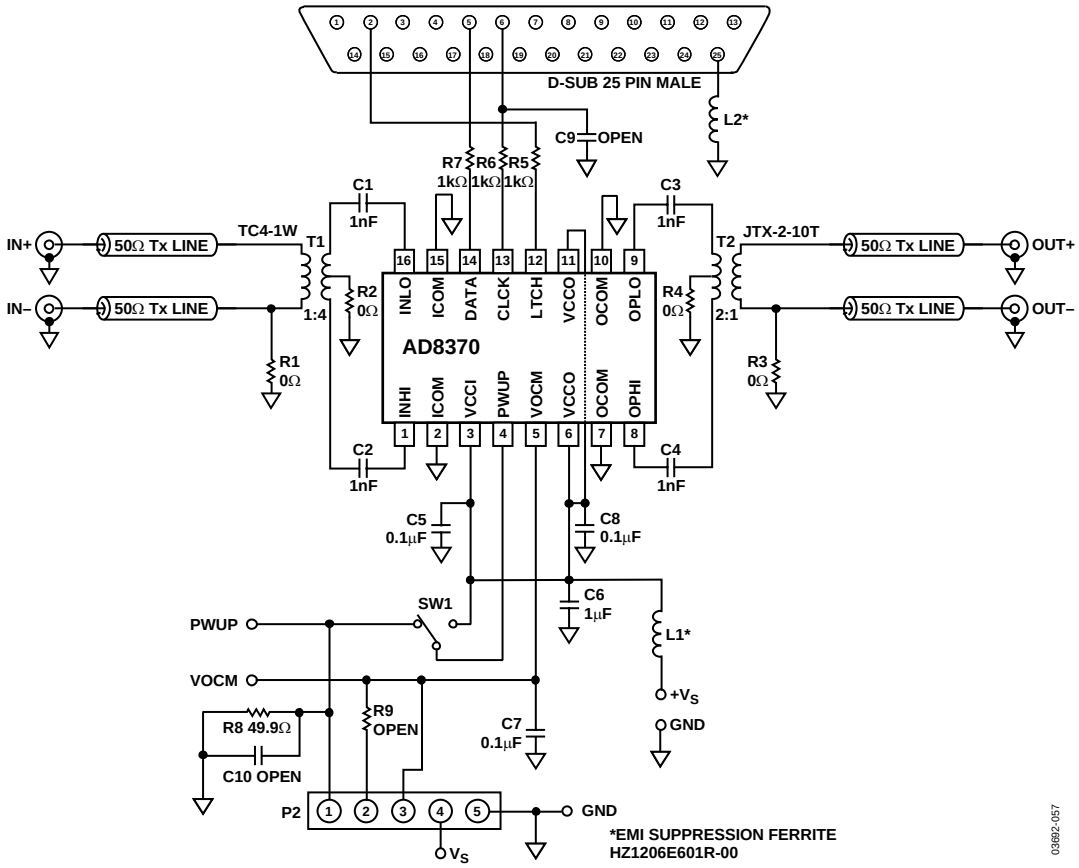

Figure 59. AD8370 Evaluation Board Schematic

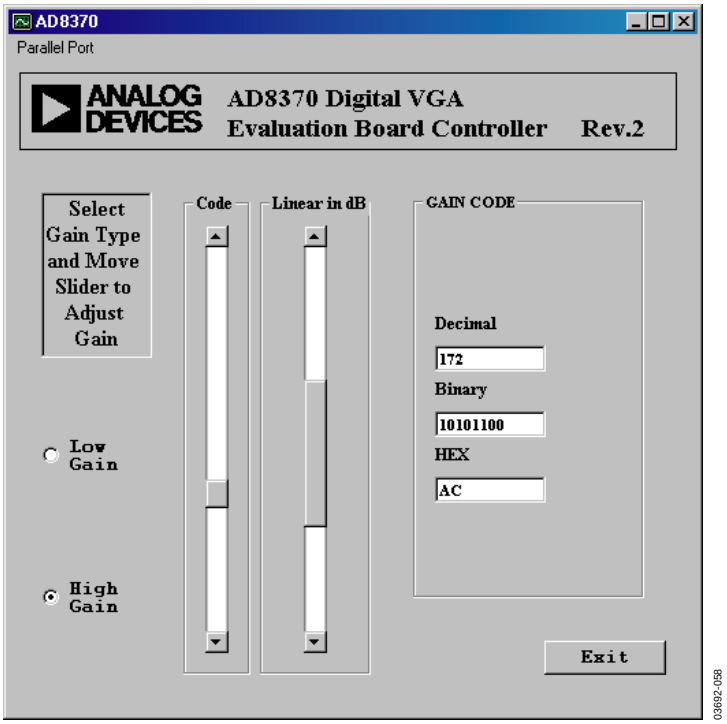

Figure 60. Evaluation Software

Table 7. AD8370 Evaluation Board Configuration Options

Component	Function	Default Condition
VS, GND, VOCM	Power Interface Vector Pins. Apply supply voltage between VS and GND. The VOCM pin allows external monitoring of the common-mode input and output bias levels.	Not applicable
SW1, R8, C10, PWUP	Device Enable. Set to Position B to power up the device. When in Position A, the PWUP pin is connected to the PWUP vector pin. The PWUP pin allows external power cycling of the device. R8 and C10 are provided to allow for proper cable termination.	SW1 = installed R8 = 49.9 Ω (Size 0805) C10 = open (Size 0805)
P1, R5, R6, R7, C9	Serial Control Interfaces. The evaluation board can be controlled using most PCs. Windows®-based control software is shipped with the evaluation kit. A 25-pin, D-sub connector cable is required to connect the PC to the evaluation board. It may be necessary to use a capacitor on the clock line, depending on the quality of the PC port signals. A 1 nF capacitor for C9 is usually sufficient for reducing clock overshoot.	P1 = installed R5, R6, R7 = 1 kΩ (Size 0603) C9 = open (Size 0603)
J1, J2, J6, J7	Input and Output Signal Connectors. These SMA connectors provide a convenient way to interface the evaluation board with 50 Ω test equipment. Typically, the device is evaluated using a single-ended source and load. The source should connect to J1 (IN+), and the load should connect to J6 (OUT+).	Not applicable
C1, C2, C3, C4	AC Coupling Capacitors. Provide ac coupling of the input and output signals.	C1, C2, C3, C4 = 1 nF (Size 0603)
T1, T2	Impedance Transformers. T1 provides a 50 Ω to 200 Ω impedance transformation. T2 provides a 100 Ω to 50 Ω impedance transformation.	T1 = TC4 –1W (Mini-Circuits) T2 = JTX–2–10T (Mini-Circuits)
R1, R2, R3, R4	Single-Ended or Differential. R2 and R4 are used to ground the center tap of the secondary windings on transformers T1 and T2. R1 and R3 should be used to ground J2 and J7 when used in single-ended applications.	R1, R2, R3, R4 = 0 Ω (Size 0603)
C5, C6, C7, C8 L1, L2	Power Supply Decoupling. Nominal supply decoupling consists of a ferrite bead series inductor followed by a 1 µF capacitor to ground followed by a 0.1 µF capacitor to ground positioned as close to the device as possible. C7 provides additional decoupling of the input common-mode voltage. L1 provides high frequency isolation between the input and output power supply. L2 provides high frequency isolation between the analog and digital ground.	C6 = 1 µF (Size 0805) C5, C7, C8 = 0.1 µF (Size 0603) L1, L2 = HZ1206E601R-00 (Steward, Size 1206)

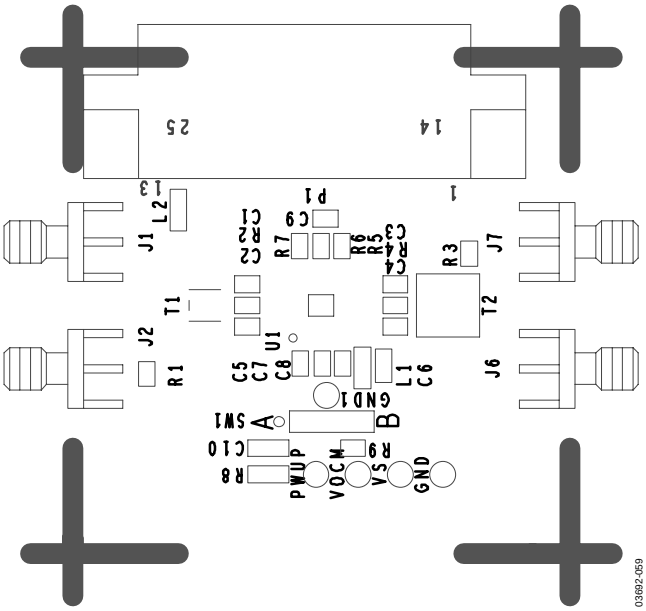

Figure 61. Evaluation Board Top Silkscreen

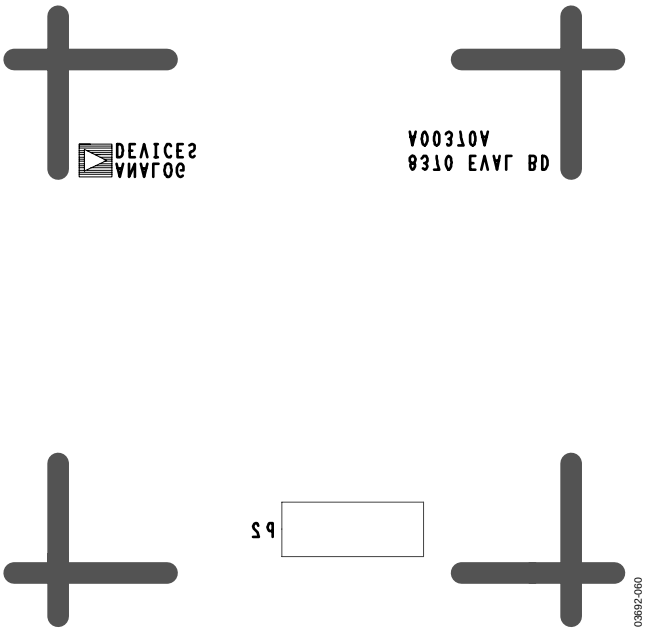

Figure 62. Evaluation Board Bottom Silkscreen

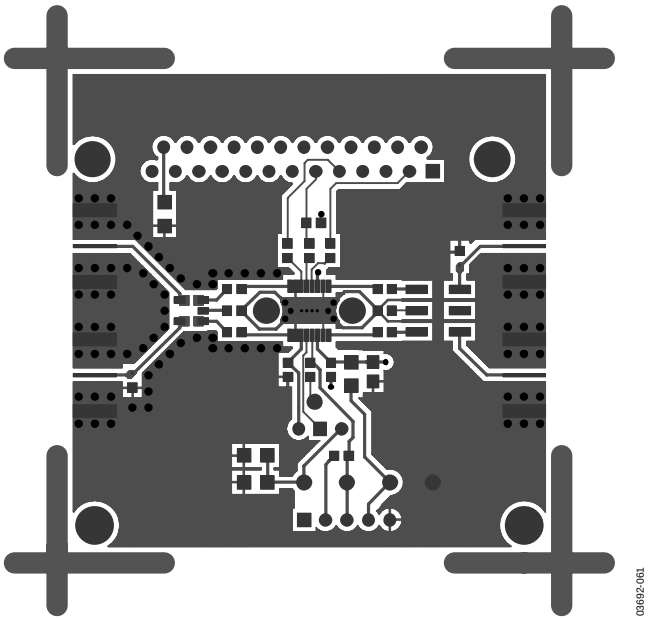

Figure 63. Evaluation Board Top

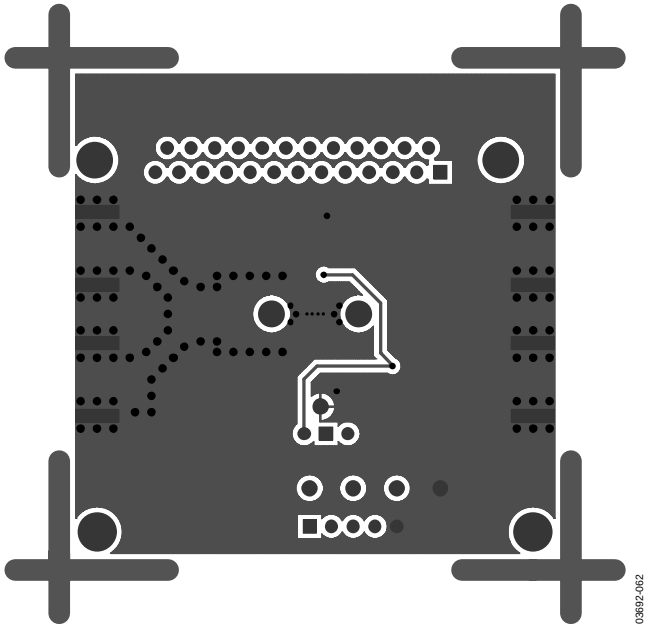

Figure 64. Evaluation Board Bottom

APPENDIX

CHARACTERIZATION EQUIPMENT

An Agilent N4441A Balanced-Measurement System was used to obtain the gain, phase, group delay, reverse isolation, CMRR, and s-parameter information contained in this data sheet. With the exception of the s-parameter information, T-attenuator pads were used to match the 50 Ω impedance of this instrument's ports to the AD8370. An Agilent 4795A Spectrum Analyzer was used to obtain nonlinear measurements IMD, IP3, and P1dB through matching baluns and/or attenuator networks. Various other measurements were taken with setups shown in this section.

COMPOSITE WAVEFORM ASSUMPTION

The nonlinear two-tone measurements made for this data sheet, that is, IMD and IP3, are based on the assumption of a fixed value composite waveform at the output, generally 1 V p-p. The frequencies of interest dictate the use of RF test equipment, and because this equipment is generally not designed to work in units of volts, but rather watts and dBm, an assumption was made to facilitate equipment setup and operation. Two sinusoidal tones can be represented as

$$V_1 = V \sin(2\pi f_1 t)$$

$$V_2 = V \sin(2\pi f_2 t)$$

The RMS average voltage of one tone is

$$\sqrt{\frac{1}{T}\int_0^T (V_1)^2\, dt} = \frac{1}{\sqrt{2}}$$

where T is the period of the waveform. The RMS average voltage of the two-tone composite signal is

$$\sqrt{\frac{1}{T}\int_0^T (V_1 + V_2)^2\, dt} = 1$$

It can be shown that the average power of this composite waveform is twice (3 dB) that of the single tone. This also means that the composite peak-to-peak voltage is twice (6 dB) that of a single tone. This principle can be used to set correct input amplitudes from generators scaled in dBm and is correct if the two tones are of equal amplitude and are reasonably close in frequency.

DEFINITIONS OF SELECTED PARAMETERS

Common-mode rejection ratio (Figure 28) has been defined for this characterization effort as

$$\frac{Differential\ Mode\ Gain}{Common\ Mode\ Gain}$$

where the numerator is the gain into a differential load at the output due to a differential source at the input, and the denominator is the gain into a differential-mode load at the output due to a common-mode source at the input. In terms of mixed-mode s-parameters, this equates to

$$\frac{SDD21}{SDC21}$$

More information on mixed-mode s-parameters can be obtained in a reference by Bockelman, D.E. and Eisenstadt, W.R., *Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation*. IEEE Transactions on Microwave Theory and Techniques, v 43, n 7, 1530 (July 1995).

Reverse isolation (Figure 26) is defined as SDD12.

Power supply rejection ratio (PSRR) is defined as

$$\frac{A_{dm}}{A_s}$$

where A_{dm} is the differential mode forward gain (SDD21), and A_s is the gain from the power supply pins (VCCI and VCCO, taken together) to the output (OPLO and OPHI, taken differentially), corrected for impedance mismatch. The following reference provides more information: Gray, P.R., Hurst, P.J., Lewis, S.H. and Meyer, R.G., *Analysis and Design of Analog Integrated Circuits*, *4th Edition*, John Wiley & Sons, Inc., page 422.

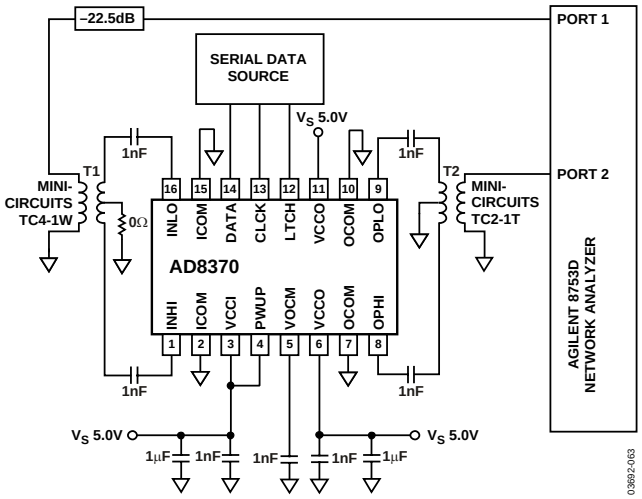

Figure 65. PSRR A_{dm} Test Setup

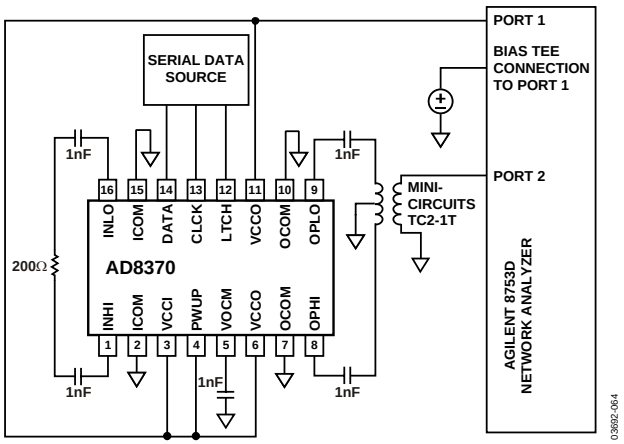

Figure 66. PSRR A_s Test Setup

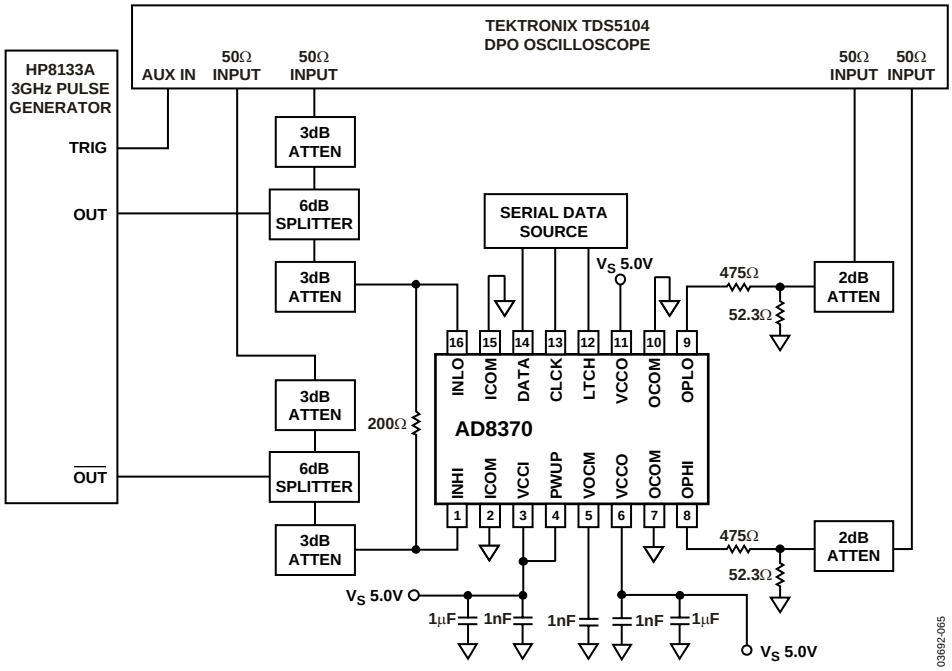

Figure 67. DC Pulse Response and Overdrive Recovery Test Setup

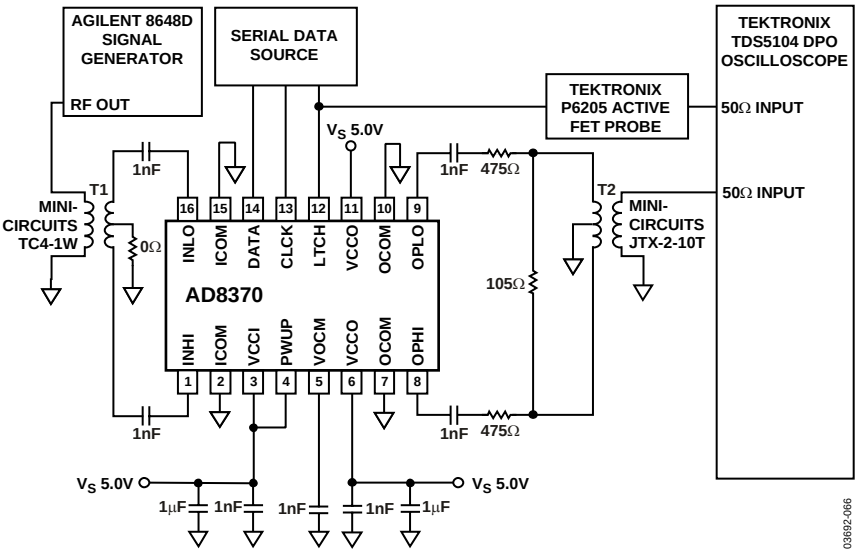

Figure 68. Gain Step Time Domain Response Test Setup

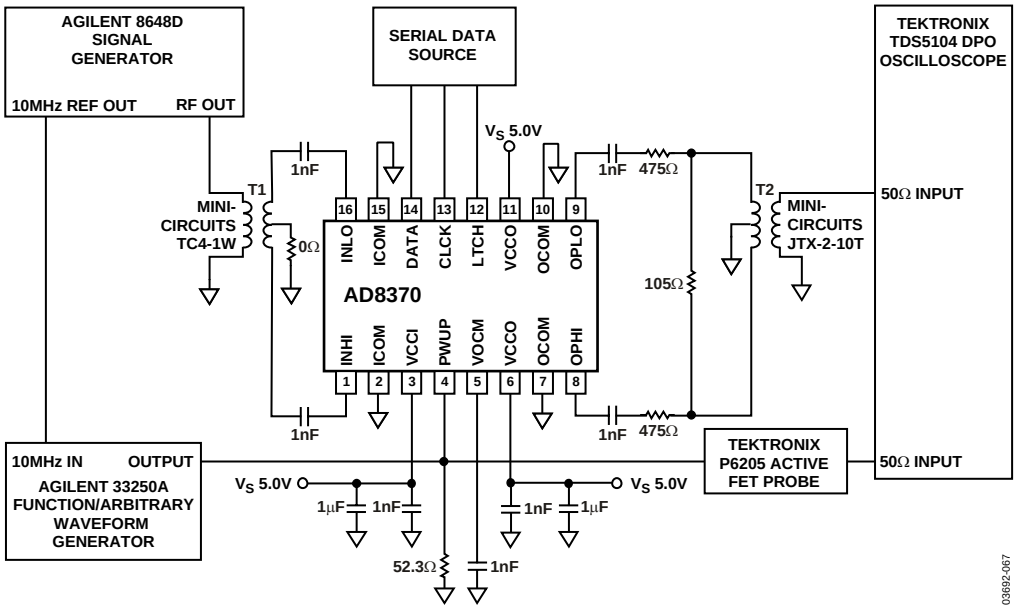

Figure 69. PWUP Response Time Domain Test Setup