3 nV/√Hz, Low Power Instrumentation Amplifier

Data Sheet

AD8421

FEATURES

- Low power
  - 2.3 mA maximum supply current
- Low noise
  - 3.2 nV/√Hz maximum input voltage noise at 1 kHz
  - 200 fA/√Hz current noise at 1 kHz
- Excellent ac specifications
  - 10 MHz bandwidth (G = 1)
  - 2 MHz bandwidth (G = 100)
  - 0.6 µs settling time to 0.001% (G = 10)
  - 80 dB CMRR at 20 kHz (G = 1)
  - 35 V/µs slew rate
- High precision dc performance (AD8421BRZ)
  - 94 dB CMRR minimum (G = 1)
  - 0.2 µV/°C maximum input offset voltage drift
  - 1 ppm/°C maximum gain drift (G = 1)
  - 500 pA maximum input bias current
- Inputs protected to 40 V from opposite supply
- ±2.5 V to ±18 V dual supply (5 V to 36 V single supply)
- Gain set with a single resistor (G = 1 to 10,000)
- Available in 8-lead LFCSP, 8-lead MSOP, and 8-lead SOIC

APPLICATIONS

- Medical instrumentation
- Precision data acquisition
- Microphone preamplification
- Vibration analysis
- Multiplexed input applications
- ADC driver

TYPICAL APPLICATION DIAGRAM

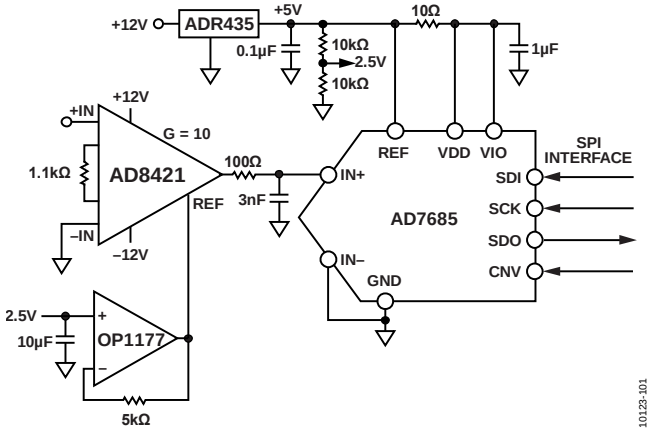

Figure 1. AD8421 Driving 16-Bit AD7685

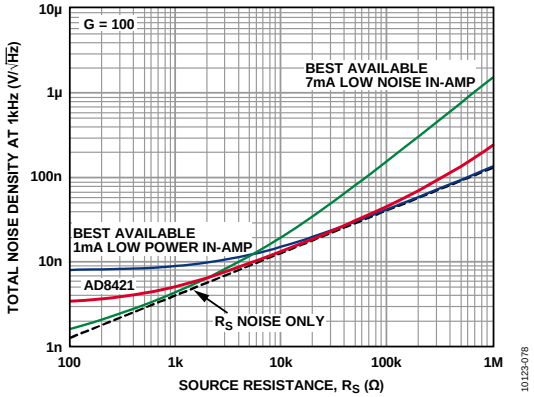

Figure 2. Noise Density vs. Source Resistance

GENERAL DESCRIPTION

The AD8421 is a low cost, low power, extremely low noise, ultralow bias current, high speed instrumentation amplifier that is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This product features extremely high CMRR, allowing it to extract low level signals in the presence of high frequency common-mode noise over a wide temperature range.

The 10 MHz bandwidth, 35 V/µs slew rate, and 0.6 µs settling time to 0.001% (G = 10) allow the AD8421 to amplify high speed signals and excel in applications that require high channel count, multiplexed systems. Even at higher gains, the current feedback architecture maintains high performance; for example, at G = 100, the bandwidth is 2 MHz and the settling time is 0.8 µs. The AD8421 has excellent distortion performance, making it suitable for use in demanding applications such as vibration analysis.

The AD8421 delivers 3 nV/√Hz input voltage noise and 200 fA/√Hz current noise with only 2 mA quiescent current, making it an ideal choice for measuring low level signals. For applications with high source impedance, the AD8421 employs innovative process technology and design techniques to provide noise performance that is limited only by the sensor.

The AD8421 uses unique protection methods to ensure robust inputs while still maintaining very low noise. This protection allows input voltages up to 40 V from the opposite supply rail without damage to the part.

A single resistor sets the gain from 1 to 10,000. The reference pin can be used to apply a precise offset to the output voltage.

The AD8421 is specified from −40°C to +85°C for the 8-lead MSOP and SOIC packages, and from −40°C to +125°C for the 8-lead LFCSP package.

Rev. A

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REVISION HISTORY

10/2020—Rev. 0 to Rev. A

Added 8-Lead LFCSP ... Throughout
Changed Pin Connection Diagram Section to Typical Application Diagram Section ... 1
Changes to Features Section, Figure 1, and General Description Section ... 1
Added ACP Grade Section and Table 3; Renumbered Sequentially ... 7
Changes to Table 5 ... 10
Changes to Figure 44 ... 18
Changes to Figure 72 ... 28
Added Figure 76; Renumbered Sequentially ... 29
Changes to Ordering Guide ... 30

5/2012—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted.

AR AND BR GRADES

Table 1.

Parameter	Test Conditions/ Comments	AR Grade			BR Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
COMMON-MODE REJECTION RATIO (CMRR)								
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V							
G = 1		86			94			dB
G = 10		106			114			dB
G = 100		126			134			dB
G = 1000		136			140			dB
Over Temperature, G = 1	T = −40°C to +85°C	80			93			dB
CMRR at 20 kHz	V_{CM} = −10 V to +10 V							
G = 1		80			80			dB
G = 10		90			100			dB
G = 100		100			110			dB
G = 1000		110			120			dB
NOISE								
Voltage Noise, 1 kHz[1]	V_{IN}+, V_{IN}− = 0 V							
Input Voltage Noise, e_{ni}			3	3.2		3	3.2	nV/√Hz
Output Voltage Noise, e_{no}				60			60	nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2	2.2	µV p-p
G = 10			0.5			0.5		µV p-p
G = 100 to 1000			0.07			0.07	0.09	µV p-p
Current Noise								
Spectral Density	f = 1 kHz		200			200		fA/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz		18			18		pA p-p
VOLTAGE OFFSET[2]								
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			60			25	µV
Over Temperature	T_A = −40°C to +85°C			86			45	µV
Average TC				0.4			0.2	µV/°C
Output Offset Voltage, V_{OSO}				350			250	µV
Over Temperature	T_A = −40°C to +85°C			0.66			0.45	mV
Average TC				6			5	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.5 V to ±18 V							
G = 1		90	120		100	120		dB
G = 10		110	120		120	140		dB
G = 100		124	130		140	150		dB
G = 1000		130	140		140	150		dB
INPUT CURRENT								
Input Bias Current			1	2		0.1	0.5	nA
Over Temperature	T_A = −40°C to +85°C			8			6	nA
Average TC			50			50		pA/°C
Input Offset Current			0.5	2		0.1	0.5	nA
Over Temperature	T_A = −40°C to +85°C			2.2			0.8	nA
Average TC			1			1		pA/°C

Parameter	Test Conditions/ Comments	AR Grade Min	AR Grade Typ	AR Grade Max	BR Grade Min	BR Grade Typ	BR Grade Max	Unit
DYNAMIC RESPONSE								
Small Signal Bandwidth	−3 dB							
G = 1			10			10		MHz
G = 10			10			10		MHz
G = 100			2			2		MHz
G = 1000			0.2			0.2		MHz
Settling Time to 0.01%	10 V step							
G = 1			0.7			0.7		µs
G = 10			0.4			0.4		µs
G = 100			0.6			0.6		µs
G = 1000			5			5		µs
Settling Time to 0.001%	10 V step							
G = 1			1			1		µs
G = 10			0.6			0.6		µs
G = 100			0.8			0.8		µs
G = 1000			6			6		µs
Slew Rate								
G = 1 to 100			35			35		V/µs
GAIN[3]	$G = 1 + (9.9\ k\Omega/R_G)$							
Gain Range		1		10,000	1		10,000	V/V
Gain Error	$V_{OUT} = \pm 10$ V							
G = 1				0.02			0.01	%
G = 10 to 1000				0.2			0.1	%
Gain Nonlinearity	$V_{OUT} = -10$ V to +10 V							
G = 1	$R_L \geq 2\ k\Omega$			1			1	ppm
	$R_L = 600\ \Omega$		1	3		1	3	ppm
G = 10 to 1000	$R_L \geq 600\ \Omega$		30	50		30	50	ppm
	$V_{OUT} = -5$ V to +5 V		5	10		5	10	ppm
Gain vs. Temperature[3]								
G = 1				5		0.1	1	ppm/°C
G > 1				−50			−50	ppm/°C
INPUT								
Input Impedance								
Differential			30||3			30||3		GΩ||pF
Common Mode			30||3			30||3		GΩ||pF
Input Operating Voltage Range[4]	$V_S = \pm 2.5$ V to ±18 V	$-V_S + 2.3$		$+V_S - 1.8$	$-V_S + 2.3$		$+V_S - 1.8$	V
Over Temperature	$T_A = -40°C$	$-V_S + 2.5$		$+V_S - 2.0$	$-V_S + 2.5$		$+V_S - 2.0$	V
	$T_A = +85°C$	$-V_S + 2.1$		$+V_S - 1.8$	$-V_S + 2.1$		$+V_S - 1.8$	V
OUTPUT	$R_L = 2\ k\Omega$							
Output Swing	$V_S = \pm 2.5$ V to ±18 V	$-V_S + 1.2$		$+Vs - 1.6$	$-V_S + 1.2$		$+V_S - 1.6$	V
Over Temperature	$T_A = -40°C$ to +85°C	$-V_S + 1.2$		$+Vs - 1.6$	$-V_S + 1.2$		$+V_S - 1.6$	V
Short-Circuit Current			65			65		mA
REFERENCE INPUT								
R_{IN}			20			20		kΩ
I_{IN}	$V_{IN}+, V_{IN}- = 0$ V		20	24		20	24	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		V/V

Parameter	Test Conditions/ Comments	AR Grade Min	AR Grade Typ	AR Grade Max	BR Grade Min	BR Grade Typ	BR Grade Max	Unit
POWER SUPPLY								
Operating Range	Dual supply	±2.5		±18	±2.5		±18	V
	Single supply	5		36	5		36	V
Quiescent Current			2	2.3		2	2.3	mA
Over Temperature	T_A = −40°C to +85°C			2.6			2.6	mA
TEMPERATURE RANGE								
For Specified Performance		−40		+85	−40		+85	°C
Operational[5]		−40		+125	−40		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2 + e_{RG}^2)}$. See the Theory of Operation section for more information.
[2] Total RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$.
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G > 1, add R_G errors to the specifications given in this table.
[4] Input voltage range of the AD8421 input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more details.
[5] See the Typical Performance Characteristics section for expected operation between 85°C and 125°C.

ARM AND BRM GRADES

Table 2.

Parameter	Test Conditions/ Comments	ARM Grade Min	ARM Grade Typ	ARM Grade Max	BRM Grade Min	BRM Grade Typ	BRM Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)								
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V							
G = 1		84			92			dB
G = 10		104			112			dB
G = 100		124			132			dB
G = 1000		134			140			dB
Over Temperature, G = 1	T_A = −40°C to +85°C	80			90			dB
CMRR at 20 kHz	V_{CM} = −10 V to +10 V							
G = 1		80			80			dB
G = 10		90			90			dB
G = 100		100			100			dB
G = 1000		100			100			dB
NOISE								
Voltage Noise, 1 kHz[1]	V_{IN}+, V_{IN}− = 0 V							
Input Voltage Noise, e_{ni}			3	3.2		3	3.2	nV/√Hz
Output Voltage Noise, e_{no}				60			60	nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2	2.2	µV p-p
G = 10			0.5			0.5		µV p-p
G = 100 to 1000			0.07			0.07	0.09	µV p-p
Current Noise								
Spectral Density	f = 1 kHz		200			200		fA/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz		18			18		pA p-p
VOLTAGE OFFSET[2]								
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			70			50	µV
Over Temperature	T_A = −40°C to +85°C			135			135	µV
Average TC				0.9			0.9	µV/°C
Output Offset Voltage, V_{OSO}				600			400	µV
Over Temperature	T_A = −40°C to +85°C			1			1	mV
Average TC				9			9	µV/°C

Parameter	Test Conditions/ Comments	ARM Grade			BRM Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Offset RTI vs. Supply (PSR)	V_S = ±2.5 V to ±18 V							
G = 1		90	120		100	120		dB
G = 10		110	120		120	140		dB
G = 100		124	130		140	150		dB
G = 1000		130	140		140	150		dB
INPUT CURRENT								
Input Bias Current			1	2		0.1	1	nA
Over Temperature	T_A = −40°C to +85°C			8			6	nA
Average TC			50			50		pA/°C
Input Offset Current			0.5	2		0.1	1	nA
Over Temperature	T_A = −40°C to +85°C			3			1.5	nA
Average TC			1			1		pA/°C
DYNAMIC RESPONSE								
Small Signal Bandwidth	−3 dB							
G = 1			10			10		MHz
G = 10			10			10		MHz
G = 100			2			2		MHz
G = 1000			0.2			0.2		MHz
Settling Time 0.01%	10 V step							
G = 1			0.7			0.7		µs
G = 10			0.4			0.4		µs
G = 100			0.6			0.6		µs
G = 1000			5			5		µs
Settling Time 0.001%	10 V step							
G = 1			1			1		µs
G = 10			0.6			0.6		µs
G = 100			0.8			0.8		µs
G = 1000			6			6		µs
Slew Rate								
G = 1 to 100			35			35		V/µs
GAIN[3]	G = 1 + (9.9 kΩ/R_G)							
Gain Range		1		10,000	1		10,000	V/V
Gain Error	V_{OUT} = ±10 V							
G = 1				0.05			0.02	%
G = 10 to 1000				0.3			0.2	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1	R_L ≥ 2 kΩ			1			1	ppm
	R_L = 600 Ω		1	3		1	3	ppm
G = 10 to 1000	R_L ≥ 600 Ω		30	50		30	50	ppm
	V_{OUT} = −5 V to +5 V		5	10		5	10	ppm
Gain vs. Temperature[3]								
G = 1				5		0.1	1	ppm/°C
G > 1				−50			−50	ppm/°C
INPUT								
Input Impedance								
Differential			30||3			30||3		GΩ||pF
Common Mode			30||3			30||3		GΩ||pF
Input Operating Voltage Range[4]	V_S = ±2.5 V to ±18 V	$-V_S$ + 2.3		$+V_S$ − 1.8	$-V_S$ + 2.3		$+V_S$ − 1.8	V
Over Temperature	T_A = −40°C	$-V_S$ + 2.5		$+V_S$ − 2.0	$-V_S$ + 2.5		$+V_S$ − 2.0	V
	T_A = +85°C	$-V_S$ + 2.1		$+V_S$ − 1.8	$-V_S$ + 2.1		$+V_S$ − 1.8	V

Parameter	Test Conditions/ Comments	ARM Grade Min	ARM Grade Typ	ARM Grade Max	BRM Grade Min	BRM Grade Typ	BRM Grade Max	Unit
OUTPUT	R_L = 2 kΩ							
Output Swing	V_S = ±2.5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ – 1.6	$-V_S$ + 1.2		+Vs – 1.6	V
Over Temperature	T_A = −40°C to +85°C	$-V_S$ + 1.2		$+V_S$ – 1.6	$-V_S$ + 1.2		+Vs – 1.6	V
Short-Circuit Current			65			65		mA
REFERENCE INPUT								
R_{IN}			20			20		kΩ
I_{IN}	V_{IN}+, V_{IN}− = 0 V		20	24		20	24	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		V/V
POWER SUPPLY								
Operating Range	Dual supply	±2.5		±18	±2.5		±18	V
	Single supply	5		36	5		36	V
Quiescent Current			2	2.3		2	2.3	mA
Over Temperature	T_A = −40°C to +85°C			2.6			2.6	mA
TEMPERATURE RANGE								
For Specified Performance		−40		+85	−40		+85	°C
Operational[5]		−40		+125	−40		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2 + e_{RG}^2)}$. See the Theory of Operation section for more information.
[2] Total RTI V_{OS} = (V_{OSI}) + (V_{OSO}/G).
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G > 1, add R_G errors to the specifications given in this table.
[4] Input voltage range of the AD8421 input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more information.
[5] See the Typical Performance Characteristics section for expected operation between 85°C and 125°C.

ACP GRADE

Table 3.

Parameter	Test Conditions/Comments	ACP Grade Min	ACP Grade Typ	ACP Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V				
G = 1			84		dB
G = 10			104		dB
G = 100			124		dB
G = 1000			134		dB
Over Temperature, G = 1	T_A = −40°C to +125°C		80		dB
CMRR at 20 kHz	V_{CM} = −10 V to +10 V				
G = 1			80		dB
G = 10			90		dB
G = 100			100		dB
G = 1000			100		dB
NOISE					
Voltage Noise, 1 kHz[1]	V_{IN}+, V_{IN}− = 0 V				
Input Voltage Noise, e_{ni}			3	3.2	nV/√Hz
Output Voltage Noise, e_{no}				60	nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz				
G = 1			2		µV p-p
G = 10			0.5		µV p-p
G = 100 to 1000			0.07		µV p-p
Current Noise					
Spectral Density	f = 1 kHz		200		fA/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz		18		pA p-p

Parameter	Test Conditions/Comments	ACP Grade Min	Typ	Max	Unit
VOLTAGE OFFSET[2]					
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			70	µV
Over Temperature	T_A = −40°C to +125°C			135	µV
Average TC				0.9	µV/°C
Output Offset Voltage, V_{OSO}				600	µV
Over Temperature	T_A = −40°C to +125°C			1	mV
Average TC				9	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.5 V to ±18 V				
G = 1		90	120		dB
G = 10		110	120		dB
G = 100		124	130		dB
G = 1000		130	140		dB
INPUT CURRENT					
Input Bias Current			1	2	nA
Over Temperature	T_A = −40°C to +125°C			8	nA
Average TC			50		pA/°C
Input Offset Current			0.5	2	nA
Over Temperature	T_A = −40°C to +125°C			3	nA
Average TC			1		pA/°C
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
G = 1			10		MHz
G = 10			10		MHz
G = 100			2		MHz
G = 1000			0.2		MHz
Settling Time 0.01%	10 V step				
G = 1			0.7		µs
G = 10			0.4		µs
G = 100			0.6		µs
G = 1000			5		µs
Settling Time 0.001%	10 V step				
G = 1			1		µs
G = 10			0.6		µs
G = 100			0.8		µs
G = 1000			6		µs
Slew Rate					
G = 1 to 100			35		V/µs
GAIN[3]	G = 1 + (9.9 kΩ/R_G)				
Gain Range		1		10,000	V/V
Gain Error	V_{OUT} = ±10 V				
G = 1				0.03	%
G = 10 to 1000				0.3	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V				
G = 1	R_L ≥ 2 kΩ			1	ppm
	R_L = 600 Ω		1	3	ppm
G = 10 to 1000	R_L ≥ 600 Ω		30	50	ppm
	V_{OUT} = −5 V to +5 V		5	10	ppm
Gain vs. Temperature[3]	T_A = −40°C to +125°C				
G = 1				1	ppm/°C
G > 1				−50	ppm/°C

Parameter	Test Conditions/Comments	ACP Grade Min	Typ	Max	Unit
INPUT					
Input Impedance					
Differential			30||3		GΩ||pF
Common Mode			30||3		GΩ||pF
Input Operating Voltage Range[4]	V_S = ±2.5 V to ±18 V	$-V_S$ + 2.3		$+V_S$ − 1.8	V
Over Temperature	T_A = −40°C	$-V_S$ + 2.5		$+V_S$ − 2.0	V
	T_A = +125°C	$-V_S$ + 2.4		$+V_S$ − 2.1	V
OUTPUT	R_L = 2 kΩ				
Output Swing	V_S = ±2.5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.7	V
Over Temperature	T_A = −40°C to +125°C	$-V_S$ + 1.2		$+V_S$ − 1.9	V
Short-Circuit Current			65		mA
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	V_{IN}+, V_{IN}− = 0 V		20	24	µA
Voltage Range		$-V_S$		$+V_S$	V
Reference Gain to Output			1 ± 0.0001		V/V
POWER SUPPLY					
Operating Range	Dual supply	±2.5		±18	V
	Single supply	5		36	V
Quiescent Current			2	2.3	mA
Over Temperature	T_A = −40°C to +125°C			2.6	mA
TEMPERATURE RANGE					
For Specified Performance		−40		+125	°C
Operational		−40		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2 + e_{RG}^2)}$. See the Theory of Operation section for more information.
[2] Total RTI V_{OS} = (V_{OSI}) + (V_{OSO}/G).
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G > 1, add R_G errors to the specifications given in this table.
[4] Input voltage range of the AD8421 input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more information.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN or +IN[1]	$-V_S$ + 40 V
Minimum Voltage at −IN or +IN	$+V_S$ − 40 V
Maximum Voltage at REF[2]	$+V_S$ + 0.3 V
Minimum Voltage at REF	$-V_S$ − 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature	150°C
ESD	
Human Body Model	2 kV
Charged Device Model	1.25 kV
Machine Model	0.2 kV

[1] For voltages beyond these limits, use input protection resistors. See the Theory of Operation section for more information.
[2] There are ESD protection diodes from the reference input to each supply, so REF cannot be driven beyond the supplies in the same way that +IN and −IN can. See the Reference Terminal section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air using a 4-layer JEDEC printed circuit board (PCB).

Table 5.

Package	θ_{JA}	Unit
8-Lead SOIC	107.8	°C/W
8-Lead MSOP	138.6	°C/W
8-Lead LFCSP	53.65	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

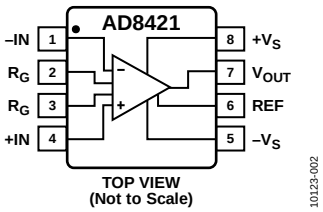

Figure 3. 8-Lead SOIC and 8-Lead MSOP Pin Configuration

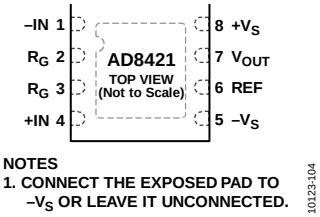

Figure 4. 8-Lead LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal.
2, 3	R_G	Gain Setting Terminals. Place resistor across the R_G pins to set the gain. G = 1 + (9.9 kΩ/R_G).
4	+IN	Positive Input Terminal.
5	$-V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, R_L = 2 kΩ, unless otherwise noted.

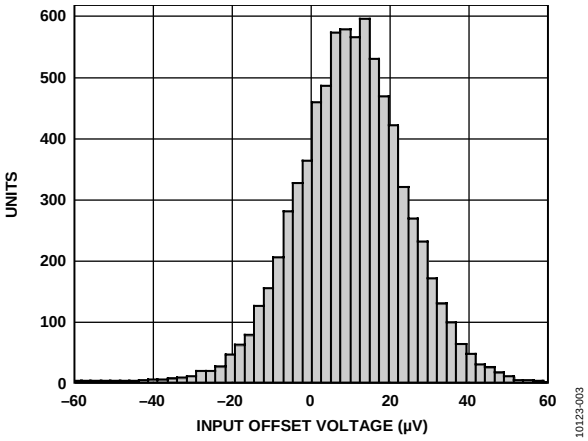

Figure 5. Typical Distribution of Input Offset Voltage

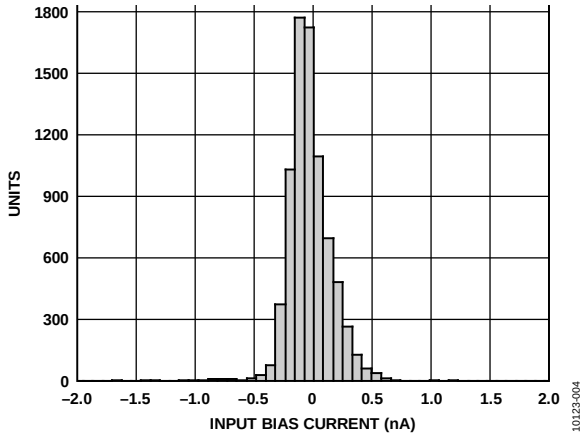

Figure 6. Typical Distribution of Input Bias Current

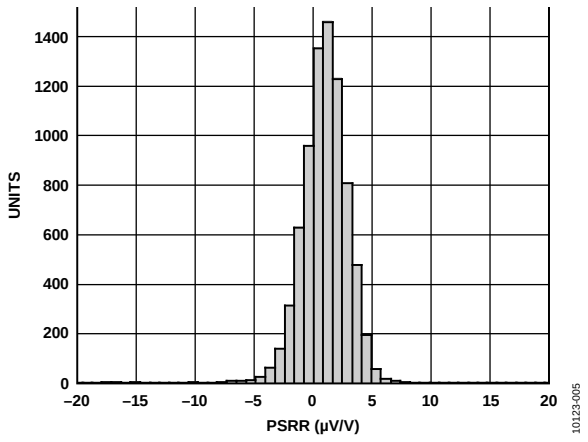

Figure 7. Typical Distribution of PSRR (G = 1)

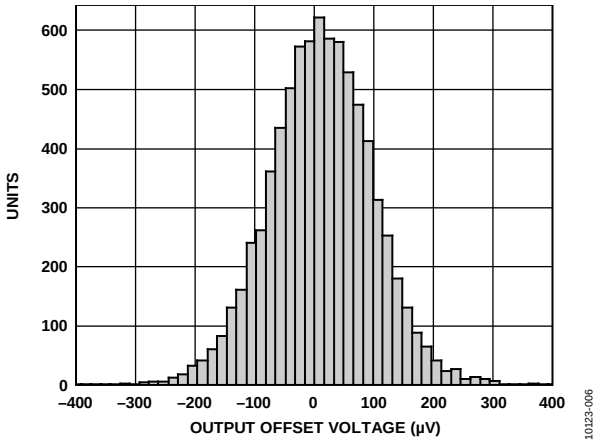

Figure 8. Typical Distribution of Output Offset Voltage

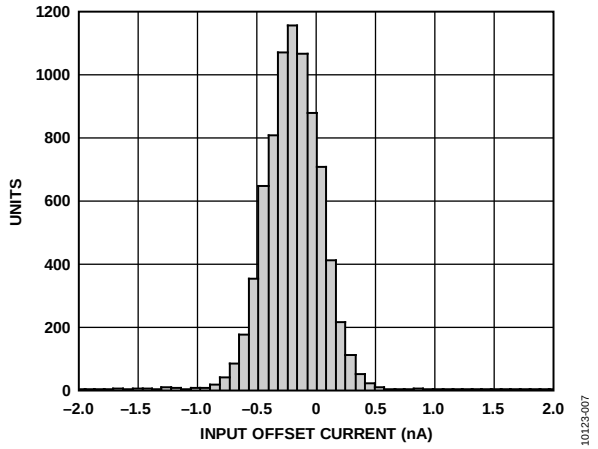

Figure 9. Typical Distribution of Input Offset Current

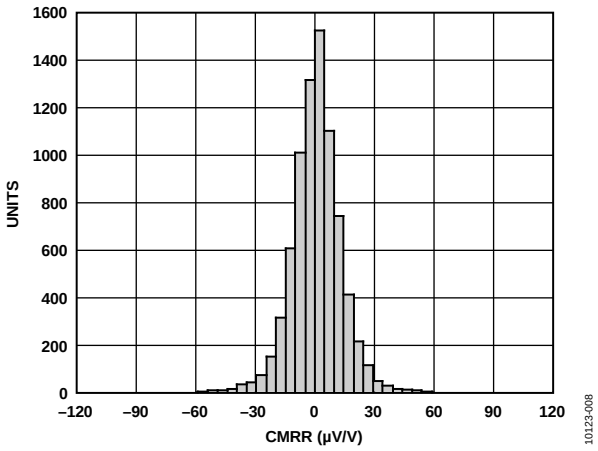

Figure 10. Typical Distribution of CMRR (G = 1)

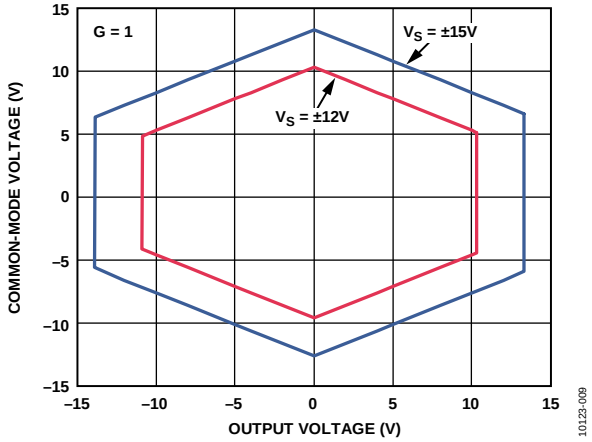

Figure 11. Input Common-Mode Voltage vs. Output Voltage; V_S = ±12 V and ±15 V (G = 1)

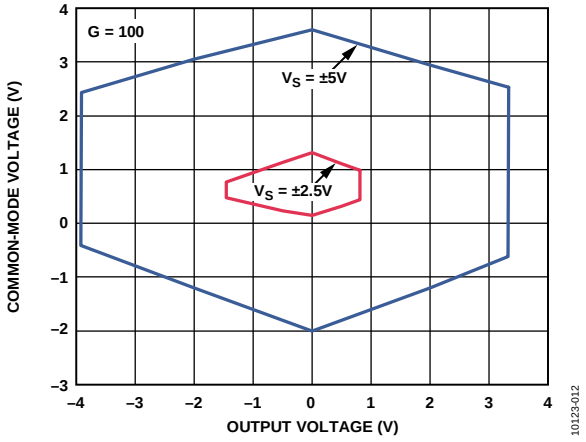

Figure 14. Input Common-Mode Voltage vs. Output Voltage; V_S = ±2.5 V and ±5 V (G = 100)

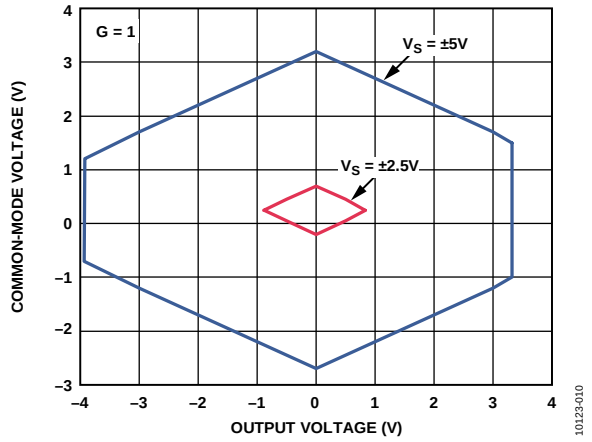

Figure 12. Input Common-Mode Voltage vs. Output Voltage; V_S = ±2.5 V and ±5 V (G = 1)

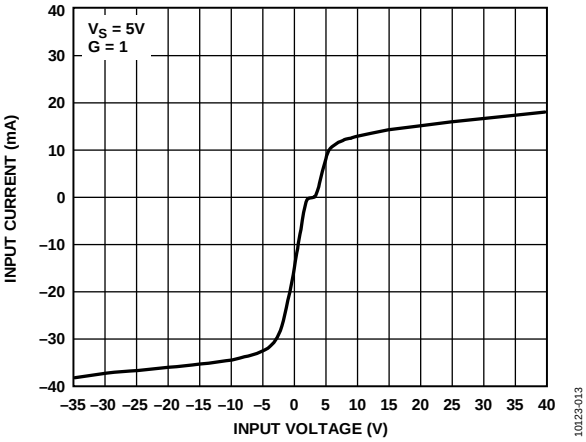

Figure 15. Input Overvoltage Performance; G = 1, $+V_S$ = 5 V, $-V_S$ = 0 V

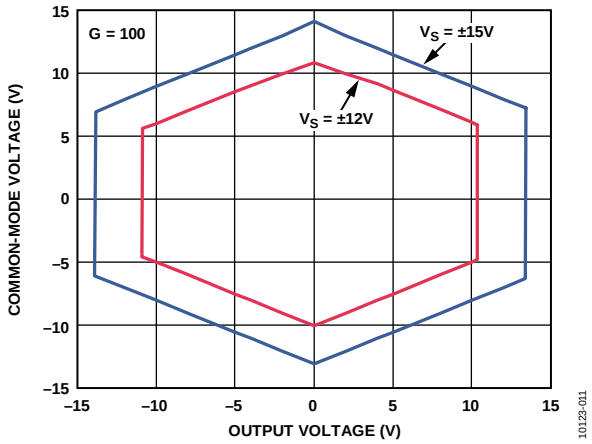

Figure 13. Input Common-Mode Voltage vs. Output Voltage; V_S = ±12 V and ±15 V (G = 100)

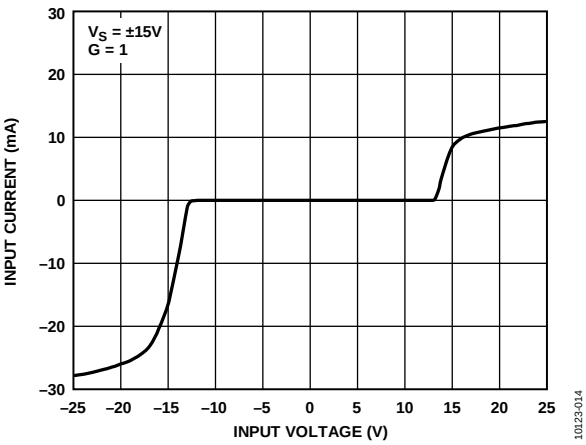

Figure 16. Input Overvoltage Performance; G = 1, V_S = ±15 V

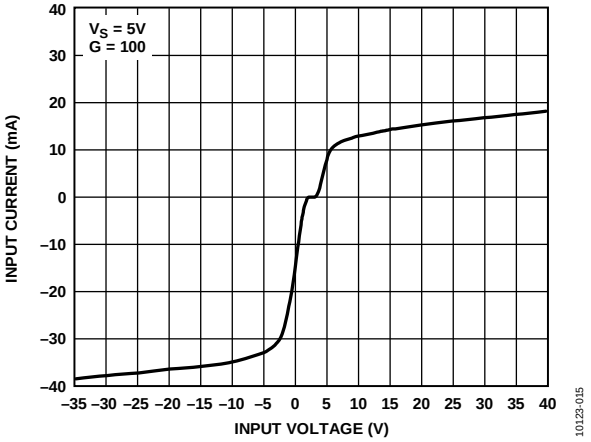

Figure 17. Input Overvoltage Performance; $+V_S$ = 5 V, $-V_S$ = 0 V, G = 100

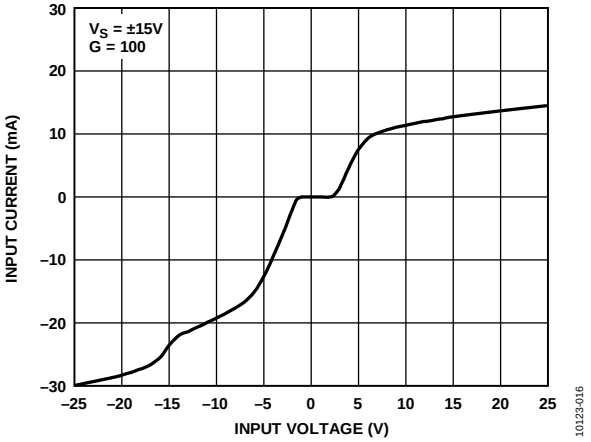

Figure 18. Input Overvoltage Performance; V_S = ±15 V, G = 100

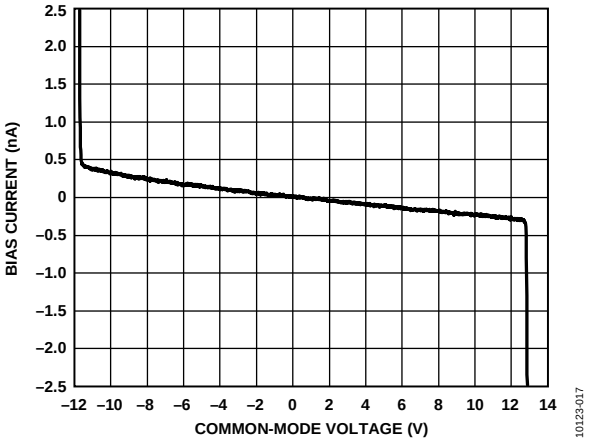

Figure 19. Input Bias Current vs. Common-Mode Voltage

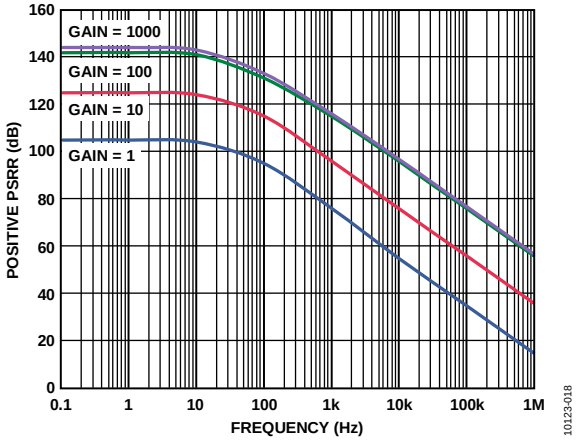

Figure 20. Positive PSRR vs. Frequency

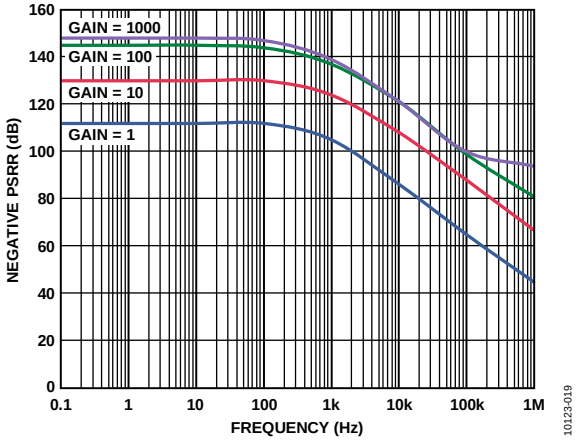

Figure 21. Negative PSRR vs. Frequency

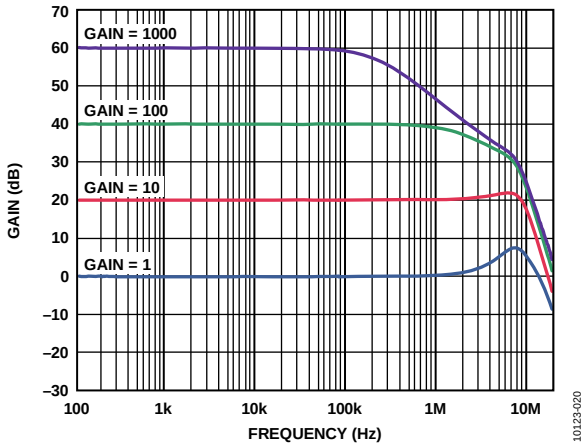

Figure 22. Gain vs. Frequency

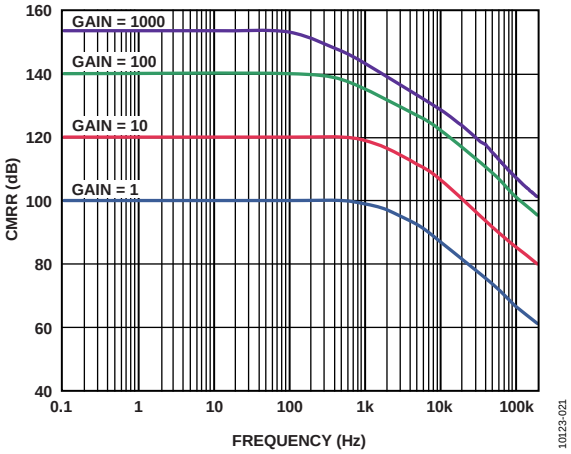

Figure 23. CMRR vs. Frequency

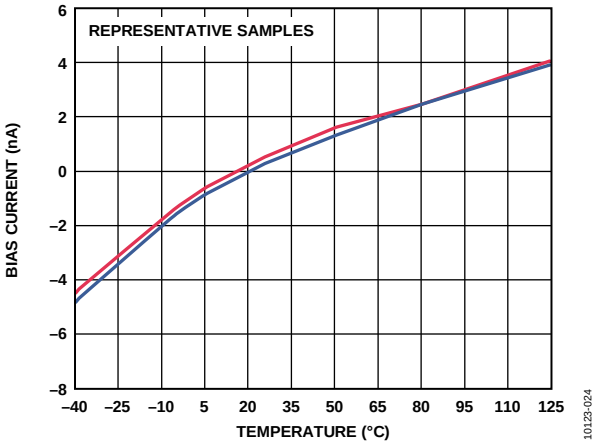

Figure 26. Input Bias Current vs. Temperature

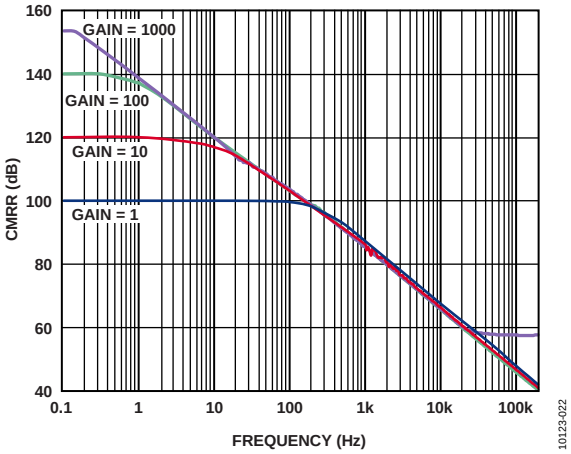

Figure 24. CMRR vs. Frequency, 1 kΩ Source Imbalance

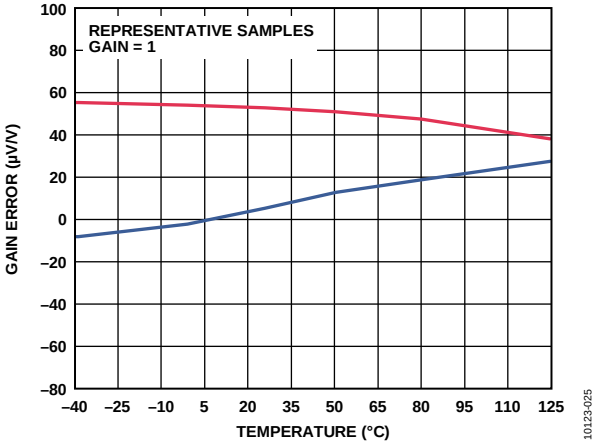

Figure 27. Gain vs. Temperature (G = 1)

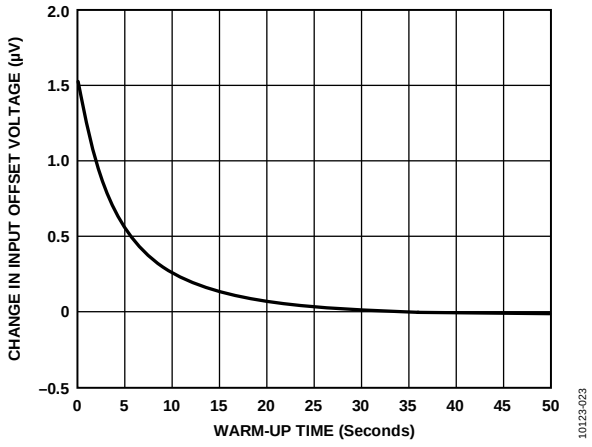

Figure 25. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

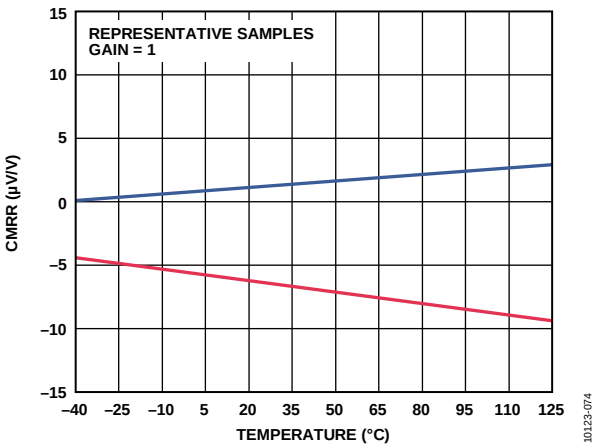

Figure 28. CMRR vs. Temperature (G = 1)

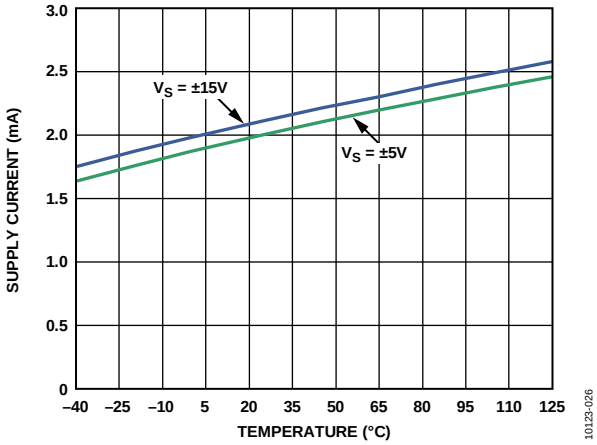

Figure 29. Supply Current vs. Temperature (G = 1)

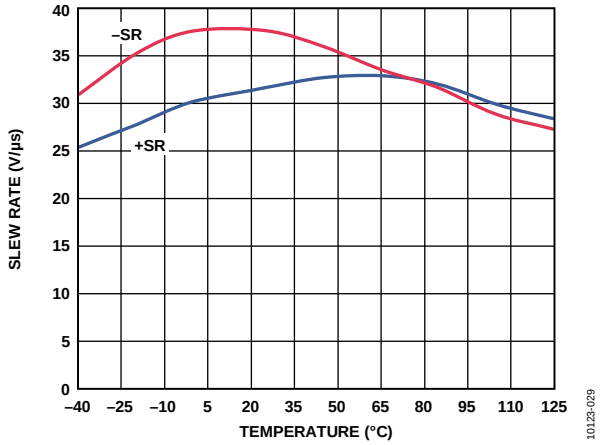

Figure 32. Slew Rate vs. Temperature, V_S = ±5 V (G = 1)

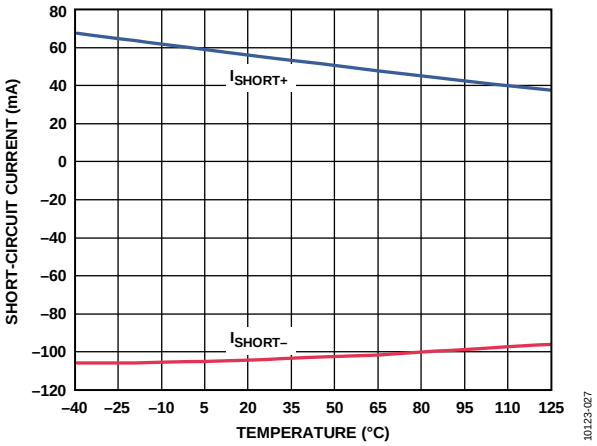

Figure 30. Short-Circuit Current vs. Temperature (G = 1)

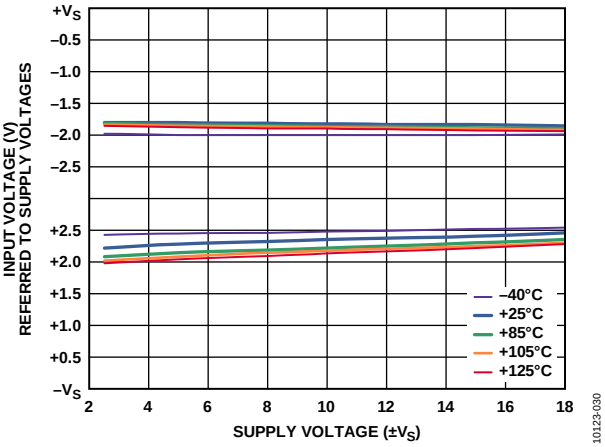

Figure 33. Input Voltage Limit vs. Supply Voltage

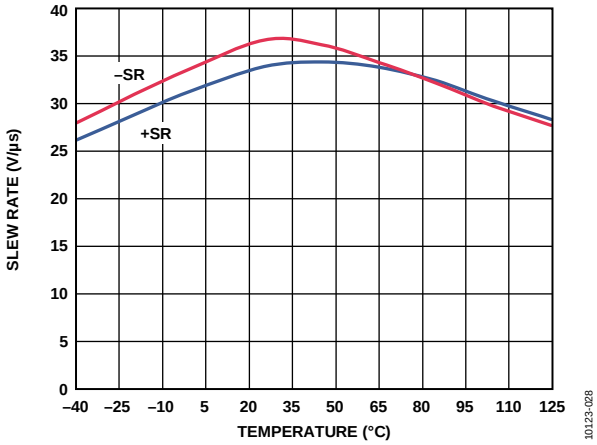

Figure 31. Slew Rate vs. Temperature, V_S = ±15 V (G = 1)

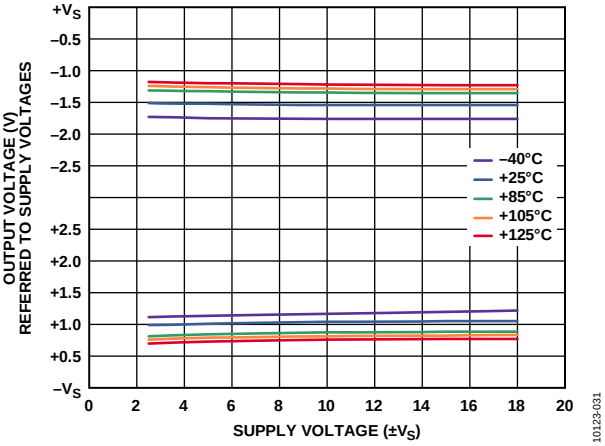

Figure 34. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

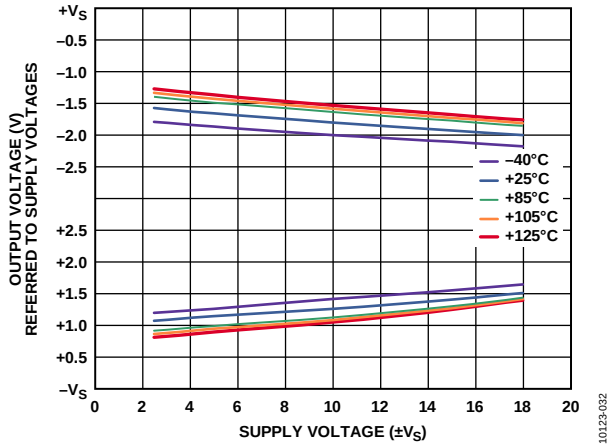

Figure 35. Output Voltage Swing vs. Supply Voltage, R_L = 600 Ω

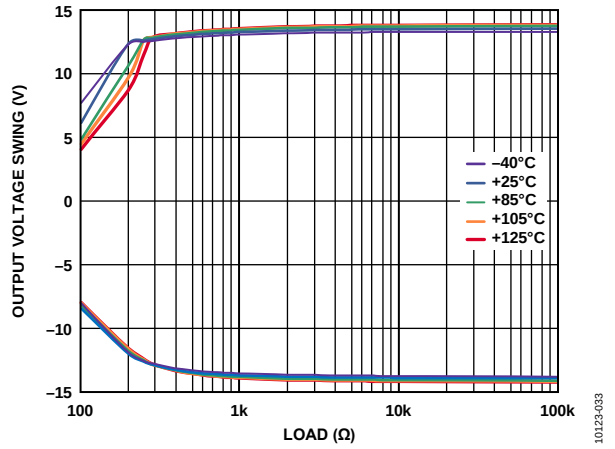

Figure 36. Output Voltage Swing vs. Load Resistance

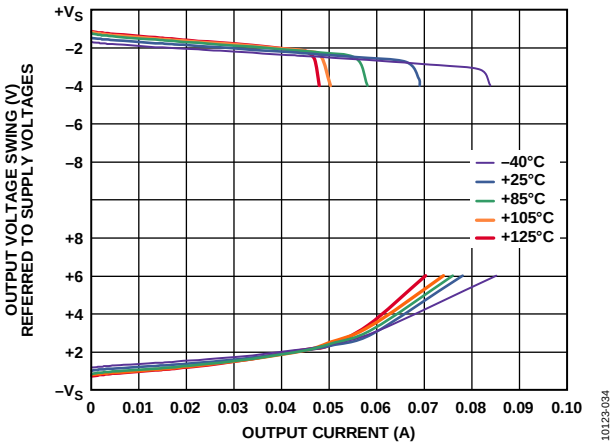

Figure 37. Output Voltage Swing vs. Output Current

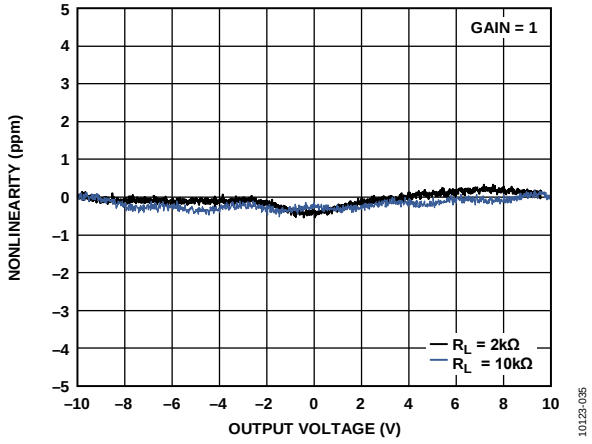

Figure 38. Gain Nonlinearity (G = 1), R_L = 10 kΩ, 2 kΩ

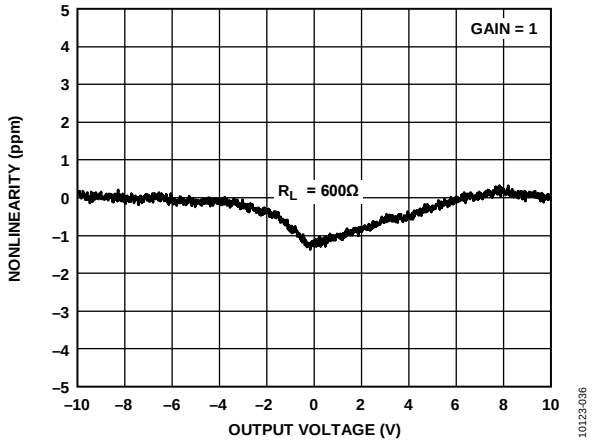

Figure 39. Gain Nonlinearity (G = 1), R_L = 600 Ω

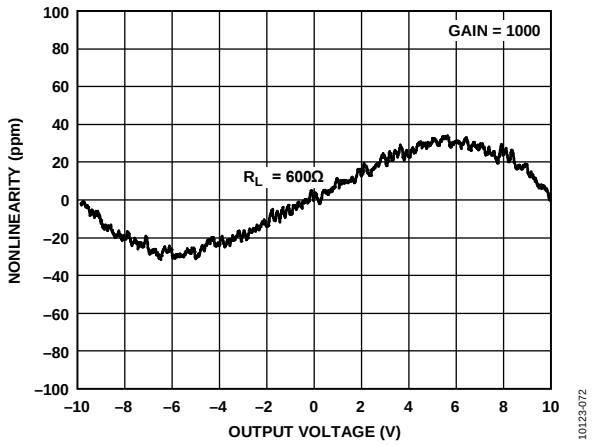

Figure 40. Gain Nonlinearity (G = 1000), R_L = 600 Ω, V_{OUT} = ±10 V

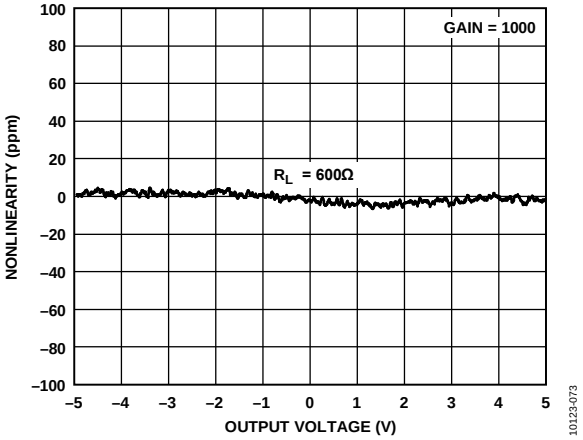

Figure 41. Gain Nonlinearity (G = 1000), R_L = 600 Ω, V_{OUT} = ±5 V

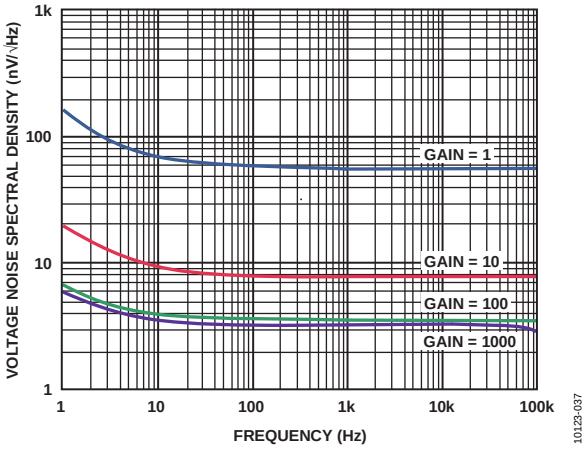

Figure 42. RTI Voltage Noise Spectral Density vs. Frequency

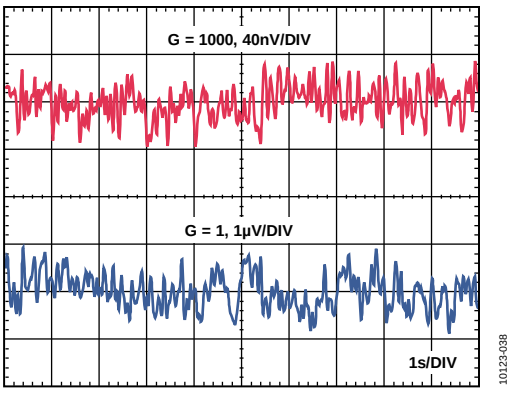

Figure 43. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1, G = 1000)

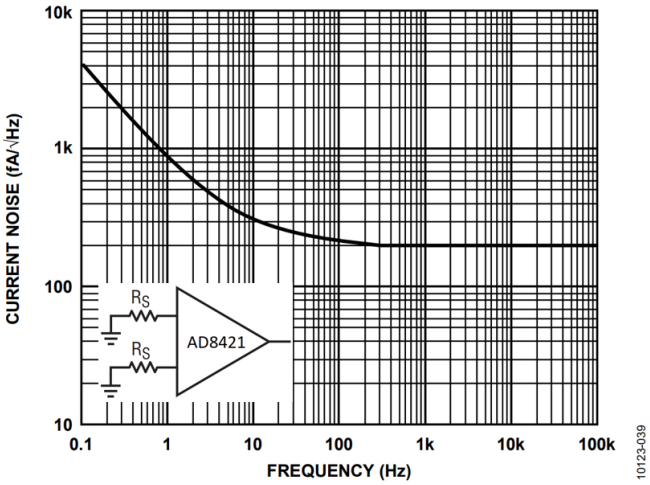

Figure 44. Current Noise Spectral Density vs. Frequency

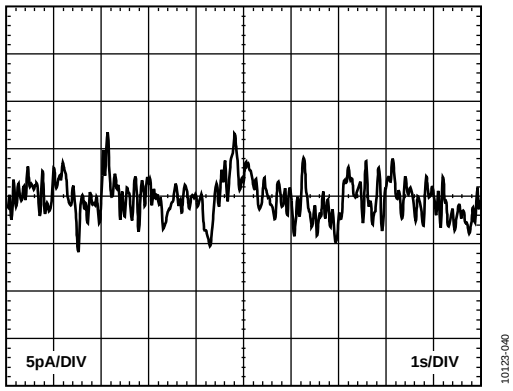

Figure 45. 0.1 Hz to 10 Hz Current Noise

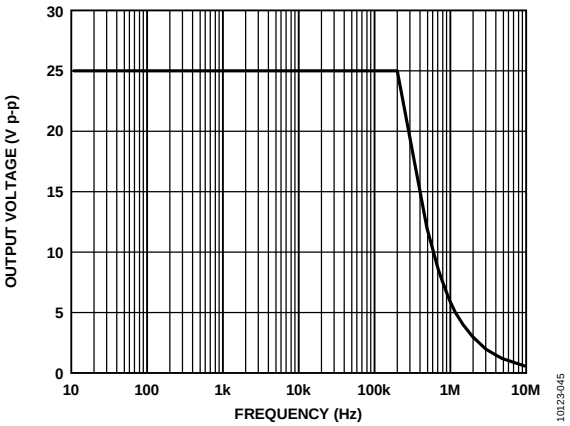

Figure 46. Large Signal Frequency Response

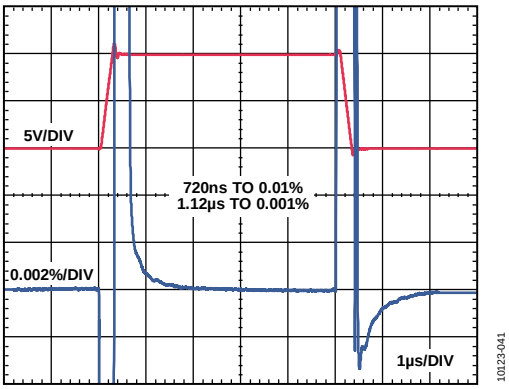

Figure 47. Large Signal Pulse Response and Settling Time (G = 1), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

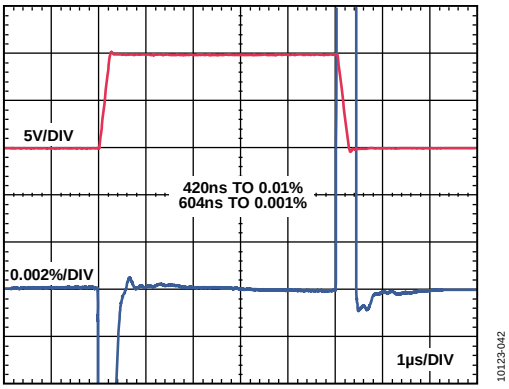

Figure 48. Large Signal Pulse Response and Settling Time (G = 10), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

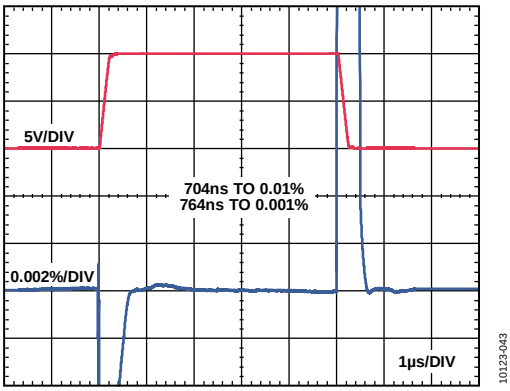

Figure 49. Large Signal Pulse Response and Settling Time (G = 100), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

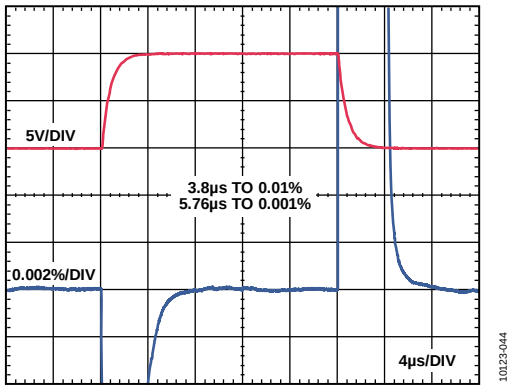

Figure 50. Large Signal Pulse Response and Settling Time (G = 1000), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

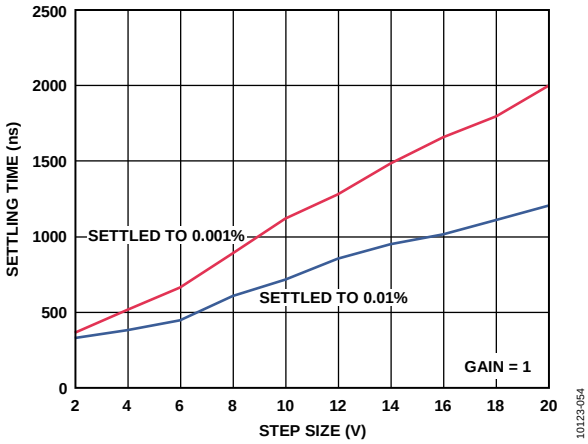

Figure 51. Settling Time vs. Step Size (G = 1), R_L = 2 kΩ, C_L = 100 pF

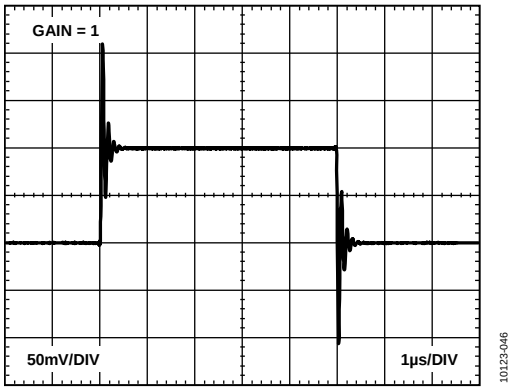

Figure 52. Small Signal Pulse Response (G = 1), R_L = 600 Ω, C_L = 100 pF

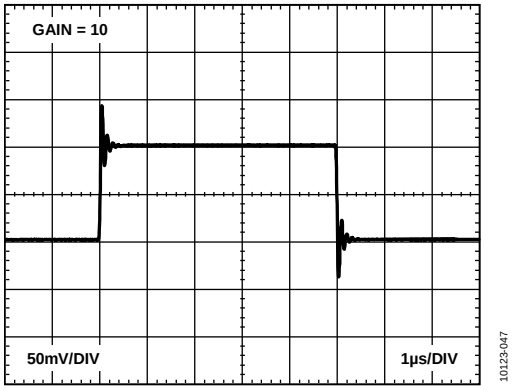

Figure 53. Small Signal Pulse Response (G = 10), R_L = 600 Ω, C_L = 100 pF

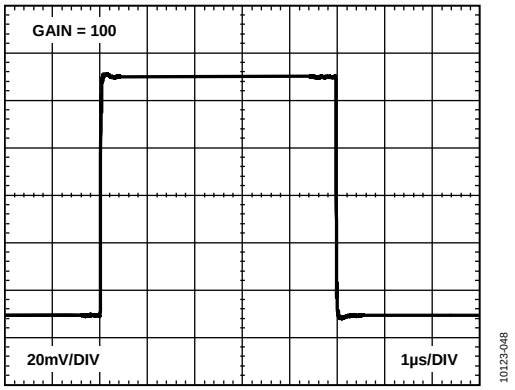

Figure 54. Small Signal Pulse Response (G = 100), RL = 600 Ω, CL = 100 pF

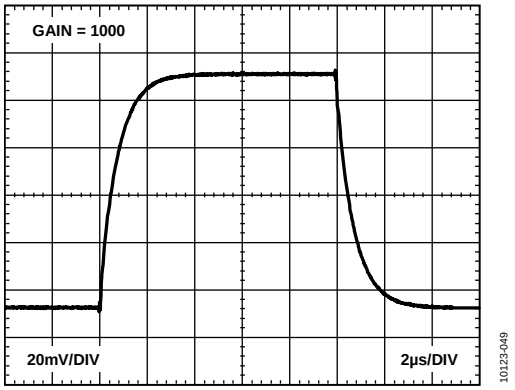

Figure 55. Small Signal Pulse Response (G = 1000), R_L = 600 Ω, C_L = 100 pF

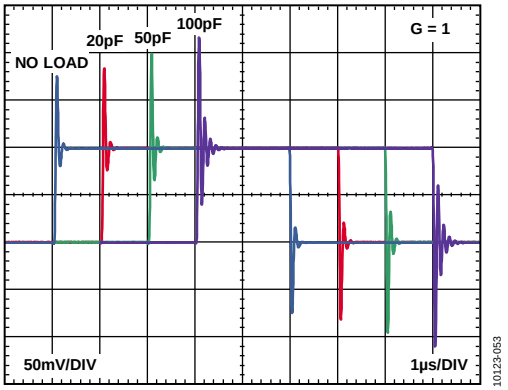

Figure 56. Small Signal Response with Various Capacitive Loads (G = 1), R_L = Infinity

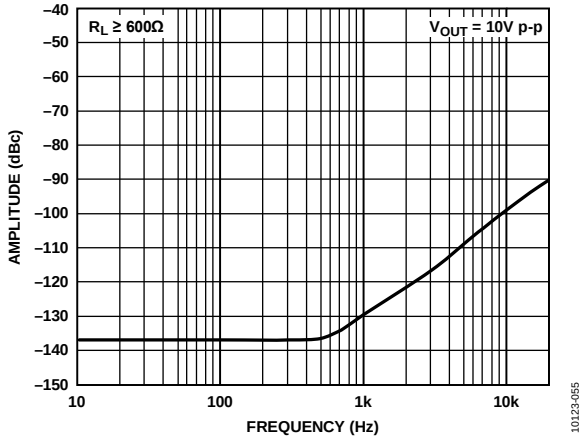

Figure 57. Second Harmonic Distortion vs. Frequency (G = 1)

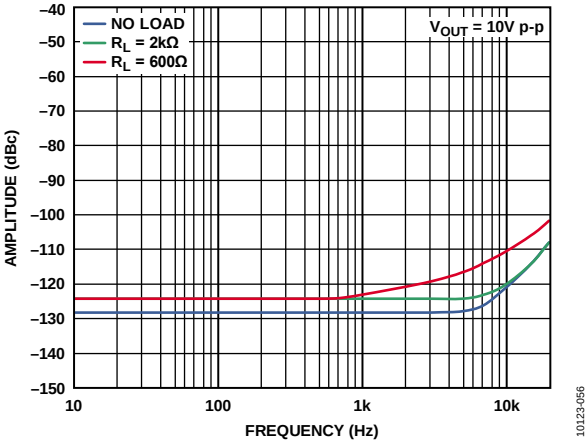

Figure 58. Third Harmonic Distortion vs. Frequency (G = 1)

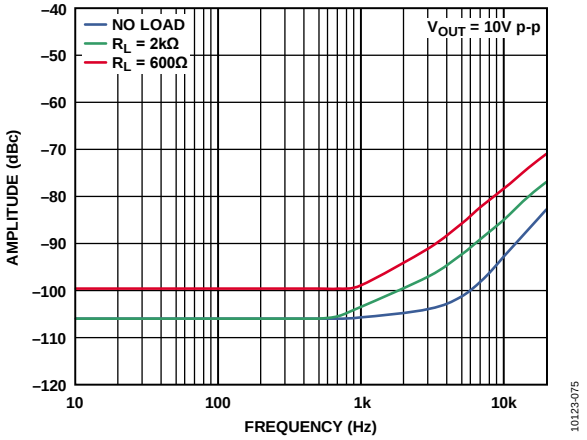

Figure 59. Second Harmonic Distortion vs. Frequency (G = 1000)

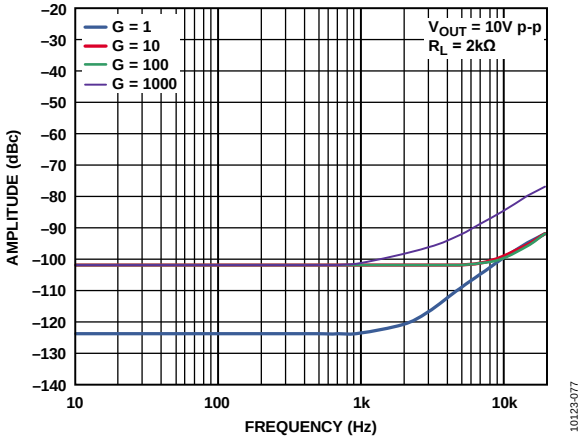

Figure 61. THD vs. Frequency

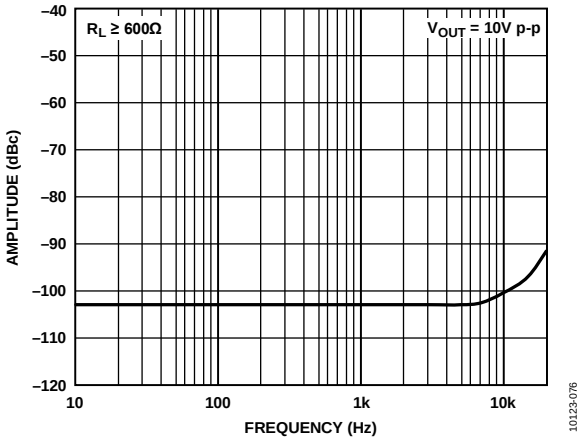

Figure 60. Third Harmonic Distortion vs. Frequency (G = 1000)

THEORY OF OPERATION

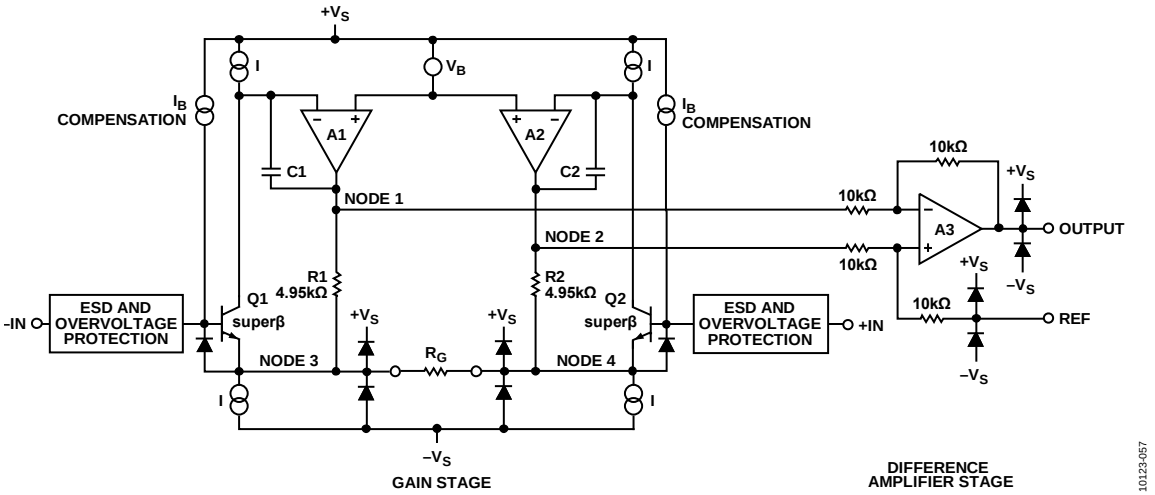

Figure 62. Simplified Schematic

ARCHITECTURE

The AD8421 is based on the classic 3-op-amp topology. This topology has two stages: a preamplifier to provide differential amplification, followed by a difference amplifier that removes the common-mode voltage. Figure 62 shows a simplified schematic of the AD8421.

Topologically, Q1, A1, R1 and Q2, A2, R2 can be viewed as precision current feedback amplifiers. Input Transistors Q1 and Q2 are biased at a fixed current so that any input signal forces the output voltages of A1 and A2 to change accordingly. The differential signal applied to the inputs is replicated across the R_G pins. Any current through R_G also flows through R1 and R2, creating a gained differential voltage between Node 1 and Node 2.

The amplified differential and common-mode signals are applied to a difference amplifier that rejects the common-mode voltage but preserves the amplified differential voltage. The difference amplifier employs innovations that result in very low output errors such as offset voltage and drift, distortion at various loads, as well as output noise. Laser-trimmed resistors allow for a highly accurate in-amp with gain error less than 0.01% and CMRR that exceeds 94 dB (G = 1). The high performance pinout and special attention given to design and layout allow for high CMRR performance across a wide frequency and temperature range.

Using superbeta input transistors and bias current compensation, the AD8421 offers extremely high input impedance, low bias current, low offset current, low current noise, and extremely low voltage noise of 3 nV/√Hz. The current-limiting and overvoltage protection scheme allow the input to go 40 V from the opposite rail at all gains without compromising the noise performance.

The transfer function of the AD8421 is

$$V_{OUT} = G \times (V_{+IN} - V_{-IN}) + V_{REF}$$

where $G = 1 + \frac{9.9\,\text{k}\Omega}{R_G}$

Users can easily and accurately set the gain using a single standard resistor.

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8421. The gain can be calculated by referring to **Error! Reference source not found.** or by using the following gain equation:

$$R_G = \frac{9.9\,\text{k}\Omega}{G - 1}$$

The AD8421 defaults to G = 1 when no gain resistor is used. To determine the total gain accuracy of the system, add the tolerance and gain drift of the R_G resistor to the specifications of the AD8421. When the gain resistor is not used, gain error and gain drift are minimal.

Table 7. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G	Calculated Gain
10 kΩ	1.99
2.49 kΩ	4.98
1.1 kΩ	10.00
523 Ω	19.93
200 Ω	50.50
100 Ω	100.0
49.9 Ω	199.4
20 Ω	496.0
10 Ω	991.0
4.99 Ω	1985

R_G Power Dissipation

The AD8421 duplicates the differential voltage across its inputs onto the R_G resistor. Choose an R_G resistor size that is sufficient to handle the expected power dissipation at ambient temperature.

REFERENCE TERMINAL

The output voltage of the AD8421 is developed with respect to the potential on the reference terminal. This can be used to sense the ground at the load, thereby taking advantage of the CMRR to reject ground noise or to introduce a precise offset to the signal at the output. For example, a voltage source can be tied to the REF pin to level shift the output, allowing the AD8421 to drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, maintain a source impedance to the REF terminal that is below 1 Ω. As shown in Figure 62, the reference terminal, REF, is at one end of a 10 kΩ resistor. Additional impedance at the REF terminal adds to this 10 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be calculated as follows:

$$2(10\ k\Omega + R_{REF})/(20\ k\Omega + R_{REF})$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

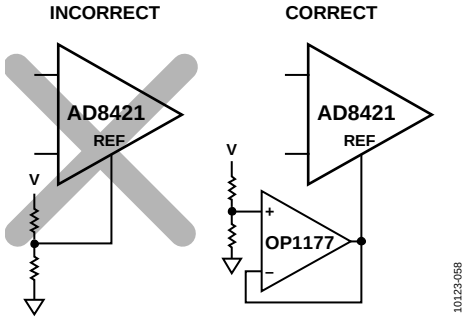

Figure 63. Driving the Reference Pin

INPUT VOLTAGE RANGE

The 3-op-amp architecture of the AD8421 applies gain in the first stage before removing the common-mode voltage in the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 62) experience a combination of a gained signal, a common-mode signal, and a diode drop. The voltage supplies can limit the combined signal, even when the individual input and output signals are not limited. Figure 11 through Figure 14 show this limitation in detail.

LAYOUT

To ensure optimum performance of the AD8421 at the PCB level, care must be taken in the design of the board layout. The pins of the AD8421 are arranged in a logical manner to aid in this task.

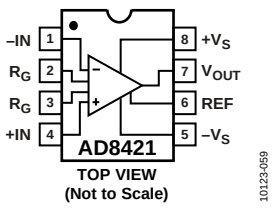

Figure 64. Pin Configuration Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To maintain high CMRR over frequency, closely match the input source impedance and capacitance of each path. Place additional source resistance in the input path (for example, input protection resistors) close to the in-amp inputs, to minimize the interaction of the resistance with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins (R_G) can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), choose a component such that the parasitic capacitance is as small as possible.

Power Supplies and Grounding

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

Place a 0.1 µF capacitor as close as possible to each supply pin. Because the length of the bypass capacitor leads is critical at high frequency, surface-mount capacitors are recommended. Any parasitic inductance in the bypass ground trace works against the low impedance that is created by the bypass capacitor. As shown in Figure 65, a 10 µF capacitor can be used farther away from the device. For these larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical. In most cases, the 10 µF capacitor can be shared by other local precision integrated circuits.

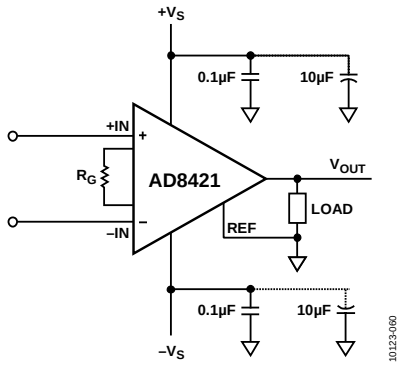

Figure 65. Supply Decoupling, REF, and Output Referred to Local Ground

A ground plane layer helps to reduce parasitic inductances, which minimizes voltage drops with changes in current. The area of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the impedance of the path at high frequency. Large changes in currents in an inductive decoupling path or ground return create unwanted effects due to the coupling of such changes into the amplifier inputs.

Because load currents flow from the supplies, the load should be connected at the same physical location as the bypass capacitor grounds.

Reference Pin

The output voltage of the AD8421 is developed with respect to the potential on the reference terminal. Ensure that REF is tied to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8421 must have a return path to ground. When using a floating source without a current return path (such as a thermocouple), create a current return path as shown in Figure 66.

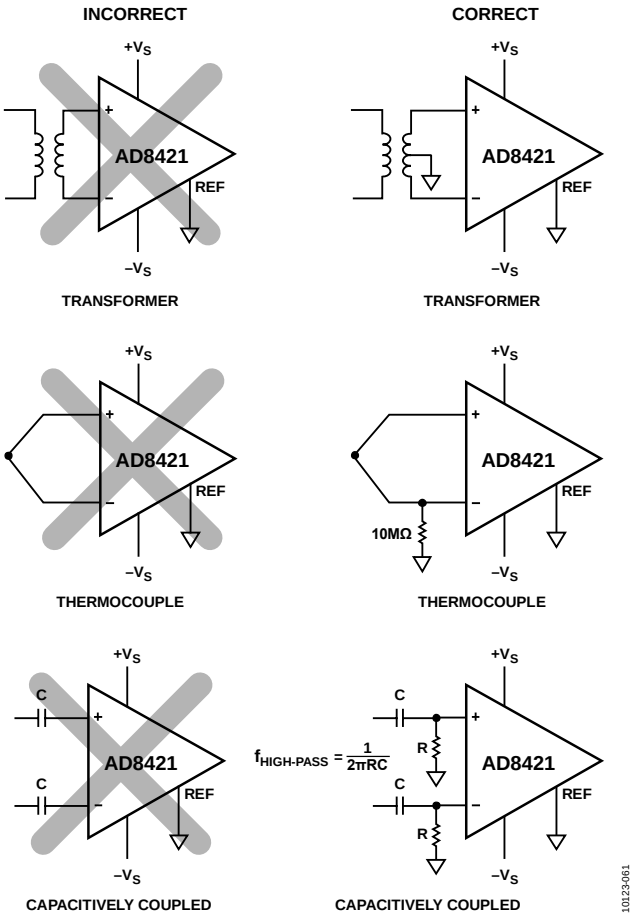

Figure 66. Creating an Input Bias Current Return Path

INPUT VOLTAGES BEYOND THE SUPPLY RAILS

The AD8421 has very robust inputs. It typically does not need additional input protection, as shown in Figure 67.

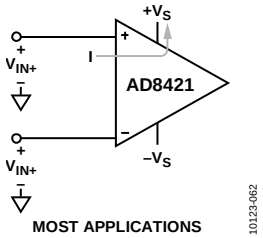

Figure 67. Typical Application; No Input Protection Required

The AD8421 inputs are current limited; therefore, input voltages can be up to 40 V from the opposite supply rail, with no input protection required at all gains. For example, if $+V_S$ = +5 V and $-V_S$ = −8 V, the part can safely withstand voltages from −35 V to +32 V.

The remaining AD8421 terminals should be kept within the supplies. All terminals of the AD8421 are protected against ESD.

Input Voltages Beyond the Maximum Ratings

For applications where the AD8421 encounters voltages beyond the limits in the Absolute Maximum Ratings table, external protection is required. This external protection depends on the duration of the overvoltage event and the noise performance that is required.

For short-lived events, transient protectors (such as metal oxide varistors (MOVs)), may be all that is required.

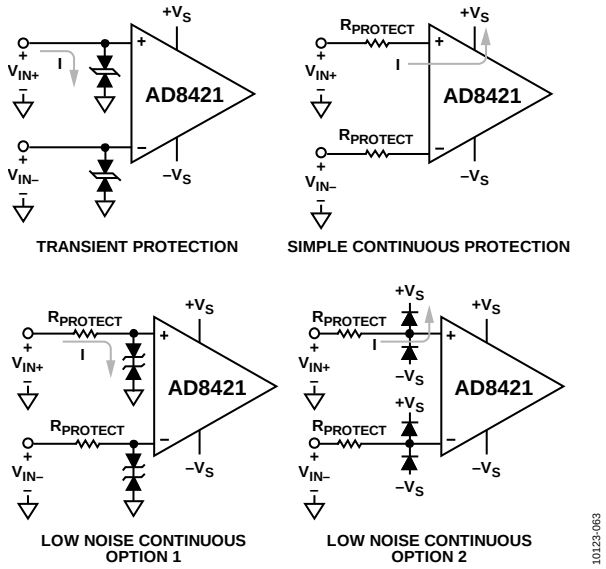

Figure 68. Input Protection Options for Input Voltages Beyond Absolute Maximum Ratings

For longer events, use resistors in series with the inputs, combined with diodes. To avoid degrading bias current performance, low leakage diodes such as the BAV199 or FJH1100 are recommended. The diodes prevent the voltage at the input of the amplifier from exceeding the maximum ratings, and the resistors limit the current into the diodes. Because most external diodes can easily handle 100 mA or more, resistor values do not need to be large and, therefore, have a minimal impact on noise performance.

At the expense of some noise performance, another solution is to use series resistors. In the case of overvoltage, current into the AD8421 inputs is internally limited. Although the AD8421 inputs must be kept within the limits defined in the Absolute Maximum Ratings section, the I × R drop across the protection resistor increases the maximum voltage that the system can withstand, as follows:

For positive input signals

$$V_{MAX\_NEW} = (40\text{ V} + Negative\ Supply) + I_{IN} \times R_{PROTECT}$$

For negative input signals

$$V_{MIN\_NEW} = (Positive\ Supply - 40\ V) - I_{OUT} \times R_{PROTECT}$$

Overvoltage performance is shown in Figure 15, Figure 16, Figure 17, and Figure 18. The AD8421 inputs can withstand a current of 40 mA at room temperature for at least a day. This time is cumulative over the life of the device. If long periods of overvoltage are expected, the use of an external protection method is recommended. Under extreme input conditions, the output of the amplifier may invert.

RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications that have strong RF signals. The problem is intensified if long leads or PCB traces are required to connect the amplifier to the signal source. The disturbance can appear as a dc offset voltage or a train of pulses.

High frequency signals can be filtered with a low-pass filter network at the input of the instrumentation amplifier, as shown in Figure 69.

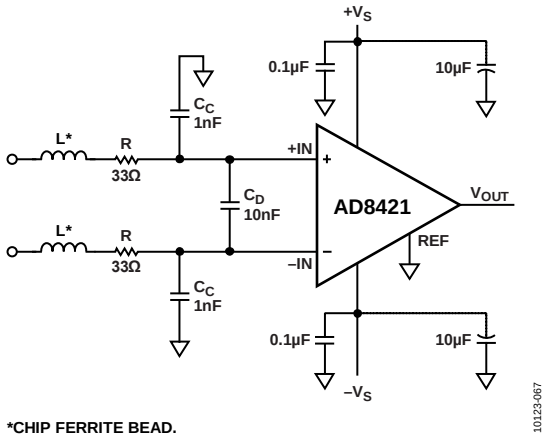

Figure 69. RFI Suppression

The choice of resistor and capacitor values depends on the desired trade-off between noise, input impedance at high frequencies, CMRR, signal bandwidth, and RFI immunity. An RC network limits both the differential and common-mode bandwidth, as shown in the following equations:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

C_D affects the differential signal, and C_C affects the common-mode signal. A mismatch between R × C_C at the positive input and R × C_C at the negative input degrades the CMRR of the AD8421. By using a value of C_D that is one order of magnitude larger than C_C, the effect of the mismatch is reduced and CMRR performance is improved near the cutoff frequencies.

To achieve low noise and sufficient RFI filtering, the use of chip ferrite beads is recommended. Ferrite beads increase their impedance with frequency, thus leaving the signal of interest unaffected while preventing RF interference to reach the amplifier. They also help to eliminate the need for large resistor values in the filter, thus minimizing the system's input-referred noise. The selection of the appropriate ferrite bead and capacitor values is a function of the interference frequency, input lead length, and RF power.

For best results, place the RFI filter network as close as possible to the amplifier. Layout is critical to ensure that RF signals are not picked up on the traces after the filter. If RF interference is too strong to be filtered sufficiently, shielding is recommended.

The resistors used for the RFI filter can be the same as those used for input protection.

CALCULATING THE NOISE OF THE INPUT STAGE

The total noise of the amplifier front end depends on much more than the 3.2 nV/√Hz specification of this data sheet. The three main contributors to noise are: the source resistance, the voltage noise of the instrumentation amplifier, and the current noise of the instrumentation amplifier.

In the following calculations, noise is referred to the input (RTI). In other words, all sources of noise are calculated as if the source appeared at the amplifier input. To calculate the noise referred to the amplifier output (RTO), multiply the RTI noise by the gain of the instru-mentation amplifier.

Source Resistance Noise

Any sensor connected to the AD8421 has some output resistance. There may also be resistance placed in series with inputs for protection from either overvoltage or radio frequency interference. This combined resistance is labeled R1 and R2 in Figure 70. Any resistor, no matter how well made, has an intrinsic level of noise. This noise is proportional to the square root of the resistor value. At room temperature, the value is approximately equal to 4 nV/√Hz × √(resistor value in kΩ).

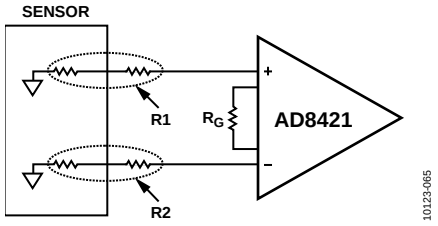

Figure 70. Source Resistance from Sensor and Protection Resistors

For example, assume that the combined sensor and protection resistance is 4 kΩ on the positive input and 1 kΩ on the negative input. Then the total noise from the input resistance is

$$\sqrt{\left(4 \times \sqrt{4}\right)^2 + \left(4 \times \sqrt{1}\right)^2} = \sqrt{64 + 16} = 8.9\ nV/\sqrt{Hz}$$

Voltage Noise of the Instrumentation Amplifier

The voltage noise of the instrumentation amplifier is calculated using three parameters: the device output noise, the input noise, and the R_G resistor noise. It is calculated as follows:

$$Total\ Voltage\ Noise = \sqrt{(Output\ Noise/G)^2 + (Input\ Noise)^2 + (Noise\ of\ R_G\ Resistor)^2}$$

For example, for a gain of 100, the gain resistor is 100 Ω. Therefore, the voltage noise of the in-amp is

$$\sqrt{(60/100)^2 + 3.2^2 + (4 \times \sqrt{0.1})^2} = 3.5\ \text{nV}/\sqrt{\text{Hz}}$$

Current Noise of the Instrumentation Amplifier

Current noise is converted to a voltage by the source resistance. The effect of current noise can be calculated by multiplying the specified current noise of the in-amp by the value of the source resistance.

For example, if the R1 source resistance in Figure 70 is 4 kΩ, and the R2 source resistance is 1 kΩ, the total effect from the current noise is calculated as follows:

$$\sqrt{(4 \times 0.2)^2 + (1 \times 0.2)^2} = 0.8\ \text{nV}/\sqrt{\text{Hz}}$$

Total Noise Density Calculation

To determine the total noise of the in-amp, referred to input, combine the source resistance noise, voltage noise, and current noise contribution by the sum of squares method.

For example, if the R1 source resistance in Figure 70 is 4 kΩ, the R2 source resistance is 1 kΩ, and the gain of the in-amp is 100, the total noise, referred to input, is

$$\sqrt{8.9^2 + 3.5^2 + 0.8^2} = 9.6\ \text{nV}/\sqrt{\text{Hz}}$$

APPLICATIONS INFORMATION

DIFFERENTIAL OUTPUT CONFIGURATION

Figure 71 shows an example of how to configure the AD8421 for differential output.

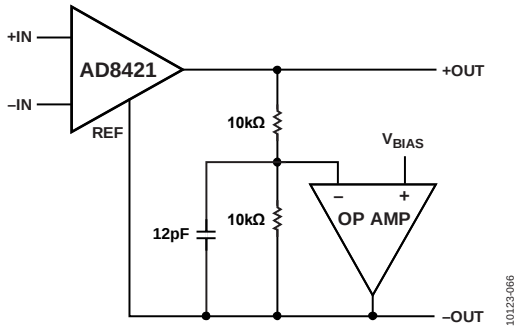

Figure 71. Differential Output Configuration with Op Amp

The differential output voltage is set by the following equation:

$$V_{DIFF\_OUT} = V_{+OUT} - V_{-OUT} = Gain \times (V_{+IN} - V_{-IN})$$

The common-mode output is set by the following equation:

$$V_{CM\_OUT} = (V_{+OUT} + V_{-OUT})/2 = V_{BIAS}$$

The advantage of this circuit is that the dc differential accuracy depends on the AD8421, not on the op amp or the resistors. In addition, this circuit takes advantage of the precise control that the AD8421 has of its output voltage relative to the reference voltage.

Although the dc performance and resistor matching of the op amp affect the dc common-mode output accuracy, such errors are likely to be rejected by the next device in the signal chain and, therefore, typically have little effect on overall system accuracy.

Because this circuit is susceptible to instability, a capacitor is included to limit the effective op amp bandwidth. This capacitor can be omitted if the amplifier pairing is stable.

The open-loop gain and phase of any amplifier may vary with process variation and temperature. Additional phase lag can be introduced by resistive or capacitive loading. To guarantee stability, the value of the capacitor in Figure 71 should be determined with a sample of circuits by evaluating the small signal pulse response of the circuit with load at the extremes of the output dynamic range.

The ambient temperature should also be varied over the expected range to evaluate its effect on stability. The voltage at +OUT may still have some overshoot after the circuit is tuned because the AD8421 output amplifier responds faster than the op amp. A 12 pF capacitor is a good starting point.

For best large signal ac performance, use an op amp with a high slew rate to match the AD8421 performance of 35 V/µs. High bandwidth is not essential because the system bandwidth is limited by the RC feedback. Some good choices for op amps are the AD8610, ADA4627-1, AD8510, and the ADA4898-1.

DRIVING AN ADC

The Class AB output stage, low noise and distortion, and high bandwidth and slew rate make the AD8421 a good choice for driving an ADC in a data acquisition system that requires front-end gain, high CMRR, and dc precision. Figure 72 shows the AD8421, in a gain-of-10 configuration, driving the AD7685, a 16-bit, 250 kSPS pseudodifferential SAR ADC. The RC low-pass filter that is shown between the AD8421 and the AD7685 has several purposes. It isolates the amplifier output from excessive loading from the dynamic ADC inputs, reduces the noise bandwidth of the amplifier, and provides overload protection for the AD7685 analog inputs. The filter cutoff can be determined empirically. To achieve the best ac performance, keep the impedance magnitude greater than 1 kΩ at the maximum input signal frequency, and set the filter cutoff to settle to ½ LSB in one sampling period for a full-scale step. For additional considerations, refer to the data sheet of the ADC in use.

In a gain-of-10 configuration, the AD8421 has approximately 8 nV/√Hz voltage noise RTI (See the Calculating the Noise of the Input Stage section.) The front-end gain makes the system ten times more sensitive to input signals, with only a 7.5 dB reduction of SNR. The high current output and load regulation of the ADR435 allow the AD7685 to be powered directly from the reference without the need to provide another analog supply rail. The reference pin buffer may be any low power, unity-gain stable, dc precision op amp with less than approximately 25 nV/√Hz of wideband noise, such as the OP1177. Not all proper decoupling is shown in Figure 72. Take care to follow decoupling guidelines for both amplifiers and the ADR435.

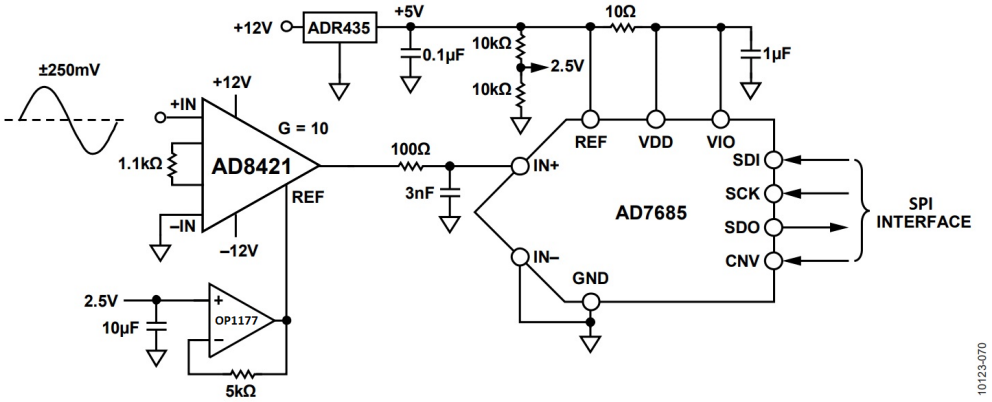

Figure 72. AD8421 Driving 16-Bit AD7685

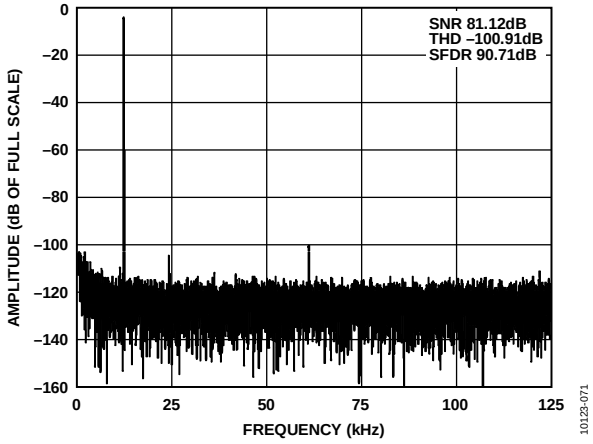

Figure 73. Typical Spectrum of the AD8421 (G = 10) Driving the AD7685

OUTLINE DIMENSIONS

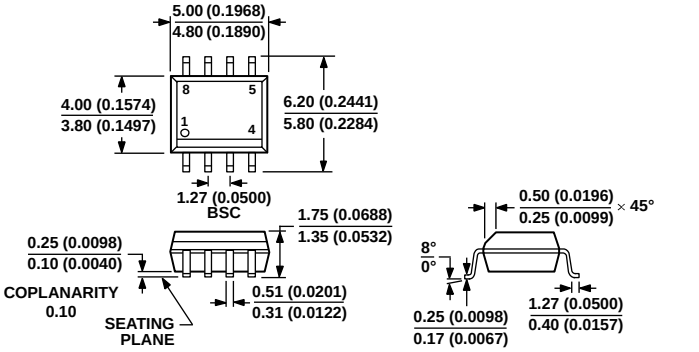

Figure 74. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

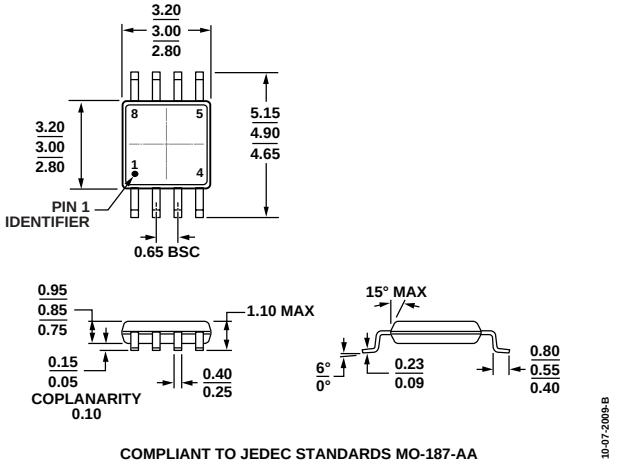

Figure 75. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

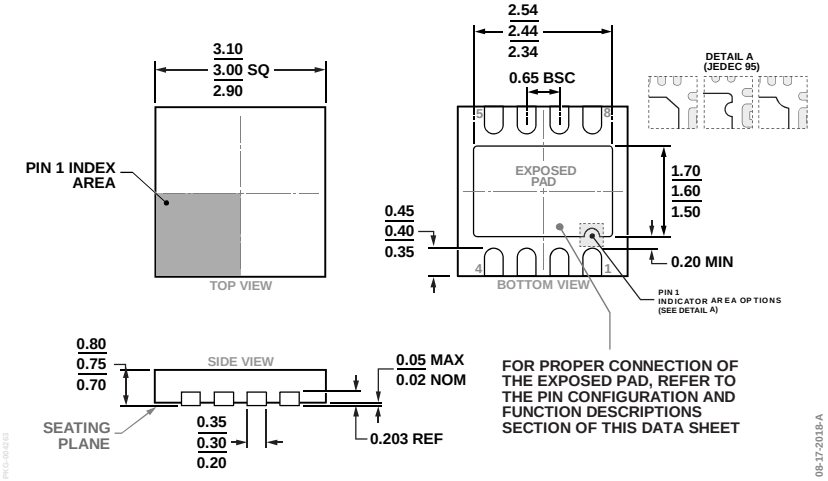

Figure 76. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8421ARZ	−40°C to +85°C	8-Lead SOIC_N, standard grade	R-8	
AD8421ARZ-R7	−40°C to +85°C	8-Lead SOIC_N, standard grade, 7″ Tape and Reel,	R-8	
AD8421ARZ-RL	−40°C to +85°C	8-Lead SOIC_N, standard grade, 13″ Tape and Reel	R-8	
AD8421BRZ	−40°C to +85°C	8-Lead SOIC_N, high performance grade	R-8	
AD8421BRZ-R7	−40°C to +85°C	8-Lead SOIC_N, high performance grade, 7″ Tape and Reel	R-8	
AD8421BRZ-RL	−40°C to +85°C	8-Lead SOIC_N, high performance grade, 13″ Tape and Reel	R-8	
AD8421ARMZ	−40°C to +85°C	8-Lead MSOP, standard grade	RM-8	Y49
AD8421ARMZ-R7	−40°C to +85°C	8-Lead MSOP, standard grade, 7″ Tape and Reel	RM-8	Y49
AD8421ARMZ-RL	−40°C to +85°C	8-Lead MSOP, standard grade, 13″ Tape and Reel	RM-8	Y49
AD8421BRMZ	−40°C to +85°C	8-Lead MSOP, high performance grade	RM-8	Y4A
AD8421BRMZ-R7	−40°C to +85°C	8-Lead MSOP, high performance grade, 7″ Tape and Reel	RM-8	Y4A
AD8421BRMZ-RL	−40°C to +85°C	8-Lead MSOP, high performance grade, 13″ Tape and Reel	RM-8	Y4A
AD8421ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP], Standard Grade, 13″ Tape and Reel	CP-8-19	A4H
AD8421ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP], Standard Grade, 7″ Tape and Reel	CP-8-19	A4H

[1] Z = RoHS Compliant Part.