ANALOG DEVICES

Low Noise, Low Gain Drift, G = 2000 Instrumentation Amplifier

Data Sheet **AD8428**

FEATURES

Fixed gain of 2000
Access to internal nodes provides flexibility
Low noise: 1.5 nV/√Hz input voltage noise
High accuracy dc performance
- **Gain drift: 5 ppm/°C**
- **Offset drift: 0.3 µV/°C**
- **Gain accuracy: 0.05%**
- **CMRR: 140 dB min**

Excellent ac specifications
- **Bandwidth: 3.5 MHz**
- **Slew rate: 40 V/µs**

Power supply range: ±4 V to ±18 V
8-lead SOIC package
ESD protection: 5000 V (HBM)
Temperature range for specified performance: −40°C to +85°C
Operational up to 125°C

APPLICATIONS

Sensor interface
Medical instrumentation
Patient monitoring

FUNCTIONAL BLOCK DIAGRAM

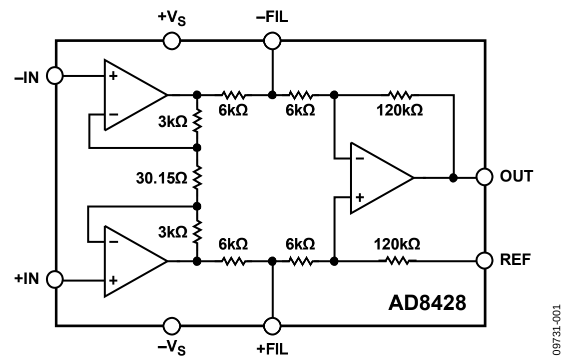

Figure 1.

Table 1. Instrumentation Amplifiers by Category[1]

General-Purpose	Zero Drift	Military Grade	Low Power	Low Noise
AD8220	AD8231	AD620	AD627	AD8428
AD8221	AD8290	AD621	AD623	AD8429
AD8222	AD8293	AD524	AD8235	
AD8224	AD8553	AD526	AD8236	
AD8228	AD8556	AD624	AD8426	
AD8295	AD8557		AD8226	
			AD8227	
			AD8420	

[1] See www.analog.com for the latest instrumentation amplifiers.

GENERAL DESCRIPTION

The AD8428 is an ultralow noise instrumentation amplifier designed to accurately measure tiny, high speed signals. It delivers industry-leading gain accuracy, noise, and bandwidth.

All gain setting resistors for the AD8428 are internal to the part and are precisely matched. Care is taken in both the chip pinout and layout. This results in excellent gain drift and quick settling to the final gain value after the part is powered on.

The high CMRR of the AD8428 prevents unwanted signals from corrupting the signal of interest. The pinout of the AD8428 is designed to avoid parasitic capacitance mismatches that can degrade CMRR at high frequencies.

The AD8428 is one of the fastest instrumentation amplifiers available. The circuit architecture is designed for high bandwidth at high gain. The AD8428 uses a current feedback topology for the initial preamplifier gain stage of 200, followed by a difference amplifier stage of 10. This architecture results in a 3.5 MHz bandwidth at a gain of 2000 for an equivalent gain bandwidth product of 7 GHz.

The AD8428 pinout allows access to internal nodes between the first and second stages. This feature can be useful for modifying the frequency response between the two amplification stages, thereby preventing unwanted signals from contaminating the output results.

The performance of the AD8428 is specified over the industrial temperature range of −40°C to +85°C. It is available in an 8-lead plastic SOIC package.

Rev. A

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10/11—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 2000, R_L = 10 kΩ, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	RTI, V_{CM} = ±10 V							
DC to 60 Hz		130			140			dB
At 50 kHz		110			120			dB
NOISE (RTI)	V_{IN}+, V_{IN}− = 0 V							
Voltage Noise	f = 1 kHz		1.3	1.5		1.3	1.5	nV/√Hz
	f = 0.1 Hz to 10 Hz		40	50		40	50	nV p-p
Current Noise	f = 1 kHz		1.5			1.5		pA/√Hz
	f = 0.1 Hz to 10 Hz		150			150		pA p-p
VOLTAGE OFFSET								
Input Offset, V_{OSI}				100			25	µV
Average TC	T_A = −40°C to +85°C			1			0.3	µV/°C
Offset RTI vs. Supply (PSRR)		120			130			dB
INPUT CURRENT								
Input Bias Current				200			50	nA
Over Temperature	T_A = −40°C to +85°C		250			250		pA/°C
Input Offset Current				50			10	nA
Over Temperature	T_A = −40°C to +85°C		20			20		pA/°C
DYNAMIC RESPONSE								
−3 dB Small Signal Bandwidth			3.5			3.5		MHz
Settling Time to 0.01%	10 V step		0.75			0.75		µs
Settling Time to 0.001%	10 V step		1.4			1.4		µs
Slew Rate		40	50		40	50		V/µs
GAIN								
First Stage Gain			200			200		V/V
Subtractor Stage Gain			10			10		V/V
Total Gain Error	V_{OUT} = −10 V to +10 V			0.2			0.05	%
Total Gain Nonlinearity	V_{OUT} = −10 V to +10 V			5			5	ppm
Gain Drift				10			5	ppm/°C
INPUT								
Impedance (Pin to Ground)[1]			1||2			1||2		GΩ||pF
Input Operating Voltage Range	V_S = ±4 V to ±18 V	$-V_S$ + 2.5		$+V_S$ − 2.5	$-V_S$ + 2.5		$+V_S$ − 2.5	V
Over Temperature	T_A = −40°C to +85°C	$-V_S$ + 2.5		$+V_S$ − 2.5	$-V_S$ + 2.5		$+V_S$ − 2.5	V
OUTPUT								
Output Voltage Swing	R_L = 2 kΩ	$-V_S$ + 1.7		$+V_S$ − 1.2	$-V_S$ + 1.7		$+V_S$ − 1.2	V
Over Temperature	T_A = −40°C	$-V_S$ + 2.0		$+V_S$ − 1.3	$-V_S$ + 2.0		$+V_S$ − 1.3	V
	T_A = +85°C	$-V_S$ + 1.6		$+V_S$ − 1.1	$-V_S$ + 1.6		$+V_S$ − 1.1	V
Output Voltage Swing	R_L = 10 kΩ	$-V_S$ + 1.7		$+V_S$ − 1.0	$-V_S$ + 1.7		$+V_S$ − 1.0	V
Over Temperature	T_A = −40°C	$-V_S$ + 1.8		$+V_S$ − 1.2	$-V_S$ + 1.8		$+V_S$ − 1.2	V
	T_A = +85°C	$-V_S$ + 1.4		$+V_S$ − 0.9	$-V_S$ + 1.4		$+V_S$ − 0.9	V
Short-Circuit Current			30			30		mA
REFERENCE INPUT								
Input Impedance, R_{IN}			132			132		kΩ
Input Current, I_{IN}	V_{IN}+, V_{IN}− = 0 V		6.5			6.5		µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
FILTER TERMINALS								
Input Impedance, R_{IN}[2]			6			6		kΩ
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
POWER SUPPLY								
Operating Range		±4		±18	±4		±18	V
Quiescent Current			6.5	6.8		6.5	6.8	mA
Over Temperature	T_A = −40°C to +85°C			8			8	mA

[1] The differential and common-mode input impedances can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[2] To calculate the actual impedance, see Figure 1.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN, +IN[1]	$\pm V_S$
Maximum Voltage at −FIL, +FIL	$\pm V_S$
Differential Input Voltage[1]	±1 V
Maximum Voltage at REF	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +85°C
Maximum Junction Temperature	140°C
ESD	
Human Body Model	5000 V
Charged Device Model	1250 V
Machine Model	400 V

[1] For voltages beyond these limits, use input protection resistors. See the Input Protection section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package	θ_{JA}	Unit
8-Lead SOIC_N	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

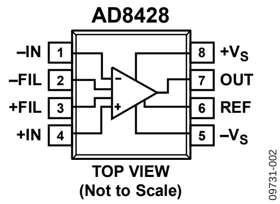

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal.
2	−FIL	Negative Filter Terminal.
3	+FIL	Positive Filter Terminal.
4	+IN	Positive Input Terminal.
5	$-V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level-shift the output.
7	OUT	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 15$ V, $V_{REF} = 0$ V, $T_A = 25°C$, G = 2000, $R_L = 10$ kΩ, unless otherwise noted.

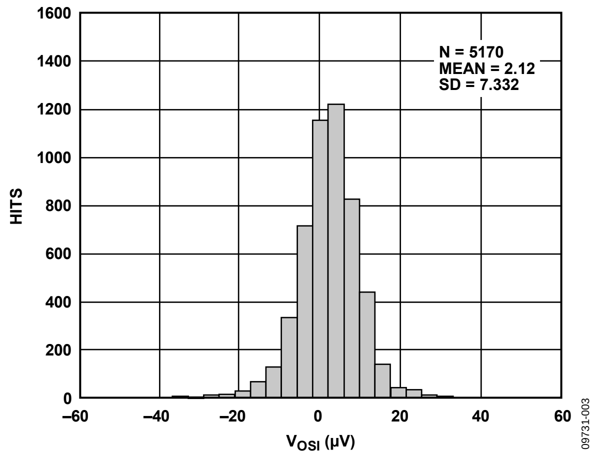

Figure 3. Typical Distribution of Input Offset Voltage, $V_S = \pm 5$ V

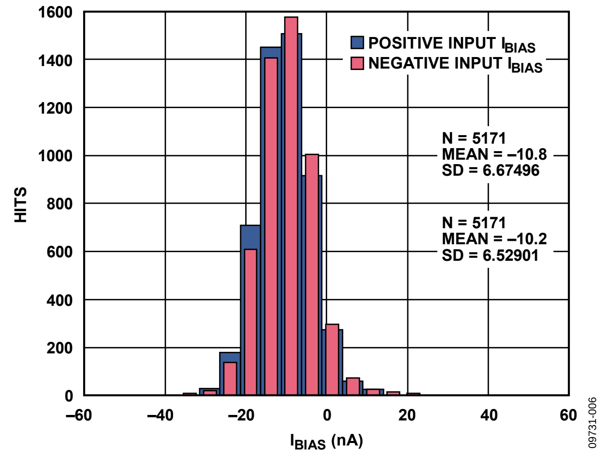

Figure 6. Typical Distribution of Input Bias Current

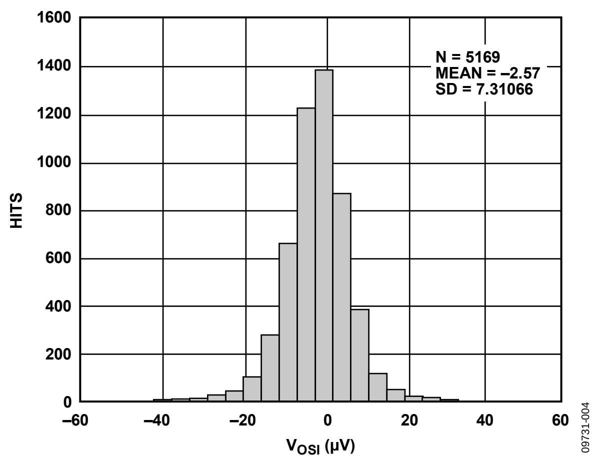

Figure 4. Typical Distribution of Input Offset Voltage, $V_S = \pm 15$ V

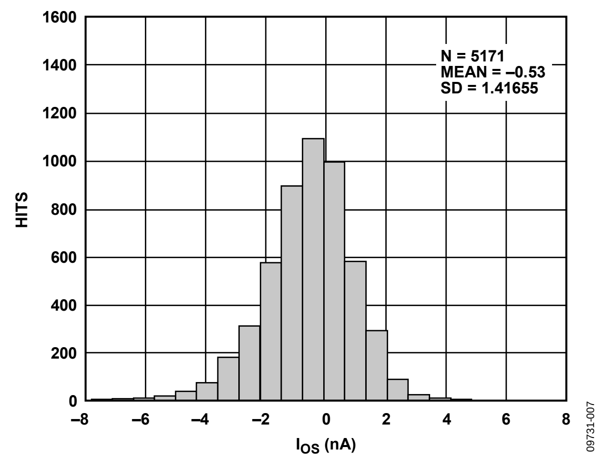

Figure 7. Typical Distribution of Input Offset Current

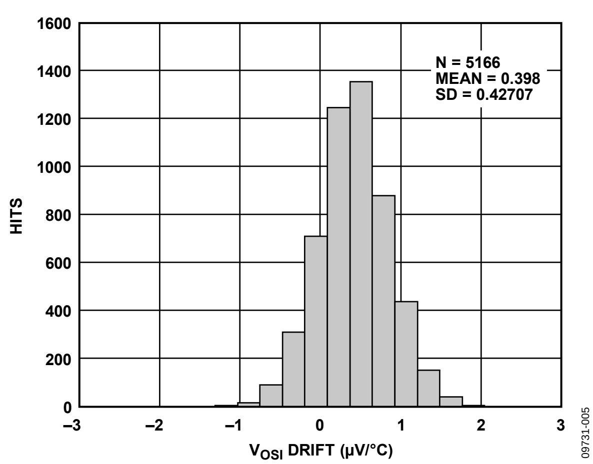

Figure 5. Typical Distribution of Input Offset Voltage Drift

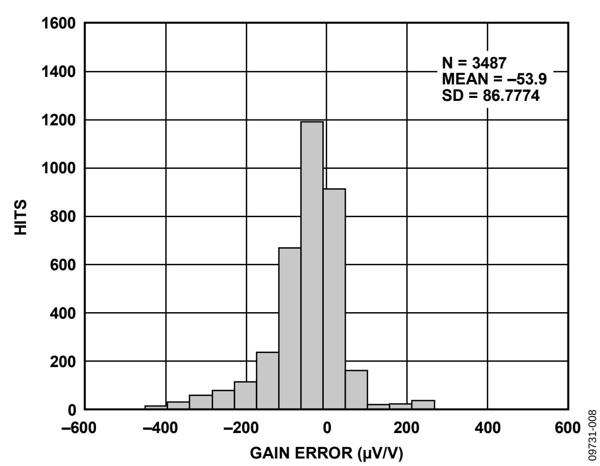

Figure 8. Typical Distribution of Gain Error, Gain = 2000, $V_S = \pm 15$ V, $R_L = 10$ kΩ

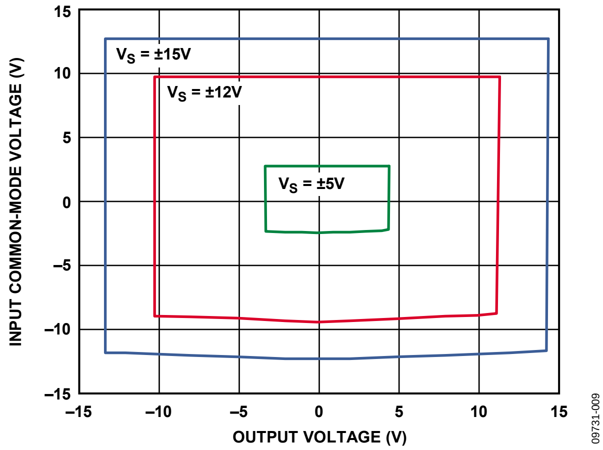

Figure 9. Input Common-Mode Voltage vs. Output Voltage, $V_S = \pm 5$ V, $V_S = \pm 12$ V, $V_S = \pm 15$ V

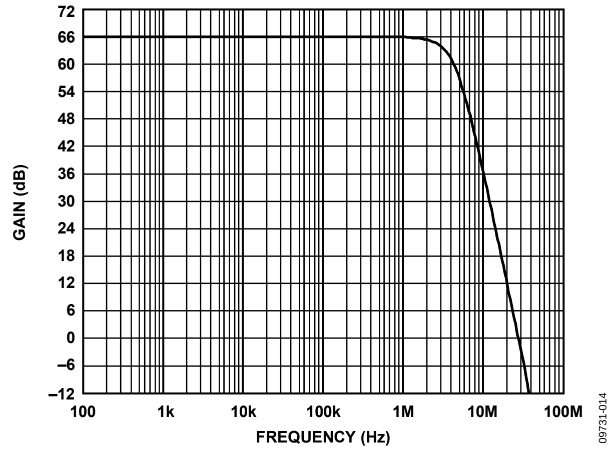

Figure 12. Gain vs. Frequency

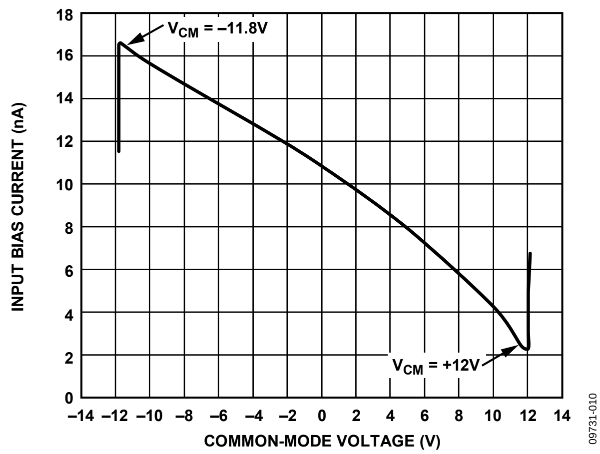

Figure 10. Input Bias Current vs. Common-Mode Voltage, $V_S = \pm 15$ V

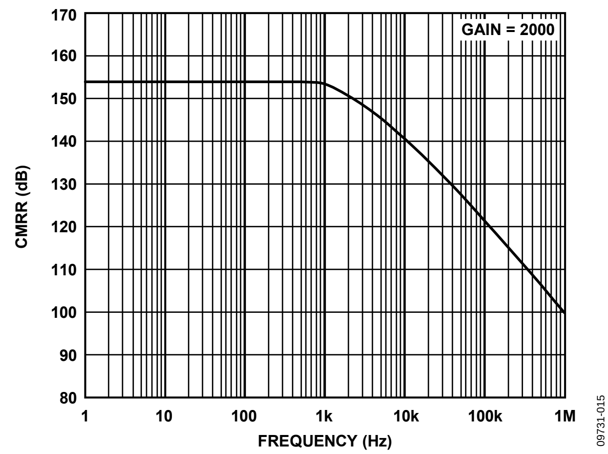

Figure 13. CMRR vs. Frequency

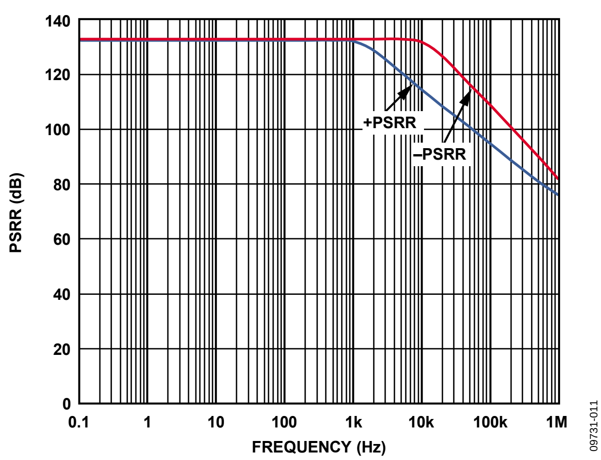

Figure 11. PSRR vs. Frequency

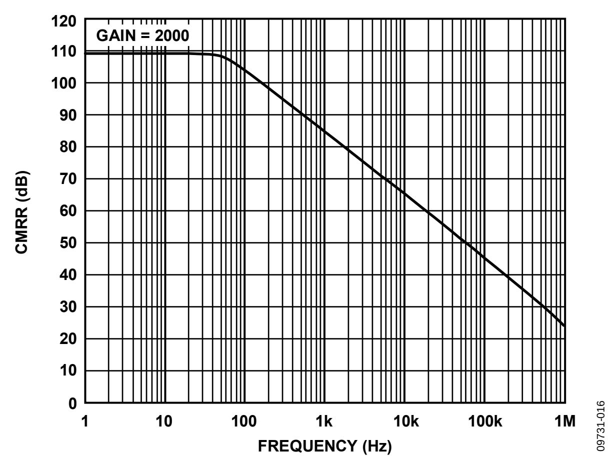

Figure 14. CMRR vs. Frequency, 1 kΩ Source Imbalance

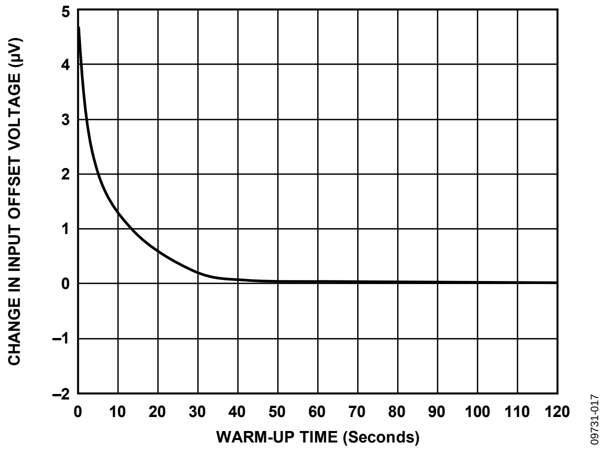

Figure 15. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

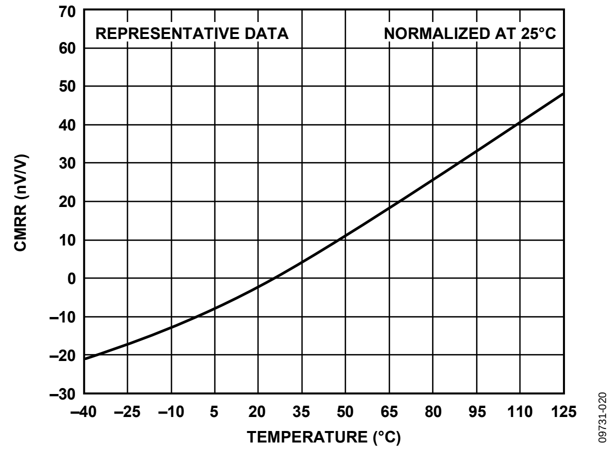

Figure 18. CMRR vs. Temperature, Normalized at 25°C

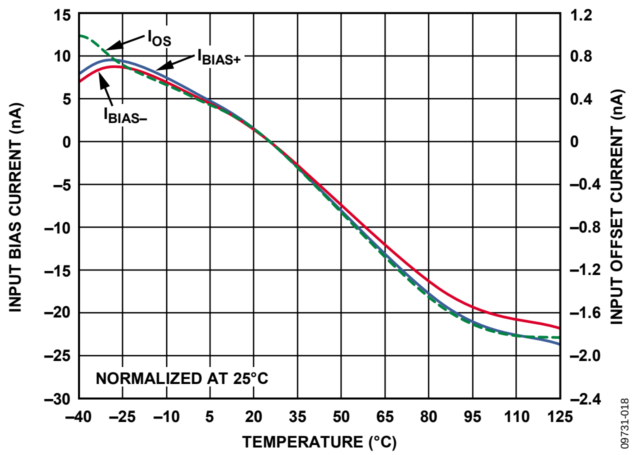

Figure 16. Input Bias Current and Input Offset Current vs. Temperature, Normalized at 25°C

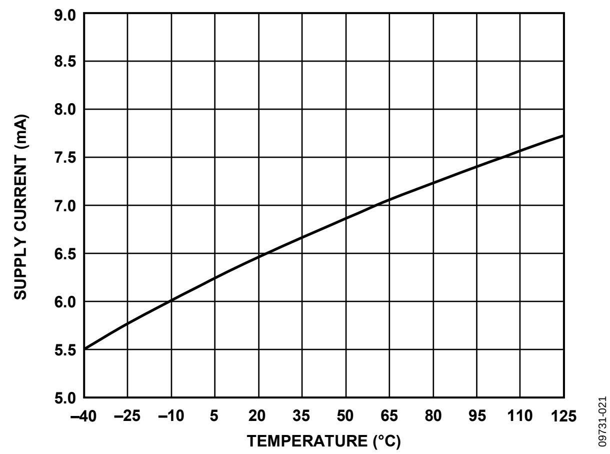

Figure 19. Supply Current vs. Temperature

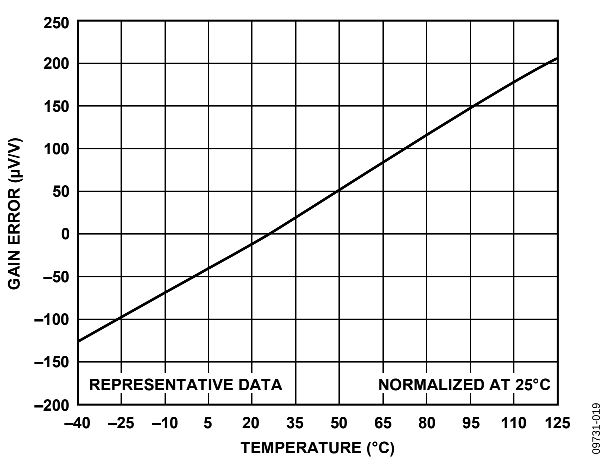

Figure 17. Gain Error vs. Temperature, Normalized at 25°C

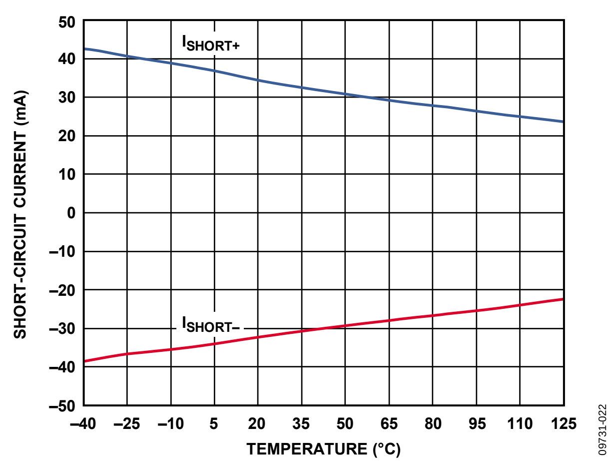

Figure 20. Short-Circuit Current vs. Temperature

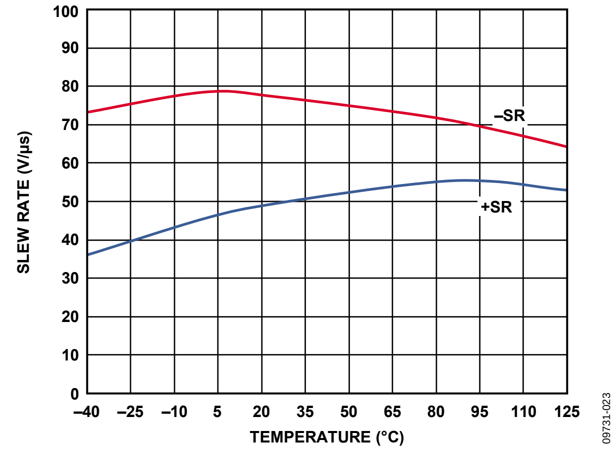

Figure 21. Slew Rate vs. Temperature, $V_S = \pm 15$ V

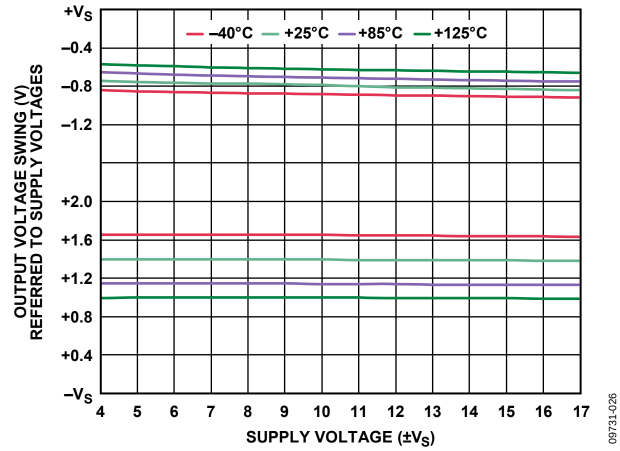

Figure 24. Output Voltage Swing vs. Supply Voltage, $R_L = 10$ kΩ

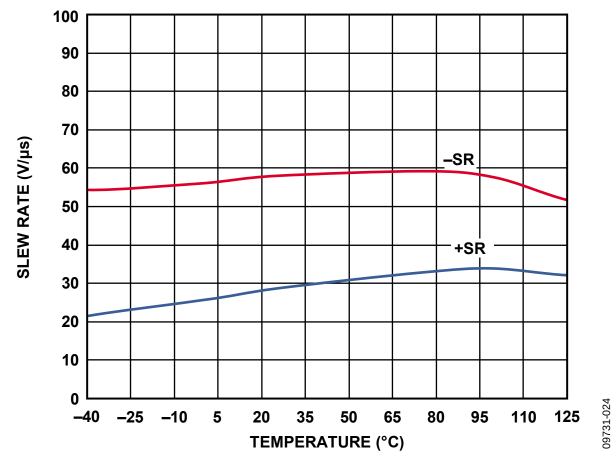

Figure 22. Slew Rate vs. Temperature, $V_S = \pm 5$ V

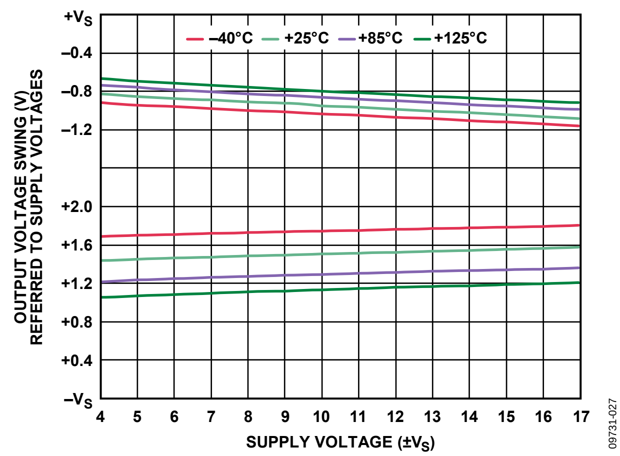

Figure 25. Output Voltage Swing vs. Supply Voltage, $R_L = 2$ kΩ

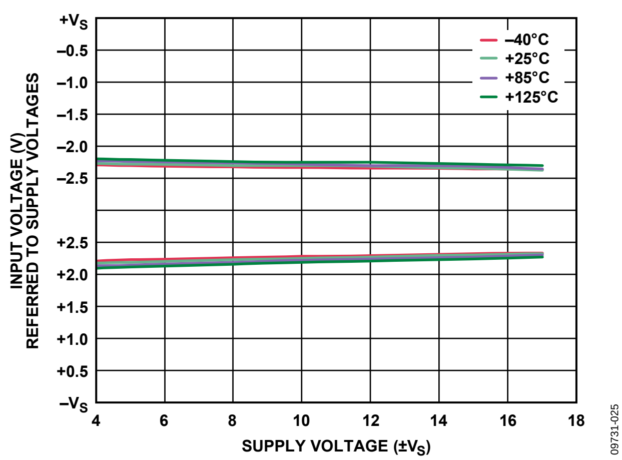

Figure 23. Input Voltage Limit vs. Supply Voltage

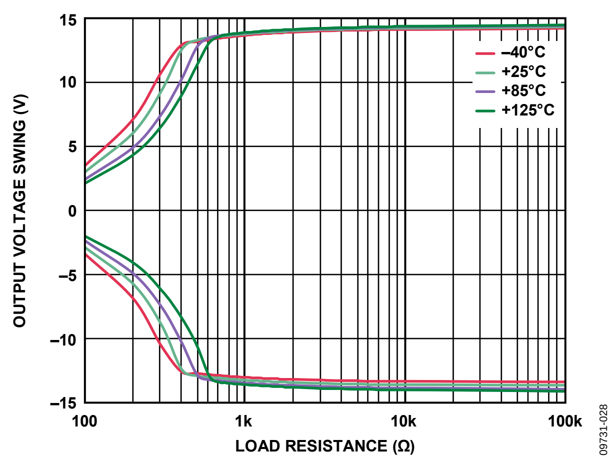

Figure 26. Output Voltage Swing vs. Load Resistance, $V_S = \pm 15$ V

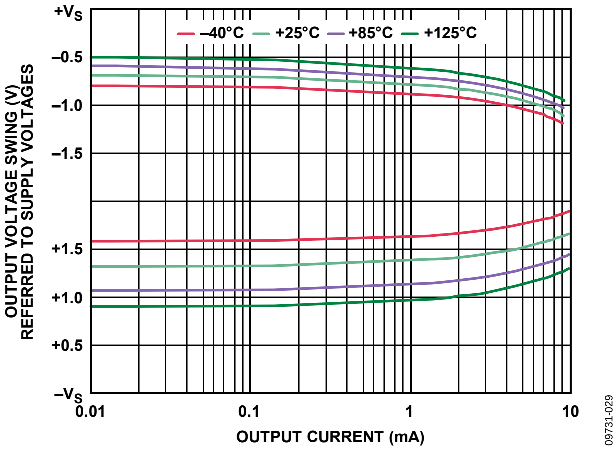

Figure 27. Output Voltage Swing vs. Output Current, $V_S = \pm 15$ V

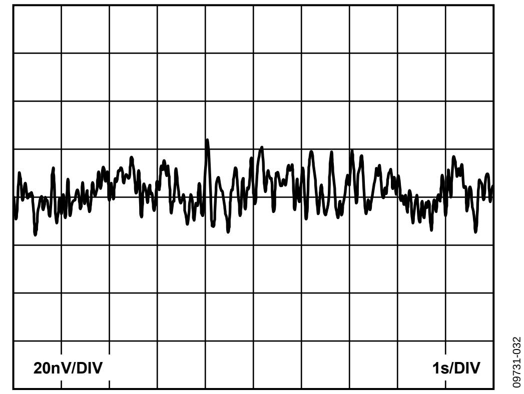

Figure 30. RTI Voltage Noise, 0.1 Hz to 10 Hz

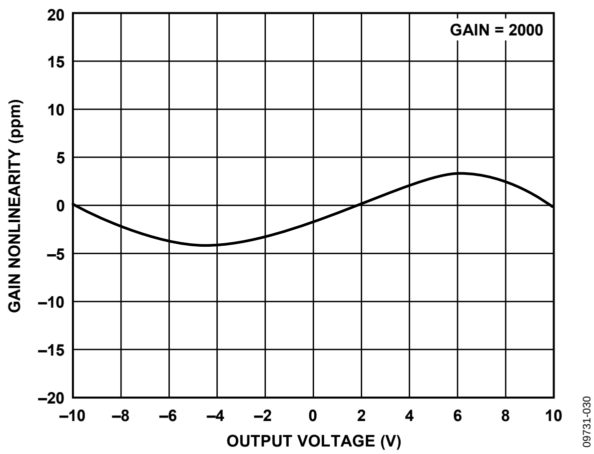

Figure 28. Gain Nonlinearity, $R_L = 10$ kΩ

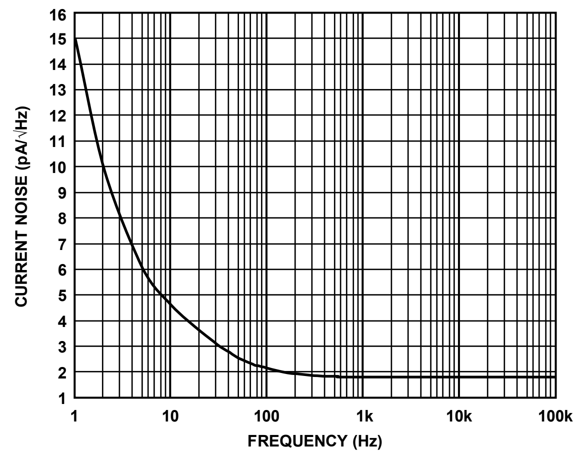

Figure 31. Current Noise Spectral Density vs. Frequency

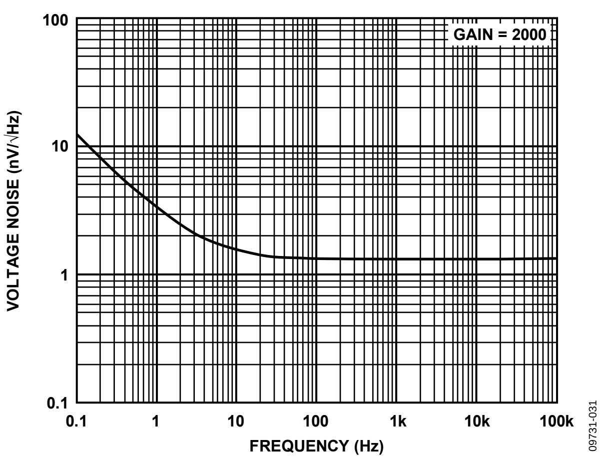

Figure 29. RTI Voltage Noise Spectral Density vs. Frequency

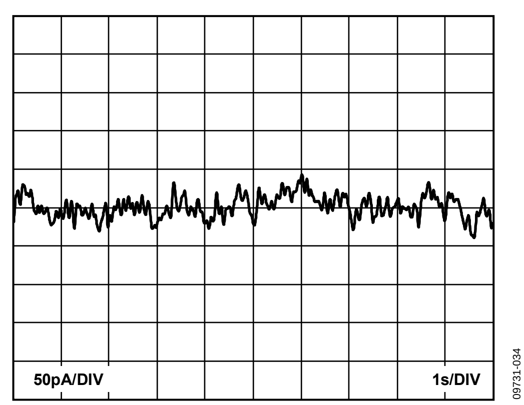

Figure 32. Current Noise, 0.1 Hz to 10 Hz

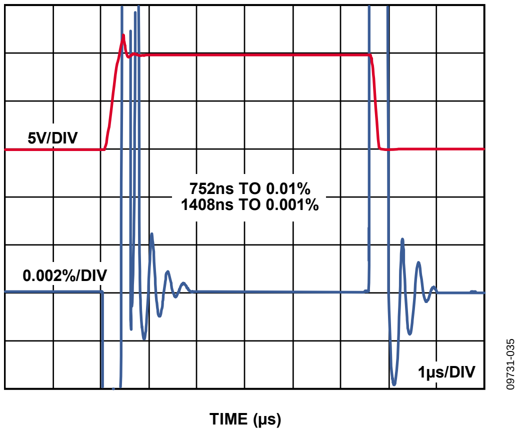

Figure 33. Large Signal Pulse Response and Settling Time, 10 V Step, V_S = ±15 V

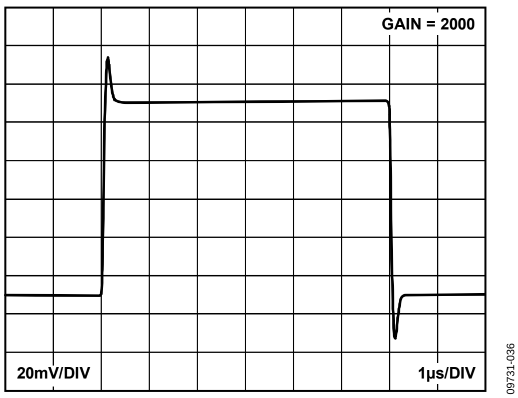

Figure 34. Small Signal Pulse Response, R_L = 10 kΩ, C_L = 100 pF

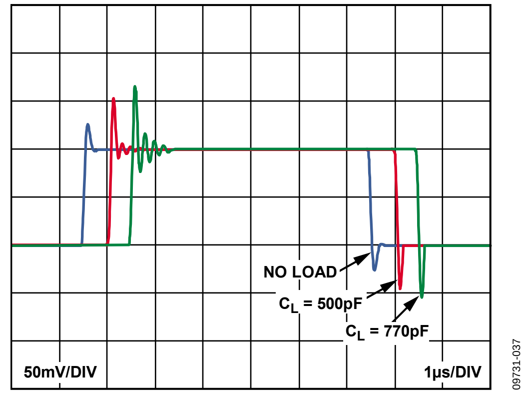

Figure 35. Small Signal Pulse Response with Various Capacitive Loads, No Resistive Load

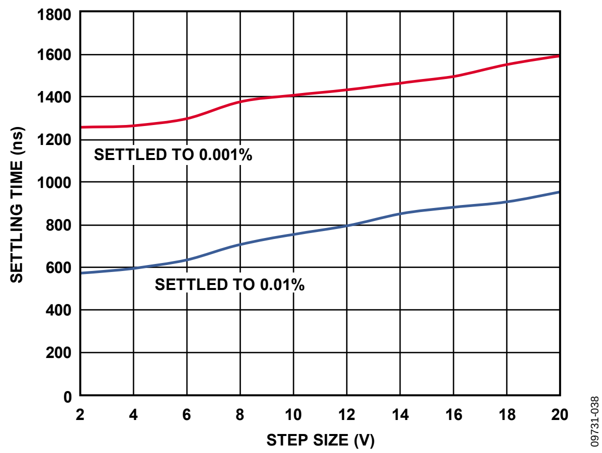

Figure 36. Settling Time vs. Step Size

THEORY OF OPERATION

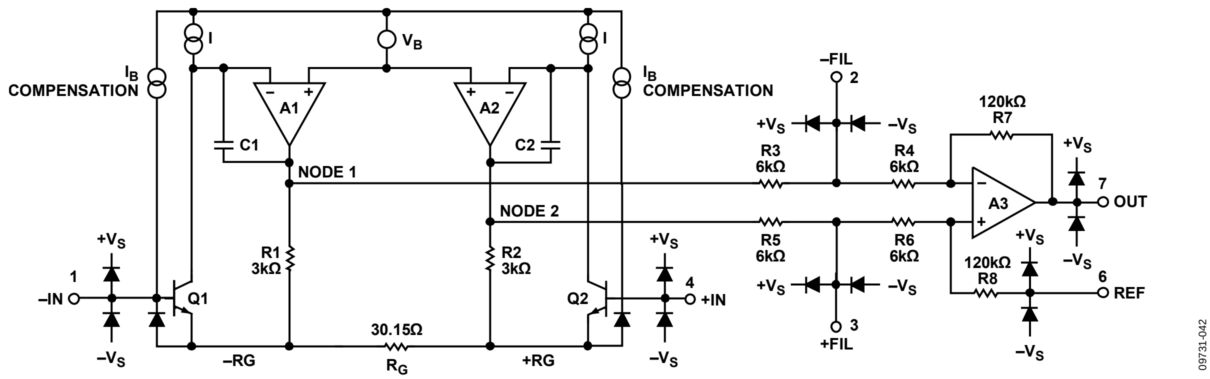

Figure 37. Simplified Schematic

ARCHITECTURE

The AD8428 is based on the classic 3-op-amp topology. This topology has two stages: a gain stage (preamplifier) to provide differential amplification by a factor of 200, followed by a difference amplifier (subtractor) stage to remove the common-mode voltage and provide additional amplification by a factor of 10. Figure 37 shows a simplified schematic of the AD8428.

The first stage works as follows. To keep its two inputs matched, Amplifier A1 must keep the collector of Q1 at a constant voltage. It does this by forcing −RG to be a constant diode drop from −IN. Similarly, A2 forces +RG to be a constant diode drop from +IN. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, R_G. The current that flows across this resistor must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs.

The second stage is a G = 10 difference amplifier, composed of Amplifier A3 and Resistors R3 through R8. This stage removes the common-mode signal from the amplified differential signal.

The transfer function of the AD8428 is

$$V_{OUT} = 2000 \times (V_{IN+} - V_{IN-}) + V_{REF}$$

FILTER TERMINALS

The −FIL and +FIL terminals allow access between R3 and R4, and between R5 and R6, respectively. Adding a filter between these two terminals modifies the gain that is applied to the signal before it reaches the second amplifier stage (see the Applications Information section).

REFERENCE TERMINAL

The output voltage of the AD8428 is developed with respect to the potential on the reference terminal. This is useful when the output signal must be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8428 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$.

For best performance, the source impedance to the REF terminal should be kept well below 1 Ω. As shown in Figure 37, the reference terminal, REF, is at one end of a 120 kΩ resistor. Additional impedance at the REF terminal adds to this 120 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be calculated as follows:

$$2 \times (120\ \text{k}\Omega + R_{REF})/(240\ \text{k}\Omega + R_{REF})$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades the CMRR of the amplifier.

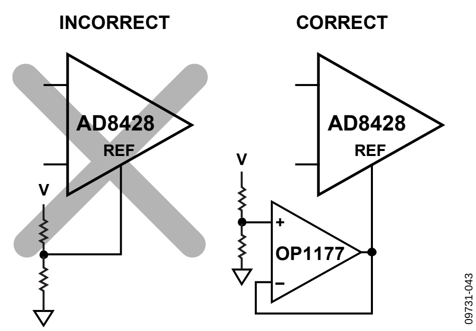

Figure 38. Driving the Reference Pin

INPUT VOLTAGE RANGE

The 3-op-amp architecture of the AD8428 applies gain in the first stage before removing the common-mode voltage in the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 37) experience a combination of an amplified differential signal, a common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited. Figure 9 shows the allowable input common-mode voltage ranges for various output voltages and supply voltages.

LAYOUT

To ensure optimum performance of the AD8428 at the PCB level, care must be taken in the design of the board layout. The pins of the AD8428 are especially arranged to simplify board layout and to help minimize parasitic imbalance between the inputs.

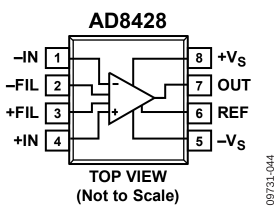

Figure 39. Pinout Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other.

To maintain high CMRR over frequency, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input paths (for example, for input protection) should be placed close to the in-amp inputs to minimize the interaction of the inputs with parasitic capacitance from the PCB traces.

Parasitic capacitance at the filter pins can also affect CMRR over frequency. If the board design has a component at the filter pins, the component should be chosen so that the parasitic capacitance is as small as possible.

Power Supplies and Grounding

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 11 for more information.

Place a 0.1 µF capacitor as close as possible to each supply pin. Because the length of the bypass capacitor leads is critical at high frequency, surface-mount capacitors are recommended. Parasitic inductance in the bypass ground trace works against the low impedance created by the bypass capacitor.

As shown in Figure 40, a 10 µF capacitor can be used farther away from the device. For larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical. In most cases, the 10 µF capacitor can be shared by other precision integrated circuits.

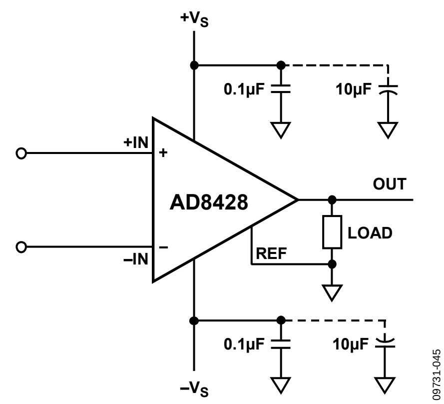

Figure 40. Supply Decoupling, REF, and Output Referred to Local Ground

A ground plane layer is helpful to reduce undesired parasitic inductances and to minimize voltage drops with changes in current. The area of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the impedance of the path at high frequency. Large changes in currents in an inductive decoupling path or ground return create unwanted effects due to the coupling of such changes into the amplifier inputs.

Because load currents flow from the supplies, the load should be connected at the same physical location as the bypass capacitor grounds.

Reference Pin

The output voltage of the AD8428 is developed with respect to the potential on the reference terminal. Ensure that REF is tied to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8428 must have a return path to ground. When the source, such as a thermocouple, cannot provide a current return path, one should be created, as shown in Figure 41.

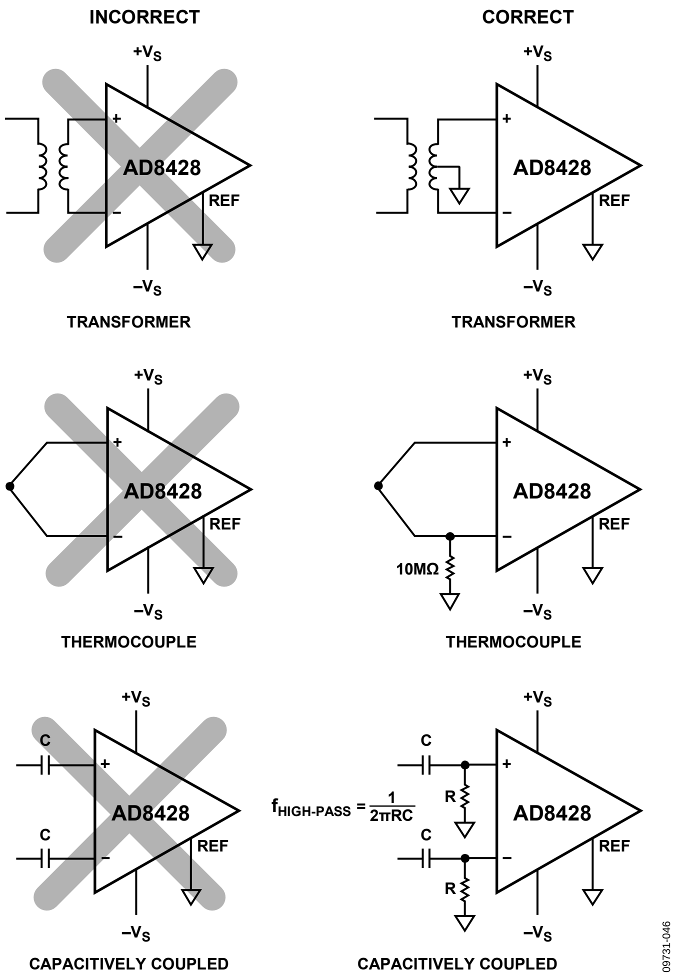

Figure 41. Creating an Input Bias Current Return Path

INPUT PROTECTION

Do not allow the inputs of the AD8428 to exceed the ratings stated in the Absolute Maximum Ratings section. If these ratings cannot be adhered to, add protection circuitry in front of the AD8428 to limit the maximum current into the inputs (see the I_{MAX} section).

I_{MAX}

The maximum current into the AD8428 inputs, I_{MAX}, depends on time and temperature. At room temperature, the device can withstand a current of 10 mA for at least one day. This time is cumulative over the life of the device.

Input Voltages Beyond the Rails

If voltages beyond the rails are expected, use an external resistor in series with each input to limit current during overload conditions. The limiting resistor at each input can be computed using the following equation:

$$R_{PROTECT} \geq \frac{|V_{IN} - V_{SUPPLY}|}{I_{MAX}}$$

Noise sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used at the inputs to shunt current away from the AD8428 inputs and, therefore, allow smaller protection resistor values. To ensure that current flows primarily through the external protection diodes, place a small value resistor, such as a 33 Ω resistor, between the diodes and the AD8428.

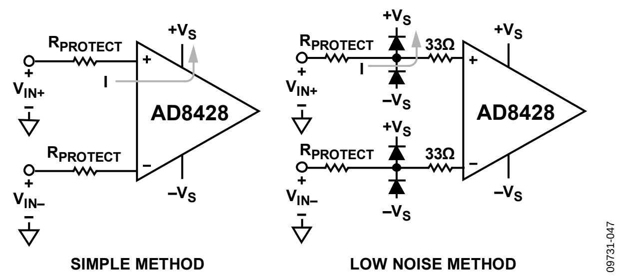

Figure 42. Protection for Voltages Beyond the Rails

Large Differential Input Voltage at High Gain

If large differential voltages at high gain are expected, use an external resistor in series with each input to limit current during overload conditions. The limiting resistor at each input can be computed using the following equation:

$$R_{PROTECT} \geq \frac{1}{2} \times \left(\frac{|V_{DIFF}| - 1\,\text{V}}{I_{MAX}} - R_G \right)$$

Noise sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used across the AD8428 inputs to shunt current away from the inputs and, therefore, allow smaller protection resistor values.

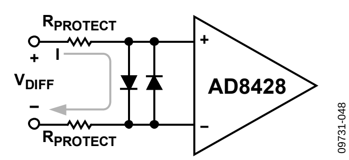

Figure 43. Protection for Large Differential Voltages

RADIO FREQUENCY INTERFERENCE (RFI)

Because of its high gain and low noise properties, the AD8428 is a highly sensitive amplifier. Therefore, RF rectification can be a problem if the AD8428 is used in applications that have strong RF signal sources present. The problem is intensified if long leads or PCB traces are required to connect the amplifier to the signal source. The disturbance can appear as a dc offset voltage or as a train of pulses.

High frequency signals can be filtered with a low-pass filter network at the input of the instrumentation amplifier, as shown in Figure 44.

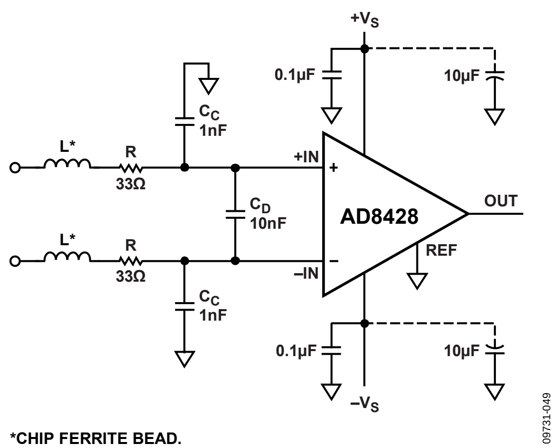

Figure 44. RFI Suppression

The filter limits both the differential and common-mode bandwidth, as shown in the following equations:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

C_D affects the differential signal, and C_C affects the common-mode signal. Choose values of R and C_C that minimize RFI. A mismatch between R × C_C at the positive input and R × C_C at the negative input degrades the CMRR of the AD8428. By using a value of C_D one order of magnitude larger than C_C, the effect of the mismatch is reduced, and performance is improved.

Resistors add noise; therefore, the choice of resistor and capacitor values depends on the desired trade-off between noise, input impedance at high frequencies, and RFI immunity. To achieve low noise and sufficient RFI filtering, the use of inductive ferrite beads is recommended (see Figure 44). Using inductive ferrite beads allows the value of the resistors to be reduced, which helps to minimize the noise at the input.

For best results, place the RFI filter network as close to the amplifier as possible. Layout is critical to ensure that RF signals are not picked up on the traces after the filter. If RF interference is too strong to be filtered, shielding is recommended.

Note that the resistors used for the RFI filter can be the same as those used for input protection (see the Input Protection section).

CALCULATING THE NOISE OF THE INPUT STAGE

The total noise of the amplifier front end depends on much more than the specifications in this data sheet. The three main contributors to noise are as follows:

- Source resistance
- Voltage noise of the instrumentation amplifier
- Current noise of the instrumentation amplifier

In the following calculations, noise is referred to the input (RTI); that is, all sources of noise are calculated as if the source appeared at the amplifier input. To calculate the noise referred to the amplifier output (RTO), multiply the RTI noise by the gain of the instrumentation amplifier.

Source Resistance Noise

Any sensor connected to the AD8428 has some output resistance. There may also be resistance placed in series with the inputs for protection from either overvoltage or radio frequency interference. This combined resistance is labeled R1 and R2 in Figure 45. Any resistor, no matter how well made, has an intrinsic level of noise. This noise is proportional to the square root of the resistor value. At room temperature, the value is approximately equal to 4 nV/√Hz × √(resistor value in kΩ).

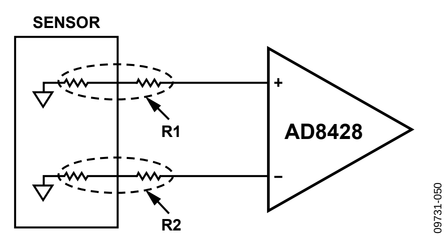

Figure 45. Source Resistance from Sensor and Protection Resistors

For example, assuming that the combined sensor and protection resistance is 4 kΩ on the positive input and 1 kΩ on the negative input, the total noise from the input resistance is

$$\sqrt{\left(4 \times \sqrt{4}\right)^2 + \left(4 \times \sqrt{1}\right)^2} = \sqrt{64 + 16} = 8.9\ \text{nV}/\sqrt{\text{Hz}}$$

Voltage Noise of the Instrumentation Amplifier

Unlike other instrumentation amplifiers in which an external resistor is used to set the gain, the voltage noise specification of the AD8428 already includes the input noise, output noise, and the R_G resistor noise.

Current Noise of the Instrumentation Amplifier

The contribution of current noise to the input stage in nV/√Hz is calculated by multiplying the source resistance in kΩ by the specified current noise of the instrumentation amplifier in pA/√Hz.

For example, if the R1 source resistance in Figure 45 is 4 kΩ and the R2 source resistance is 1 kΩ, the total effect from the current noise is calculated as follows:

$$\sqrt{(4 \times 1.5)^2 + (1 \times 1.5)^2} = \sqrt{36 + 2.25} = 6.2 \text{ nV}/\sqrt{\text{Hz}}$$

Total Noise Density Calculation

To determine the total noise of the in-amp, referred to input, combine the source resistance noise, voltage noise, and current noise contribution by the sum of squares method.

For example, if the R1 source resistance in Figure 45 is 4 kΩ and the R2 source resistance is 1 kΩ, the total noise, referred to input, is

$$\sqrt{8.9^2 + 1.5^2 + 6.2^2} = 11.0 \text{ nV}/\sqrt{\text{Hz}}$$

APPLICATIONS INFORMATION

The classic 3-op-amp topology used for instrumentation amplifiers typically places all the gain in the first stage and subtracts the common-mode signals only in the second stage. When operated at high gain, any amplifier is sensitive to large interfering signals that can saturate it, thus making it impossible to recover the signal of interest.

The AD8428 splits the total gain of 2000 into two stages: 200 in the preamplification stage and 10 in the subtractor stage. Reducing the gain of the first stage helps to increase the common-mode range vs. differential signal range by avoiding saturation of the preamps.

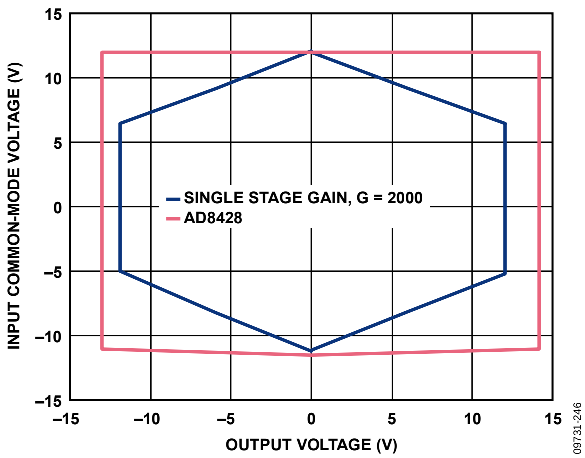

Figure 46. AD8428 vs. Single Stage Gain Topology, G = 2000

In addition, filtering between stages can help to attenuate signals before they reach the second amplification stage. This filtering helps to prevent saturation of the second stage amplifier as long as the signals are located in frequencies other than the signal of interest.

EFFECT OF PASSIVE NETWORK ACROSS THE FILTER TERMINALS

The AD8428 filter terminals allow access between the two amplification stages. Adding a passive network between the two terminals can shape the transfer function over the frequency of the amplifier. The general expression for the transfer function is represented by Equation 1.

$$G(s) = \frac{2000 \times Z(s)}{Z(s) + 6000} \quad (1)$$

where $Z(s)$ is the frequency dependent impedance of the network across the filter terminals.

CIRCUITS USING THE FILTER TERMINALS

Setting the Amplifier to Different Gains

In its simplest form, the transfer function equation (Equation 1) implies that the AD8428 can be configured for gains lower than 2000. This can be achieved by attaching a resistor across the filter pins. Unlike the gain configuration of traditional instrumentation amplifiers, this resistor attenuates the signal that was previously amplified by the initial gain of 200.

Because this resistor appears inside the feedback of the subtractor stage, it modifies the gain of the subtractor as well. The total gain formula is a simplified version of the transfer function equation (Equation 1).

$$G = \frac{2000 \times R_G}{R_G + 6000} \quad (2)$$

The R_G unit is in ohms. The resistor value required to obtain the desired gain can be calculated using the following formula:

$$R_G = \frac{6000 \times G}{2000 - G}$$

The AD8428 defaults to G = 2000 when no gain resistor is used. When setting the amplifier to a different gain, the absolute gain accuracy is only 10%. In addition, the temperature mismatch of the external gain resistor increases the gain drift of the instrumentation amplifier. Gain error and gain drift are at a guaranteed minimum when a gain resistor is not used. For applications that require accuracy at different gains, low noise, and wide bandwidth, the AD8429 should be considered.

Low-Pass Filter

To help limit undesired differential signals, a first-order, low-pass filter can be implemented by adding a capacitor across the filter terminals of the AD8428, as shown in Figure 47.

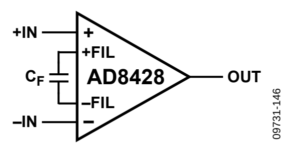

Figure 47. Differential Low-Pass Filter

This single-pole filter limits the signal bandwidth, as shown in the following equation:

$$f_C = \frac{1}{2\pi(6\ \text{k}\Omega)C_F}$$

The 6 kΩ factor comes from the internal resistor values. The tolerance of these resistors is 10%; therefore, using capacitors with a tolerance better than 5% does not provide a significant improvement on the absolute tolerance of the cutoff frequency.

Limiting the bandwidth of the amplifier also helps to minimize the amount of out-of-band noise present at the output.

Note that filtering common-mode signals by adding a capacitor on each filter terminal to ground degrades the performance of the amplifier. This practice is generally discouraged because it degrades CMRR performance. In addition, filtering common-mode signals has little effect on preventing the saturation of the internal nodes. On the contrary, the load added to the preamplifiers causes them to saturate with even smaller common-mode signals.

Notch Filter

In cases where the frequency of the interfering signal is well known, a notch filter can be implemented to help minimize the impact of the known signal on the measurement. The filter can be realized by adding a series LC network between the filter pins, as shown in Figure 48.

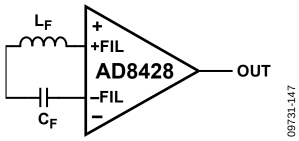

Figure 48. Notch Filter Example

The inductor and capacitor form a resonant circuit that rejects frequencies near the notch. The center frequency can be calculated using the following equation:

$$f_N = \frac{1}{2\pi\sqrt{L_F C_F}}$$

The Q factor of the filter is given by the following equation:

$$Q = \frac{1}{6000}\sqrt{\frac{L_F}{C_F}}$$

The accuracy of the center frequency, f_N, depends only on the tolerance of the capacitor and inductor values, not on the value of the internal resistors. However, the Q of the circuit depends on both the tolerance of the external components and the absolute tolerance of the internal resistors, which is typically 10%.

The Q factor is a filter parameter that indicates how narrow the notch filter is. It is defined as follows:

$$Q = \frac{f_N}{f_B - f_A}$$

where f_A and f_B are the frequencies at which there is −3 dB attenuation on each side of the notch.

This equation indicates that the higher the Q, the narrower the notch—that is, high values of Q increase the selectivity of the notch. In other words, although high values of Q reduce the effect of the notch on the amplitude and phase in neighboring frequencies, the ability to reject the undesired frequency may also be reduced due to mismatch between it and the actual center frequency. This mismatch can be caused by frequency variations on the affecting source and the tolerance of the filter inductor and capacitor values.

In contrast, low values of Q work better to ensure that the interfering frequency is attenuated, but these low values also affect the signal of interest if it is located close to the center frequency of the notch.

For example, if the goal is to attenuate the interfering signal by 20 dB, a large Q value reduces the frequency range where the notch is effective, as shown in Figure 49.

In contrast, a small Q value increases the range for the same attenuation, which relaxes the tolerance requirements between the inductor and capacitor and the frequency uncertainty of the undesired signal. However, the lower Q value has a significant effect on signal bandwidth one decade before the notch frequency.

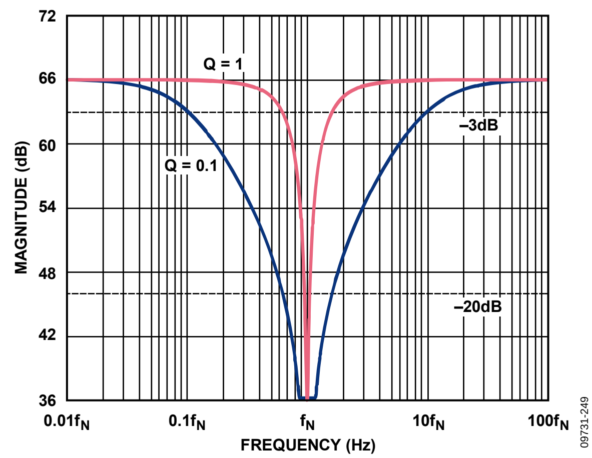

Figure 49. Notch Filter Attenuation with Q = 0.1 and Q = 1 Around the Center Frequency

The maximum attenuation that can be achieved with a notch filter is at its center frequency, f_N. This maximum attenuation (or depth of the notch) depends on the equivalent series resistance of the inductor and capacitor at the center frequency. Choosing components with high quality factors improves the rejection at the filter's center frequency. For information about calculating the maximum allowed series resistance at the frequency of interest to obtain the desired attenuation, see the Setting the Amplifier to Different Gains section.

Extracting the Common-Mode Voltage of the Input

The common-mode signal present at the input terminals can be extracted by inserting two resistors between the filter terminals and tapping from the center, as shown in Figure 50. The common-mode voltage, V_{CM}, is the average of the voltages present at the two inputs minus a 0.6 V drop.

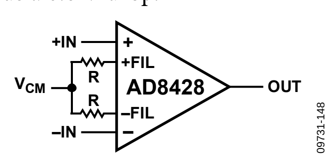

Figure 50. Extracting the Common-Mode Voltage

Use resistor values that are high enough to minimize the impact on gain accuracy. For example, resistor values of 2 MΩ introduce an additional gain error of less than 0.2%. For information about the impact of these resistors on the gain of the amplifier, see the Effect of Passive Network Across the Filter Terminals section.