

## Precision Micropower, Low Noise CMOS, Rail-to-Rail Input/Output Operational Amplifiers

### FEATURES

- ▶ Low offset voltage: 50  $\mu$ V maximum
- ▶ Low input bias current: 1 pA maximum
- ▶ Single-supply operation: 1.8 V to 5 V
- ▶ Low noise: 22 nV/ $\sqrt{\text{Hz}}$
- ▶ Micropower: 50  $\mu$ A maximum
- ▶ Low distortion
- ▶ No phase reversal
- ▶ Unity gain stable

### APPLICATIONS

- ▶ Battery-powered instrumentation
- ▶ Multipole filters
- ▶ Sensors
- ▶ Low power ASIC input or output amplifiers

### GENERAL DESCRIPTION

The AD8603/AD8607/AD8609 are single/dual/quad micro-power rail-to-rail input and output amplifiers, respectively, that feature very low offset voltage as well as low input voltage and current noise.

These amplifiers use a patented trimming technique that achieves superior precision without laser trimming. The parts are fully specified to operate from 1.8 V to 5.0 V single supply or from  $\pm 0.9$  V to  $\pm 2.5$  V dual supply. The combination of low offsets, low noise, very low input bias currents, and low power consumption makes the AD8603/AD8607/AD8609 especially useful in portable and loop-powered instrumentation.

The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power, single-supply systems.

The AD8603 is available in a [tiny 5-lead TSOT package](#). The AD8607 is available in [8-lead MSOP](#) and [8-lead SOIC packages](#). The AD8609 is available in [14-lead TSSOP](#) and [14-lead SOIC packages](#).

### PIN CONFIGURATIONS

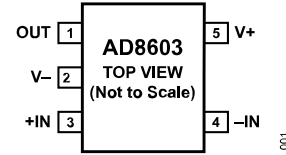


Figure 1. 5-Lead TSOT (UJ Suffix)

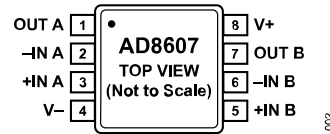


Figure 2. 8-Lead MSOP (RM Suffix)

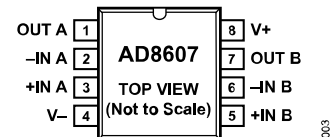


Figure 3. 8-Lead SOIC (R Suffix)

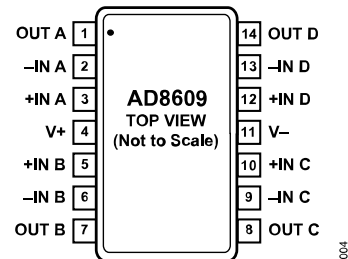


Figure 4. 14-Lead TSSOP (RU Suffix)

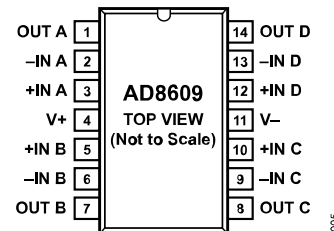


Figure 5. 14-Lead SOIC (R Suffix)

**TABLE OF CONTENTS**

Features.....	1	No Phase Reversal.....	13
Applications.....	1	Input Overvoltage Protection.....	13
General Description.....	1	Driving Capacitive Loads.....	13
Pin Configurations.....	1	Proximity Sensors.....	14
Specifications.....	3	Composite Amplifiers.....	14
Electrical Characteristics.....	3	Battery-Powered Applications.....	14
Absolute Maximum Ratings.....	6	Photodiodes.....	14
ESD Caution.....	6	Outline Dimensions.....	15
Typical Performance Characteristics.....	7	Ordering Guide.....	16
Applications.....	13		

**REVISION HISTORY****10/2023—Rev. C to Rev. D**

Change to Large Signal Voltage Gain Parameter, Table 2.....	4
Updated Outline Dimensions.....	15
Changes to Ordering Guide.....	16

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_S = 5\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
INPUT CHARACTERISTICS							
Offset Voltage	$V_{OS}$	$V_S = 3.3\text{ V @ } V_{CM} = 0.5\text{ V and } 2.8\text{ V}$		12	50	$\mu\text{V}$	
		$-0.3\text{ V} < V_{CM} < +5.2\text{ V}$		40	300	$\mu\text{V}$	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}, -0.3\text{ V} < V_{CM} < +5.2\text{ V}$				700	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4.5	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2	1	$\text{pA}$	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				50	$\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				500	$\text{pA}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.1	0.5	$\text{pA}$	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				50	$\text{pA}$
Input Voltage Range	IVR		-0.3		+5.2	V	
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 5\text{ V}$	85	100		dB	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80			dB	
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega, 0.5\text{ V} < V_O < 4.5\text{ V}$					
			AD8603	400	1000		V/mV
AD8607/AD8609	250	450			V/mV		
Input Capacitance	$C_{DIFF}$			1.9		$\text{pF}$	
	$C_{CM}$			2.5		$\text{pF}$	
OUTPUT CHARACTERISTICS							
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	4.95	4.97		V	
		$-40^\circ\text{C to } +125^\circ\text{C}$	4.9			V	
		$I_L = 10\text{ mA}$	4.65	4.97		V	
		$-40^\circ\text{C to } +125^\circ\text{C}$	4.50			V	
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$		16	30	mV	
		$-40^\circ\text{C to } +125^\circ\text{C}$			50	mV	
		$I_L = 10\text{ mA}$		160	250	mV	
		$-40^\circ\text{C to } +125^\circ\text{C}$			330	mV	
Short-Circuit Current	$I_{SC}$			$\pm 70$		mA	
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}, A_V = 1$		36		$\Omega$	
POWER SUPPLY							
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$	80	100		dB	
Supply Current per Amplifier	$I_{SY}$	$V_O = 0\text{ V}$		40	50	$\mu\text{A}$	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			60	$\mu\text{A}$	
DYNAMIC PERFORMANCE							
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ $\mu\text{s}$	
Settling Time 0.1%	$t_S$	$G = \pm 1, 2\text{ V step}$		23		$\mu\text{s}$	
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$		400		kHz	
		$R_L = 10\text{ k}\Omega$		316		kHz	
Phase Margin	$\phi_O$	$R_L = 10\text{ k}\Omega, R_L = 100\text{ k}\Omega$		70		Degrees	
NOISE PERFORMANCE							
Peak-to-Peak Noise	$e_{n,p-p}$	0.1 Hz to 10 Hz		2.3	3.5	$\mu\text{V}$	
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 10\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$	
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$	

## SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Channel Separation	$C_S$	$f = 10 \text{ kHz}$		-115		dB
		$f = 100 \text{ kHz}$		-110		dB

$V_S = 1.8 \text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
<b>INPUT CHARACTERISTICS</b>							
Offset Voltage	$V_{OS}$	$V_S = 3.3 \text{ V}$ @ $V_{CM} = 0.5 \text{ V}$ and $2.8 \text{ V}$		12	50	$\mu\text{V}$	
		$-0.3 \text{ V} < V_{CM} < +1.8 \text{ V}$		40	300	$\mu\text{V}$	
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ , $-0.3 \text{ V} < V_{CM} < +1.8 \text{ V}$				500	$\mu\text{V}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , $-0.3 \text{ V} < V_{CM} < +1.7 \text{ V}$				700	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4.5	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2	1	$\text{pA}$	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				50	$\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$				500	$\text{pA}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	$\text{pA}$	
Input Voltage Range	IVR		-0.3		+1.8	V	
Common-Mode Rejection Ratio	CMRR	$0 \text{ V} < V_{CM} < 1.8 \text{ V}$	80	98		dB	
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	70			dB	
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10 \text{ k}\Omega$ , $0.5 \text{ V} < V_O < 1.3 \text{ V}$		150	3000	$\text{V}/\text{mV}$	
				100	2000	$\text{V}/\text{mV}$	
Input Capacitance	$C_{DIFF}$ $C_{CM}$			2.1		$\text{pF}$	
				3.8		$\text{pF}$	
<b>OUTPUT CHARACTERISTICS</b>							
Output Voltage High	$V_{OH}$	$I_L = 1 \text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	1.65	1.72		V	
			1.6			V	
Output Voltage Low	$V_{OL}$	$I_L = 1 \text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		38	60	$\text{mV}$	
					80	$\text{mV}$	
Short-Circuit Current	$I_{SC}$		$\pm 10$			$\text{mA}$	
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 10 \text{ kHz}$ , $A_V = 1$		36		$\Omega$	
<b>POWER SUPPLY</b>							
Power Supply Rejection Ratio	PSRR	$1.8 \text{ V} < V_S < 5 \text{ V}$	80	100		dB	
Supply Current per Amplifier	$I_{SY}$	$V_O = 0 \text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		40	50	$\mu\text{A}$	
					60	$\mu\text{A}$	
<b>DYNAMIC PERFORMANCE</b>							
Slew Rate	SR	$R_L = 10 \text{ k}\Omega$		0.1		$\text{V}/\mu\text{s}$	
Settling Time 0.1%	$t_S$	$G = \pm 1$ , $1 \text{ V}$ step		9.2		$\mu\text{s}$	
Gain Bandwidth Product	GBP	$R_L = 100 \text{ k}\Omega$		385		$\text{kHz}$	
		$R_L = 10 \text{ k}\Omega$		316		$\text{kHz}$	
Phase Margin	$\phi_O$	$R_L = 10 \text{ k}\Omega$ , $R_L = 100 \text{ k}\Omega$		70		Degrees	
<b>NOISE PERFORMANCE</b>							
Peak-to-Peak Noise	$e_{n \text{ p-p}}$	0.1 Hz to 10 Hz		2.3	3.5	$\mu\text{V}$	
Voltage Noise Density	$e_n$	$f = 1 \text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 10 \text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$	

## SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Noise Density	$i_n$	$f = 1 \text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation	$C_S$	$f = 10 \text{ kHz}$		-115		dB
		$f = 100 \text{ kHz}$		-110		dB

**ABSOLUTE MAXIMUM RATINGS**

Absolute maximum ratings apply at 25°C, unless otherwise noted.

**Table 3.**

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to $V_S$
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**Table 4. Package Characteristics**

Package Type	$\theta_{JA}$ <sup>1</sup>	$\theta_{JC}$	Unit
5-Lead TSOT (UJ)	207	61	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC_N (R)	158	43	°C/W
14-Lead SOIC_N (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

<sup>1</sup>  $\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for a device soldered in a circuit board for surface-mount packages.

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

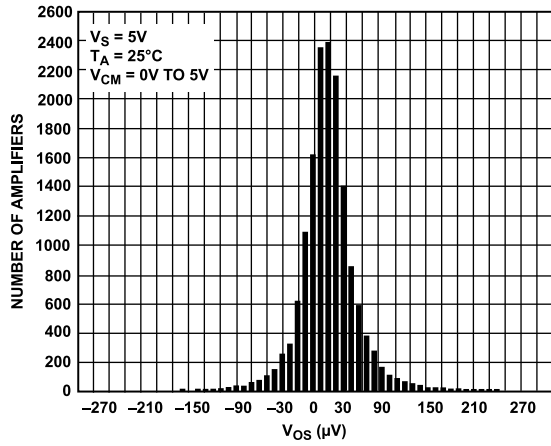


Figure 6. Input Offset Voltage Distribution

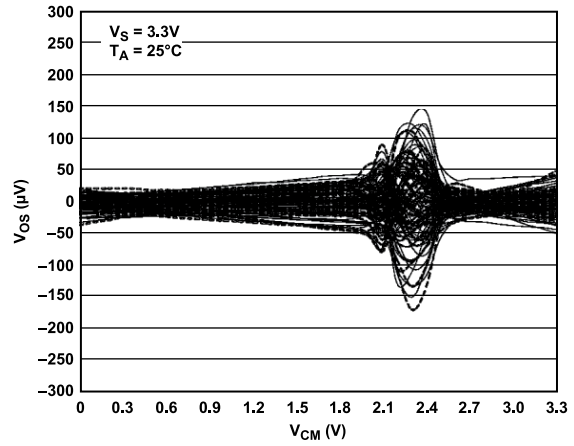


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

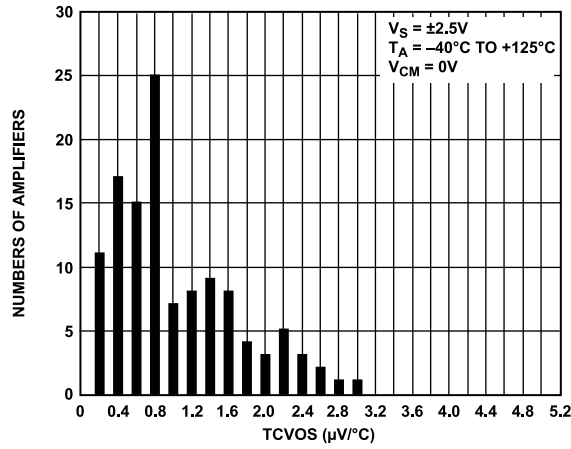


Figure 7. Input Offset Voltage Drift Distribution

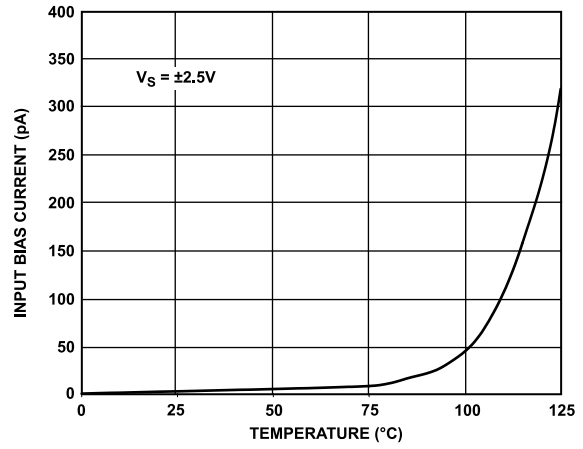


Figure 10. Input Bias Current vs. Temperature

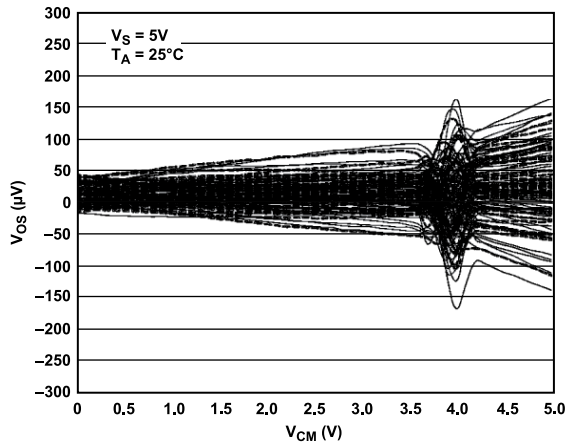


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

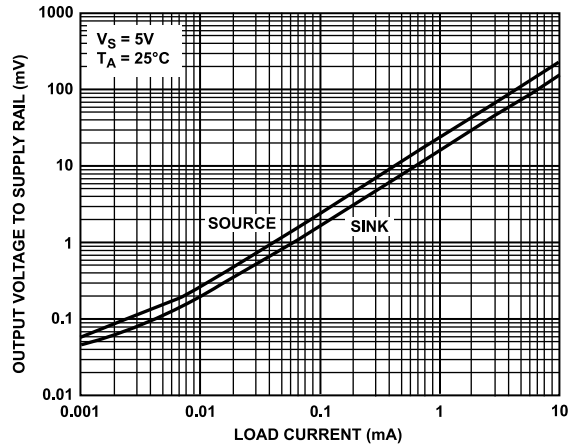


Figure 11. Output Voltage to Supply Rail vs. Load Current

TYPICAL PERFORMANCE CHARACTERISTICS

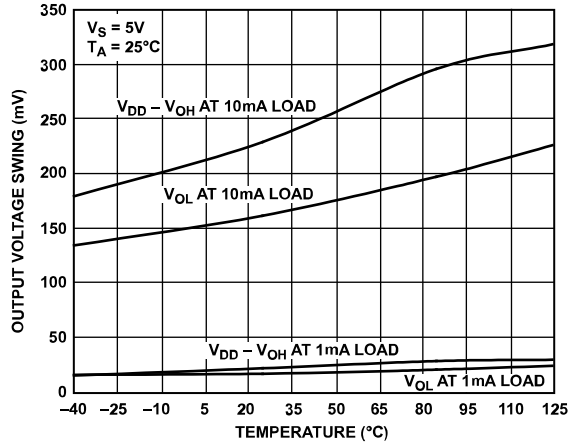


Figure 12. Output Voltage Swing vs. Temperature

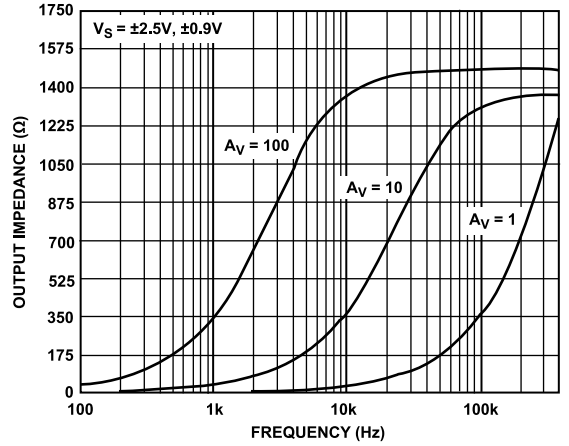


Figure 15. Output Impedance vs. Frequency

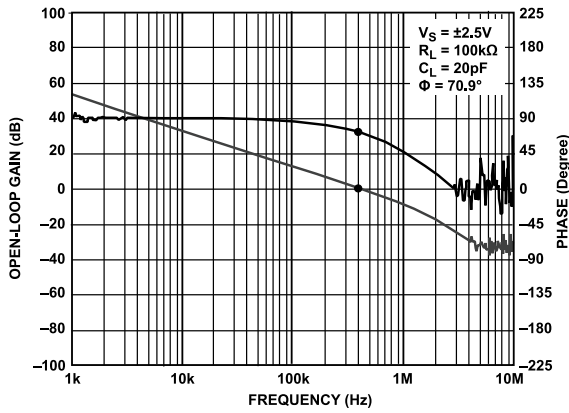


Figure 13. Open-Loop Gain and Phase vs. Frequency

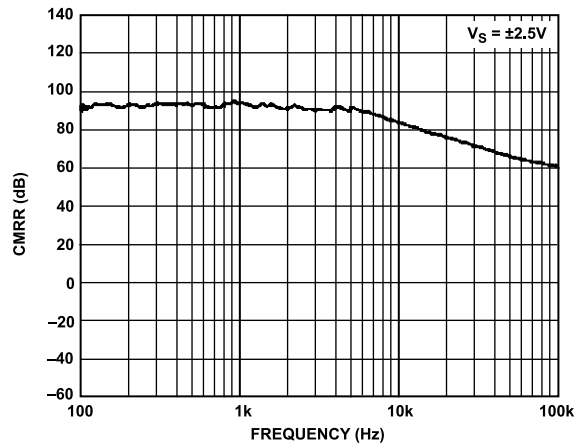


Figure 16. CMRR vs. Frequency

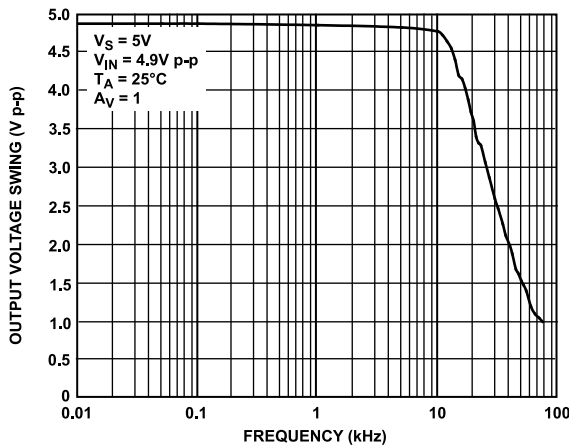


Figure 14. Closed-Loop Output Voltage Swing vs. Frequency

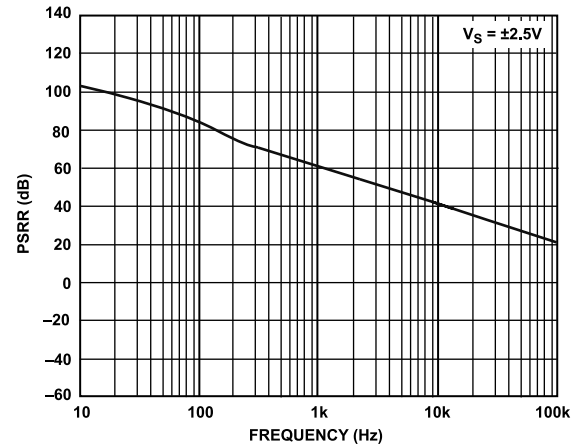


Figure 17. PSRR vs. Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

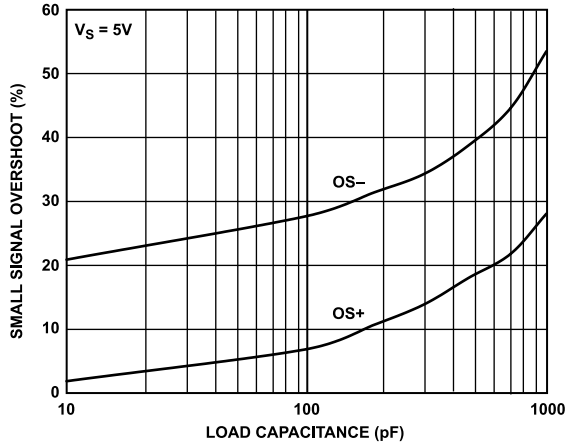


Figure 18. Small Signal Overshoot vs. Load Capacitance

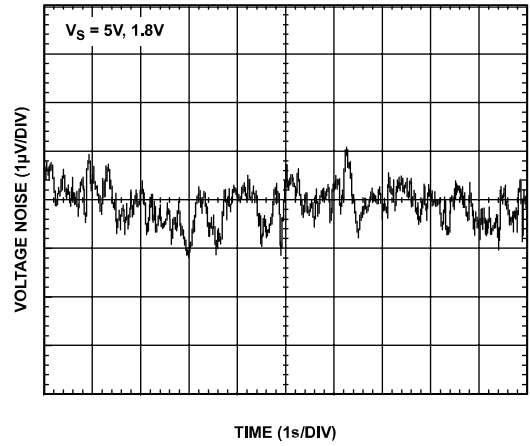


Figure 21. 0.1 Hz to 10 Hz Input Voltage Noise

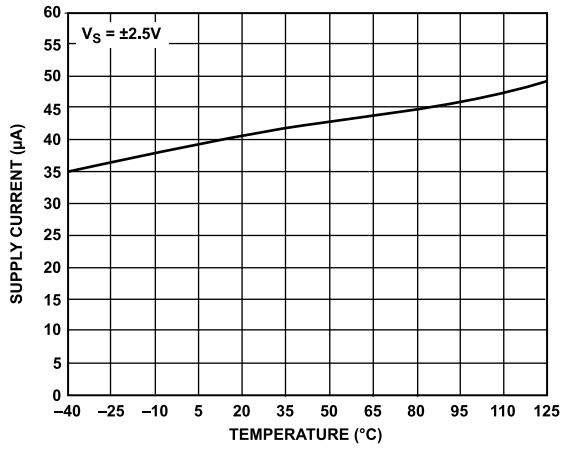


Figure 19. Supply Current vs. Temperature

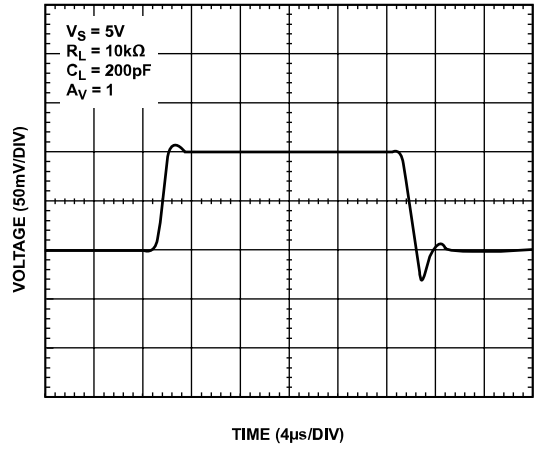


Figure 22. Small Signal Transient

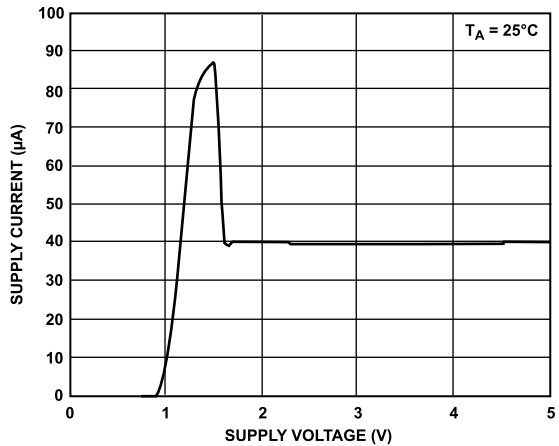


Figure 20. Supply Current vs. Supply Voltage

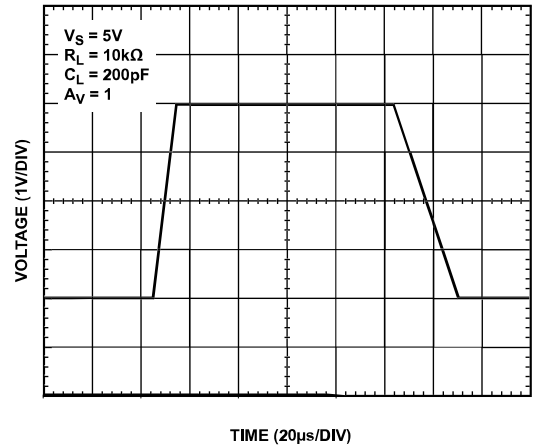


Figure 23. Large Signal Transient

TYPICAL PERFORMANCE CHARACTERISTICS

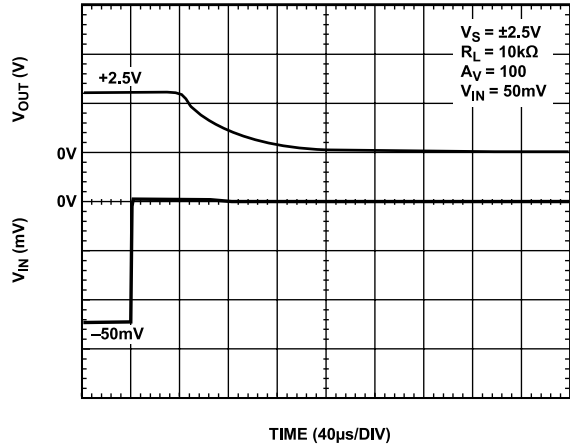


Figure 24. Negative Overload Recovery

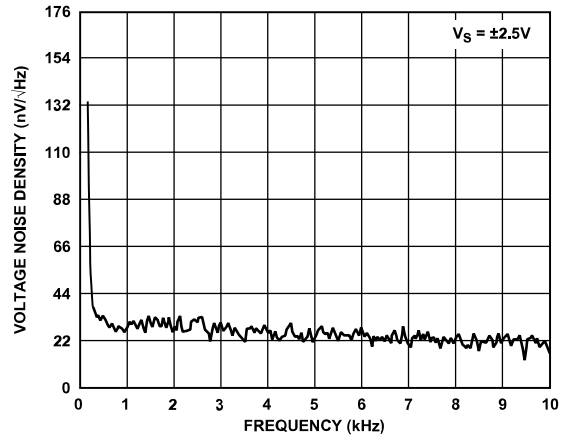


Figure 27. Voltage Noise Density vs. Frequency

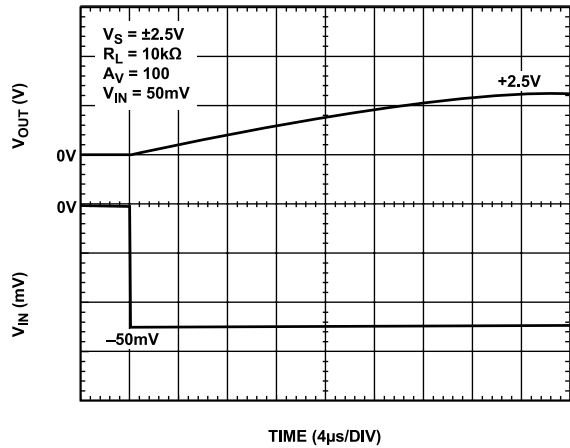


Figure 25. Positive Overload Recovery

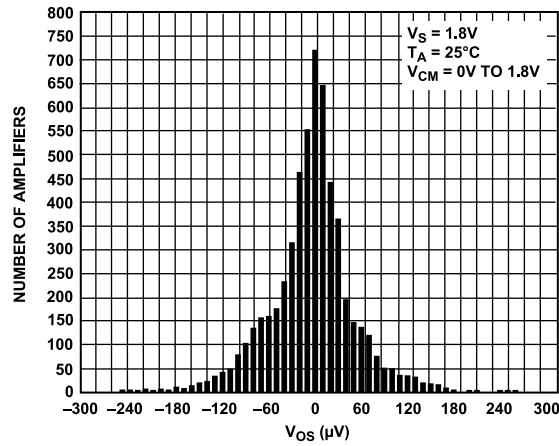


Figure 28.  $V_{OS}$  Distribution

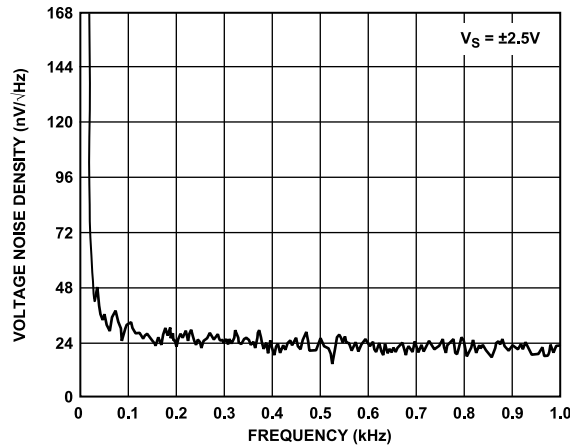


Figure 26. Voltage Noise Density vs. Frequency

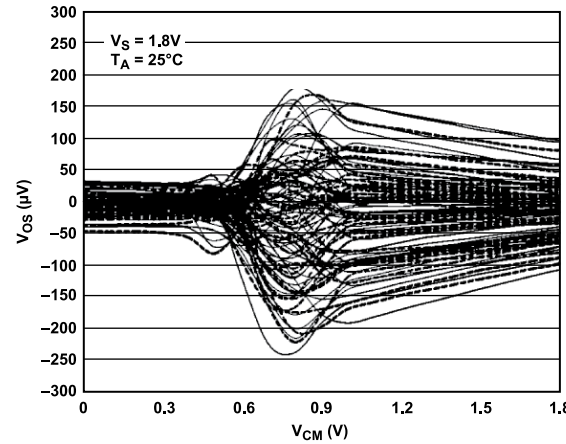


Figure 29. Input Offset Voltage vs. Common-Mode Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

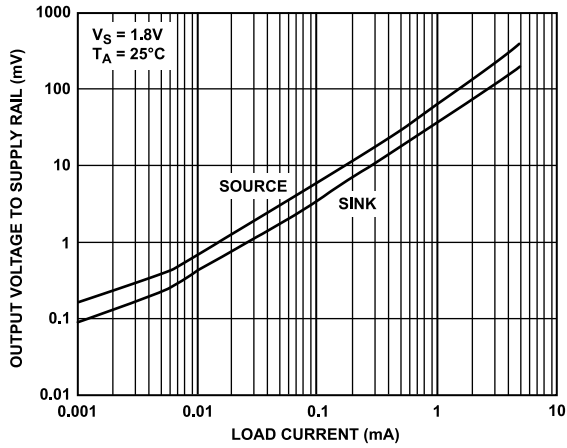


Figure 30. Output Voltage to Supply Rail vs. Load Current

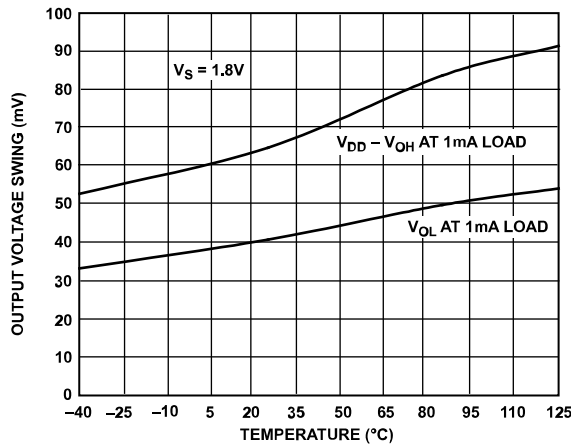


Figure 31. Output Voltage Swing vs. Temperature

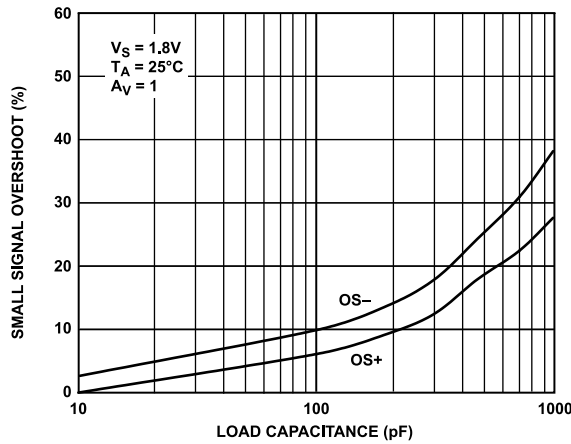


Figure 32. Small Signal Overshoot vs. Load Capacitance

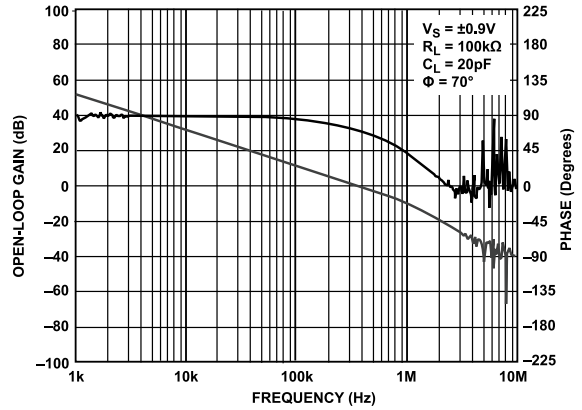


Figure 33. Open-Loop Gain and Phase vs. Frequency

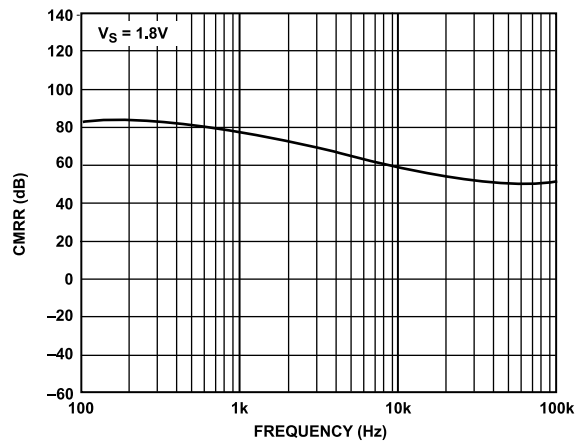


Figure 34. CMRR vs. Frequency

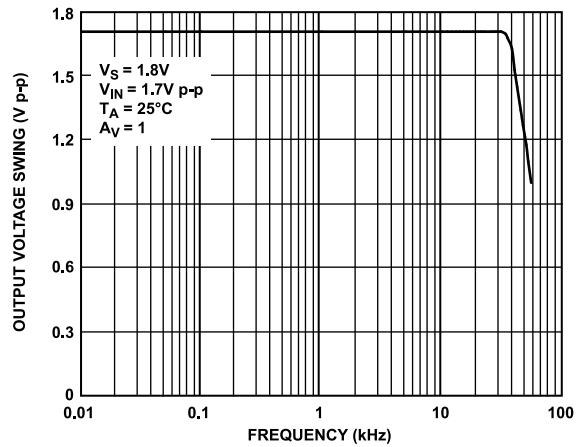


Figure 35. Closed-Loop Output Voltage Swing vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

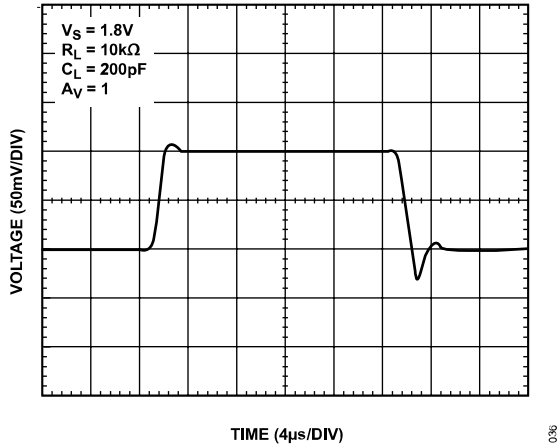


Figure 36. Small Signal Transient

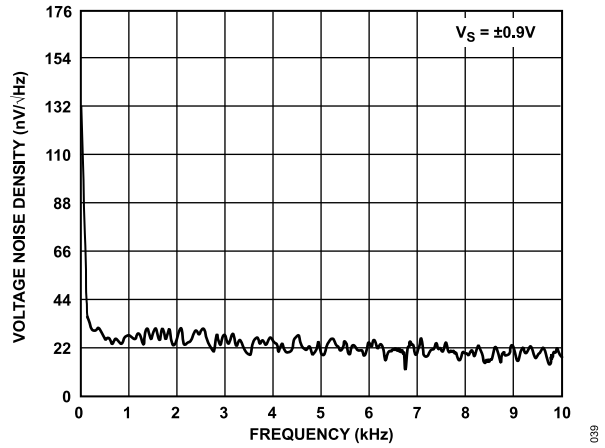


Figure 39. Voltage Noise Density vs. Frequency

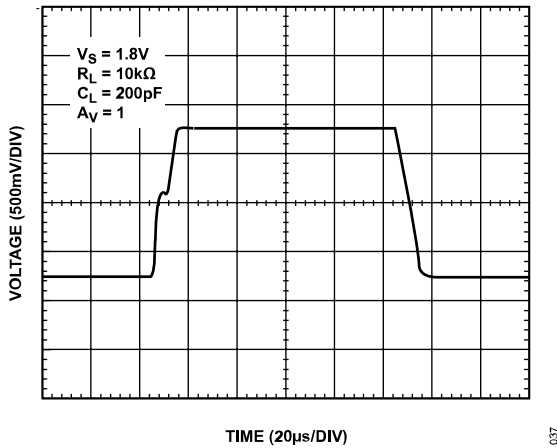


Figure 37. Large Signal Transient

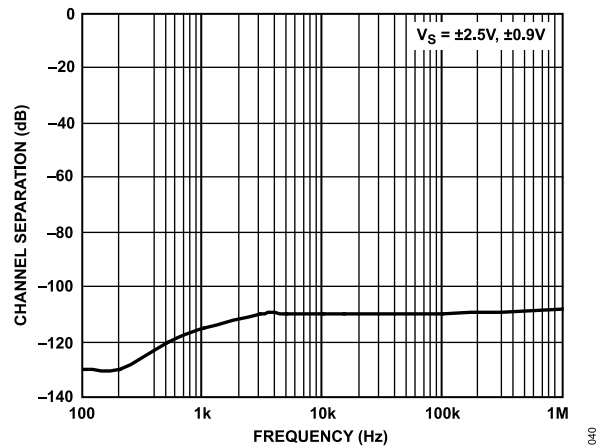


Figure 40. Channel Separation vs. Frequency

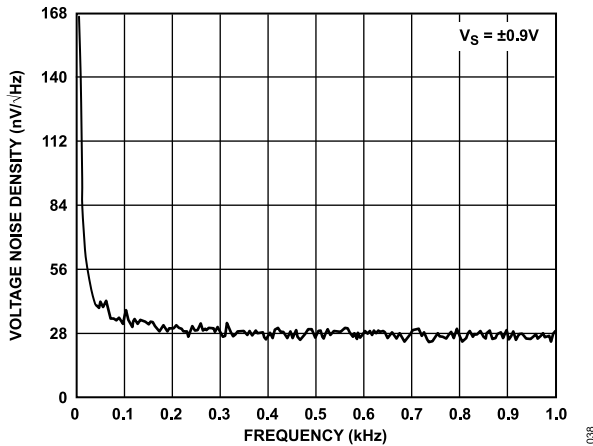


Figure 38. Voltage Noise Density vs. Frequency

## APPLICATIONS

## NO PHASE REVERSAL

The AD8603/AD8607/AD8609 do not exhibit phase inversion even when the input voltage exceeds the maximum input common-mode voltage. Phase reversal can cause permanent damage to the amplifier, resulting in system lockups. The AD8603/AD8607/AD8609 can handle voltages of up to 1 V over the supply.

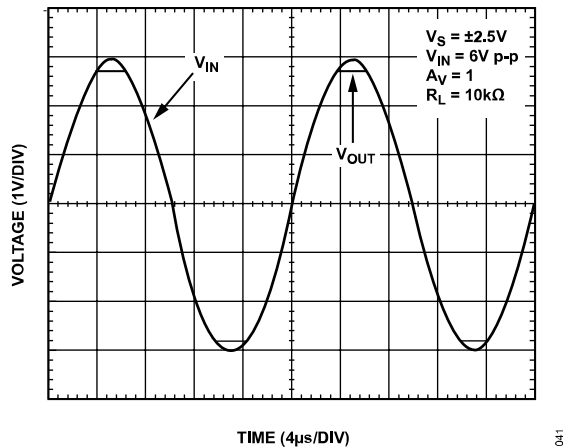


Figure 41. No Phase Response

## INPUT OVERVOLTAGE PROTECTION

If a voltage 1 V higher than the supplies is applied at either input, the use of a limiting series resistor is recommended. If both inputs are used, each one should be protected with a series resistor.

To ensure good protection, the current should be limited to a maximum of 5 mA. The value of the limiting resistor can be determined from the following equation:

$$(V_{IN} - V_S)/(R_S + 200 \Omega) \leq 5 \text{ mA} \quad (1)$$

## DRIVING CAPACITIVE LOADS

The AD8603/AD8607/AD8609 are capable of driving large capacitive loads without oscillating. Figure 42 shows the output of the AD8603/AD8607/AD8609 in response to a 100 mV input signal, with a 2 nF capacitive load.

Although it is configured in positive unity gain (the worst case), the AD8603 shows less than 20% overshoot. Simple additional circuitry can eliminate ringing and overshoot.

One technique is the snubber network, which consists of a series RC and a resistive load (see Figure 43). With the snubber in place, the AD8603/AD8607/AD8609 are capable of driving capacitive loads of 2 nF with no ringing and less than 3% overshoot.

The use of the snubber circuit is usually recommended for unity gain configurations. Higher gain configurations help improve the stability of the circuit. Figure 44 shows the same output response with the snubber in place.

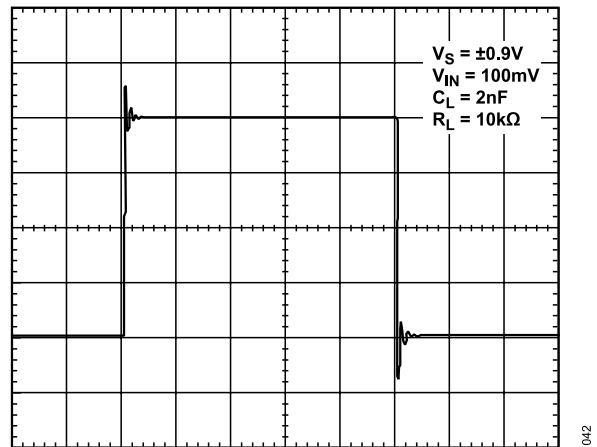


Figure 42. Output Response to a 2 nF Capacitive Load, Without Snubber

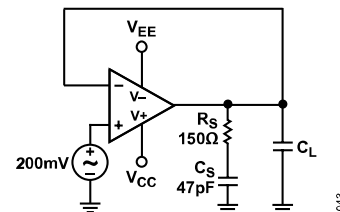


Figure 43. Snubber Network

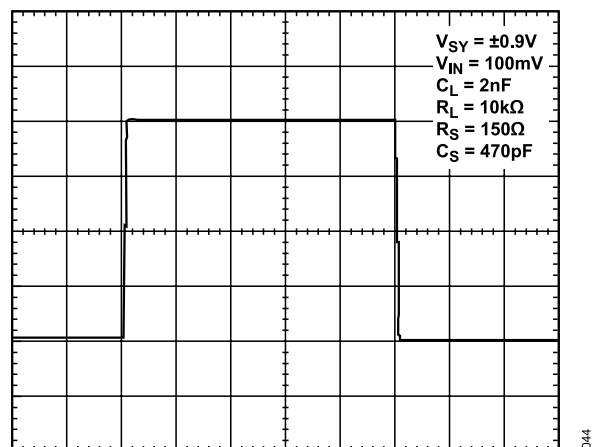


Figure 44. Output Response to a 2 nF Capacitive Load with Snubber

Optimum values for  $R_S$  and  $C_S$  are determined empirically; Table 5 lists a few starting values.

Table 5. Optimum Values for the Snubber Network

$C_L$ (pF)	$R_S$ ( $\Omega$ )	$C_S$ (pF)
100 to ~500	500	680
1500	100	330
1600 to ~2000	400	100

APPLICATIONS

PROXIMITY SENSORS

Proximity sensors can be capacitive or inductive and are used in a variety of applications. One of the most common applications is liquid level sensing in tanks. This is particularly popular in pharmaceutical environments where a tank must know when to stop filling or mixing a given liquid. In aerospace applications, these sensors detect the level of oxygen used to propel engines. Whether in a combustible environment or not, capacitive sensors generally use low voltage. The precision and low voltage of the AD8603/AD8607/AD8609 make the parts an excellent choice for such applications.

COMPOSITE AMPLIFIERS

A composite amplifier can provide a very high gain in applications where high closed-loop dc gains are needed. The high gain achieved by the composite amplifier comes at the expense of a loss in phase margin. Placing a small capacitor,  $C_F$ , in the feedback in parallel with  $R_2$  (see Figure 45) improves the phase margin. Picking  $C_F = 50$  pF yields a phase margin of about  $45^\circ$  for the values shown in Figure 45.

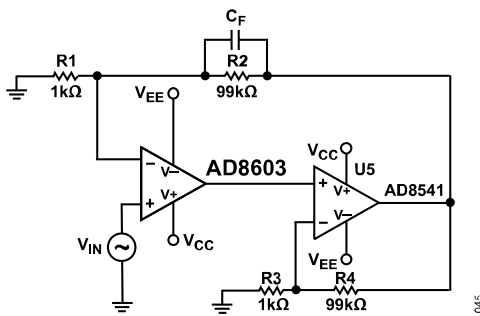


Figure 45. High Gain Composite Amplifier

A composite amplifier can be used to optimize dc and ac characteristics. Figure 46 shows an example using the AD8603 and the AD8541. This circuit offers many advantages. The band-width is increased substantially, and the input offset voltage and noise of the AD8541 become insignificant because they are divided by the high gain of the AD8603.

The circuit in Figure 46 offers high bandwidth (nearly double that of the AD8603), high output current, and very low power consumption of less than 100  $\mu$ A.

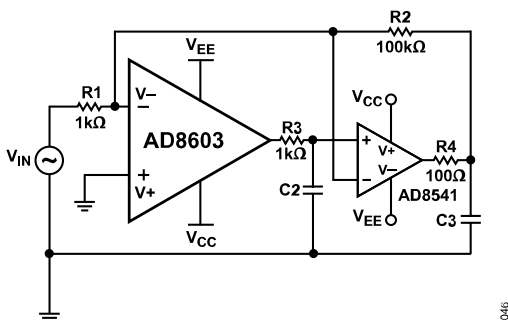


Figure 46. Low Power Composite Amplifier

BATTERY-POWERED APPLICATIONS

The AD8603/AD8607/AD8609 are ideal for battery-powered applications. The parts are tested at 5 V, 3.3 V, 2.7 V, and 1.8 V and are suitable for various applications whether in single or dual supply.

In addition to their low offset voltage and low input bias, the AD8603/AD8607/AD8609 have a very low supply current of 40  $\mu$ A, making the parts an excellent choice for portable electronics. The TSOT package allows the AD8603 to be used on smaller board spaces.

PHOTODIODES

Photodiodes have a wide range of applications from barcode scanners to precision light meters and CAT scanners. The very low noise and low input bias current of the AD8603/AD8607/AD8609 make the parts very attractive amplifiers for I-V conversion applications.

Figure 47 shows a simple photodiode circuit. The feedback capacitor helps the circuit maintain stability. The signal band-width can be increased at the expense of an increase in the total noise; a low-pass filter can be implemented by a simple RC network at the output to reduce the noise. The signal bandwidth can be calculated by  $\frac{1}{2\pi R_2 C_2}$ , and the closed-loop bandwidth is the intersection point of the open-loop gain and the noise gain.

The circuit shown in Figure 47 has a closed-loop bandwidth of 58 kHz and a signal bandwidth of 16 Hz. Increasing  $C_2$  to 50 pF yields a closed-loop bandwidth of 65 kHz, but only 3.2 Hz of signal bandwidth can be achieved.

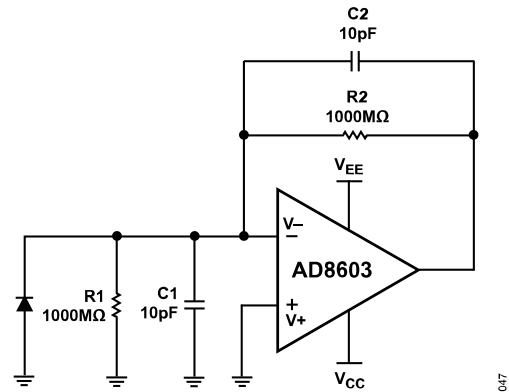
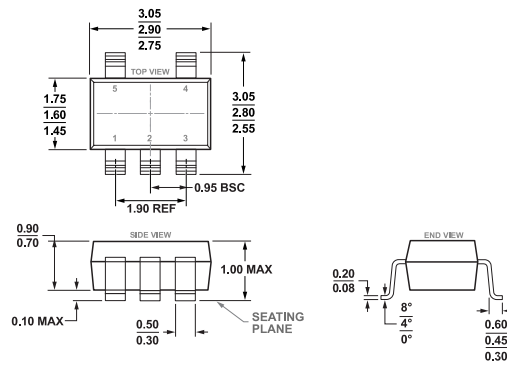


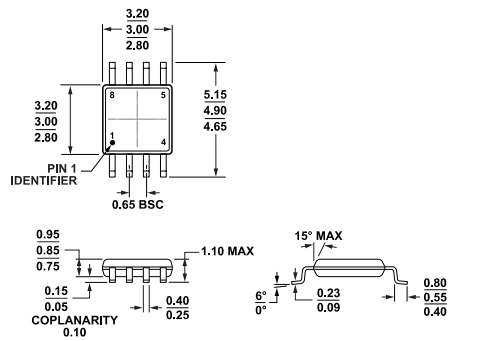
Figure 47. Photodiode Circuit

OUTLINE DIMENSIONS



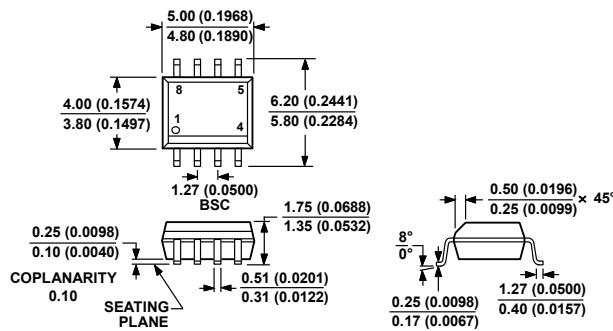
COMPLIANT TO JEDEC STANDARDS MO-193-AB

Figure 48. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)  
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

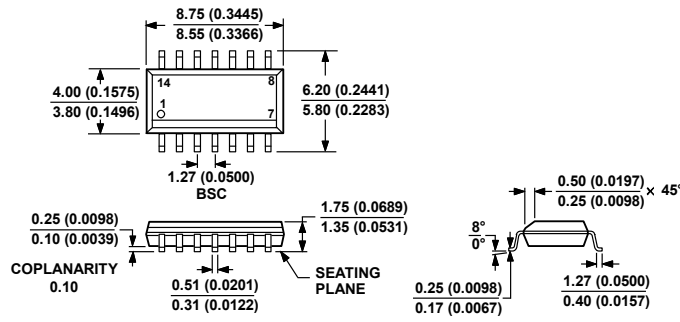
Figure 49. 8-Lead Mini Small Outline Package [MSOP] (RM-8)  
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 50. 8-Lead Standard Small Outline Package [SOIC\_N] (R-8)  
Dimensions shown in millimeters and (inches)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 51. 14-Lead Standard Small Outline Package [SOIC\_N] (R-14)  
 Dimensions shown in millimeters and (inches)

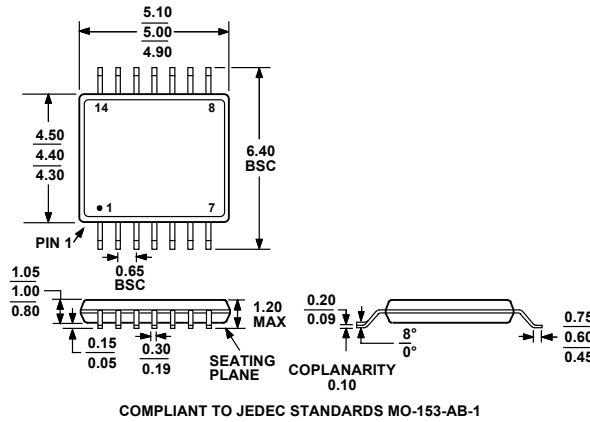


Figure 52. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)  
 Dimensions shown in millimeters

Updated: October 10, 2023

ORDERING GUIDE

Table 6. Ordering Guide

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
AD8603AUJZ-R2	-40°C to +125°C	5-Lead TSOT	Reel, 250	UJ-5	A0X
AD8603AUJZ-REEL	-40°C to +125°C	5-Lead TSOT	Reel, 10000	UJ-5	A0X
AD8603AUJZ-REEL7	-40°C to +125°C	5-Lead TSOT	Reel, 3000	UJ-5	A0X
AD8607ARMZ	-40°C to +125°C	8-Lead MSOP		RM-8	A0G
AD8607ARMZ-REEL	-40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A0G
AD8607ARZ	-40°C to +125°C	8-Lead SOIC		R-8	
AD8607ARZ-REEL	-40°C to +125°C	8-Lead SOIC	Reel, 2500	R-8	
AD8607ARZ-REEL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8	
AD8609ARUZ	-40°C to +125°C	14-Lead TSSOP		RU-14	
AD8609ARUZ-REEL	-40°C to +125°C	14-Lead TSSOP	Reel, 2500	RU-14	