

FEATURES

- Low supply current: 250 μ A max**
- Very low input bias current: 1 pA max**
- Low offset voltage: 750 μ V max**
- Single-supply operation: 5 V to 26 V**
- Dual-supply operation: ± 2.5 V to ± 13 V**
- Rail-to-rail output**
- Unity-gain stable**
- No phase reversal**
- SC70 package**

APPLICATIONS

- Line-/battery-powered instruments**
- Photodiode amplifiers**
- Precision current sensing**
- Medical instrumentation**
- Industrial controls**
- Precision filters**
- Portable audio**
- ATE**

GENERAL DESCRIPTION

The [AD8641/AD8642/AD8643](#) are low power, precision JFET input amplifiers featuring extremely low input bias current and rail-to-rail output. The ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables designers to buffer complementary metal-oxide semiconductor digital-to-analog converters (CMOS DACs), ASICs, and other wide output swing devices in single-supply systems. The outputs remain stable with capacitive loads of more than 500 pF.

The [AD8641/AD8642/AD8643](#) are suitable for applications utilizing multichannel boards that require low power to manage heat. Other applications include photodiodes, ATE reference level drivers, battery management, and industrial controls.

The [AD8641/AD8642/AD8643](#) are fully specified over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$. The [AD8641](#) is available in 5-lead SC70 and 8-lead SOIC lead-free packages. The [AD8642](#) is available in 8-lead MSOP and 8-lead SOIC lead-free packages. The [AD8643](#) is available in 14-lead SOIC and 16-lead, 3 mm \times 3 mm, LFCSP lead-free packages.

PIN CONFIGURATIONS

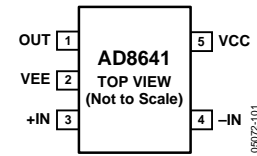
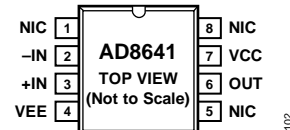


Figure 1. 5-Lead SC70 (KS-5)



NIC = NO INTERNAL CONNECTION.

Figure 2. 8-Lead SOIC (R-8)



Figure 3. 8-Lead SOIC (R-8)

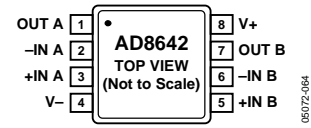


Figure 4. 8-Lead MSOP (RM-8)

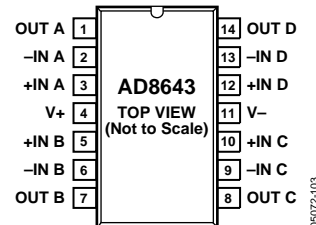
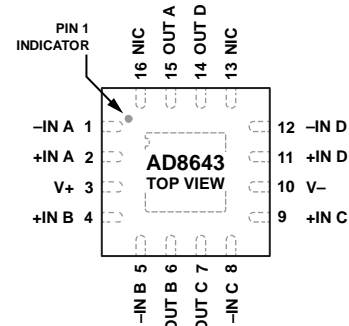


Figure 5. 14-Lead SOIC (R-14)



NOTES

1. NIC = NO INTERNAL CONNECTION.
2. EXPOSED PAD SHOULD BE CONNECTED TO V+.

Figure 6. 16-Lead LFCSP (CP-16-27) (Not Drawn to Scale)

Rev. F

[Document Feedback](#)

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REVISION HISTORY

4/16—Rev. E to Rev. F

Changed CP-16-3 to CP-16-27	Throughout
Changes to Figure 2 and Figure 6	1
Updated Outline Dimensions	13
Changes to Ordering Guide	14

9/11—Rev. D to Rev. E

Changes to Thermal Resistance Section	5
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7/11—Rev. C to Rev. D

Changes to Figure 6	1
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11/10—Rev. B to Rev. C

Changes to Figure 6	1
Added Thermal Resistance Section and Table 4	5
Updated Outline Dimensions	13
Changes to Ordering Guide	15

4/05—Rev. A to Rev. B

Added AD8643	Universal
Added 14-Lead SOIC	Universal
Added 16-Lead LFCSP	Universal
Updated Outline Dimensions	13
Changes to Ordering Guide	14

Absolute Maximum Ratings	5
Thermal Resistance	5
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Outline Dimensions	13
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3/05—Rev. 0 to Rev. A

Added AD8642	Universal
Changes to General Description	1
Added Figure 3 and Figure 4	1
Changes to Specifications	3
Changes to Absolute Maximum Ratings	5
Changes to Figure 22	8
Changes to Figure 23	9
Changes to Figure 41	12
Updated Outline Dimensions	13
Changes to Ordering Guide	14

10/04—Initial Version: Revision 0

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	AD8643 LFCSP only $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $+85^\circ\text{C} < T_A < +125^\circ\text{C}$, $V_{CM} = 1.5\text{ V}$		50	750	μV
					1	mV
					1.5	mV
					1.6	mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	1	μA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			180	μA
					0.5	μA
					60	μA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.5\text{ V}$	74	93		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.5\text{ to } 4.5\text{ V}$	80	140		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2.5		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$, $-40^\circ\text{C to } +125^\circ\text{C}$	4.95			V
			4.94			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$, $-40^\circ\text{C to } +125^\circ\text{C}$			0.05	V
Output Current	I_{OUT}			0.01	0.05	V
				± 6		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to } 26\text{ V}$	90	107		dB
Supply Current/Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		195	250	μA
					270	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR			2		V/ μs
Gain Bandwidth Product	GBP	AD8641 , AD8642 AD8643		3		MHz
				2.5		MHz
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	$f = 0.1\text{ Hz to } 10\text{ Hz}$		4.0		$\mu\text{V p-p}$
Voltage Noise Density	e_N	$f = 1\text{ kHz}$		28.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1\text{ kHz}$		0.5		fA/ $\sqrt{\text{Hz}}$

$V_S = \pm 13\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	AD8643 LFCSP only $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		70	750	μV mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			260	pA
Input Voltage Range			-13		65	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13\text{ V to }+10\text{ V}$	90	107	+10	dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = -11\text{ V to }+11\text{ V}$	215	290		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2.5		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$, $-40^\circ\text{C to }+125^\circ\text{C}$	+12.95			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$, $-40^\circ\text{C to }+125^\circ\text{C}$	+12.94		-12.95	V
Output Current	I_{OUT}			± 12	-12.94	V mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V to } \pm 13\text{ V}$	90	107		dB
Supply Current/Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		200	290	μA
					330	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR			3		V/ μs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	ϕ_m			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	$f = 0.1\text{ Hz to }10\text{ Hz}$		4.2		$\mu\text{V p-p}$
Voltage Noise Density	e_N	$f = 1\text{ kHz}$		27.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1\text{ kHz}$		0.5		fA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	27.3 V
Input Voltage	VS– to VS+
Differential Input Voltage	±Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
KS-5, R-8, RM-8, R-14, CP-16 Packages	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	
KS-5, R-8, RM-8, R-14, CP-16 Packages	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board. For the LFCSP, solder the exposed pad to a copper plane, which should be connected to V+.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS)	430	149	°C/W
8-Lead SOIC (R)	121	43	°C/W
8-Lead MSOP (RM)	142	45	°C/W
14-Lead SOIC (R)	110	36	°C/W
16-Lead LFCSP (CP)	81	16	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

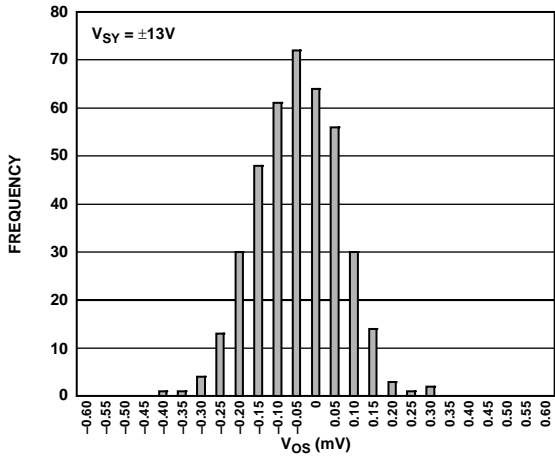


Figure 7. Input Offset Voltage

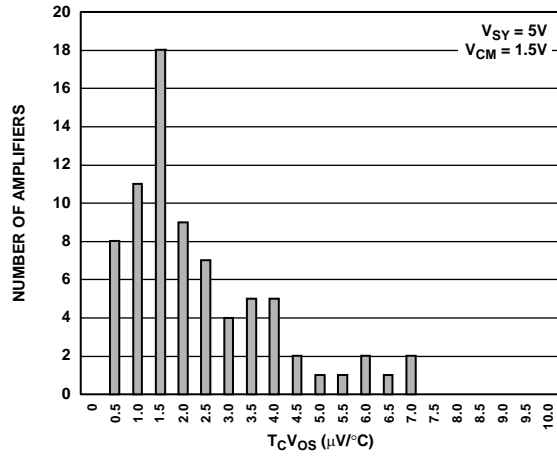


Figure 10. Offset Voltage Drift

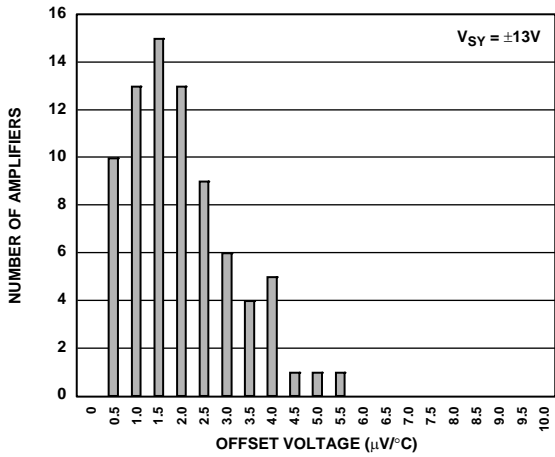


Figure 8. Offset Voltage Drift

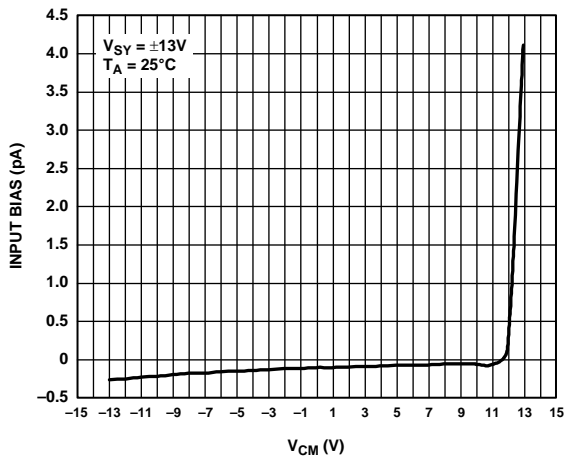


Figure 11. Input Bias Current vs. V_{CM}

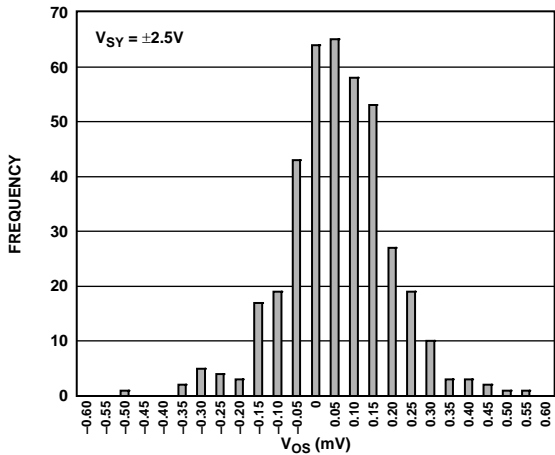


Figure 9. Input Offset Voltage

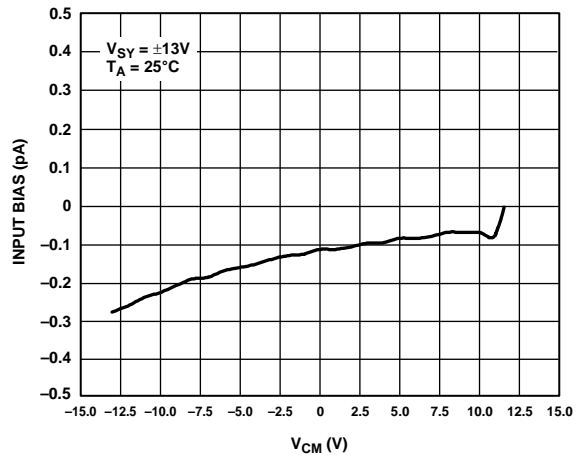


Figure 12. Input Bias Current vs. V_{CM}

05072-002

05072-005

05072-003

05072-006

05072-004

05072-007

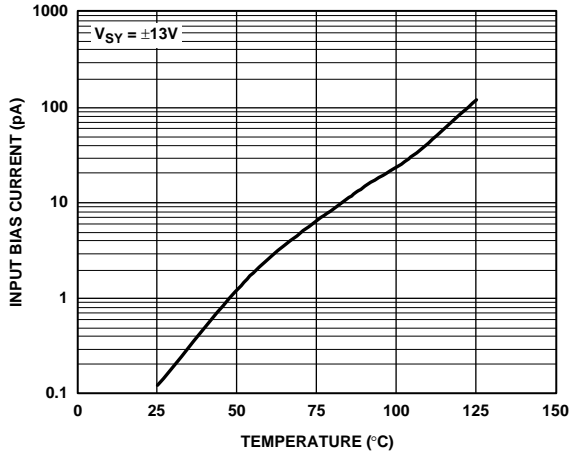


Figure 13. Input Bias Current vs. Temperature

05072-008

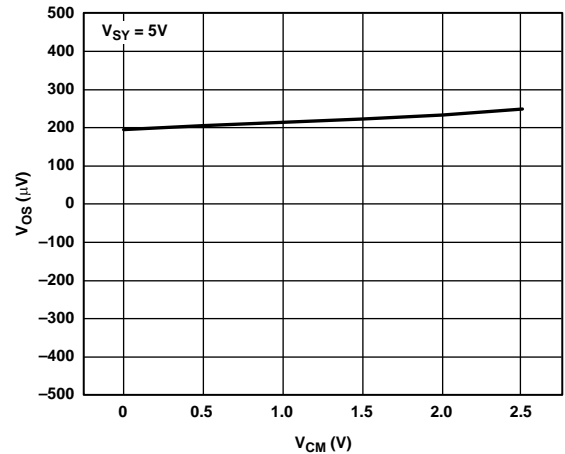


Figure 16. Input Offset Voltage vs. V_{CM}

05072-011

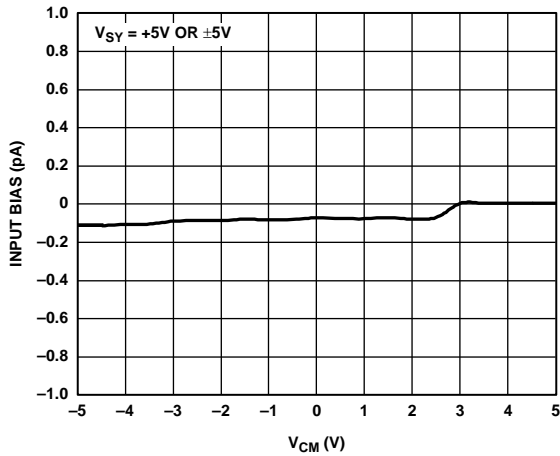


Figure 14. Input Bias Current vs. V_{CM}

05072-009

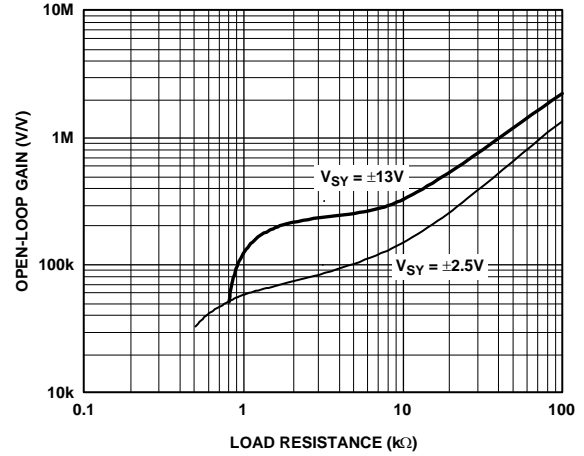


Figure 17. Open-Loop Gain vs. Load Resistance

05072-012

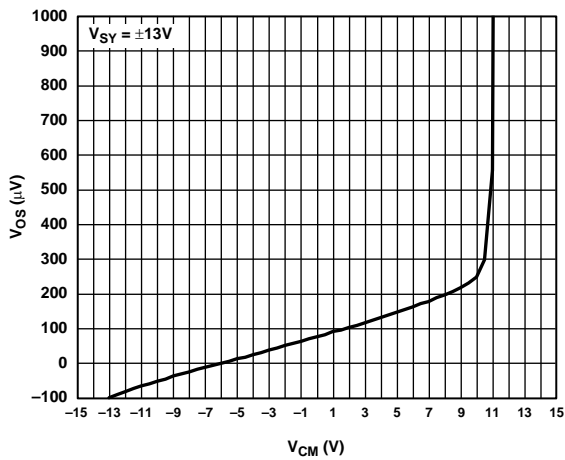


Figure 15. Input Offset Voltage vs. V_{CM}

05072-010

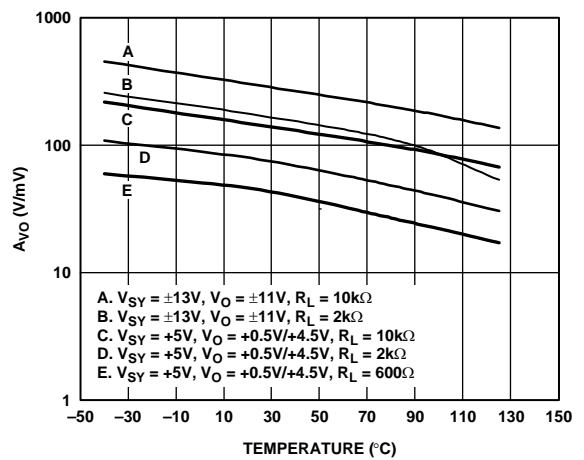
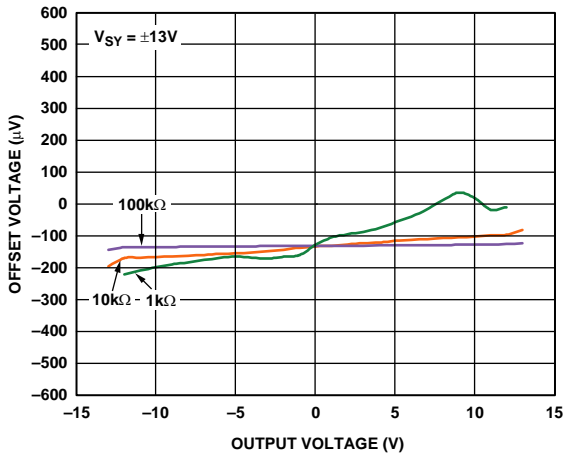


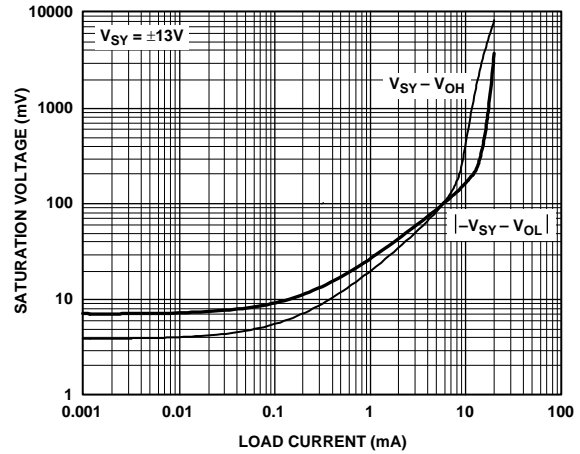
Figure 18. Open-Loop Gain vs. Temperature

05072-013



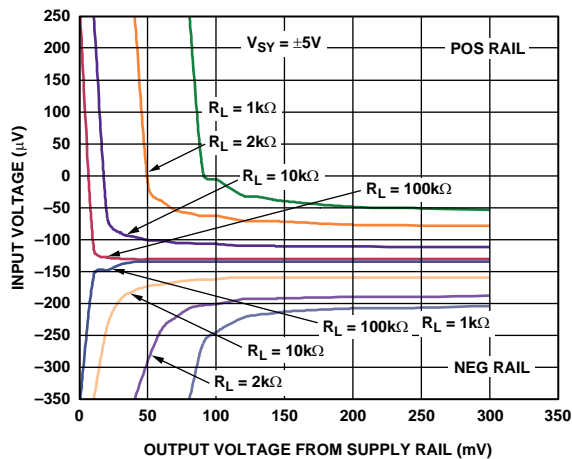
06072-014

Figure 19. Input Error Voltage vs. Output Voltage for Resistive Loads



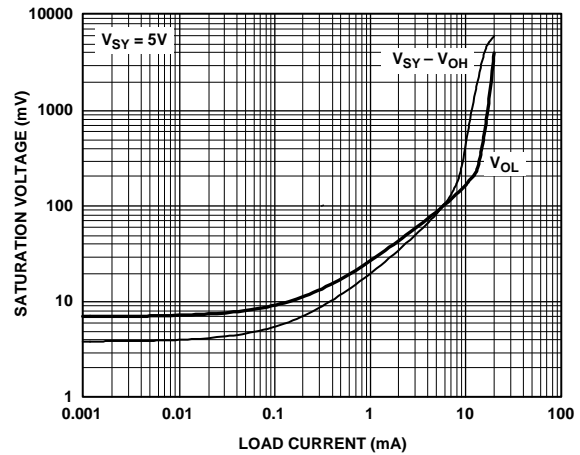
06072-017

Figure 22. Output Saturation Voltage vs. Load Current



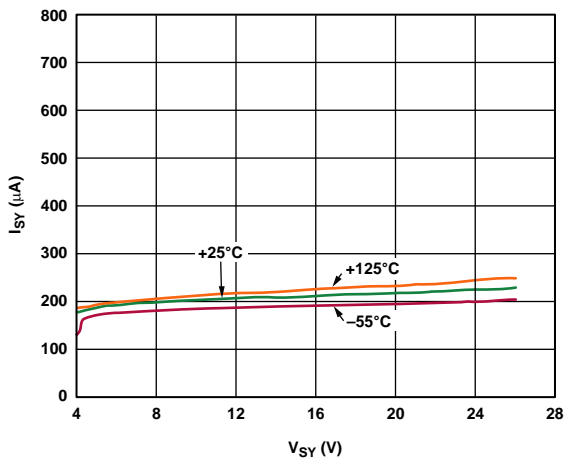
06072-015

Figure 20. Input Error Voltage vs. Output Voltage Within 300 mV of Supply Rails



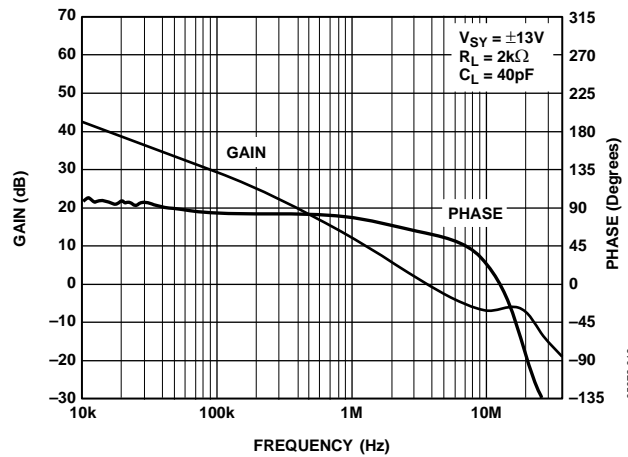
06072-018

Figure 23. Output Saturation Voltage vs. Load Current



06072-016

Figure 21. Quiescent Current vs. Supply Voltage at Different Temperatures



06072-019

Figure 24. Open-Loop Gain and Phase Margin vs. Frequency

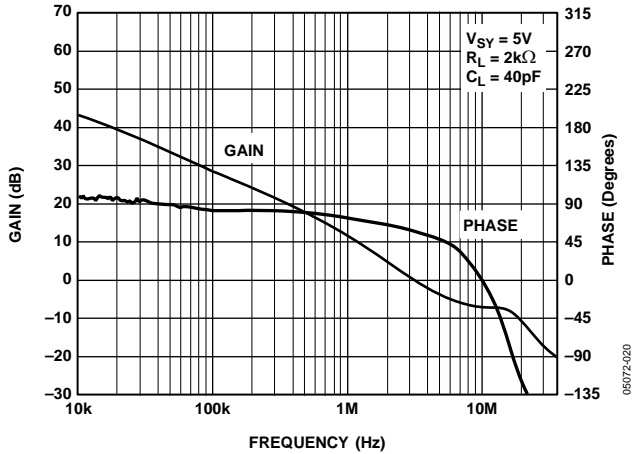


Figure 25. Open-Loop Gain and Phase Margin vs. Frequency

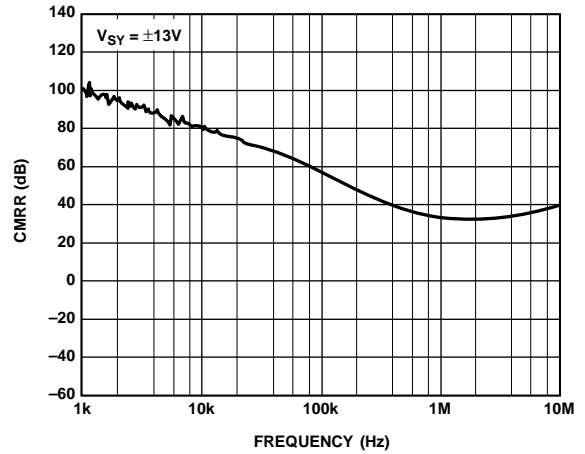


Figure 28. CMRR vs. Frequency

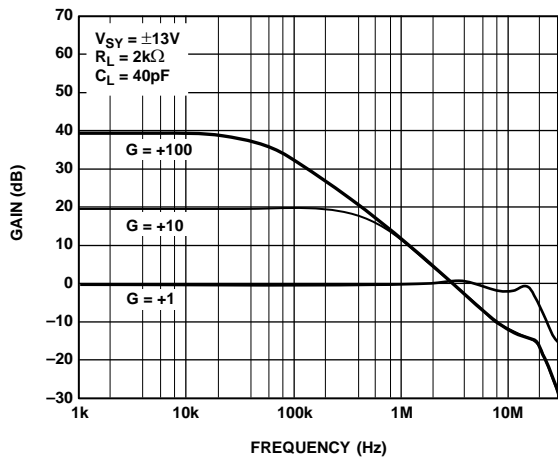


Figure 26. Closed-Loop Gain vs. Frequency

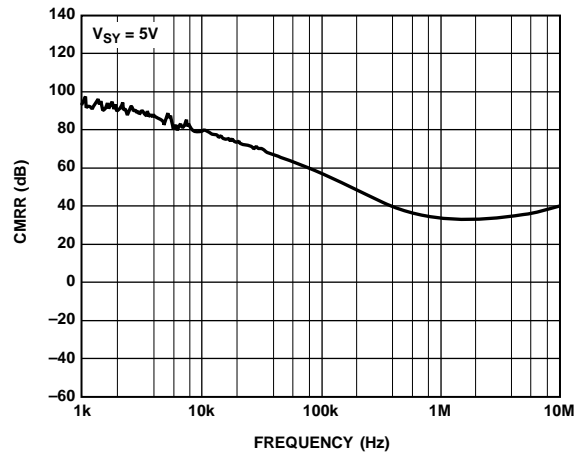


Figure 29. CMRR vs. Frequency

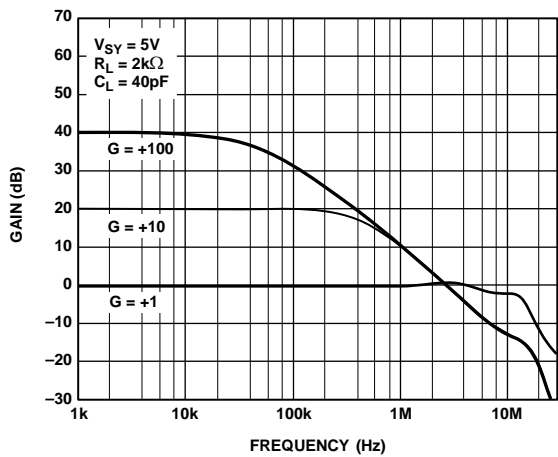


Figure 27. Closed-Loop Gain vs. Frequency

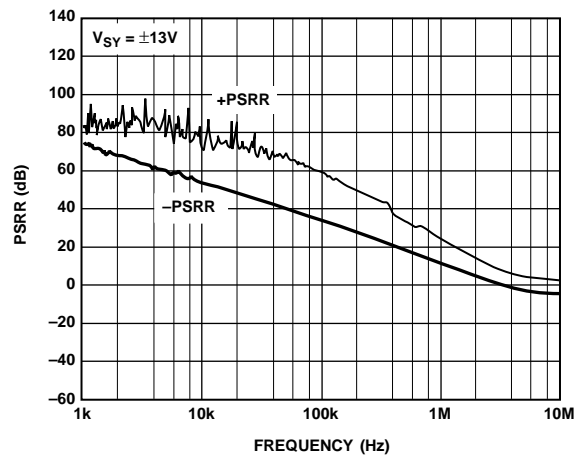


Figure 30. PSRR vs. Frequency

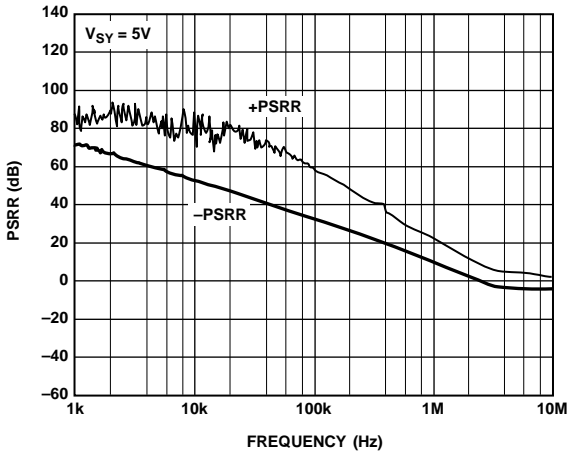


Figure 31. PSRR vs. Frequency

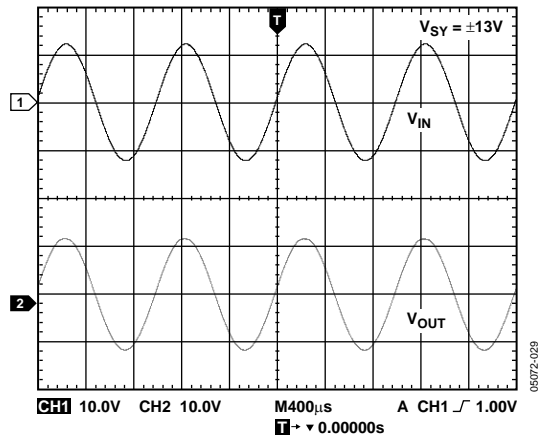


Figure 34. No Phase Reversal

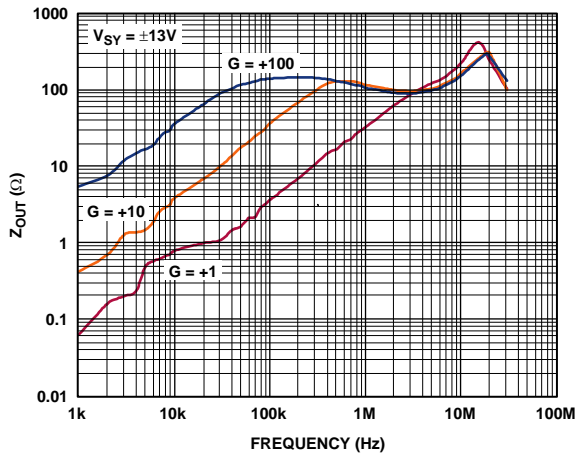


Figure 32. Output Impedance vs. Frequency

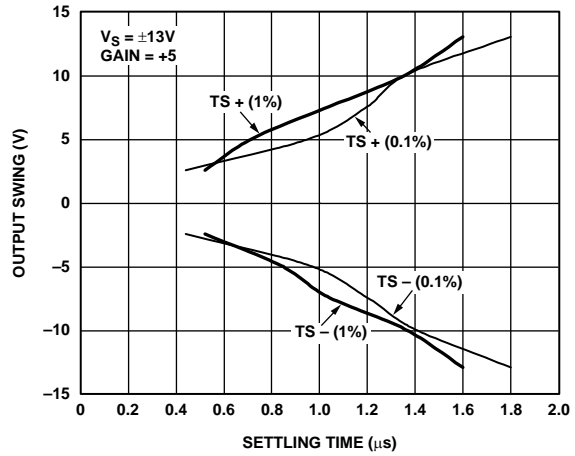


Figure 35. Output Swing and Error vs. Settling Time

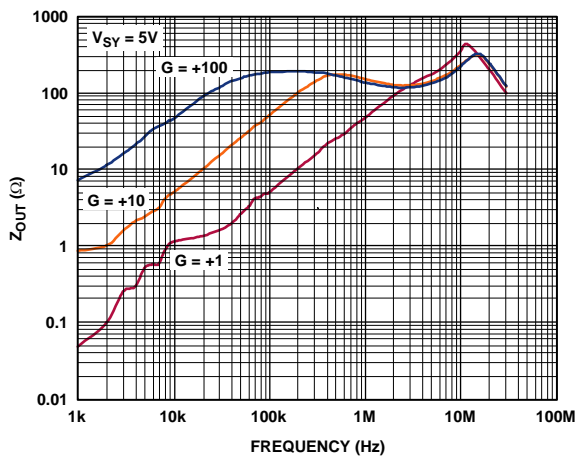


Figure 33. Output Impedance vs. Frequency

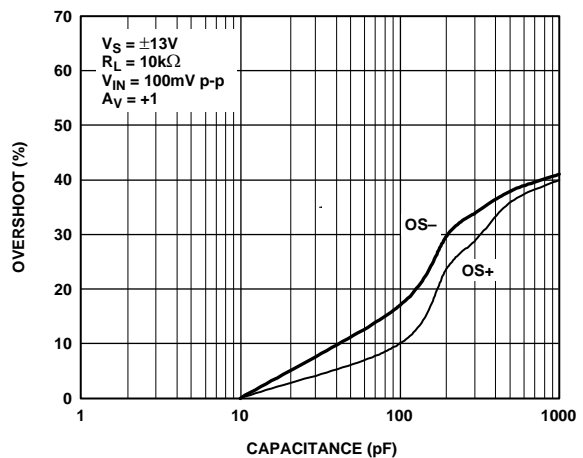


Figure 36. Small Signal Overshoot vs. Load Capacitance

05072-026

05072-029

05072-027

05072-030

05072-028

05072-031

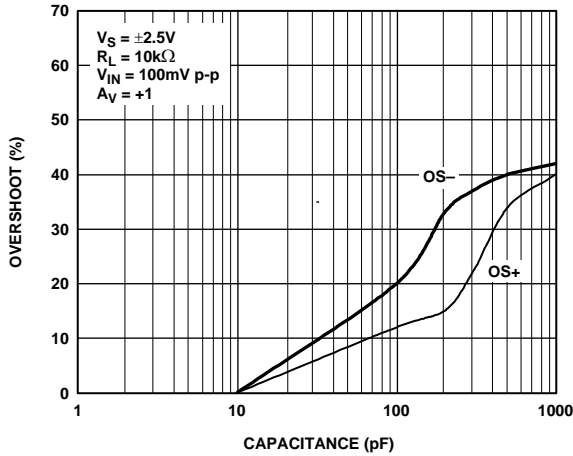


Figure 37. Small Signal Overshoot vs. Load Capacitance

06072-032

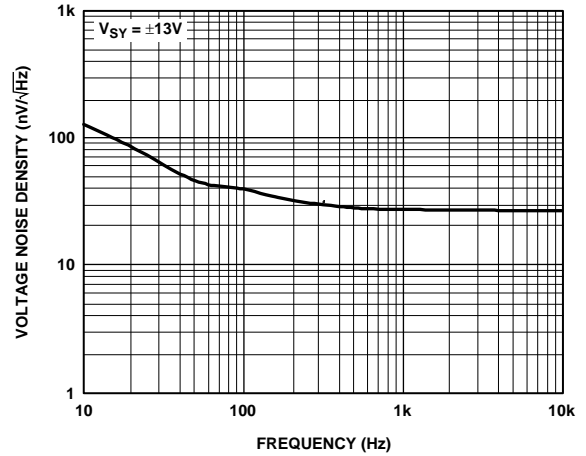


Figure 40. Voltage Noise Density

06072-036

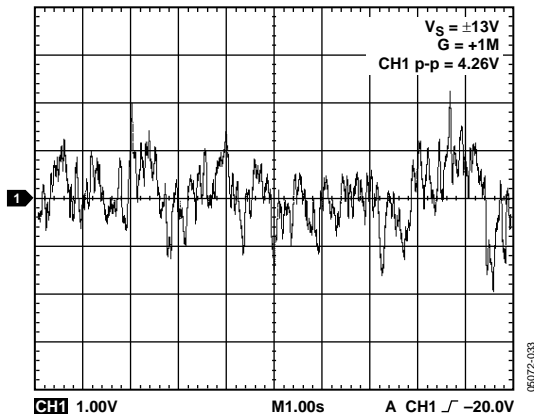


Figure 38. 0.1 Hz to 10 Hz Noise

06072-033

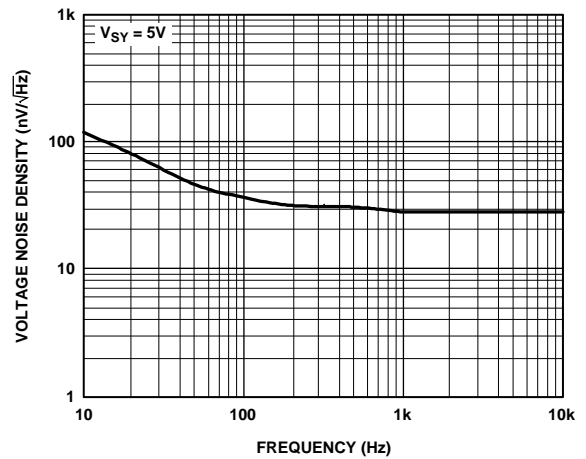


Figure 41. Voltage Noise Density

06072-036

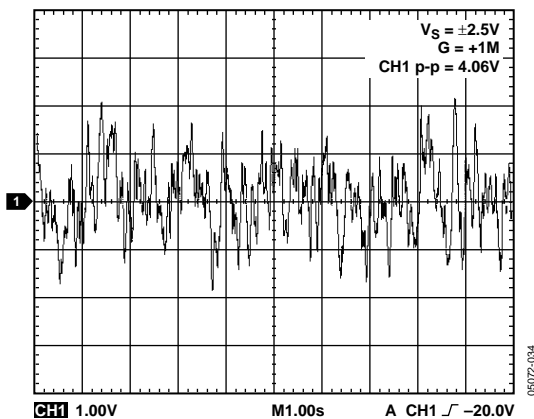


Figure 39. 0.1 Hz to 10 Hz Noise

06072-034

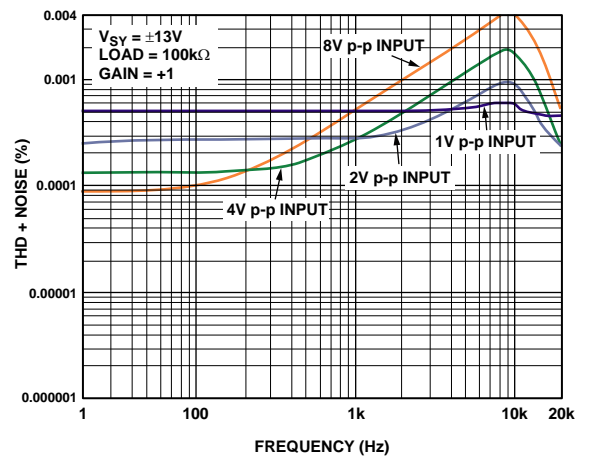


Figure 42. Total Harmonic Distortion + Noise vs. Frequency

06072-037

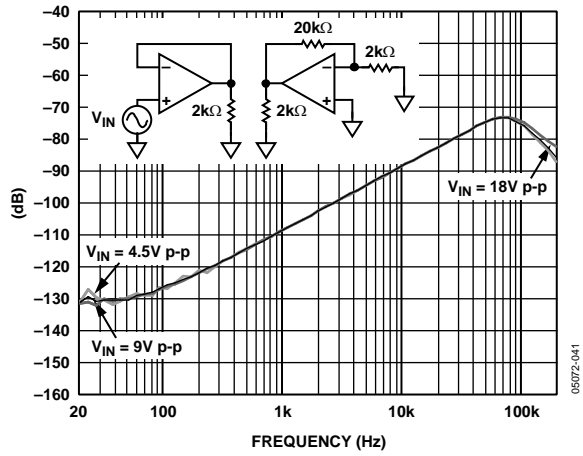
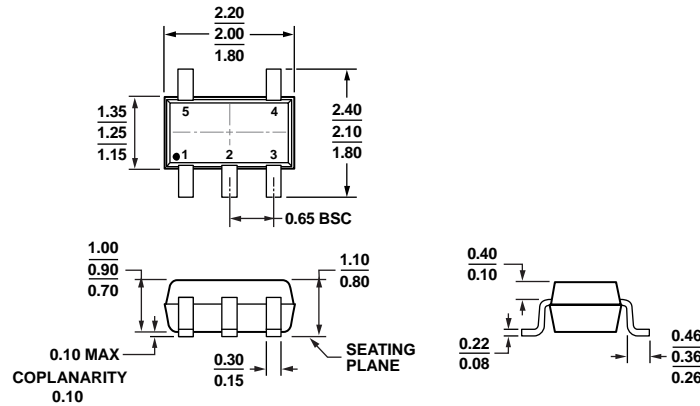


Figure 43. Channel Separation

05072-041

OUTLINE DIMENSIONS

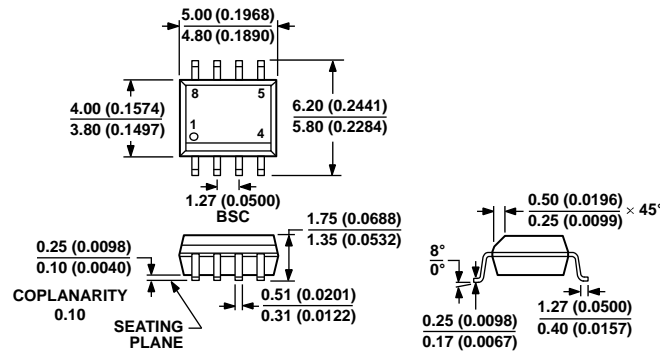


COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 44. 5-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-5)

Dimensions shown in millimeters

072009-A



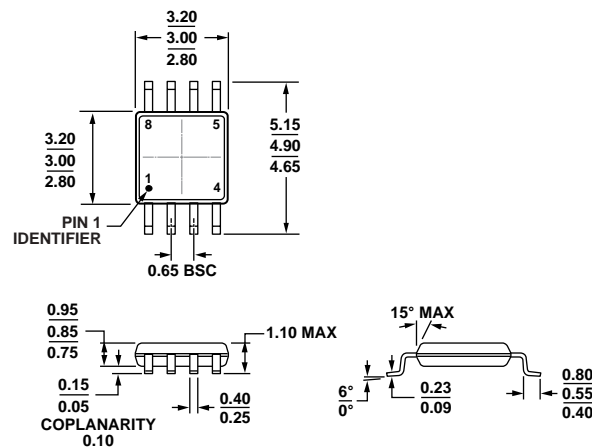
COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N] (R-8)

Dimensions shown in millimeters and (inches)

012407-A

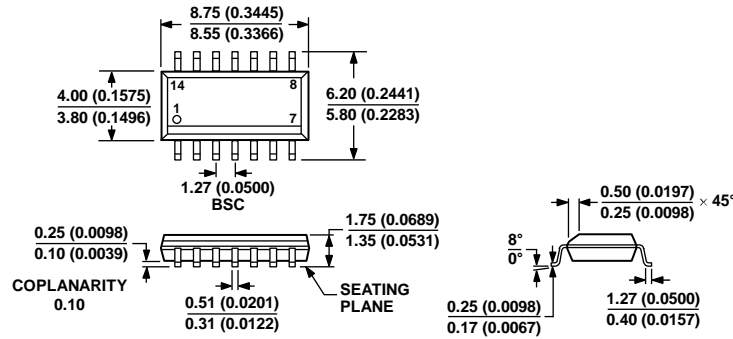


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 46. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

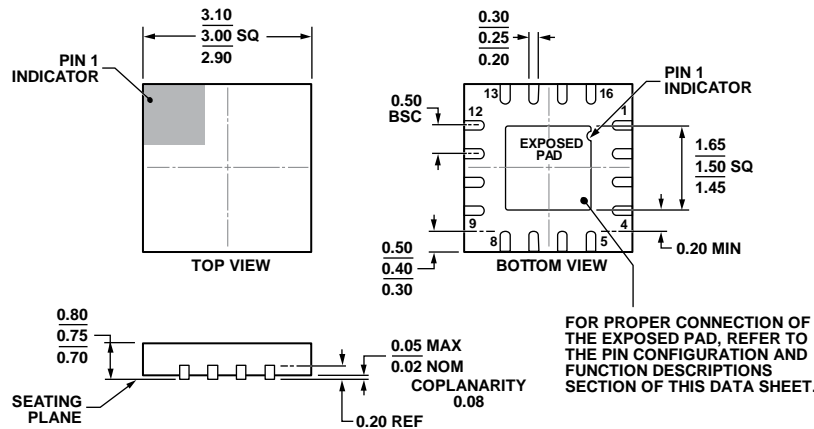
10-07-2009-B



COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 47. 14-Lead Standard Small Outline Package [SOIC_N]
 (R-14)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP]
 3 mm × 3 mm Body and 0.75 mm Package Height
 (CP-16-27)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8641AKSZ-R2	-40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	A07
AD8641AKSZ-REEL7	-40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	A07
AD8641ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8641ARZ-REEL7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8642ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A0A
AD8642ARMZ-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A0A
AD8642ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8642ARZ-REEL7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8642ARZ-REEL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8643ARZ	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8643ARZ-REEL7	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8643ACPZ-R2	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-27	AUA
AD8643ACPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-27	AUA

¹ Z = RoHS Compliant Part.