

## FEATURES

- Low offset voltage: 175  $\mu$ V maximum @  $V_{SY} = 5$  V
- Low supply current: 275  $\mu$ A maximum per amplifier
- Single-supply operation: 5 V to 16 V
- Low noise: 23 nV/ $\sqrt{\text{Hz}}$
- Low input bias current: 300 fA
- Unity-gain stable
- Small packages available
  - 3 mm  $\times$  3 mm, 8-lead LFCSP
  - 8-lead MSOP
- Other packages
  - 8-lead SOIC
  - 14-lead SOIC
  - 14-lead TSSOP

## APPLICATIONS

- Sensor front ends
- Transimpedance amplifiers
- Electrometer applications
- Photodiode amplification
- Low power ADC drivers
- Medical diagnostic instruments
- pH and ORP meters and probes
- DAC or REF buffers

## GENERAL DESCRIPTION

The [AD8663/AD8667/AD8669](#) are rail-to-rail output amplifiers that use the Analog Devices, Inc., patented DigiTrim<sup>®</sup> trimming technique to achieve low offset voltage. The [AD8663/AD8667/AD8669](#) feature an extended operating range with supply voltages up to 16 V. They also feature low input bias current, low input offset voltage, and low current noise.

The combination of low offset, very low input bias current, and a wide supply range makes these amplifiers useful in a wide variety of applications usually associated with higher priced JFET amplifiers. Systems using high impedance sensors, such as photodiodes, benefit from the combination of low input bias current, low noise, low offset, and wide bandwidth.

The ability to operate the device for single (5 V to 16 V) or dual supplies ( $\pm 2.5$  V to  $\pm 8$  V) supports many applications. The rail-to-rail outputs provide increased dynamic range to drive low

## PIN CONFIGURATIONS

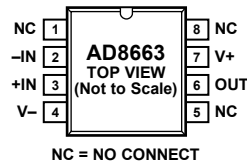


Figure 1. 8-Lead SOIC (R-8)

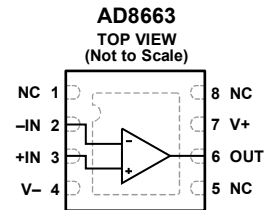
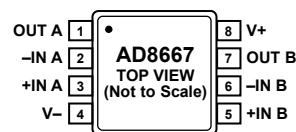
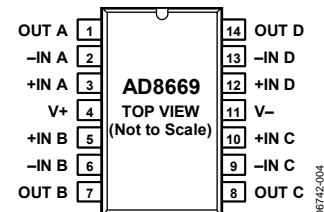


Figure 2. 8-Lead LFCSP (CP-8-13)


 Figure 3. 8-Lead MSOP (RM-8),  
8-Lead SOIC (R-8)

 Figure 4. 14-Lead SOIC (R-14),  
14-Lead TSSOP (RU-14)

frequency data converters. The low bias current drift is well-suited for precision I-to-V converters. The combination of precision offset, offset drift, and low noise also make the op amps ideal for gain, dc offset adjust, and active filter in both instrumentation and medical applications. These low power op amps can be used in IR thermometers, pH and ORP instruments, pressure transducer front ends, and other sensor signal conditioning circuits that are used in remote or wireless applications.

The [AD8663/AD8667/AD8669](#) are specified over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The single [AD8663](#) is available in a narrow 8-lead SOIC package and a very thin, 8-lead LFCSP. The dual [AD8667](#) is available in a narrow 8-lead SOIC package and an 8-lead MSOP. The quad [AD8669](#) is available in a 14-lead SOIC and 14-lead small TSSOP.

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## REVISION HISTORY

### 5/2016—Rev. C to Rev. D

Changed CP-8-2 to CP-8-13 .....	Throughout
Changes to Figure 2.....	1
Changes to Table 4.....	5
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	15

### 4/2013—Rev. B to Rev. C

Changes to Figure 2.....	1
Added Exposed Pad Notation to Outline Dimensions .....	14
Changes to Ordering Guide .....	15

### 1/2008—Rev. A to Rev. B

Added TSSOP .....	Universal
Change to Table 4 .....	5
Changes to Figure 8 and Figure 9.....	6
Changes to Figure 23 and Figure 26.....	9
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	15

### 10/2007—Rev. 0 to Rev. A

Added AD8667 and AD8669.....	Universal
Changes to Features .....	1
Changes to General Description .....	1
Inserted Figure 3 and Figure 4.....	1
Changes to Table 1, Power Supply Section.....	3
Changes to Table 2.....	4
Reformatted Typical Performance Characteristics Section .....	6
Changes to Figure 5.....	6
Changes to Figure 13.....	7
Changes to Figure 17 and Figure 20 .....	8
Inserted Figure 35 through Figure 39.....	11
Inserted Figure 40 and Figure 41.....	12
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	15

### 7/2007—Revision 0: Initial Version

**SPECIFICATIONS****ELECTRICAL CHARACTERISTICS**

$V_{SY} = 5.0\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		30	175	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	450	$\mu\text{V}$ $\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	105	$\text{pA}$ $\text{pA}$
Input Voltage Range			0.2		3.0	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0.2\text{ V to } 3.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	76	100		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_{OUT} = 0.5\text{ V to } 4.5\text{ V}$ $R_L = 2\text{ k}\Omega$ , $V_{OUT} = 0.5\text{ V to } 4.5\text{ V}$	76	100		dB
Offset Voltage Drift	$TCV_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	106	114		dB
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.95	4.97		V
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.90	4.80		V
Output Voltage Low	$V_{OL}$	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.65		25	V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.60		35	V
Short-Circuit Current	$I_{SC}$			$\pm 7$	250	mV
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 100\text{ kHz}$ , $A_V = 1$		120		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 5\text{ V to } 16\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	105		dB
Supply Current per Amplifier	$I_{SY}$	$V_{OUT} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	210	275	dB $\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		0.26		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP	$C_L = 20\text{ pF}$		520		kHz
Phase Margin	$\Phi_M$	$C_L = 20\text{ pF}$		60		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		23		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		pA/ $\sqrt{\text{Hz}}$

$V_{SY} = 16.0\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		40	300	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	500	$\mu\text{V}$ $\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	45	$\text{pA}$
Input Voltage Range			0.2		120	$\text{pA}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0.2\text{ V to }14.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	87	109	65	$\text{pA}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_{OUT} = 0.5\text{ V to }15.5\text{ V}$ $R_L = 2\text{ k}\Omega$ , $V_{OUT} = 0.5\text{ V to }15.5\text{ V}$	115	140		$\text{dB}$
Offset Voltage Drift	$TCV_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	5	$\mu\text{V}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.95	15.98		$\text{V}$
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.90	15.92		$\text{V}$
Output Voltage Low	$V_{OL}$	$I_L = 100\text{ }\mu\text{A}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.85		25	$\text{mV}$
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.80		35	$\text{mV}$
Short-Circuit Current	$I_{SC}$			$\pm 50$	100	$\text{mV}$ $\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 100\text{ kHz}$ , $A_V = 1$		100		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 5\text{ V to }16\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	105		$\text{dB}$
Supply Current per Amplifier	$I_{SY}$	$V_{OUT} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	230	285	$\text{dB}$ $\mu\text{A}$
					355	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		0.3		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP	$C_L = 20\text{ pF}$		540		$\text{kHz}$
Phase Margin	$\Phi_M$	$C_L = 20\text{ pF}$		64		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		23		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		21		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	-0.1 V to $V_{SY}$
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-60°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC (R-8)	121	43	°C/W
8-Lead LFCSP (CP-8-13)	75 <sup>1</sup>	18 <sup>1</sup>	°C/W
8-Lead MSOP (RM-8)	145	45	°C/W
14-Lead SOIC (R-14)	90	45	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W

<sup>1</sup> Exposed pad soldered to application board.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

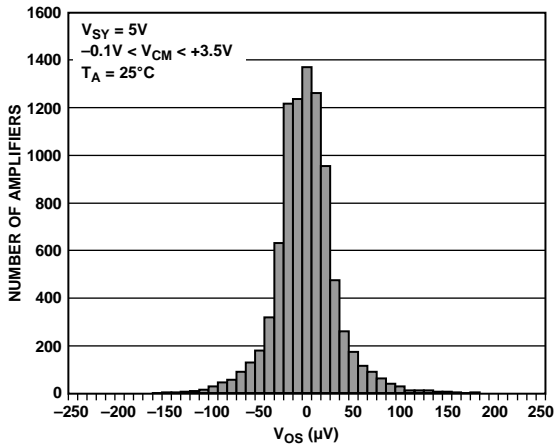


Figure 5. Input Offset Voltage Distribution

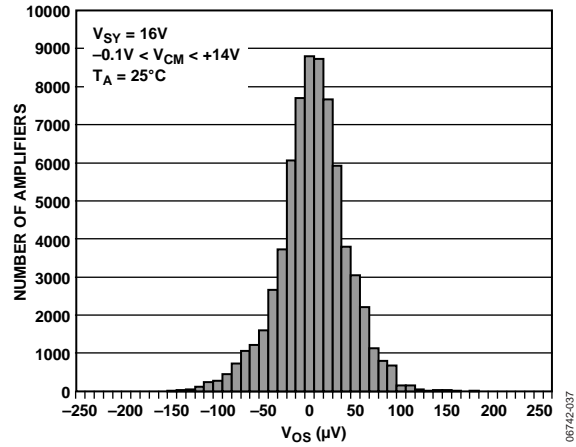


Figure 8. Input Offset Voltage Distribution

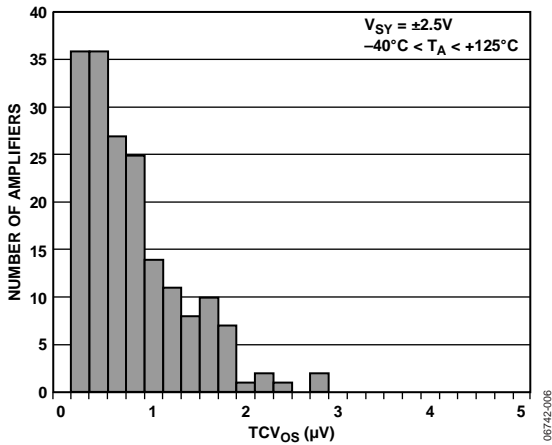


Figure 6. Offset Voltage Drift Distribution

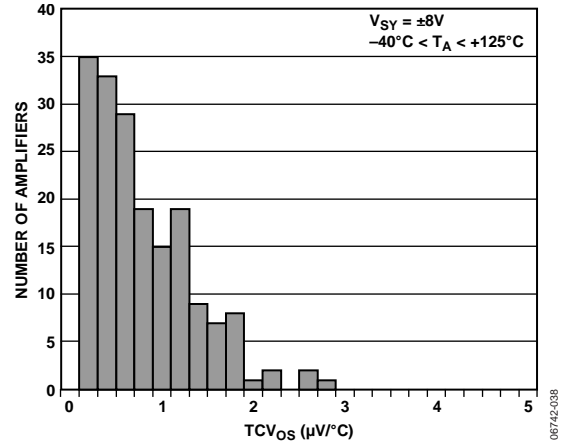


Figure 9. Offset Voltage Drift Distribution

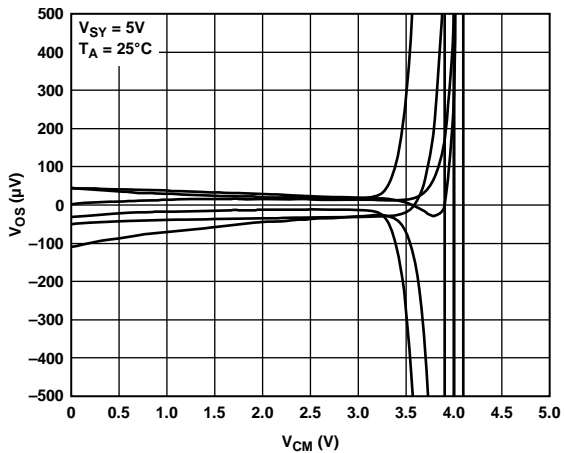


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

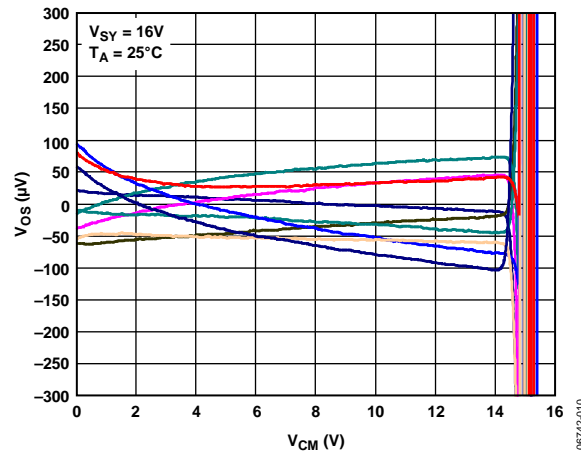


Figure 10. Input Offset Voltage vs. Common-Mode Voltage

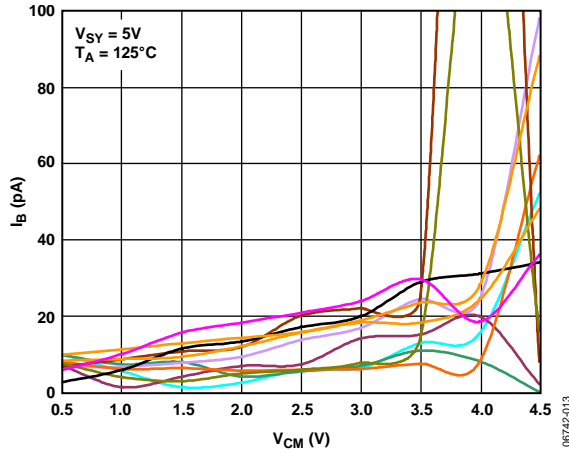


Figure 11. Input Bias Current vs. Common-Mode Voltage at 125°C

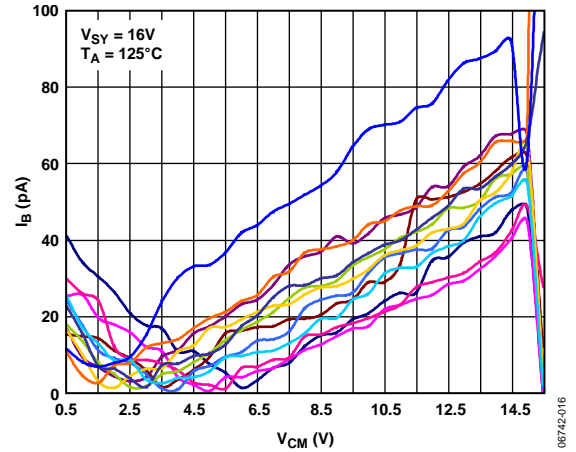


Figure 14. Input Bias Current vs. Common-Mode Voltage at 125°C

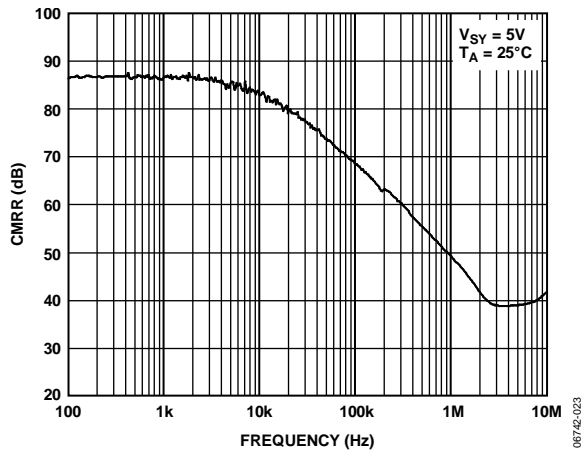


Figure 12. CMRR vs. Frequency,  $V_{SY} = 5V$

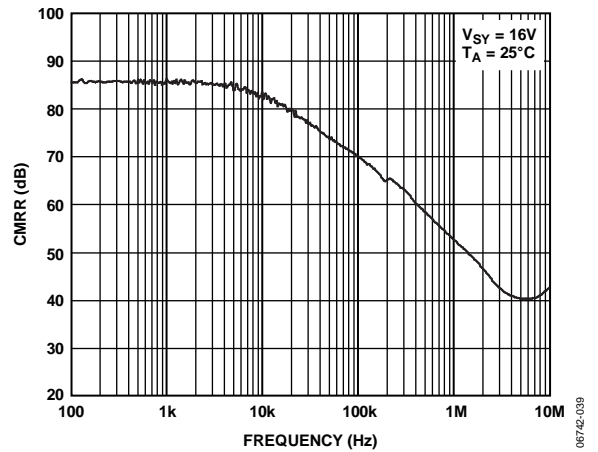


Figure 15. CMRR vs. Frequency,  $V_{SY} = 16V$

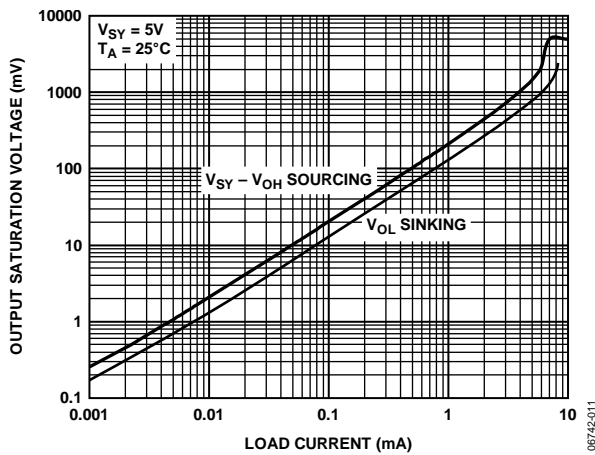


Figure 13. Output Swing Saturation Voltage vs. Load Current

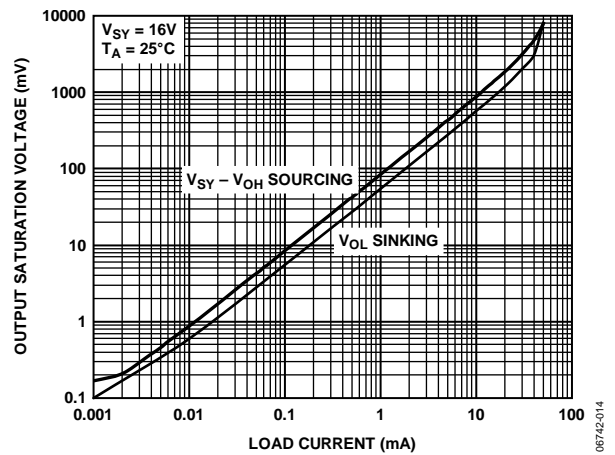


Figure 16. Output Swing Saturation Voltage vs. Load Current

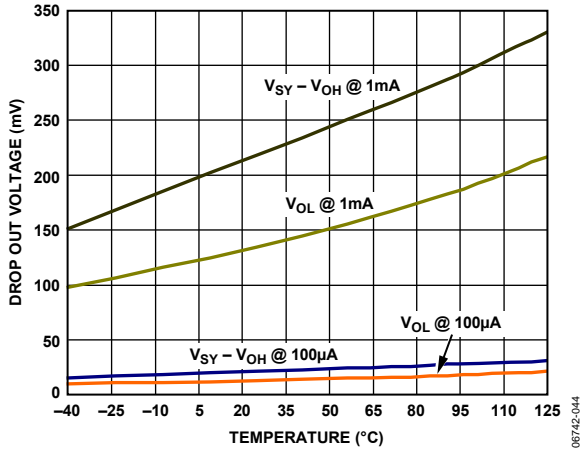


Figure 17. Output Voltage Saturation vs. Temperature

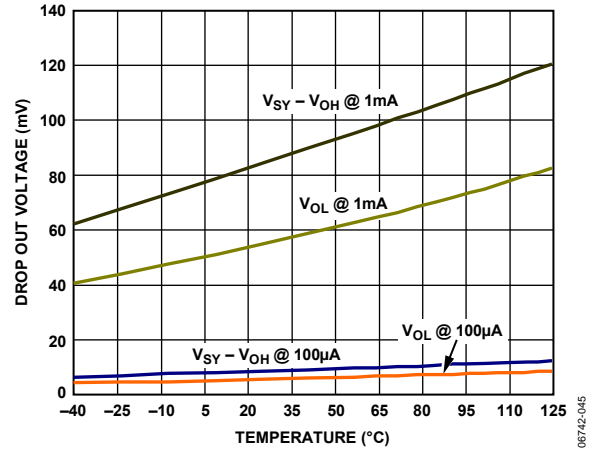


Figure 20. Output Voltage Saturation vs. Temperature

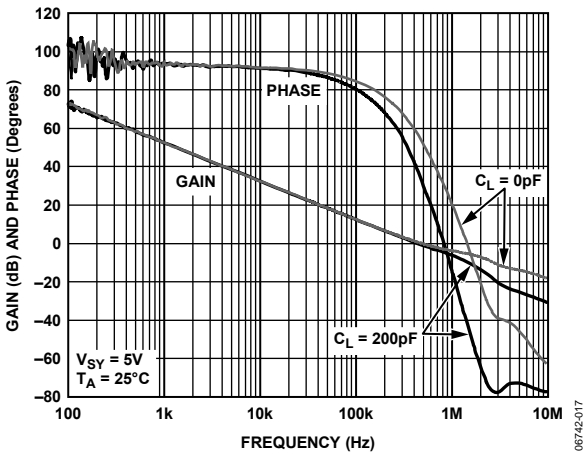


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

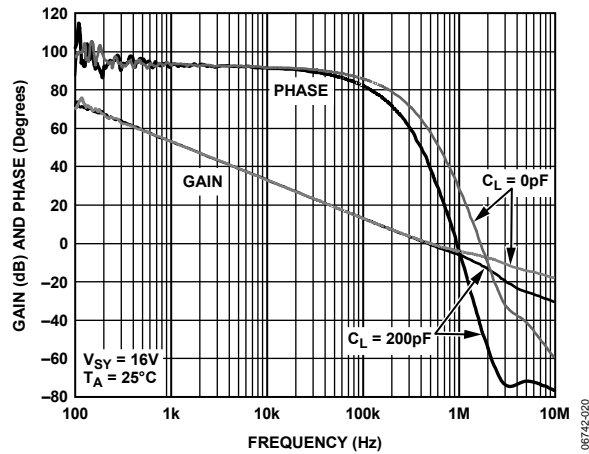


Figure 21. Open-Loop Gain and Phase Shift vs. Frequency

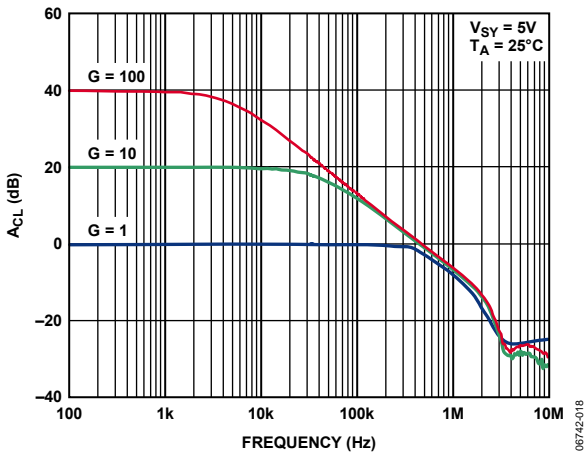


Figure 19. Closed-Loop Gain vs. Frequency

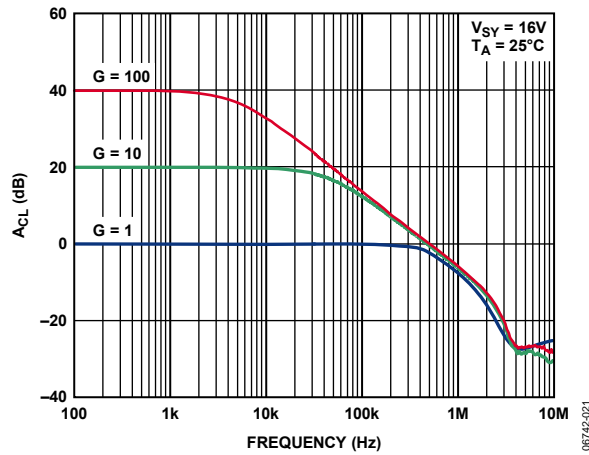


Figure 22. Closed-Loop Gain vs. Frequency,  $V_{SY} = 16V$



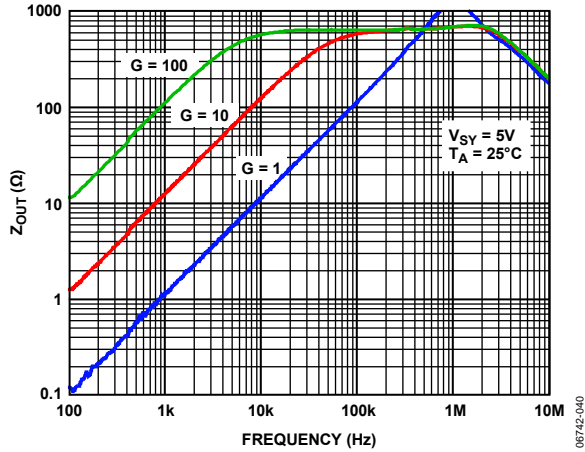


Figure 23. Closed-Loop Output Impedance vs. Frequency,  $V_{SY} = 5\text{ V}$

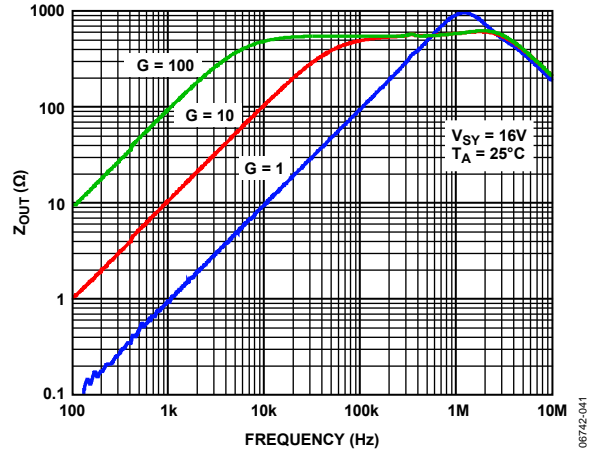


Figure 26. Closed-Loop Output Impedance vs. Frequency,  $V_{SY} = 16\text{ V}$

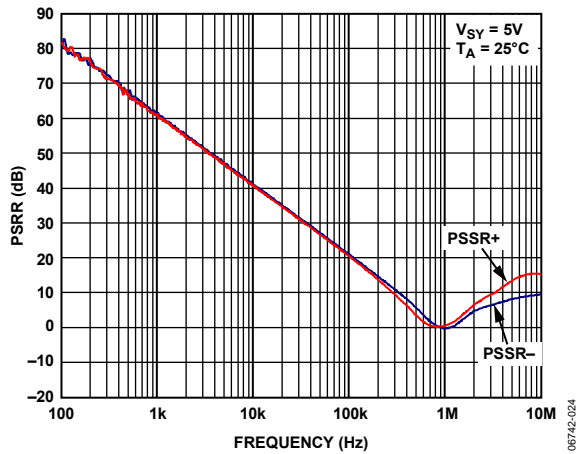


Figure 24. PSRR vs. Frequency,  $V_{SY} = 5\text{ V}$

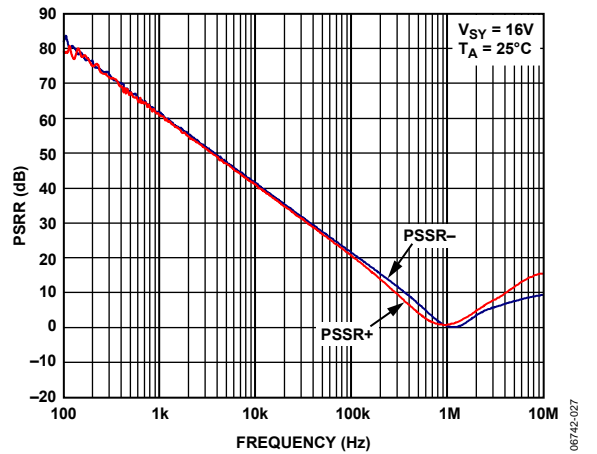


Figure 27. PSRR vs. Frequency,  $V_{SY} = 16\text{ V}$

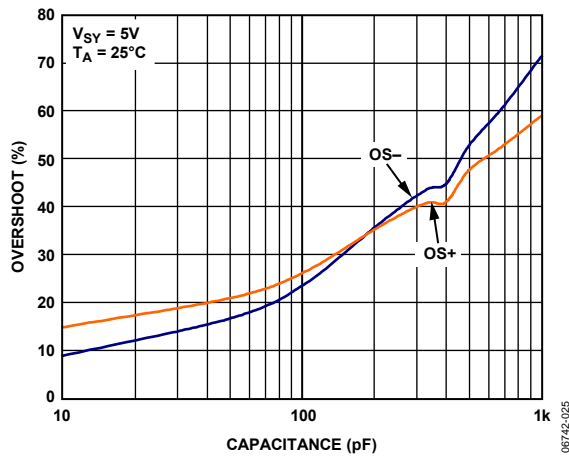


Figure 25. Small-Signal Overshoot vs. Load Capacitance,  $V_{SY} = 5\text{ V}$

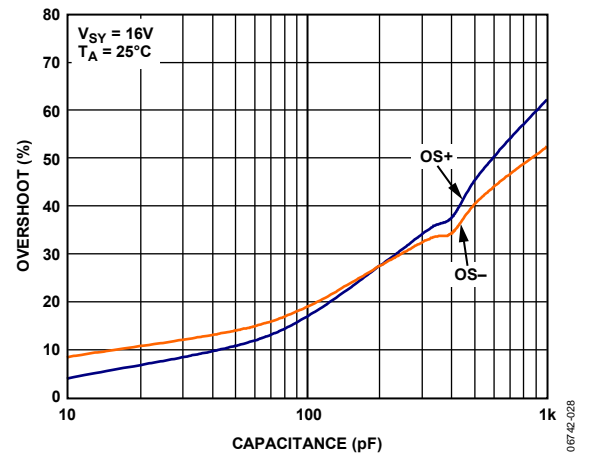


Figure 28. Small-Signal Overshoot vs. Load Capacitance,  $V_{SY} = 16\text{ V}$

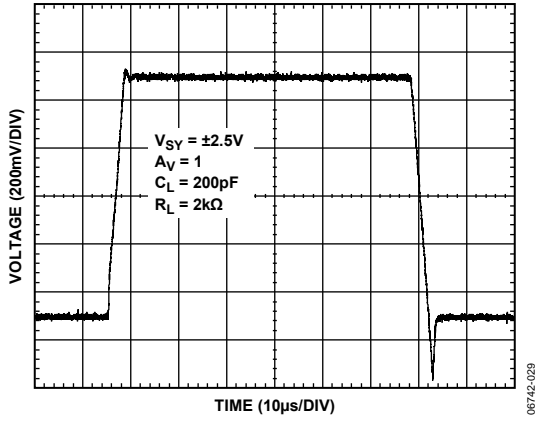


Figure 29. Large Signal Transient Response,  $V_{SY} = \pm 2.5\text{ V}$

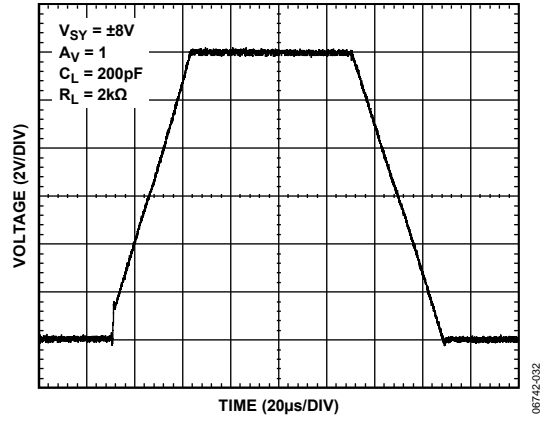


Figure 32. Large Signal Transient Response,  $V_{SY} = \pm 8\text{ V}$

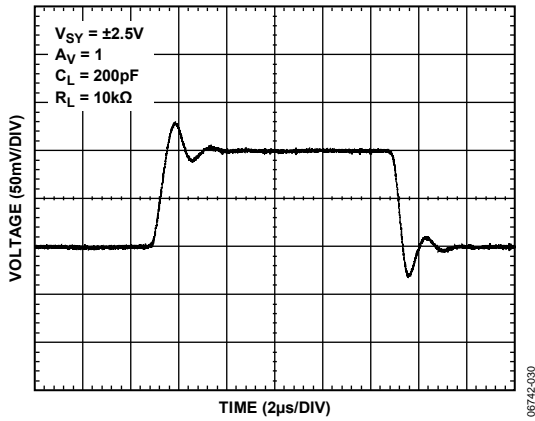


Figure 30. Small Signal Transient Response,  $V_{SY} = \pm 2.5\text{ V}$

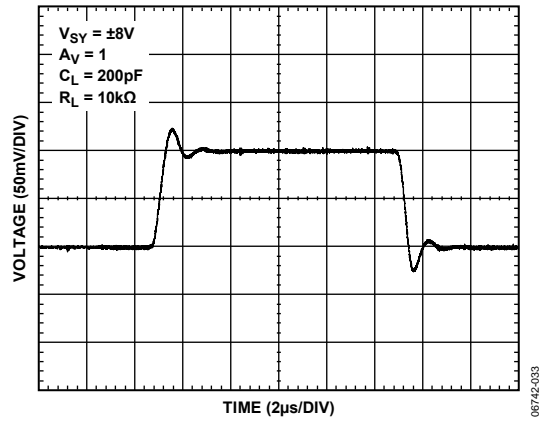


Figure 33. Small Signal Transient Response,  $V_{SY} = \pm 8\text{ V}$

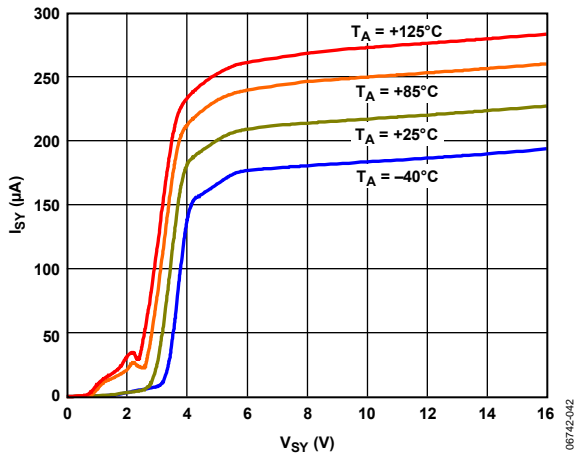


Figure 31. AD8663, Supply Current vs. Supply Voltage

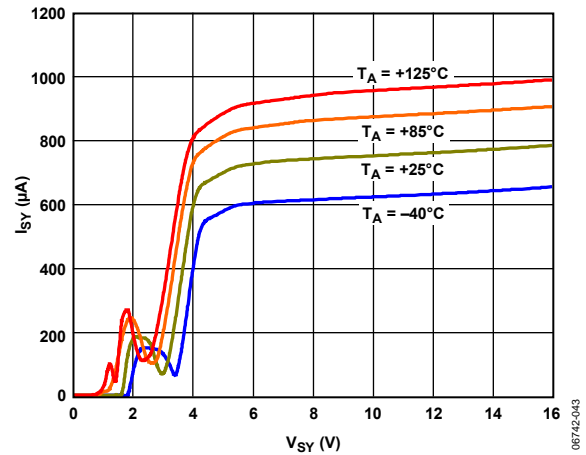


Figure 34. AD8669, Supply Current vs. Supply Voltage

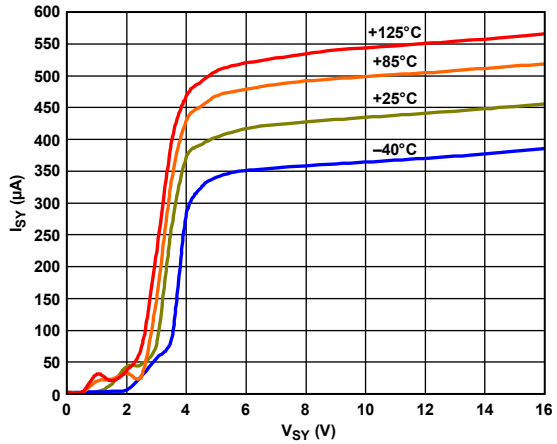


Figure 35. AD8667, Supply Current vs. Supply Voltage

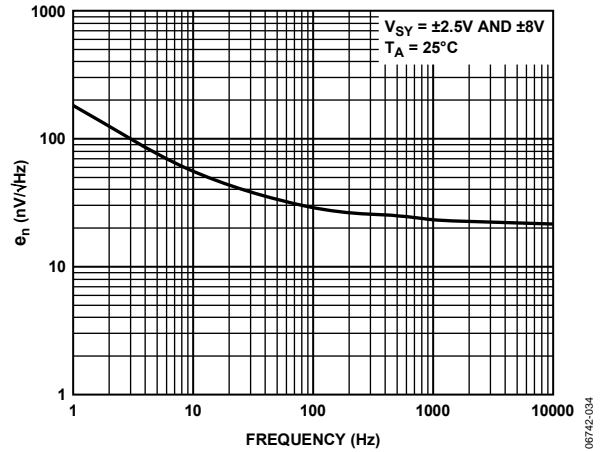


Figure 38. Voltage Noise Density

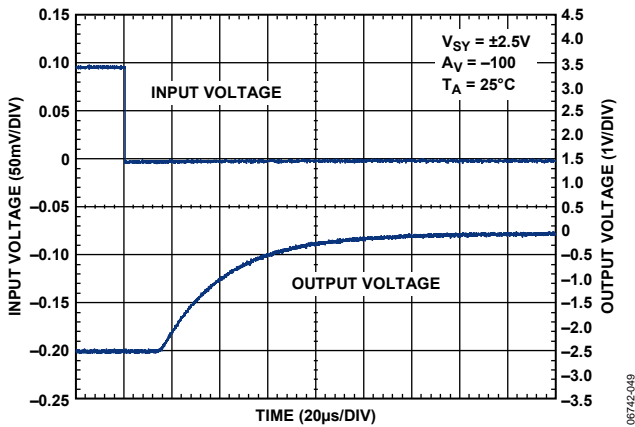


Figure 36. Positive Overload Recovery

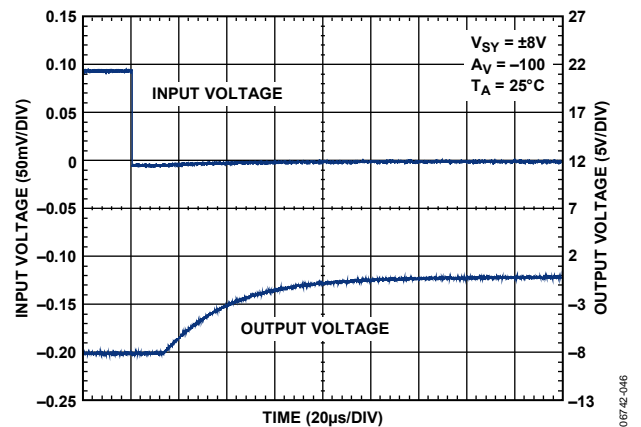


Figure 39. Positive Overload Recovery

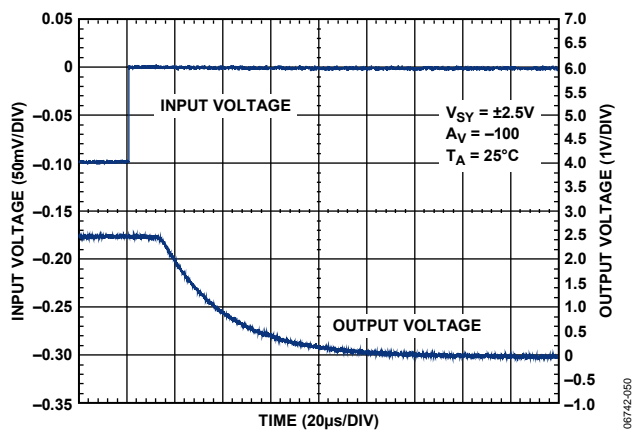


Figure 37. Negative Overload Recovery

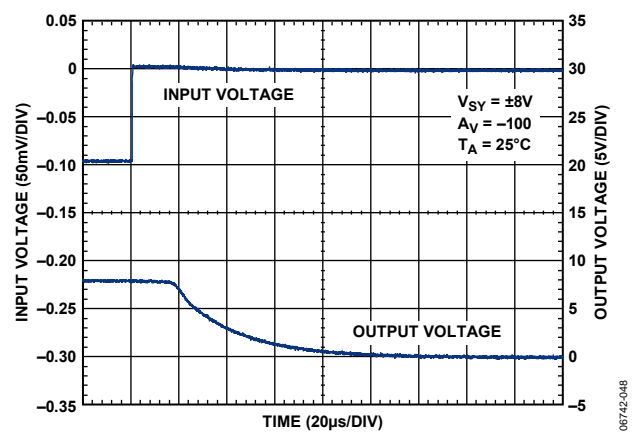


Figure 40. Negative Overload Recovery

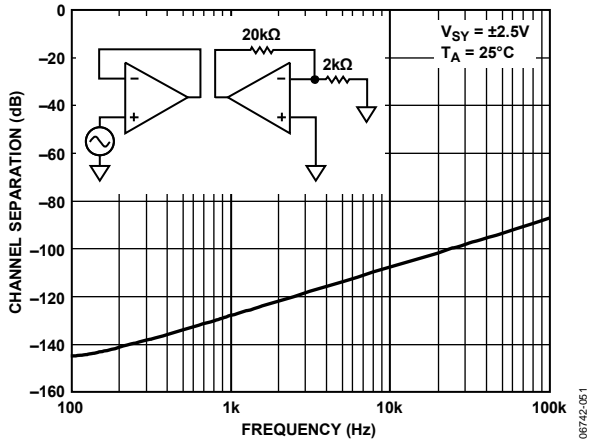


Figure 41. Channel Separation vs. Frequency

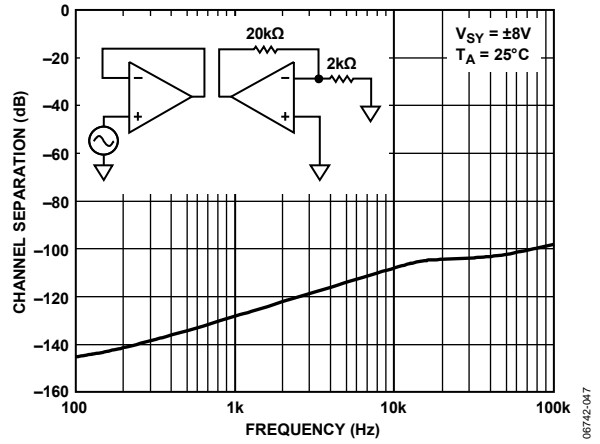
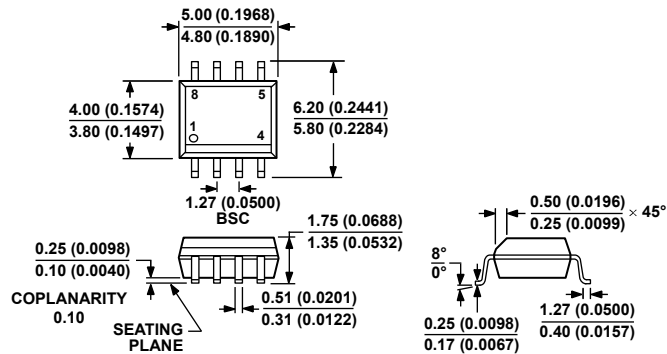


Figure 42. Channel Separation vs. Frequency

OUTLINE DIMENSIONS

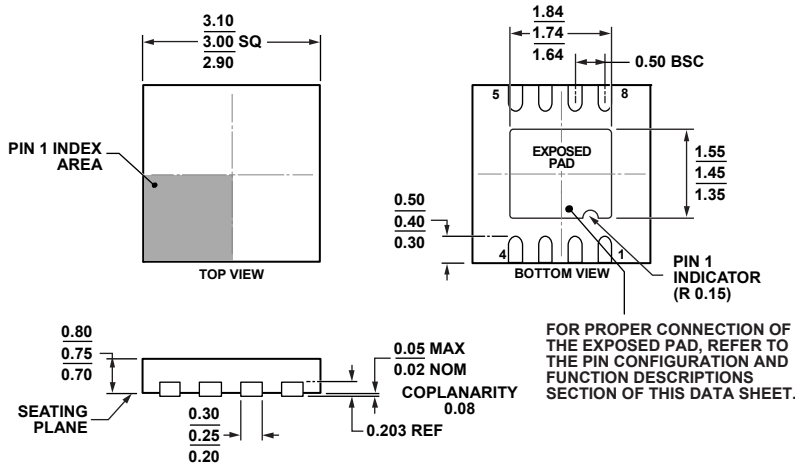


COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 43. 8-Lead Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

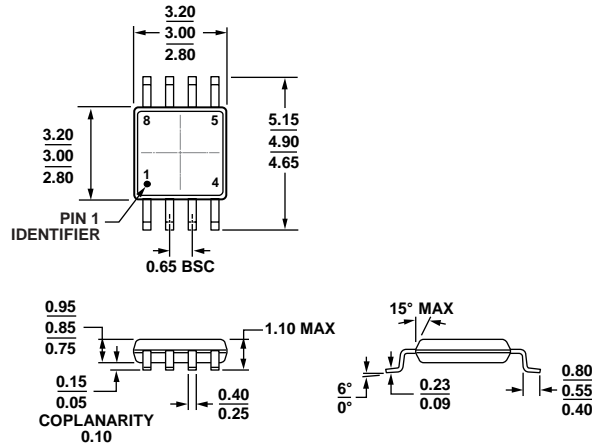


COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 44. 8-Lead Lead Frame Chip Scale Package [LFCSP\_VD]  
 3 mm x 3 mm and 0.75 mm Package Height  
 (CP-8-13)

Dimensions shown in millimeters

12407-2010-A

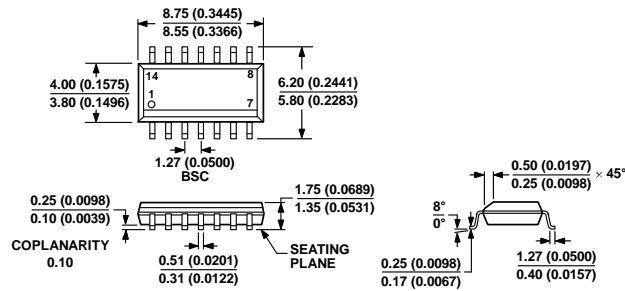


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 45. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2008-B

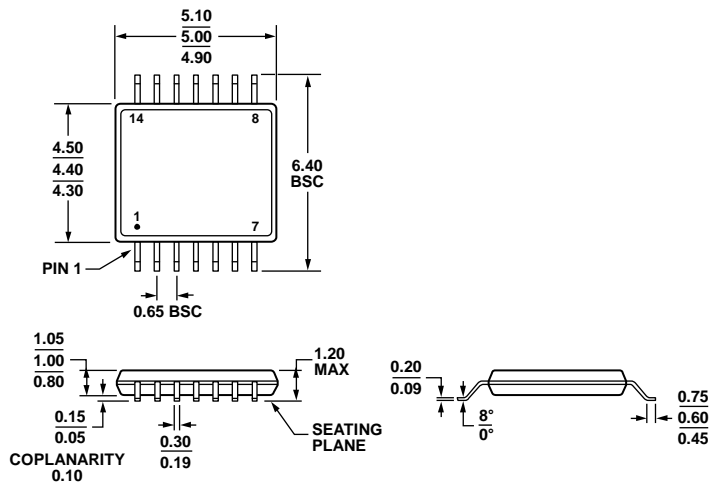


COMPLIANT TO JEDEC STANDARDS MS-012-AB  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 46. 14-Lead Small Outline Package [SOIC\_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

06/06/06-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 47. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

06/19/06-A