Low Noise, Precision, 16 V, CMOS, Rail-to-Rail Operational Amplifiers

Data Sheet

AD8663/AD8667/AD8669

FEATURES

- Low offset voltage: 175 µV maximum @ V_{SY} = 5 V
- Low supply current: 275 µA maximum per amplifier
- Single-supply operation: 5 V to 16 V
- Low noise: 23 nV/√Hz
- Low input bias current: 300 fA
- Unity-gain stable
- Small packages available
  - 3 mm × 3 mm, 8-lead LFCSP
  - 8-lead MSOP
- Other packages
  - 8-lead SOIC
  - 14-lead SOIC
  - 14-lead TSSOP

APPLICATIONS

- Sensor front ends
- Transimpedance amplifiers
- Electrometer applications
- Photodiode amplification
- Low power ADC drivers
- Medical diagnostic instruments
- pH and ORP meters and probes
- DAC or REF buffers

PIN CONFIGURATIONS

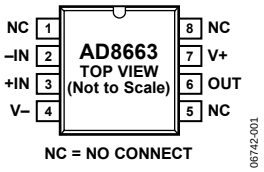

Figure 1. 8-Lead SOIC (R-8)

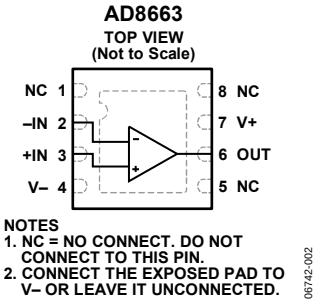

Figure 2. 8-Lead LFCSP (CP-8-13)

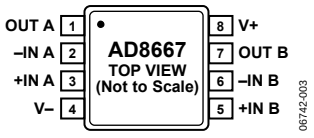

Figure 3. 8-Lead MSOP (RM-8), 8-Lead SOIC (R-8)

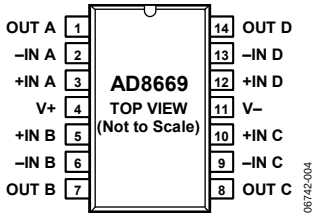

Figure 4. 14-Lead SOIC (R-14), 14-Lead TSSOP (RU-14)

GENERAL DESCRIPTION

The AD8663/AD8667/AD8669 are rail-to-rail output amplifiers that use the Analog Devices, Inc., patented DigiTrim® trimming technique to achieve low offset voltage. The AD8663/AD8667/AD8669 feature an extended operating range with supply voltages up to 16 V. They also feature low input bias current, low input offset voltage, and low current noise.

The combination of low offset, very low input bias current, and a wide supply range makes these amplifiers useful in a wide variety of applications usually associated with higher priced JFET amplifiers. Systems using high impedance sensors, such as photodiodes, benefit from the combination of low input bias current, low noise, low offset, and wide bandwidth.

The ability to operate the device for single (5 V to 16 V) or dual supplies (±2.5 V to ±8 V) supports many applications. The rail-to-rail outputs provide increased dynamic range to drive low frequency data converters. The low bias current drift is well-suited for precision I-to-V converters. The combination of precision offset, offset drift, and low noise also make the op amps ideal for gain, dc offset adjust, and active filter in both instrumentation and medical applications. These low power op amps can be used in IR thermometers, pH and ORP instruments, pressure transducer front ends, and other sensor signal conditioning circuits that are used in remote or wireless applications.

The AD8663/AD8667/AD8669 are specified over the extended industrial temperature range of −40°C to +125°C. The single AD8663 is available in a narrow 8-lead SOIC package and a very thin, 8-lead LFCSP. The dual AD8667 is available in a narrow 8-lead SOIC package and an 8-lead MSOP. The quad AD8669 is available in a 14-lead SOIC and 14-lead small TSSOP.

Rev. D
Document Feedback

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4/2013—Rev. B to Rev. C

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = 5.0 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$		30	175	µV
		−40°C < T_A < +125°C			450	µV
Input Bias Current	I_B			0.3		pA
		−40°C < T_A < +85°C			45	pA
		−40°C < T_A < +125°C			105	pA
Input Offset Current	I_{OS}			0.2		pA
		−40°C < T_A < +85°C			35	pA
		−40°C < T_A < +125°C			65	pA
Input Voltage Range			0.2		3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.2 V to 3.0 V	76	100		dB
		−40°C < T_A < +125°C	76	100		dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_{OUT} = 0.5 V to 4.5 V	115	140		dB
		R_L = 2 kΩ, V_{OUT} = 0.5 V to 4.5 V	106	114		dB
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +125°C		1.5	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA	4.95	4.97		V
		−40°C < T_A < +125°C	4.90			V
Output Voltage High	V_{OH}	I_L = 1 mA	4.65	4.80		V
		−40°C < T_A < +125°C	4.60			V
Output Voltage Low	V_{OL}	I_L = 100 µA		17	25	mV
		−40°C < T_A < +125°C			35	mV
Output Voltage Low	V_{OL}	I_L = 1 mA		150	200	mV
		−40°C < T_A < +125°C			250	mV
Short-Circuit Current	I_{SC}			±7		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		120		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 5 V to 16 V	95	105		dB
		−40°C < T_A < +125°C	95			dB
Supply Current per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$		210	275	µA
		−40°C < T_A < +125°C			325	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.26		V/µs
Gain Bandwidth Product	GBP	C_L = 20 pF		520		kHz
Phase Margin	Φ_M	C_L = 20 pF		60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		23		nV/√Hz
		f = 10 kHz		21		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

V_{SY} = 16.0 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$		40	300	µV
		−40°C < T_A < +125°C			500	µV
Input Bias Current	I_B			0.3		pA
		−40°C < T_A < +85°C			45	pA
		−40°C < T_A < +125°C			120	pA
Input Offset Current	I_{OS}			0.2		pA
		−40°C < T_A < +85°C			35	pA
		−40°C < T_A < +125°C			65	pA
Input Voltage Range			0.2		14.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.2 V to 14.5 V	87	109		dB
		−40°C < T_A < +125°C	87	109		dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_{OUT} = 0.5 V to 15.5 V	115	140		dB
		R_L = 2 kΩ, V_{OUT} = 0.5 V to 15.5 V	106	111		dB
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +125°C		1.5	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA	15.95	15.98		V
		−40°C < T_A < +125°C	15.90			V
Output Voltage High	V_{OH}	I_L = 1 mA	15.85	15.92		V
		−40°C < T_A < +125°C	15.80			V
Output Voltage Low	V_{OL}	I_L = 100 µA		17	25	mV
		−40°C < T_A < +125°C			35	mV
Output Voltage Low	V_{OL}	I_L = 1 mA		70	100	mV
		−40°C < T_A < +125°C			125	mV
Short-Circuit Current	I_{SC}			±50		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 5 V to 16 V	95	105		dB
		−40°C < T_A < +125°C	95			dB
Supply Current per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$		230	285	µA
		−40°C < T_A < +125°C			355	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.3		V/µs
Gain Bandwidth Product	GBP	C_L = 20 pF		540		kHz
Phase Margin	Φ_M	C_L = 20 pF		64		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		23		nV/√Hz
		f = 10 kHz		21		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	−0.1 V to V_{SY}
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	121	43	°C/W
8-Lead LFCSP (CP-8-13)	75[1]	18[1]	°C/W
8-Lead MSOP (RM-8)	145	45	°C/W
14-Lead SOIC (R-14)	90	45	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W

[1] Exposed pad soldered to application board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

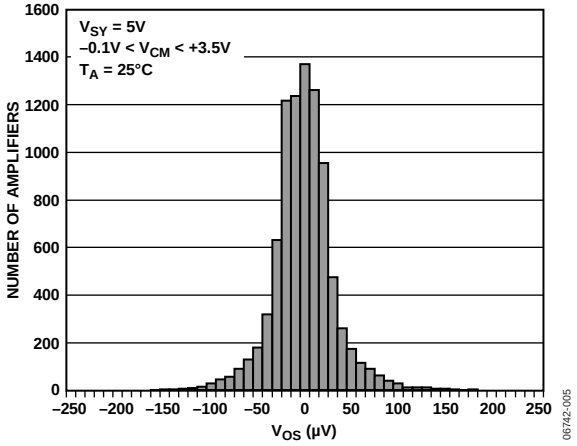


Figure 5. Input Offset Voltage Distribution

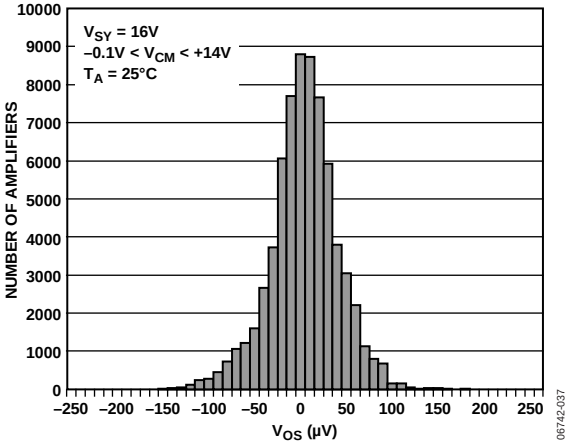


Figure 8. Input Offset Voltage Distribution

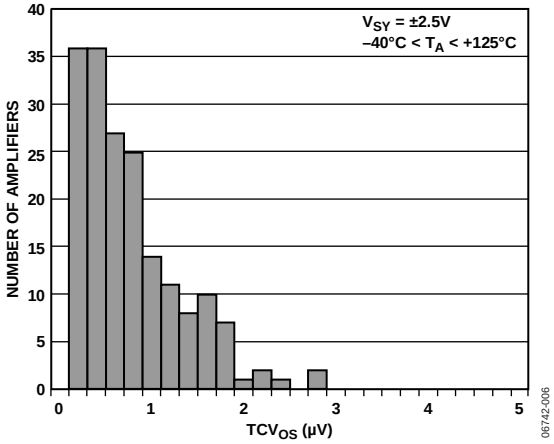


Figure 6. Offset Voltage Drift Distribution

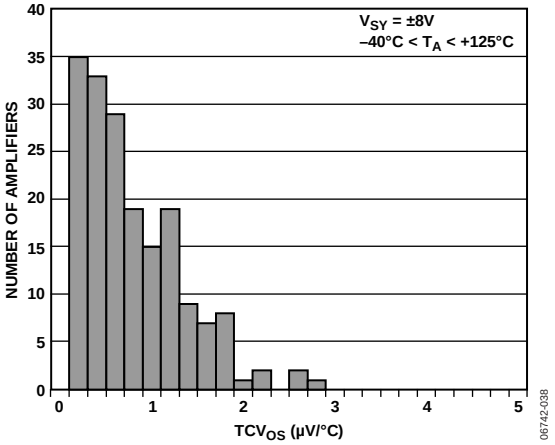


Figure 9. Offset Voltage Drift Distribution

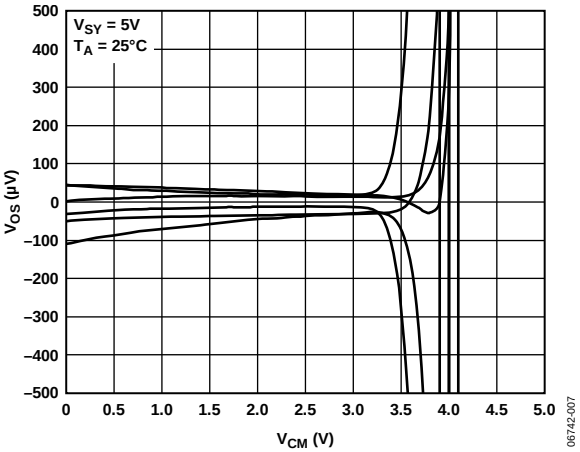


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

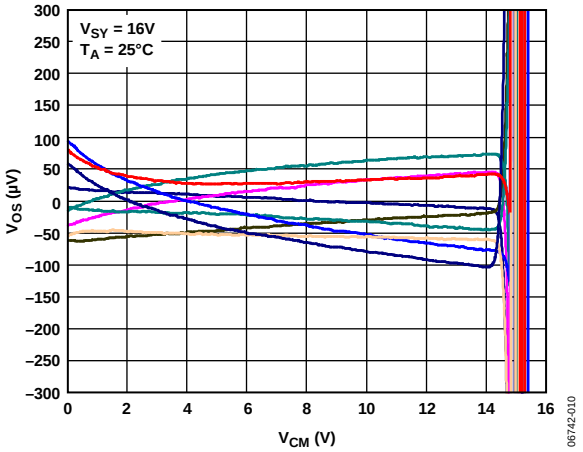
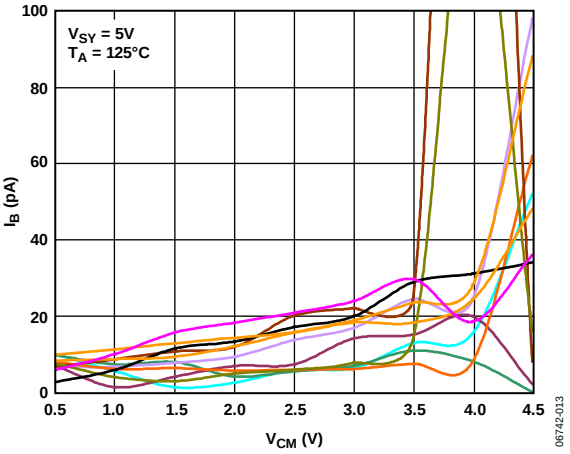


Figure 10. Input Offset Voltage vs. Common-Mode Voltage



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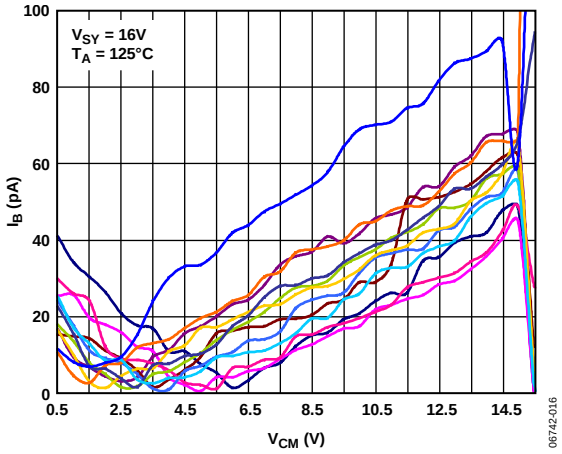


Figure 14. Input Bias Current vs. Common-Mode Voltage at 125°C

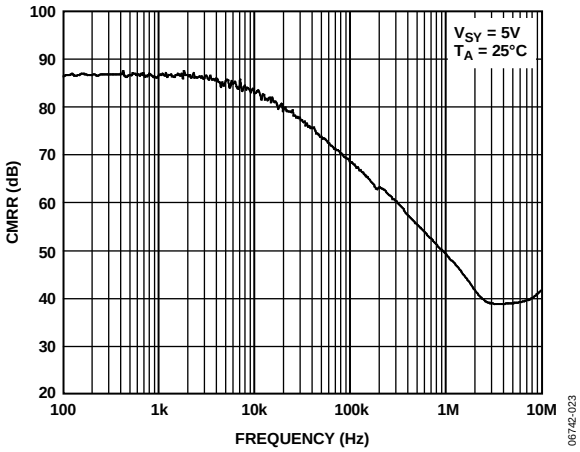
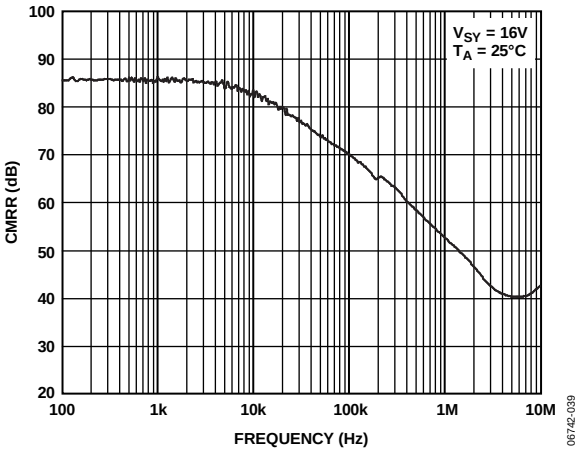


Figure 12. CMRR vs. Frequency, V_{SY} = 5 V



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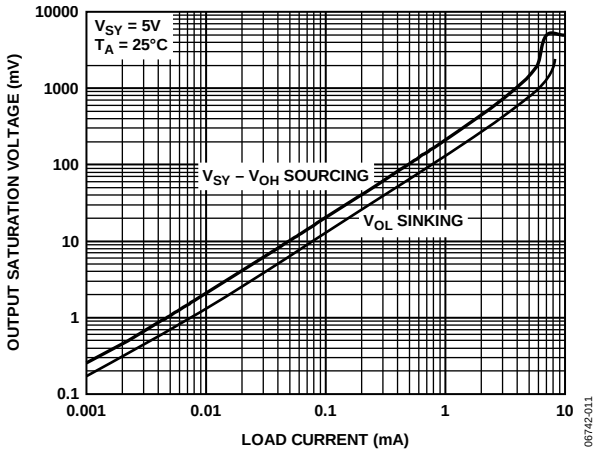


Figure 13. Output Swing Saturation Voltage vs. Load Current

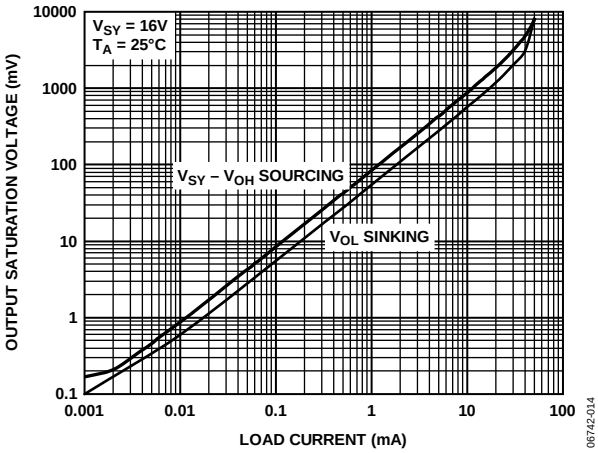


Figure 16. Output Swing Saturation Voltage vs. Load Current

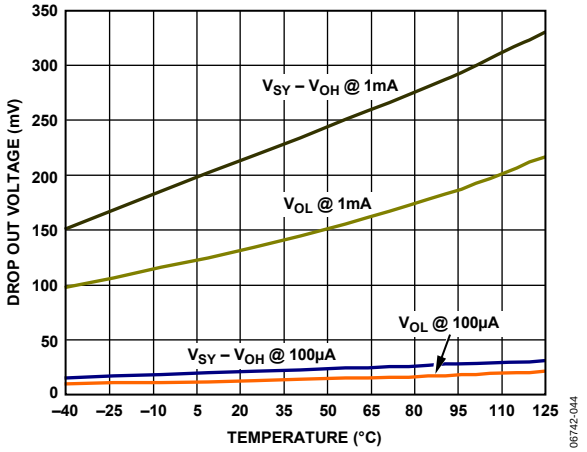


Figure 17. Output Voltage Saturation vs. Temperature

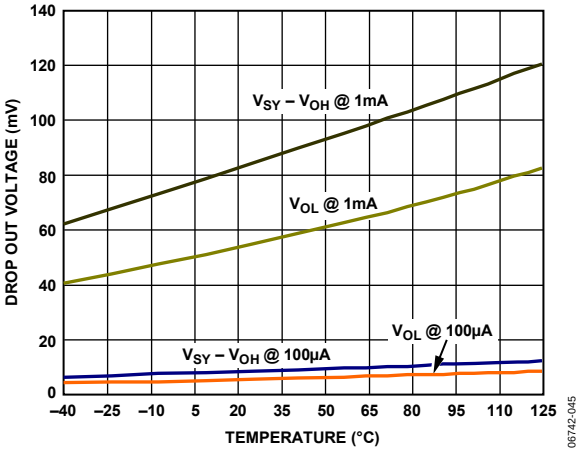


Figure 20. Output Voltage Saturation vs. Temperature

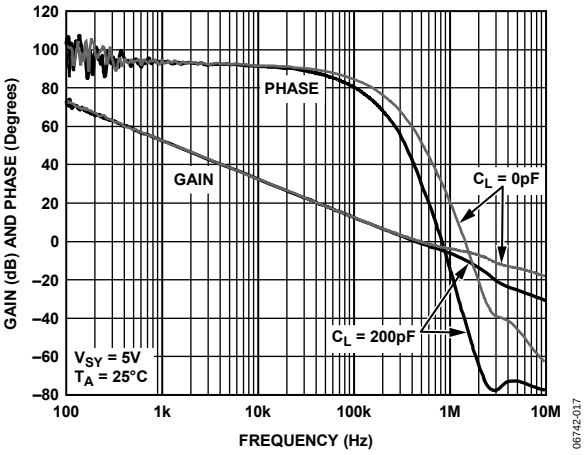


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

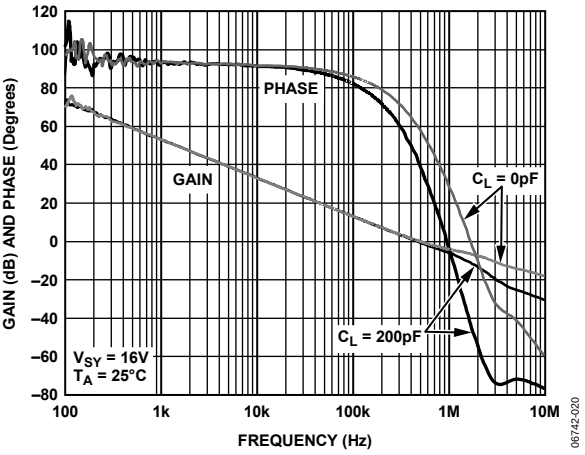


Figure 21. Open-Loop Gain and Phase Shift vs. Frequency

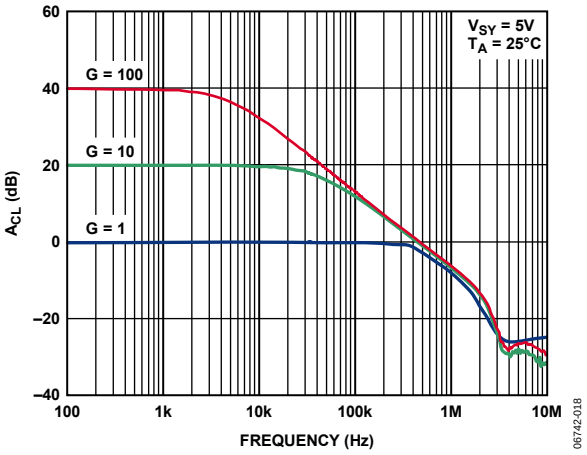


Figure 19. Closed-Loop Gain vs. Frequency

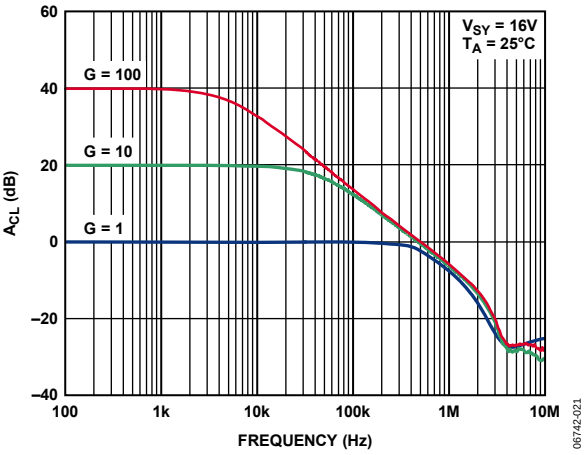


Figure 22. Closed-Loop Gain vs. Frequency, V_{SY} = 16 V

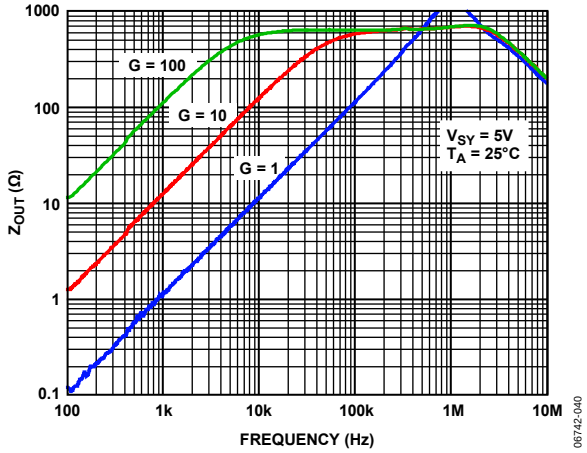


Figure 23. Closed-Loop Output Impedance vs. Frequency, V_{SY} = 5 V

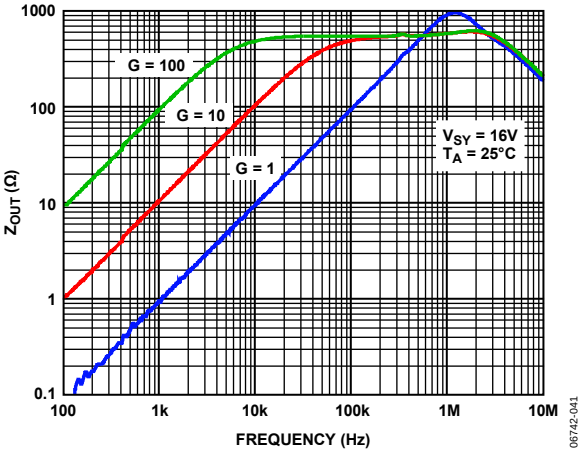


Figure 26. Closed-Loop Output Impedance vs. Frequency, V_{SY} = 16 V

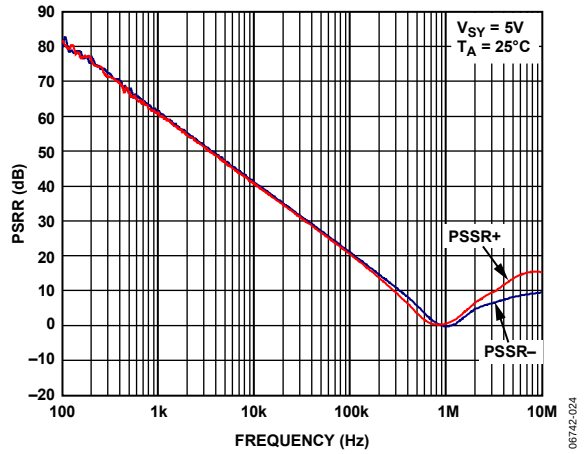


Figure 24. PSRR vs. Frequency, V_{SY} = 5 V

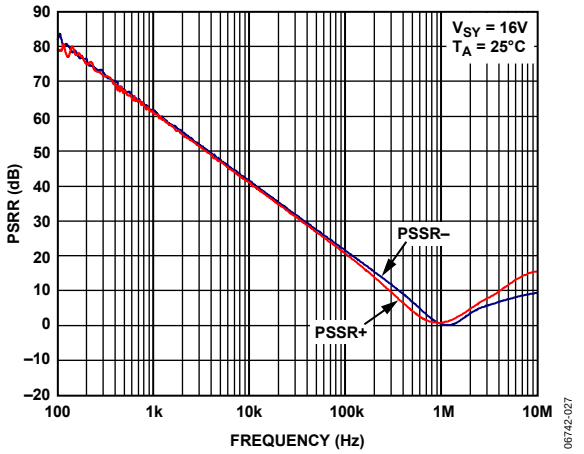


Figure 27. PSRR vs. Frequency, V_{SY} = 16 V

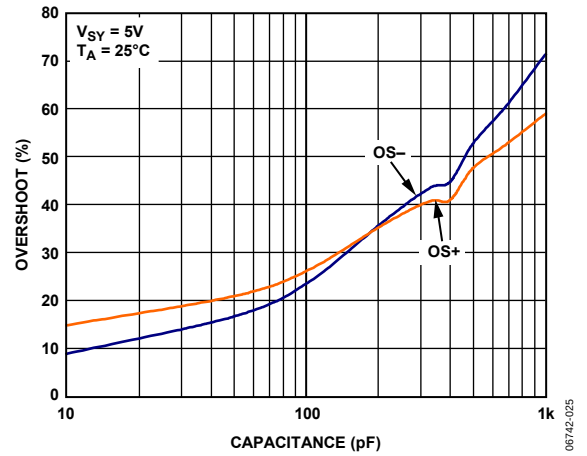


Figure 25. Small-Signal Overshoot vs. Load Capacitance, V_{SY} = 5 V

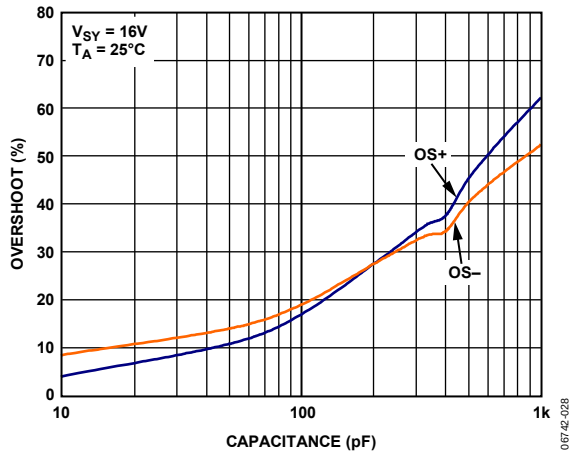


Figure 28. Small-Signal Overshoot vs. Load Capacitance, V_{SY} = 16 V

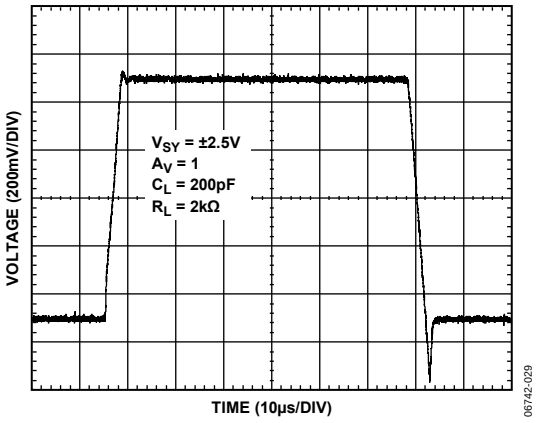


Figure 29. Large Signal Transient Response, V_{SY} = ±2.5 V

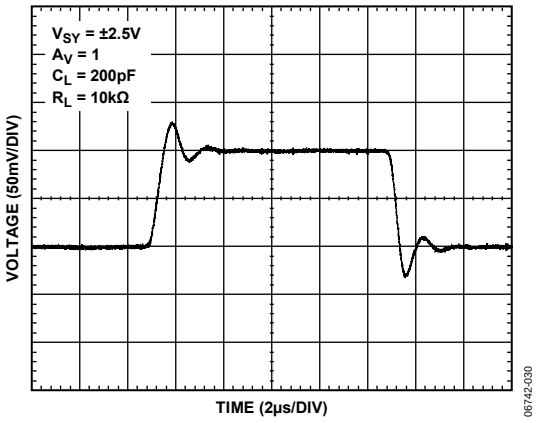


Figure 30. Small Signal Transient Response, V_{SY} = ±2.5 V

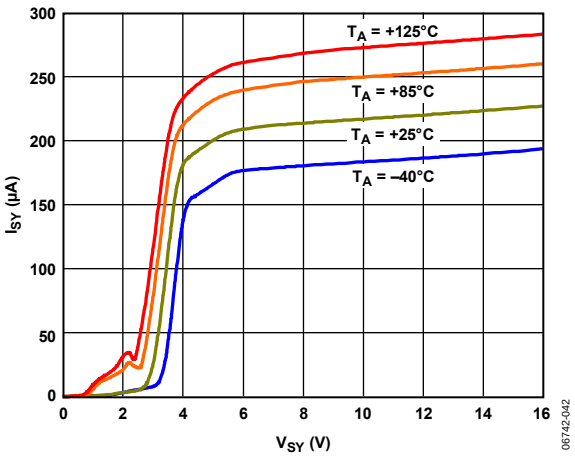


Figure 31. AD8663, Supply Current vs. Supply Voltage

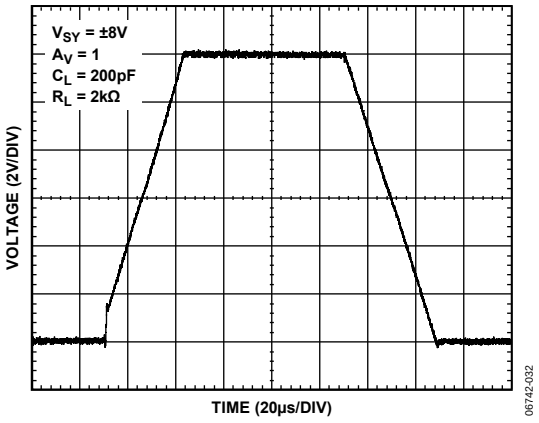


Figure 32. Large Signal Transient Response, V_{SY} = ±8 V

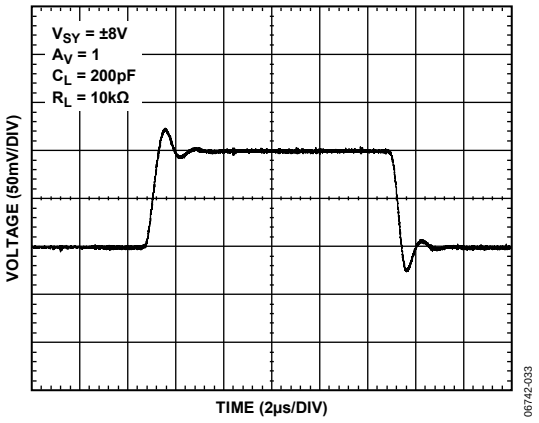


Figure 33. Small Signal Transient Response, V_{SY} = ±8 V

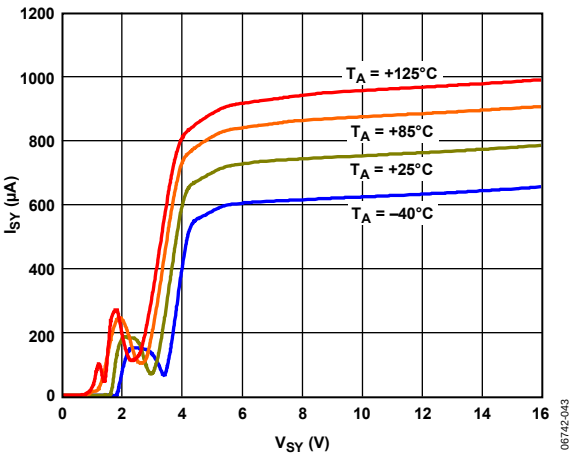


Figure 34. AD8669, Supply Current vs. Supply Voltage

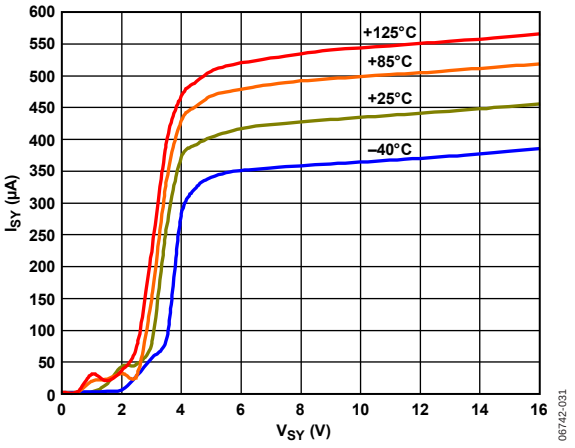


Figure 35. AD8667, Supply Current vs. Supply Voltage

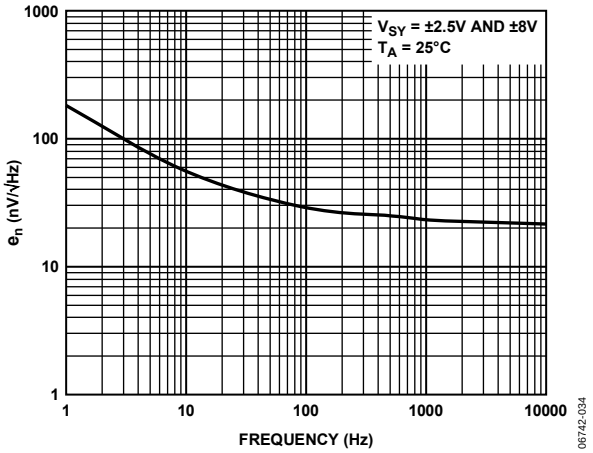


Figure 38. Voltage Noise Density

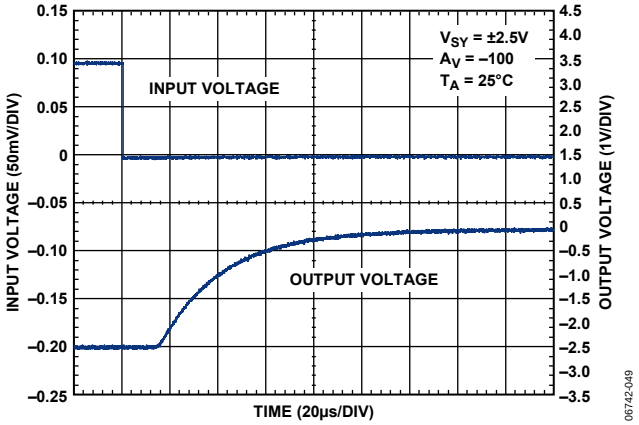


Figure 36. Positive Overload Recovery

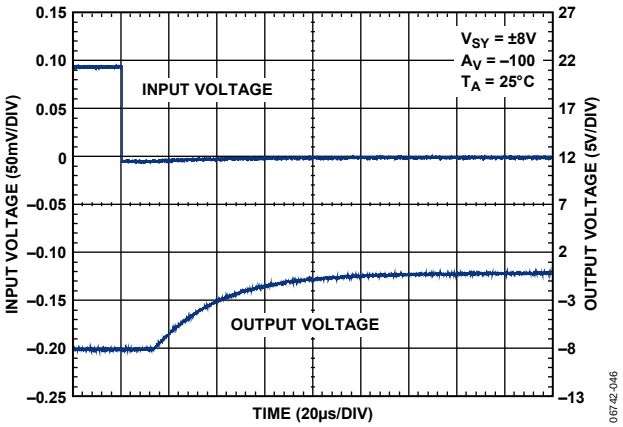


Figure 39. Positive Overload Recovery

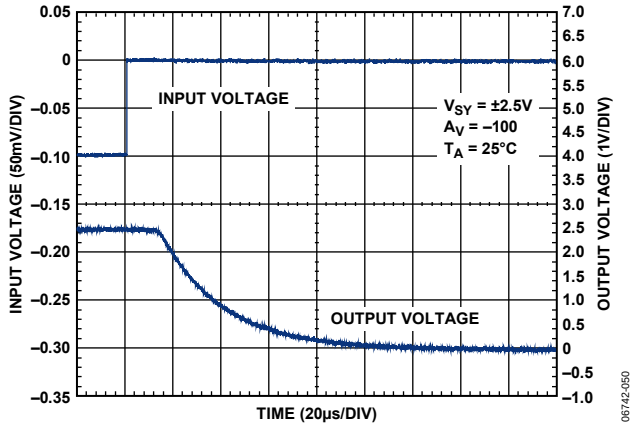


Figure 37. Negative Overload Recovery

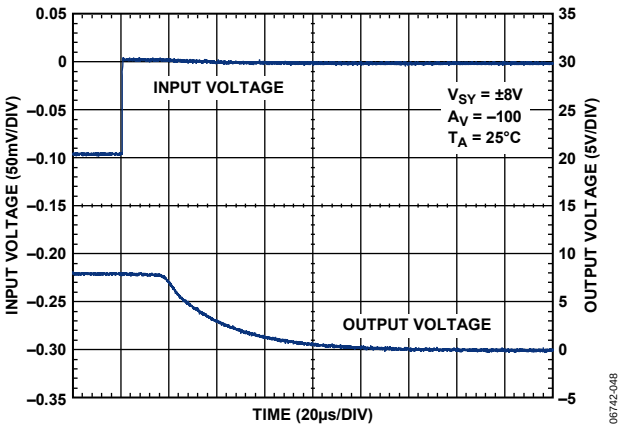


Figure 40. Negative Overload Recovery

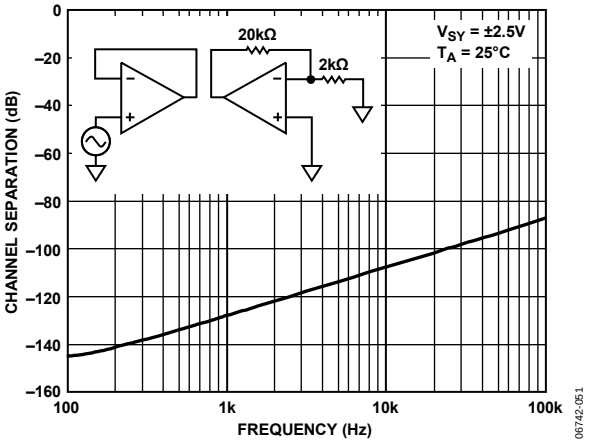


Figure 41. Channel Separation vs. Frequency

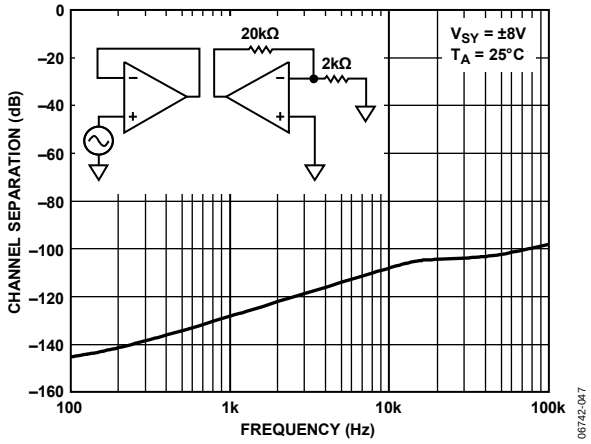


Figure 42. Channel Separation vs. Frequency

OUTLINE DIMENSIONS

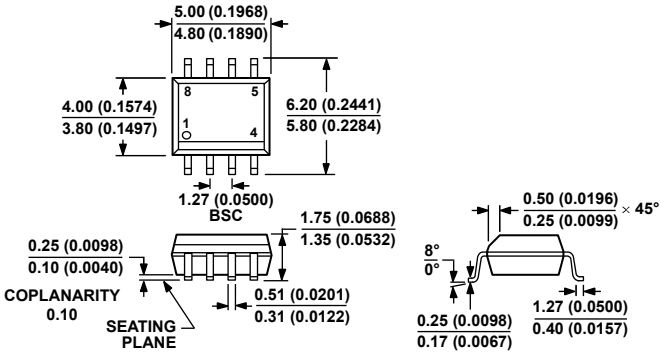


Figure 43. 8-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

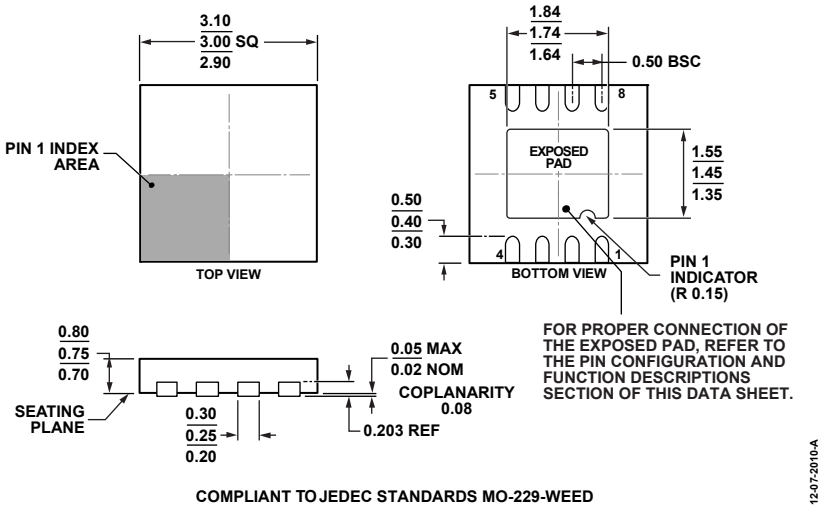
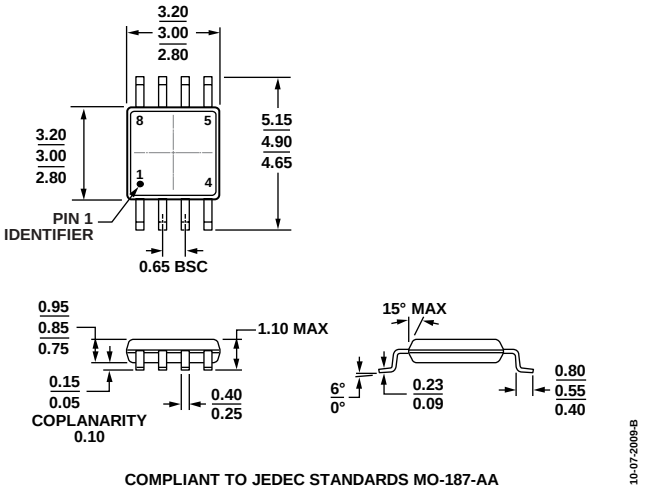
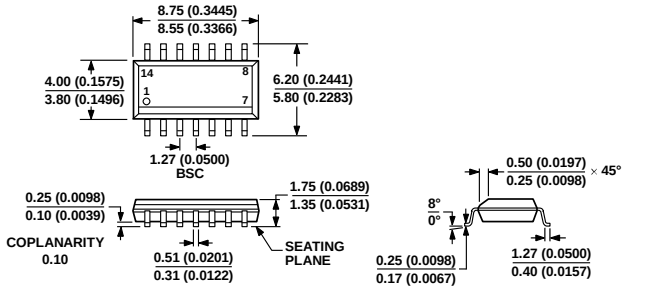


Figure 44. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters



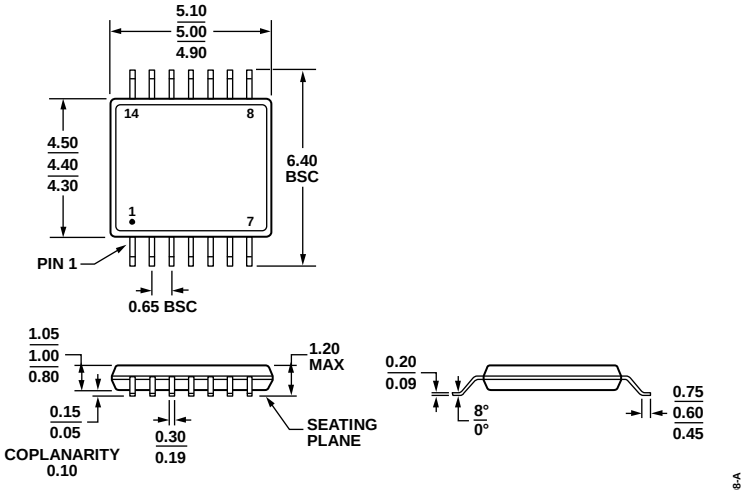
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 45. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 46. 14-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 47. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters