ANALOG DEVICES

36 V Precision, 2.8 nV/√Hz Rail-to-Rail Output Op Amp

Data Sheet **AD8675**

FEATURES

Very low voltage noise: 2.8 nV/√Hz
Rail-to-rail output swing
Low input bias current: 2 nA maximum
Very low offset voltage: 75 μV maximum
Low input offset drift: 0.6 μV/°C maximum
Very high gain: 120 dB
Wide bandwidth: 10 MHz typical
±5 V to ±18 V operation

APPLICATIONS

Precision instrumentation
PLL filters
Laser diode control loops
Strain gage amplifiers
Medical instrumentation
Thermocouple amplifiers

PIN CONFIGURATIONS

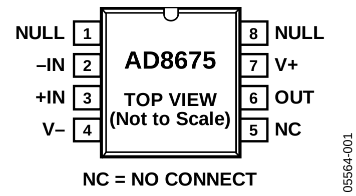

Figure 1. 8-Lead SOIC_N (R-8)

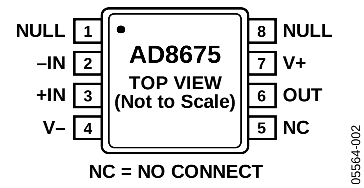

Figure 2. 8-Lead MSOP (RM-8)

GENERAL DESCRIPTION

The AD8675 precision operational amplifier has ultralow offset, drift, and voltage noise combined with very low input bias currents over the full operating temperature range. The AD8675 is a precision, wide bandwidth op amp featuring rail-to-rail output swings and very low noise. Operation is fully specified from ±5 V to ±15 V.

The AD8675 features a rail-to-rail output like that of the OP184, but with wide bandwidth and even lower voltage noise, combined with the precision and low power consumption like that of the industry-standard OP07 amplifier. Unlike other low noise, rail-to-rail op amps, the AD8675 has very low input bias current and low input current noise.

With typical offset voltage of only 10 μV, offset drift of 0.2 μV/°C, and noise of only 0.10 μV p-p (0.1 Hz to 10 Hz), the AD8675 is perfectly suited for applications where large error sources cannot be tolerated. For applications with even lower offset tolerances, the proprietary nulling capability allows a combination of both device and system offset errors up to 3.5 mV (referred to the input) to be compensated externally. Unlike previous circuits, the AD8675 accommodates this adjustment without adversely affecting the offset drift, CMRR, and PSRR of the amplifier. Precision instrumentation, PLL, and other precision filter circuits, position and pressure sensors, medical instrumentation, and strain gage amplifiers benefit greatly from the very low noise, low input bias current, and wide bandwidth. Many systems can take advantage of the low noise, dc precision, and rail-to-rail output swing provided by the AD8675 to maximize SNR and dynamic range.

The smaller packages and low power consumption afforded by the AD8675 allow maximum channel density or minimum board size for space-critical equipment.

The AD8675 is specified for the extended industrial temperature range (−40°C to +125°C). The AD8675 amplifier is available in the tiny 8-lead MSOP, and the popular 8-lead, narrow SOIC, RoHS compliant packages. MSOP packaged devices are only available in tape and reel format.

For the dual version of this ultraprecision, rail-to-rail op amp, see the AD8676 data sheet.

The AD8675 and AD8676 are members of a growing series of low noise op amps offered by Analog Devices, Inc.

Table 1. Voltage Noise

Package	0.9 nV	1.1 nV	1.8 nV	2.8 nV	3.8 nV
Single	AD797	AD8597	ADA4004-1	AD8675	AD8671
Dual		AD8599	ADA4004-2	AD8676	AD8672
Quad			ADA4004-4		AD8674

Rev. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

7/12—Rev. D to Rev. E
Added Power Sequencing Section 5
Added Figure 28 and Figure 29; Renumbered Sequentially 10

8/11—Rev. C to Rev. D
Added Input Capacitance, Common Mode Parameter and Input Capacitance, Differential Mode Parameter, Table 3 4

6/10—Rev. B to Rev. C
Changes to Figure 10 7

5/10—Rev. A to Rev. B
Changes to General Description Section 1
Added Table 1; Renumbered Sequentially 1
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Added Figure 27; Renumbered Sequentially 10
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4/07—Rev. 0 to Rev. A
Added Figure 7 and Figure 8; Renumbered Sequentially 6

10/05—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_S = ±5.0 V, V_{CM} = 0 V, V_O = 0 V, T_A = +25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	75	µV
		−40°C ≤ T_A ≤ +125°C		12	240	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.2	0.6	µV/°C
Input Bias Current	I_B		−2	+0.5	+2	nA
		−40°C ≤ T_A ≤ +125°C	−5.5	−2	+5.5	nA
Input Offset Current	I_{OS}		−1	+0.1	+1	nA
		−40°C ≤ T_A ≤ +125°C	−2.8	+0.1	+2.8	nA
Input Voltage Range	IVR		−3.0		+3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.0 V to +3.0 V	105	130		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ to ground, V_O = −3.5 V to +3.5 V	120	126		dB
		−40°C ≤ T_A ≤ +125°C	117			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to ground	4.90	4.95		V
		−40°C ≤ T_A ≤ +125°C	4.85			V
		R_L = 2 kΩ to ground	4.80	4.90		V
		−40°C ≤ T_A ≤ +125°C	4.75			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to ground		−4.98	−4.90	V
		−40°C ≤ T_A ≤ +125°C			−4.85	V
		R_L = 2 kΩ to ground		−4.91	−4.86	V
		−40°C ≤ T_A ≤ +125°C			−4.82	V
Short-Circuit Limit	I_{SC}			±35		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±5.0 V to ±15.0 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		2.3	2.7	mA
		−40°C ≤ T_A ≤ +125°C			3.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		2.5		V/µs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\,p\text{-}p}$	0.1 Hz to 10 Hz		0.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		0.3		pA/√Hz

V_S = ±15 V, V_{CM} = 0 V, V_O = 0 V, T_A = +25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	75	µV
		−40°C ≤ T_A ≤ +125°C		12	240	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.2	0.6	µV/°C
Input Bias Current	I_B		−2	+0.5	+2	nA
		−40°C ≤ T_A ≤ +125°C	−4.5	+1	+4.5	nA
Input Offset Current	I_{OS}		−1	+0.1	+1	nA
		−40°C ≤ T_A ≤ +125°C	−2.8	+0.1	+2.8	nA
Input Voltage Range	IVR		−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	114	130		dB
		−40°C ≤ T_A ≤ +125°C	114			dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ to ground, V_O = −13.5 V to +13.5 V	123	132		dB
		−40°C ≤ T_A ≤ +125°C	117			dB
Input Capacitance, Common Mode	C_{INCM}			3.8		pF
Input Capacitance, Differential Mode	C_{INDM}			9.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to ground	14.85	14.92		V
		−40°C ≤ T_A ≤ +125°C	14.80			V
		R_L = 2 kΩ to ground	14.60	14.80		V
		−40°C ≤ T_A ≤ +125°C	14.40			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to ground		−14.96	−14.94	V
		−40°C ≤ T_A ≤ +125°C			−14.90	V
		R_L = 2 kΩ to ground		−14.85	−14.75	V
		−40°C ≤ T_A ≤ +125°C			−14.69	V
Short-Circuit Limit	I_{SC}			±35		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±5.0 V to ±15.0 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		2.5	2.9	mA
		−40°C ≤ T_A ≤ +125°C			3.8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.5		V/µs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\,p\text{-}p}$	0.1 Hz to 10 Hz		0.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		0.3		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±V supply
Input Current	±5 mA
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
RM-8, R-8 Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	
RM-8, R-8 Packages	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C
NULL Pins (Pin 1, Pin 8), Input Current Maximum	<50 μA, V_S < V+

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages and measured using a standard 4-layer board, unless otherwise specified.

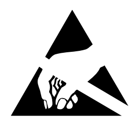
Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead SOIC_N (R-8)	120	45	°C/W

POWER SEQUENCING

Establish the op amp supplies simultaneously with, or before, any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

±15 V and ±5 V, T_A = 25°C, unless otherwise specified.

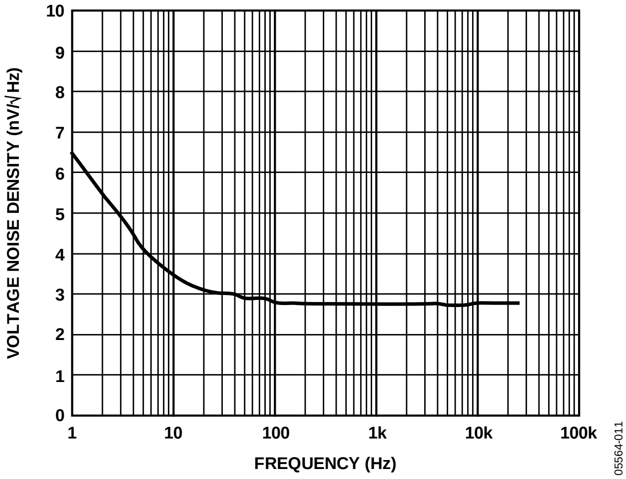


Figure 3. Voltage Noise Density vs. Frequency

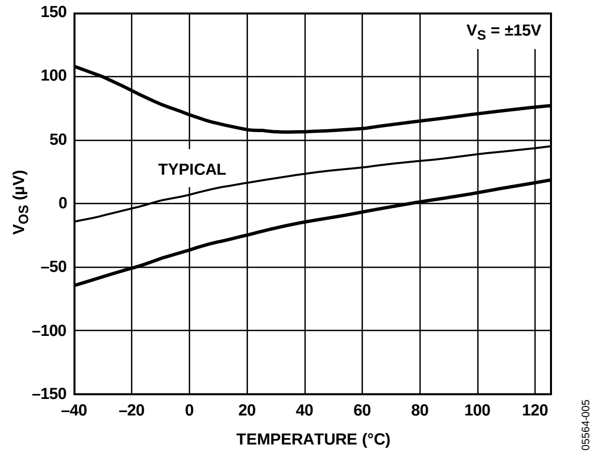


Figure 6. Offset Voltage vs. Temperature

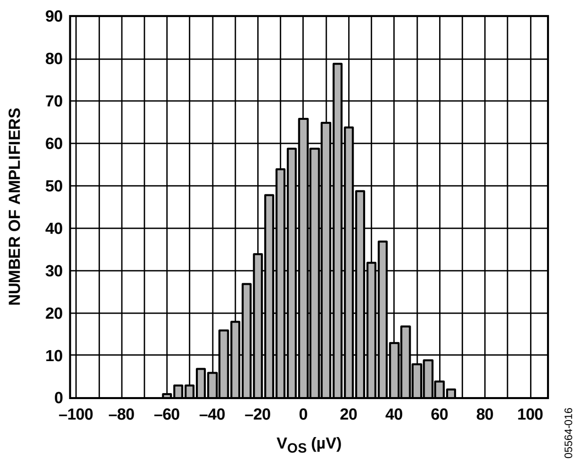


Figure 4. Input Offset Voltage Distribution

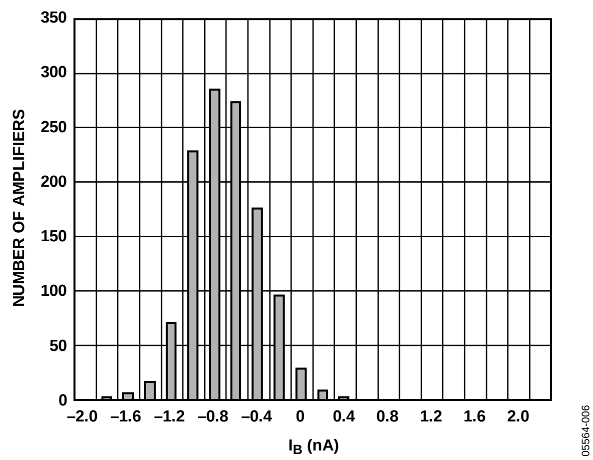


Figure 7. Input Bias Current, V_S = ±15 V

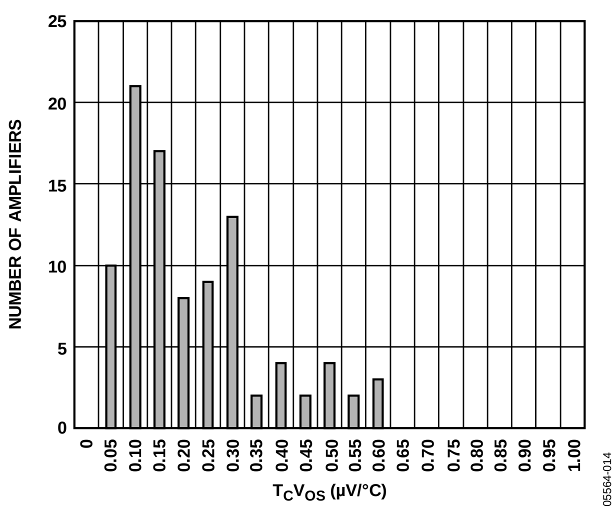


Figure 5. T_CV_{OS}

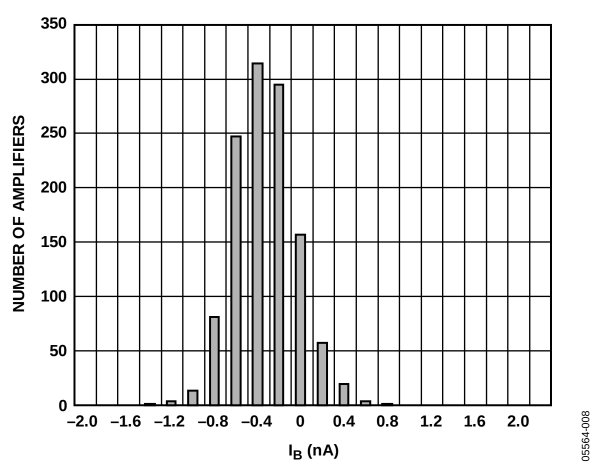


Figure 8. Input Bias Current, V_S = ±5 V

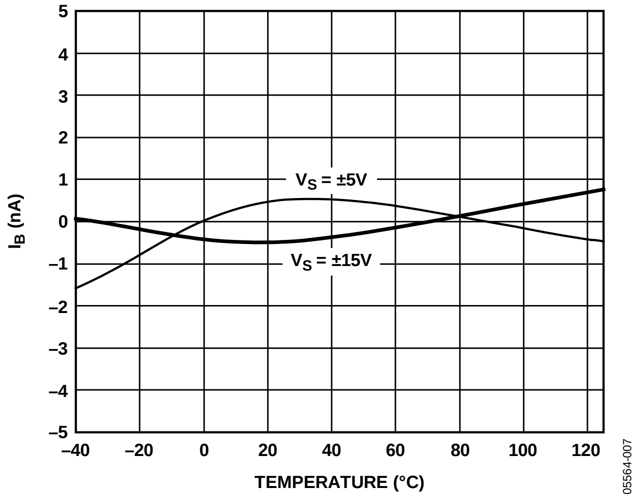


Figure 9. Input Bias Current vs. Temperature

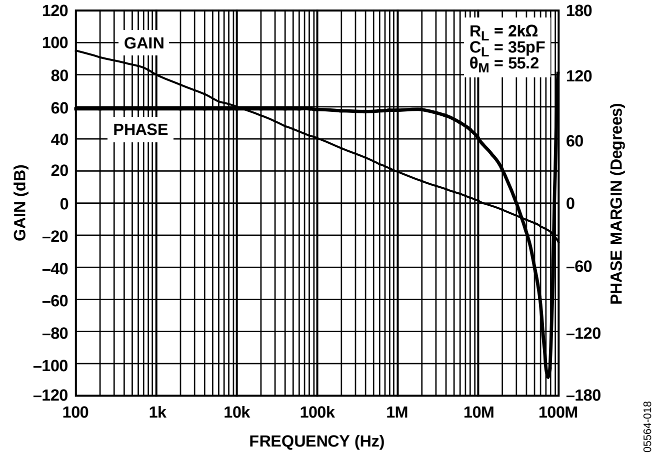


Figure 12. Gain and Phase vs. Frequency

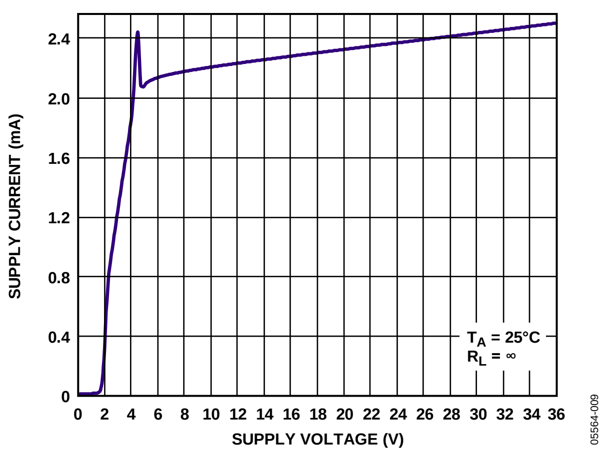


Figure 10. Supply Current vs. Total Supply Voltage

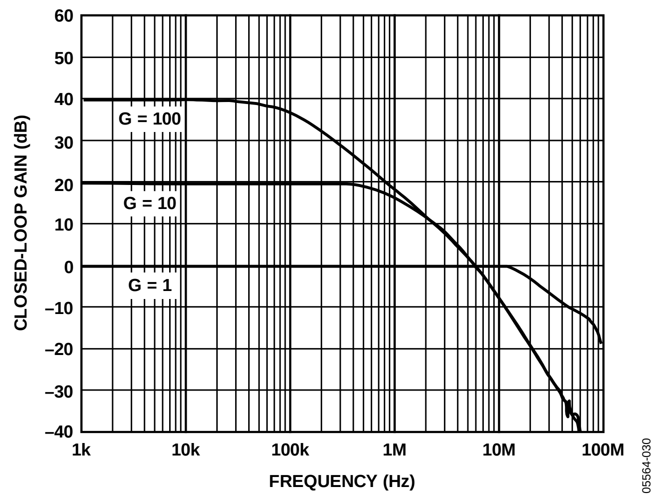


Figure 13. Closed-Loop Gain vs. Frequency

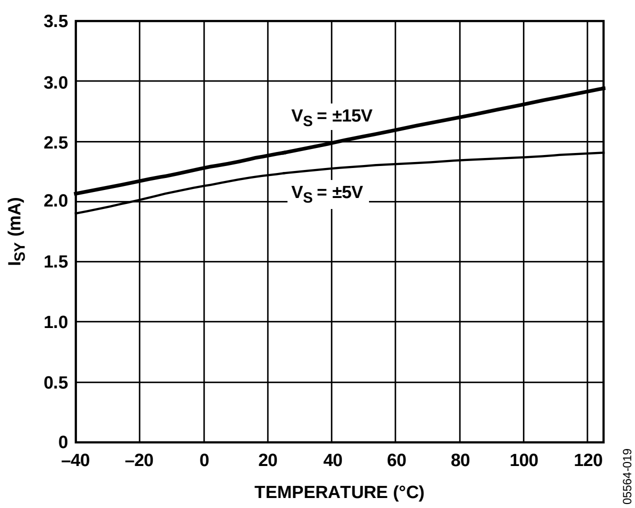


Figure 11. Supply Current vs. Temperature

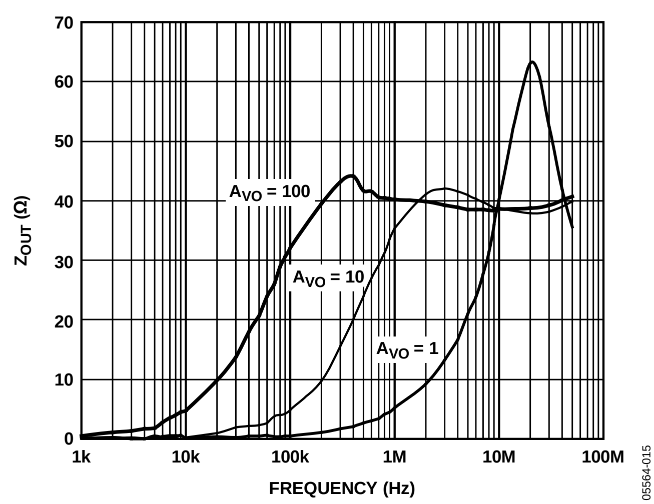


Figure 14. Z_{OUT} vs. Frequency

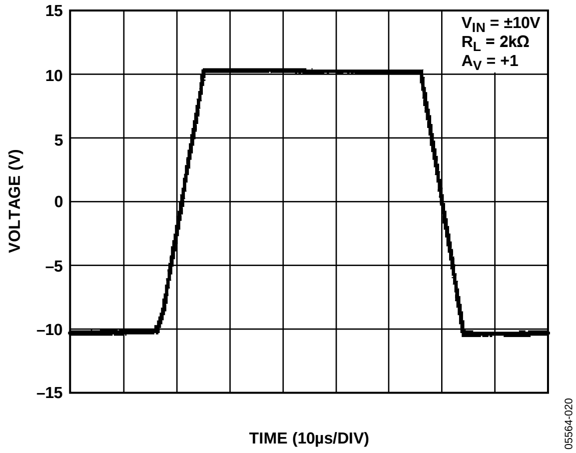


Figure 15. Large-Signal Transient Response, $V_{SY} = \pm 15$ V

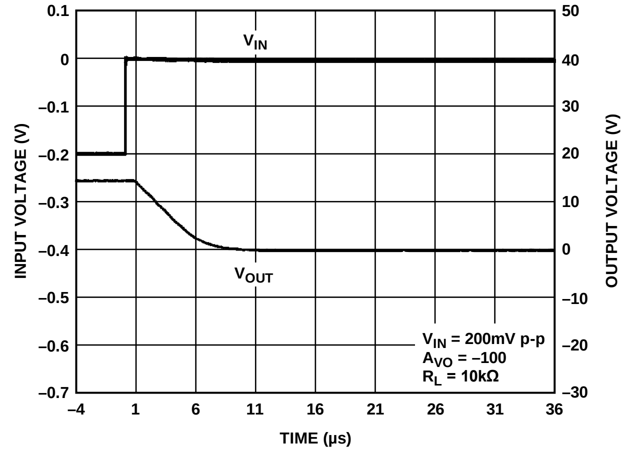


Figure 18. Positive Overvoltage Recovery

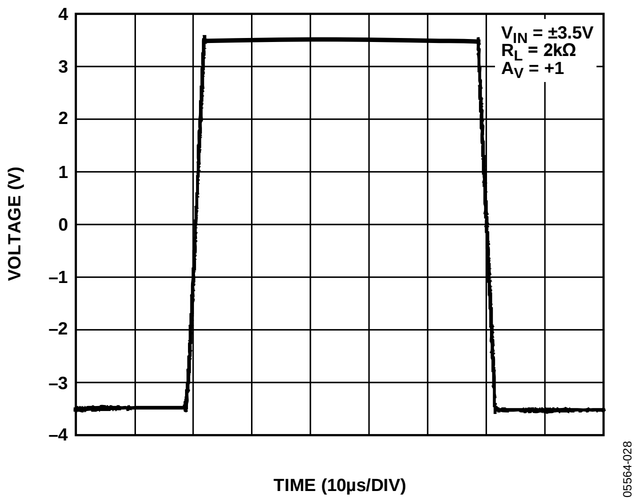


Figure 16. Large-Signal Transient Response, $V_{SY} = \pm 5$ V

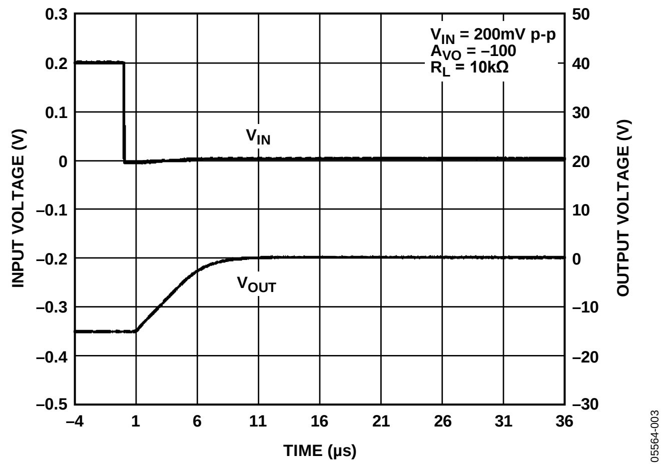


Figure 19. Negative Overvoltage Recovery

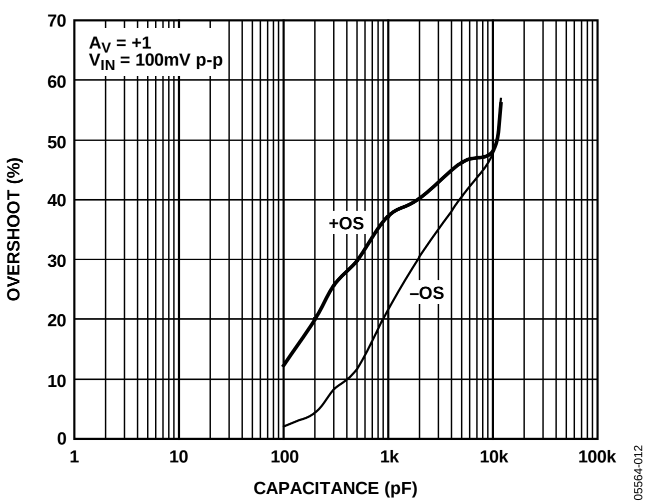


Figure 17. Small-Signal Overshoot vs. Load Capacitance

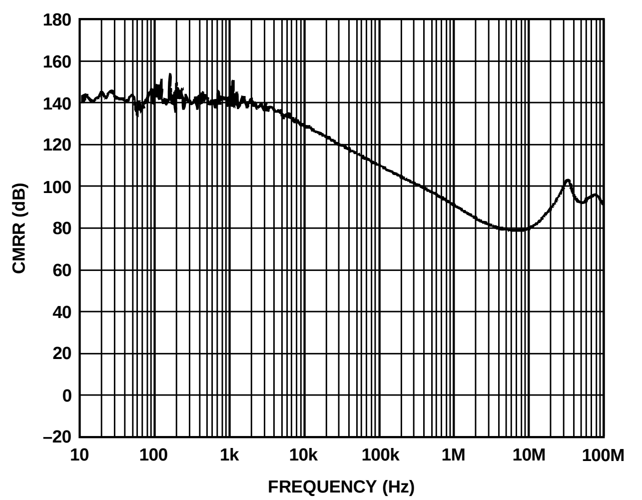


Figure 20. CMRR vs. Frequency

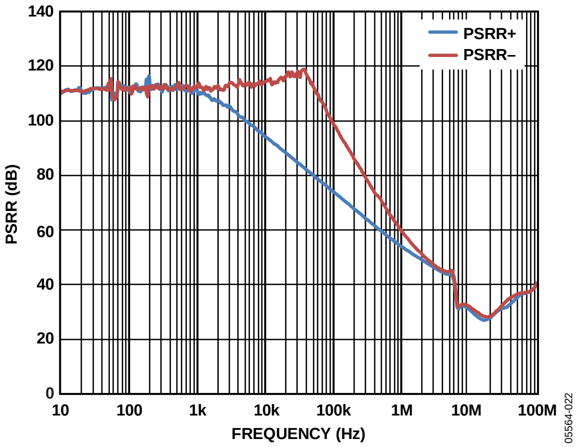


Figure 21. Power Supply Rejection Ratio vs. Frequency

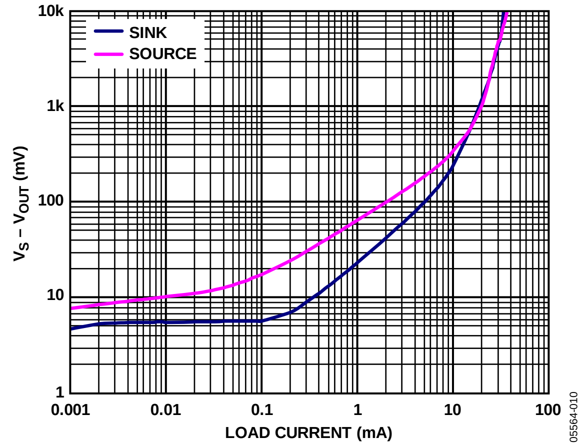


Figure 24. Output Saturation Voltage vs. Output Current

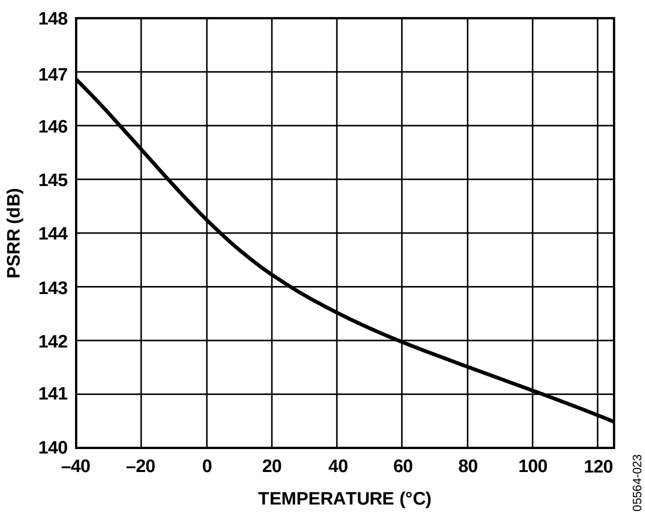


Figure 22. Power Supply Rejection Ratio vs. Temperature

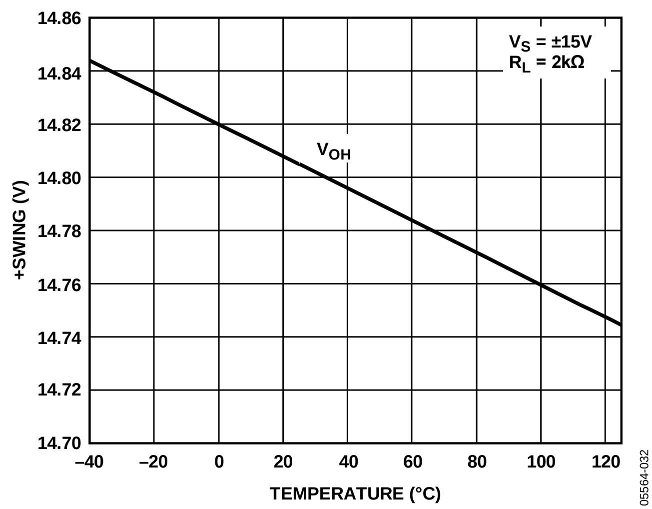


Figure 25. Swing vs. Temperature, V_{OH}

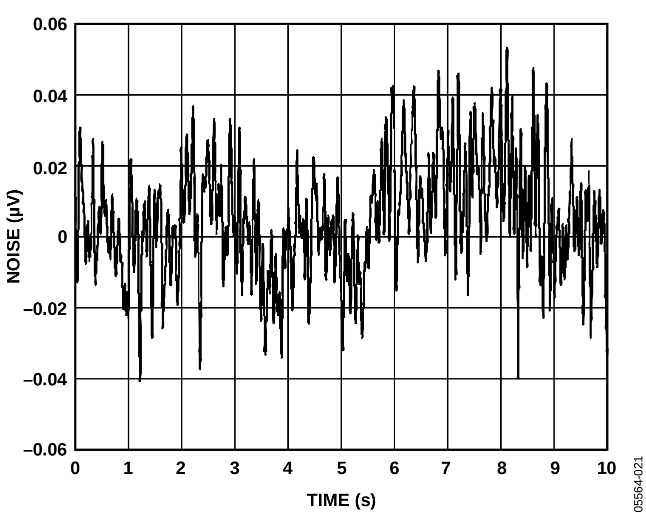


Figure 23. Voltage Noise (0.1 Hz to 10 Hz)

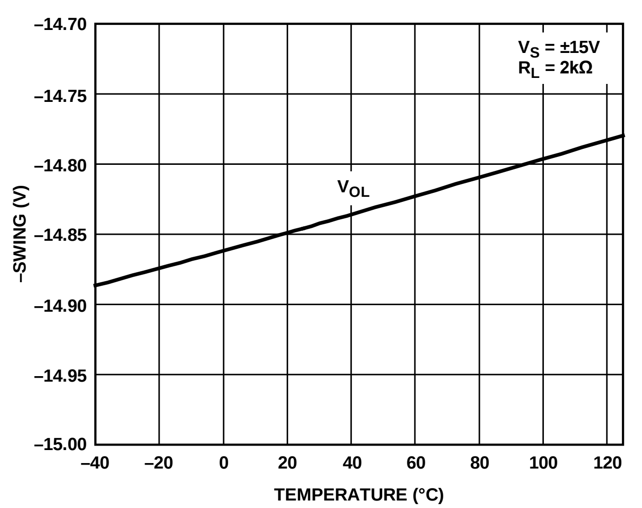


Figure 26. Swing vs. Temperature, V_{OL}

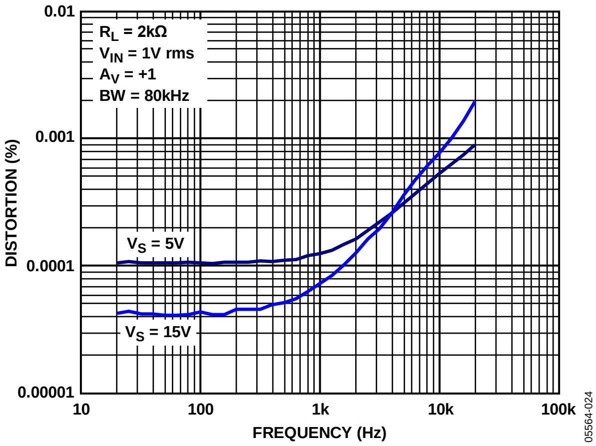


Figure 27. Distortion vs. Frequency

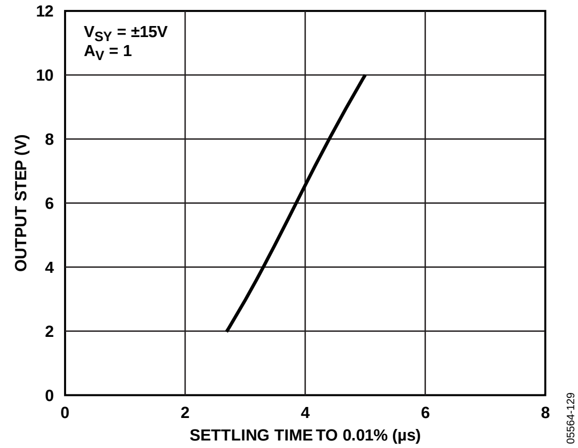


Figure 29. Output Step vs. Settling Time to 0.01%

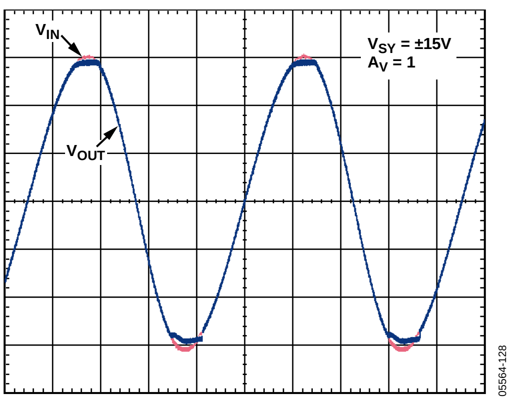


Figure 28. No Phase Reversal

TEST CIRCUIT

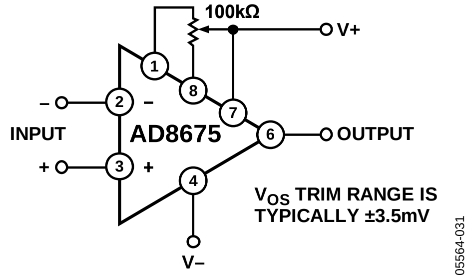


Figure 30. Optional Offset Nulling Circuit