Low Power, 12.65 mW, 2.3 V to 5.5 V, Programmable Waveform Generator

Data Sheet **AD9833**

FEATURES

- Digitally programmable frequency and phase
- 12.65 mW power consumption at 3 V
- 0 MHz to 12.5 MHz output frequency range
- 28-bit resolution: 0.1 Hz at 25 MHz reference clock
- Sinusoidal, triangular, and square wave outputs
- 2.3 V to 5.5 V power supply
- No external components required
- 3-wire SPI interface
- Extended temperature range: −40°C to +105°C
- Power-down option
- 10-lead MSOP package
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Frequency stimulus/waveform generation
- Liquid and gas flow measurement
- Sensory applications: proximity, motion, and defect detection
- Line loss/attenuation
- Test and medical equipment
- Sweep/clock generators
- Time domain reflectometry (TDR) applications

GENERAL DESCRIPTION

The AD9833 is a low power, programmable waveform generator capable of producing sine, triangular, and square wave outputs. Waveform generation is required in various types of sensing, actuation, and time domain reflectometry (TDR) applications. The output frequency and phase are software programmable, allowing easy tuning. No external components are needed. The frequency registers are 28 bits wide: with a 25 MHz clock rate, resolution of 0.1 Hz can be achieved; with a 1 MHz clock rate, the AD9833 can be tuned to 0.004 Hz resolution.

The AD9833 is written to via a 3-wire serial interface. This serial interface operates at clock rates up to 40 MHz and is compatible with DSP and microcontroller standards. The device operates with a power supply from 2.3 V to 5.5 V.

The AD9833 has a power-down function (SLEEP). This function allows sections of the device that are not being used to be powered down, thus minimizing the current consumption of the part. For example, the DAC can be powered down when a clock output is being generated.

The AD9833 is available in a 10-lead MSOP package.

FUNCTIONAL BLOCK DIAGRAM

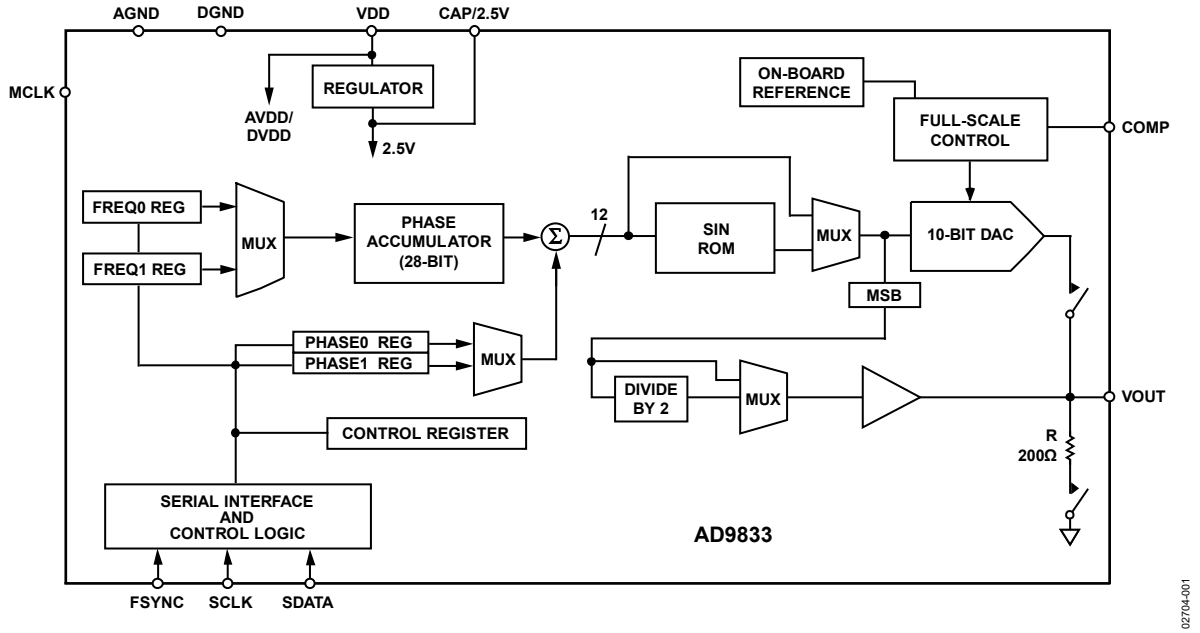

Figure 1.

Rev. G
Document Feedback

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SPECIFICATIONS

VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, R_{SET} = 6.8 kΩ for VOUT, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate			25	MSPS	
VOUT Maximum		0.65		V	
VOUT Minimum		38		mV	
VOUT Temperature Coefficient		200		ppm/°C	
DC Accuracy					
Integral Nonlinearity		±1.0		LSB	
Differential Nonlinearity		±0.5		LSB	
DDS SPECIFICATIONS (SFDR)					
Dynamic Specifications					
Signal-to-Noise Ratio (SNR)	55	60		dB	AD9833BRMZ, f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/4096
	54	60		dB	AD9833WBRMZ-REEL, f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/4096
Total Harmonic Distortion (THD)		−66	−56	dBc	AD9833BRMZ, f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/4096
		−66	−55	dBc	AD9833WBRMZ-REEL, f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/4096
Spurious-Free Dynamic Range (SFDR)					
Wideband (0 to Nyquist)		−60		dBc	f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/50
Narrow-Band (±200 kHz)		−78		dBc	f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/50
Clock Feedthrough		−60		dBc	
Wake-Up Time		1		ms	
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.7			V	2.3 V to 2.7 V power supply
	2.0			V	2.7 V to 3.6 V power supply
	2.8			V	4.5 V to 5.5 V power supply
Input Low Voltage, V_{INL}			0.5	V	2.3 V to 2.7 V power supply
			0.7	V	2.7 V to 3.6 V power supply
			0.8	V	4.5 V to 5.5 V power supply
Input Current, I_{INH}/I_{INL}			10	µA	
Input Capacitance, C_{IN}		3		pF	
POWER SUPPLIES					f_{MCLK} = 25 MHz, f_{OUT} = f_{MCLK}/4096
VDD	2.3		5.5	V	
I_{DD}		4.5	5.5	mA	I_{DD} code dependent; see Figure 7
Low Power Sleep Mode		0.5		mA	DAC powered down, MCLK running

[1] Operating temperature range is −40°C to +105°C; typical specifications are at +25°C.

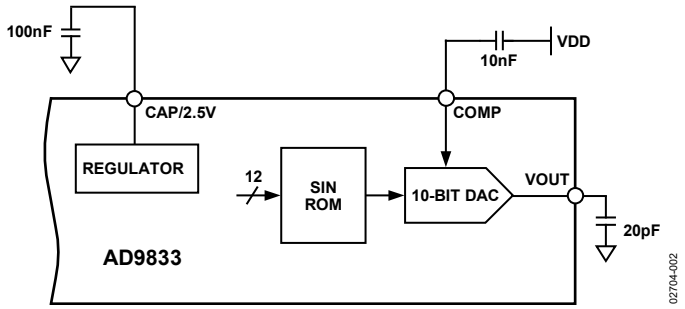

Figure 2. Test Circuit Used to Test Specifications

TIMING CHARACTERISTICS

VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	40	ns min	MCLK period
t_2	16	ns min	MCLK high duration
t_3	16	ns min	MCLK low duration
t_4	25	ns min	SCLK period
t_5	10	ns min	SCLK high duration
t_6	10	ns min	SCLK low duration
t_7	5	ns min	FSYNC to SCLK falling edge setup time
$t_{8\ min}$	10	ns min	FSYNC to SCLK hold time
$t_{8\ max}$	$t_4 - 5$	ns max	
t_9	5	ns min	Data setup time
t_{10}	3	ns min	Data hold time
t_{11}	5	ns min	SCLK high to FSYNC falling edge setup time

[1] Guaranteed by design, not production tested.

Timing Diagrams

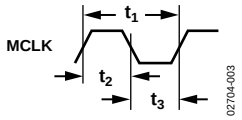

Figure 3. Master Clock

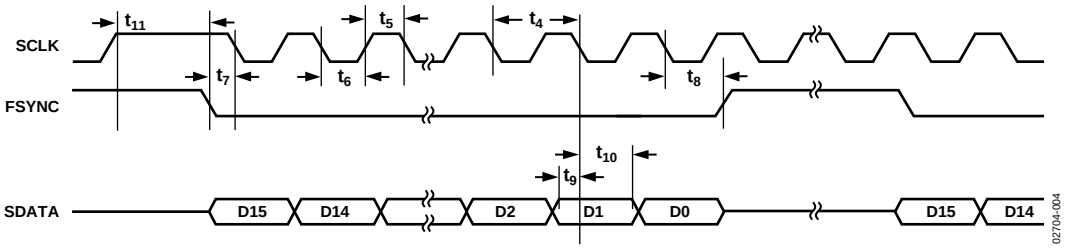

Figure 4. Serial Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to AGND	−0.3 V to +6 V
VDD to DGND	−0.3 V to +6 V
AGND to DGND	−0.3 V to +0.3 V
CAP/2.5V	2.75 V
Digital I/O Voltage to DGND	−0.3 V to VDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

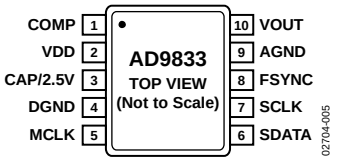

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	DAC Bias Pin. This pin is used for decoupling the DAC bias voltage.
2	VDD	Positive Power Supply for the Analog and Digital Interface Sections. The on-board 2.5 V regulator is also supplied from VDD. VDD can have a value from 2.3 V to 5.5 V. A 0.1 µF and a 10 µF decoupling capacitor should be connected between VDD and AGND.
3	CAP/2.5V	The digital circuitry operates from a 2.5 V power supply. This 2.5 V is generated from VDD using an on-board regulator when VDD exceeds 2.7 V. The regulator requires a decoupling capacitor of 100 nF typical, which is connected from CAP/2.5V to DGND. If VDD is less than or equal to 2.7 V, CAP/2.5V should be tied directly to VDD.
4	DGND	Digital Ground.
5	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. This clock determines the output frequency accuracy and phase noise.
6	SDATA	Serial Data Input. The 16-bit serial data-word is applied to this input.
7	SCLK	Serial Clock Input. Data is clocked into the AD9833 on each falling edge of SCLK.
8	FSYNC	Active Low Control Input. FSYNC is the frame synchronization signal for the input data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
9	AGND	Analog Ground.
10	VOUT	Voltage Output. The analog and digital output from the AD9833 is available at this pin. An external load resistor is not required because the device has a 200 Ω resistor on-board.

TYPICAL PERFORMANCE CHARACTERISTICS

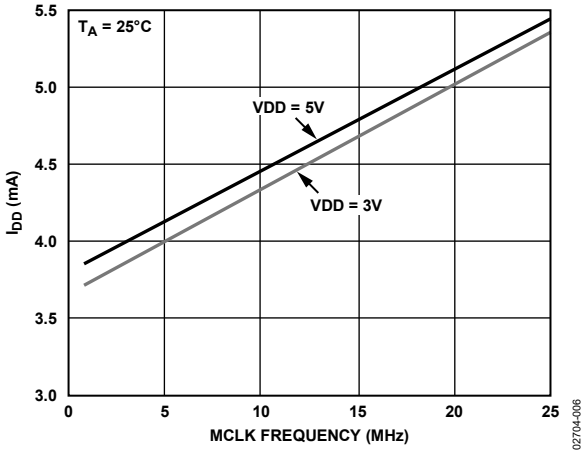

Figure 6. Typical Current Consumption (I_{DD}) vs. MCLK Frequency for f_{OUT} = MCLK/10

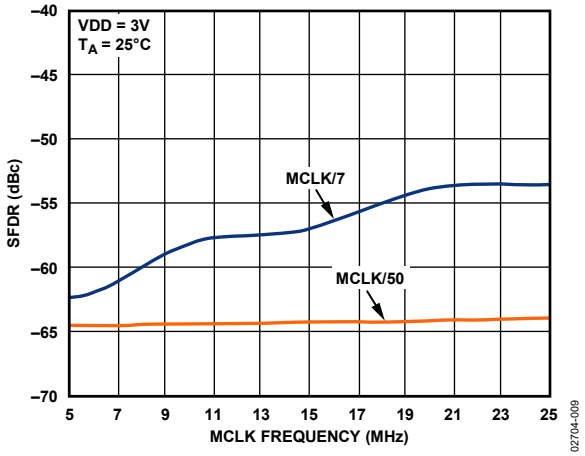

Figure 9. Wideband SFDR vs. MCLK Frequency

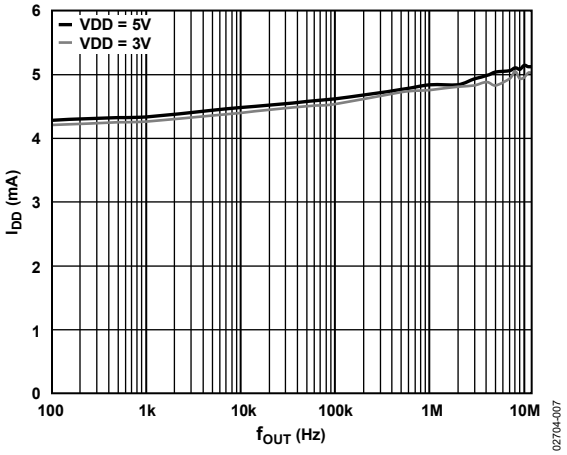

Figure 7. Typical I_{DD} vs. f_{OUT} for f_{MCLK} = 25 MHz

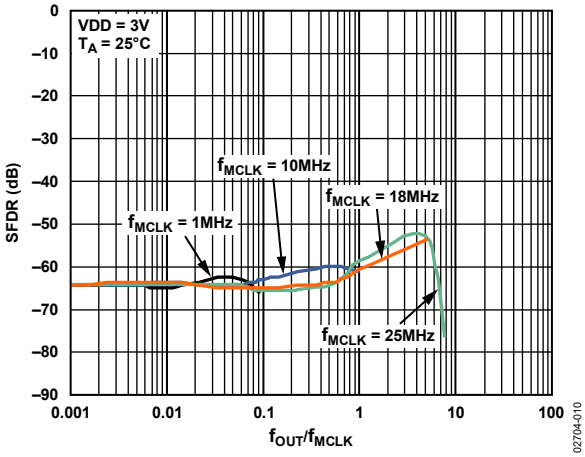

Figure 10. Wideband SFDR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

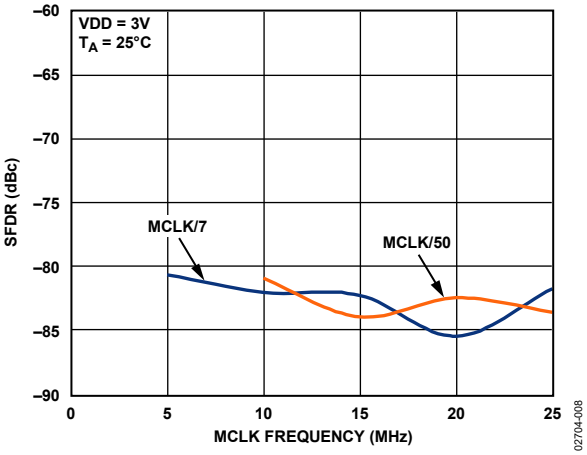

Figure 8. Narrow-Band SFDR vs. MCLK Frequency

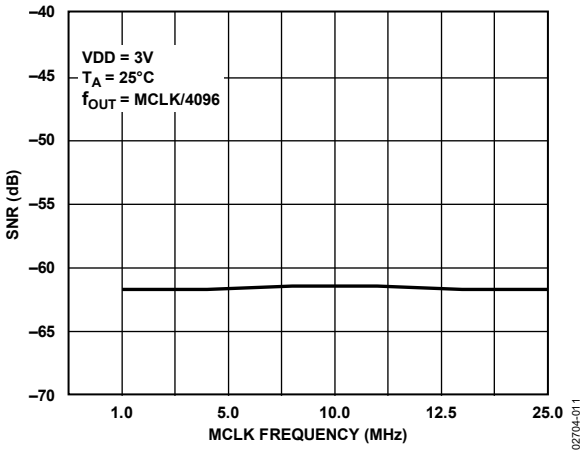

Figure 11. SNR vs. MCLK Frequency

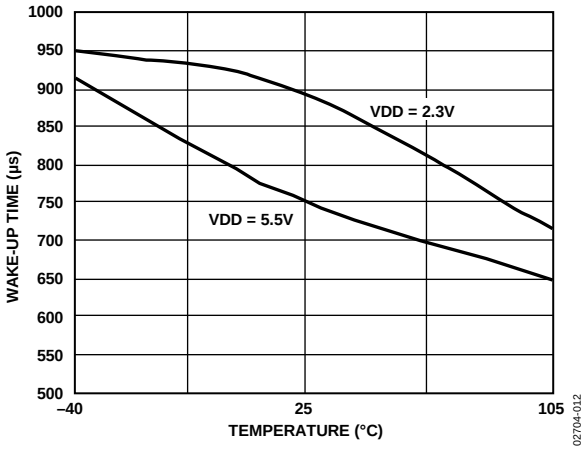

Figure 12. Wake-Up Time vs. Temperature

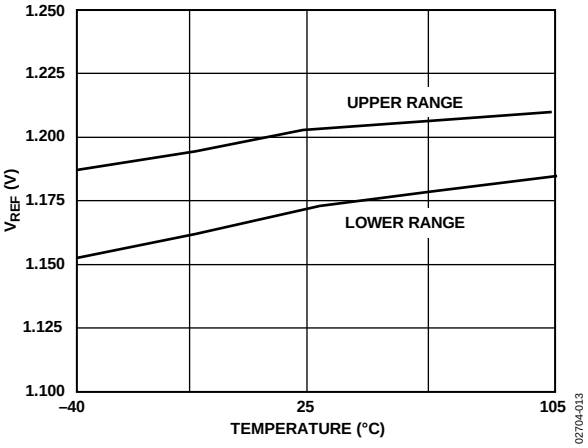

Figure 13. V_{REF} vs. Temperature

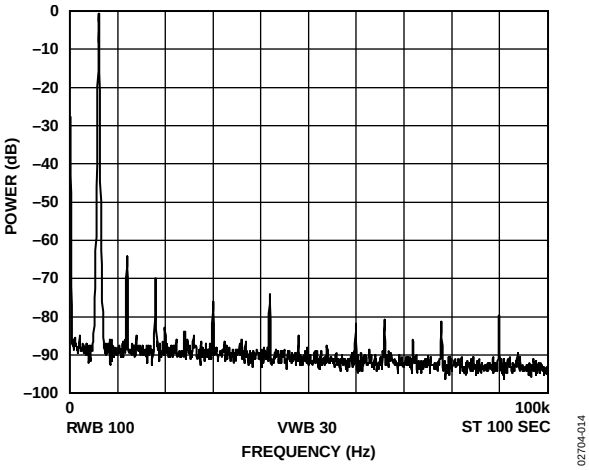

Figure 14. Power vs. Frequency, f_{MCLK} = 10 MHz, f_{OUT} = 2.4 kHz, Frequency Word = 0x000FBA9

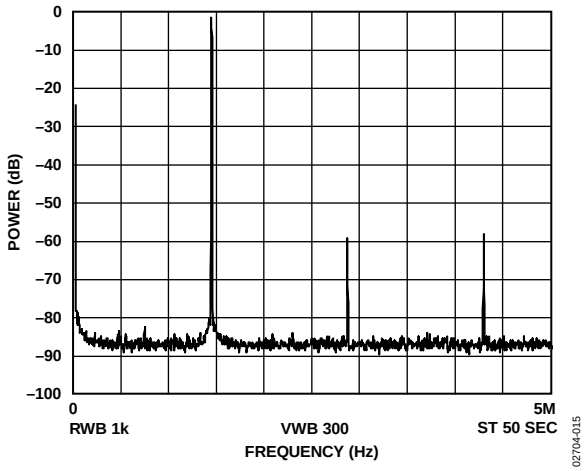

Figure 15. Power vs. Frequency, f_{MCLK} = 10 MHz, f_{OUT} = 1.43 MHz = f_{MCLK}/7, Frequency Word = 0x2492492

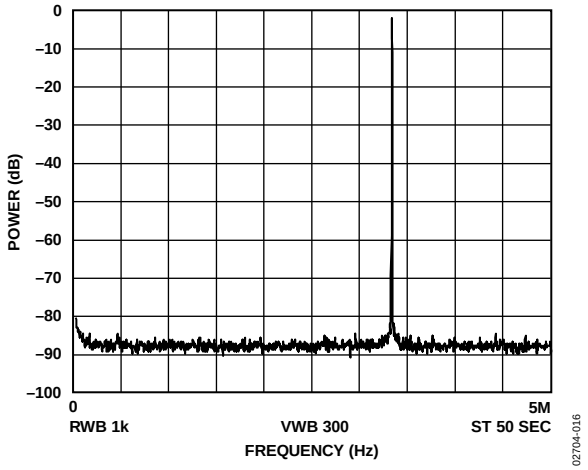

Figure 16. Power vs. Frequency, f_{MCLK} = 10 MHz, f_{OUT} = 3.33 MHz = f_{MCLK}/3, Frequency Word = 0x5555555

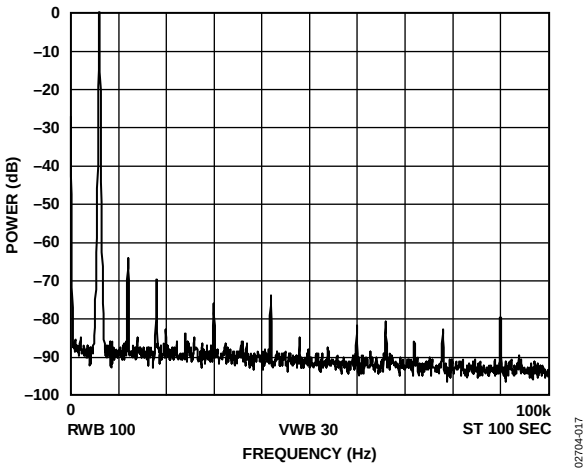

Figure 17. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 6 kHz, Frequency Word = 0x000FBA9

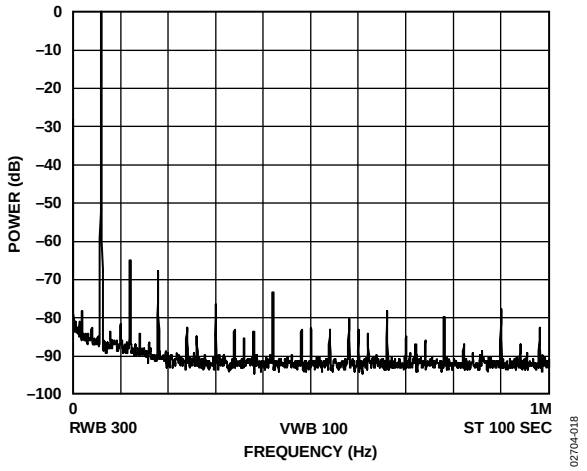

Figure 18. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 60 kHz, Frequency Word = 0x009D495

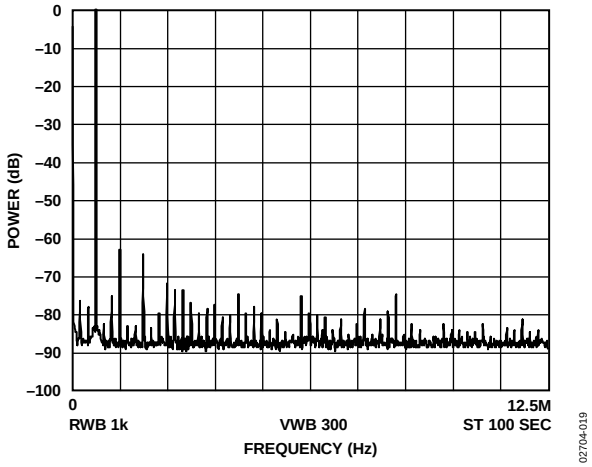

Figure 19. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 600 kHz, Frequency Word = 0x0624DD3

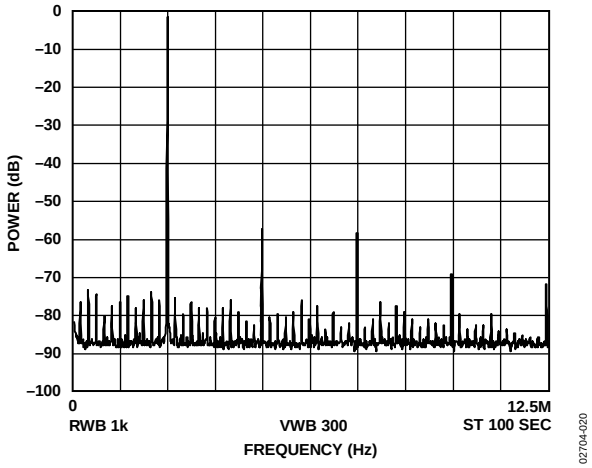

Figure 20. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 2.4 MHz, Frequency Word = 0x189374D

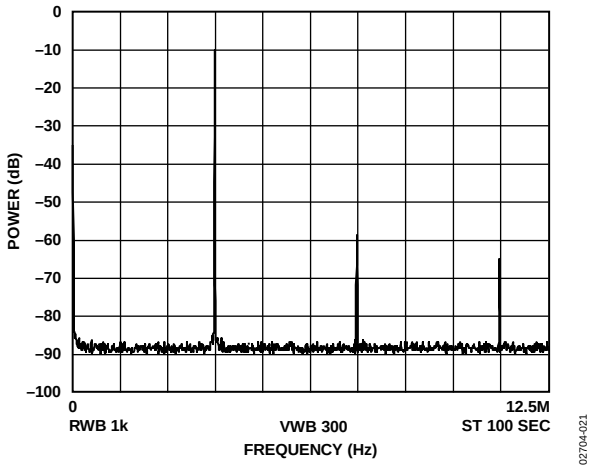

Figure 21. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 3.857 MHz = f_{MCLK}/7, Frequency Word = 0x2492492

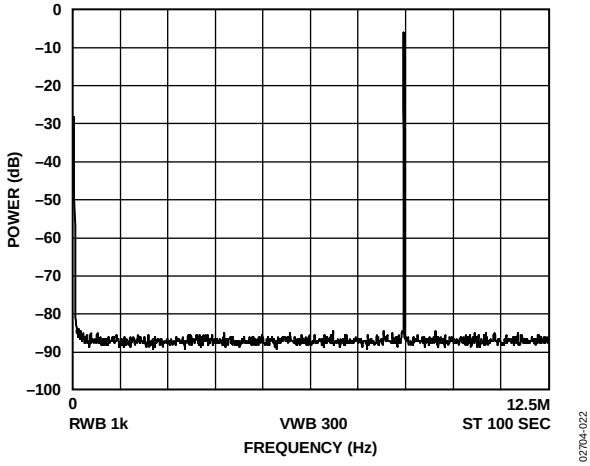

Figure 22. Power vs. Frequency, f_{MCLK} = 25 MHz, f_{OUT} = 8.333 MHz = f_{MCLK}/3, Frequency Word = 0x5555555

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 … 00 to 000 … 01), and full scale, a point 0.5 LSB above the last code transition (111 … 10 to 111 … 11). The error is expressed in LSBs.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC. A specified DNL of ±1 LSB maximum ensures monotonicity.

Output Compliance
Output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9833 may not meet the specifications listed in the data sheet.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. SFDR refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest spur or harmonic relative to the magnitude of the fundamental frequency in the zero to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz about the fundamental frequency.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9833, THD is defined as

$$\text{THD} = 20\log\sqrt{\frac{V_2^2+V_3^2+V_4^2+V_5^2+V_6^2}{V_1}}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Clock Feedthrough
There is feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the output spectrum of the AD9833.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form: a(t) = sin(ωt). However, these sine waves are nonlinear and not easy to generate except through piecewise construction. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of $\omega = 2\pi f$.

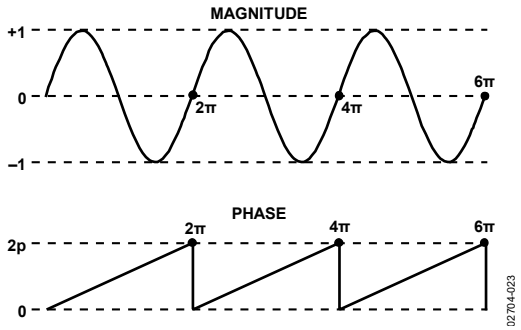

Figure 23. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined.

$$\Delta Phase = \omega \Delta t$$

Solving for ω,

$$\omega = \Delta Phase/\Delta t = 2\pi f$$

Solving for f and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \Delta t$)

$$f = \Delta Phase \times f_{MCLK}/2\pi$$

The AD9833 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits: numerically controlled oscillator (NCO) and phase modulator, SIN ROM, and digital-to-analog converter (DAC).

Each subcircuit is described in the Circuit Description section.

CIRCUIT DESCRIPTION

The AD9833 is a fully integrated direct digital synthesis (DDS) chip. The chip requires one reference clock, one low precision resistor, and decoupling capacitors to provide digitally created sine waves up to 12.5 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain, allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

The internal circuitry of the AD9833 consists of the following main sections: a numerically controlled oscillator (NCO), frequency and phase modulators, SIN ROM, a DAC, and a regulator.

NUMERICALLY CONTROLLED OSCILLATOR PLUS PHASE MODULATOR

This consists of two frequency select registers, a phase accumulator, two phase offset registers, and a phase offset adder. The main component of the NCO is a 28-bit phase accumulator. Continuous time signals have a phase range of 0 to 2π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9833 is implemented with 28 bits. Therefore, in the AD9833, $2\pi = 2^{28}$. Likewise, the ΔPhase term is scaled into this range of numbers:

$$0 < \Delta Phase < 2^{28} - 1$$

With these substitutions, the previous equation becomes

$$f = \Delta Phase \times f_{MCLK}/2^{28}$$

where $0 < \Delta Phase < 2^{28} - 1$.

The input to the phase accumulator can be selected from either the FREQ0 register or the FREQ1 register and is controlled by the FSELECT bit. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit phase registers. The contents of one of these phase registers are added to the most significant bits of the NCO. The AD9833 has two phase registers; their resolution is 2π/4096.

SIN ROM

To make the output from the NCO useful, it must be converted from phase information into a sinusoidal value. Because phase information maps directly into amplitude, the SIN ROM uses the digital phase information as an address to a lookup table and converts the phase information into amplitude. Although the NCO contains a 28-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary, because this would require a lookup table of 2^{28} entries. It is necessary only to have sufficient phase resolution such that the errors due to truncation are smaller than the resolution of the 10-bit DAC. This requires that the SIN ROM have two bits of phase resolution more than the 10-bit DAC.

The SIN ROM is enabled using the mode bit (D1) in the control register (see Table 15).

DIGITAL-TO-ANALOG CONVERTER (DAC)

The AD9833 includes a high impedance, current source 10-bit DAC. The DAC receives the digital words from the SIN ROM and converts them into the corresponding analog voltages.

The DAC is configured for single-ended operation. An external load resistor is not required because the device has a 200 Ω resistor on-board. The DAC generates an output voltage of typically 0.6 V p-p.

REGULATOR

VDD provides the power supply required for the analog section and the digital section of the AD9833. This supply can have a value of 2.3 V to 5.5 V.

The internal digital section of the AD9833 is operated at 2.5 V. An on-board regulator steps down the voltage applied at VDD to 2.5 V. When the applied voltage at the VDD pin of the AD9833 is less than or equal to 2.7 V, the CAP/2.5V and VDD pins should be tied together, thus bypassing the on-board regulator.

FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The AD9833 has a standard 3-wire serial interface that is compatible with the SPI, QSPI™, MICROWIRE®, and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 4.

The FSYNC input is a level-triggered input that acts as a frame synchronization and chip enable. Data can be transferred into the device only when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC-to-SCLK falling edge setup time, t_7. After FSYNC goes low, serial data is shifted into the input shift register of the device on the falling edges of SCLK for 16 clock pulses. FSYNC may be taken high after the 16th falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8. Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses and then brought high at the end of the data transfer. In this way, a continuous stream of 16-bit words can be loaded while FSYNC is held low; FSYNC goes high only after the 16th SCLK falling edge of the last word loaded.

The SCLK can be continuous, or it can idle high or low between write operations. In either case, it must be high when FSYNC goes low (t_{11}).

For an example of how to program the AD9833, see the AN-1070 Application Note on the Analog Devices, Inc., website.

POWERING UP THE AD9833

The flowchart in Figure 26 shows the operating routine for the AD9833. When the AD9833 is powered up, the part should be reset. This resets the appropriate internal registers to 0 to provide an analog output of midscale.

To avoid spurious DAC outputs during AD9833 initialization, the reset bit should be set to 1 until the part is ready to begin generating an output. A reset does not reset the phase, frequency, or control registers. These registers will contain invalid data and, therefore, should be set to known values by the user. The reset bit should then be set to 0 to begin generating an output. The data appears on the DAC output seven or eight MCLK cycles after the reset bit is set to 0.

LATENCY PERIOD

A latency period is associated with each asynchronous write operation in the AD9833. If a selected frequency or phase register is loaded with a new word, there is a delay of seven or eight MCLK cycles before the analog output changes. The delay can be seven or eight cycles, depending on the position of the MCLK rising edge when the data is loaded into the destination register.

CONTROL REGISTER

The AD9833 contains a 16-bit control register that allows the user to configure the operation of the AD9833. All control bits other than the mode bit are sampled on the internal falling edge of MCLK.

Table 6 describes the individual bits of the control register. The different functions and the various output options of the AD9833 are described in more detail in the Frequency and Phase Registers section.

To inform the AD9833 that the contents of the control register will be altered, D15 and D14 must be set to 0, as shown in Table 5.

Table 5. Control Register Bits

D15	D14	D13	D0
0	0	Control Bits	

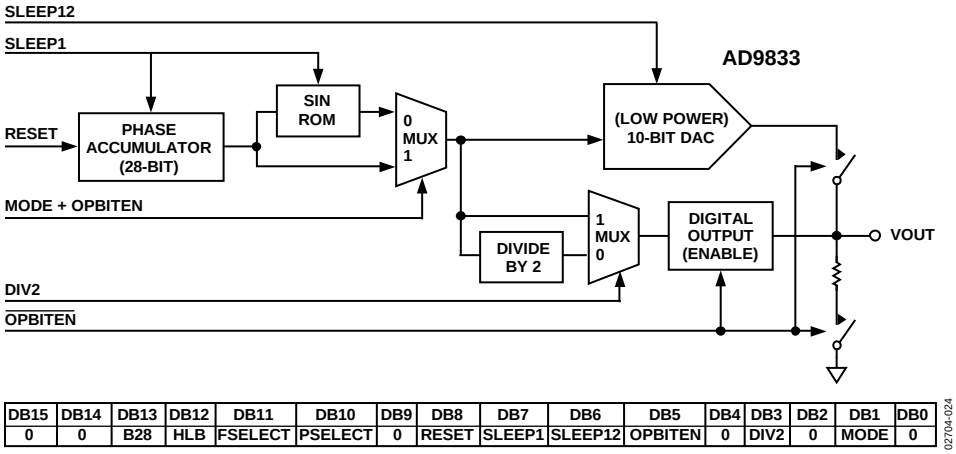

Figure 24. Function of Control Bits

Table 6. Description of Bits in the Control Register

Bit	Name	Function
D13	B28	Two write operations are required to load a complete word into either of the frequency registers. B28 = 1 allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains the 14 LSBs of the frequency word, and the next write contains the 14 MSBs. The first two bits of each 16-bit word define the frequency register to which the word is loaded, and should therefore be the same for both of the consecutive writes. See Table 8 for the appropriate addresses. The write to the frequency register occurs after both words have been loaded; therefore, the register never holds an intermediate value. An example of a complete 28-bit write is shown in Table 9. When B28 = 0, the 28-bit frequency register operates as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs, and vice versa. To alter the 14 MSBs or the 14 LSBs, a single write is made to the appropriate frequency address. The control bit D12 (HLB) informs the AD9833 whether the bits to be altered are the 14 MSBs or 14 LSBs.
D12	HLB	This control bit allows the user to continuously load the MSBs or LSBs of a frequency register while ignoring the remaining 14 bits. This is useful if the complete 28-bit resolution is not required. HLB is used in conjunction with D13 (B28). This control bit indicates whether the 14 bits being loaded are being transferred to the 14 MSBs or 14 LSBs of the addressed frequency register. D13 (B28) must be set to 0 to be able to change the MSBs and LSBs of a frequency word separately. When D13 (B28) = 1, this control bit is ignored. HLB = 1 allows a write to the 14 MSBs of the addressed frequency register. HLB = 0 allows a write to the 14 LSBs of the addressed frequency register.
D11	FSELECT	The FSELECT bit defines whether the FREQ0 register or the FREQ1 register is used in the phase accumulator.
D10	PSELECT	The PSELECT bit defines whether the PHASE0 register or the PHASE1 register data is added to the output of the phase accumulator.
D9	Reserved	This bit should be set to 0.
D8	Reset	Reset = 1 resets internal registers to 0, which corresponds to an analog output of midscale. Reset = 0 disables reset. This function is explained further in Table 13.
D7	SLEEP1	When SLEEP1 = 1, the internal MCLK clock is disabled, and the DAC output remains at its present value because the NCO is no longer accumulating. When SLEEP1 = 0, MCLK is enabled. This function is explained further in Table 14.
D6	SLEEP12	SLEEP12 = 1 powers down the on-chip DAC. This is useful when the AD9833 is used to output the MSB of the DAC data. SLEEP12 = 0 implies that the DAC is active. This function is explained further in Table 14.
D5	OPBITEN	The function of this bit, in association with D1 (mode), is to control what is output at the VOUT pin. This is explained further in Table 15. When OPBITEN = 1, the output of the DAC is no longer available at the VOUT pin. Instead, the MSB (or MSB/2) of the DAC data is connected to the VOUT pin. This is useful as a coarse clock source. The DIV2 bit controls whether it is the MSB or MSB/2 that is output. When OPBITEN = 0, the DAC is connected to VOUT. The mode bit determines whether it is a sinusoidal or a ramp output that is available.
D4	Reserved	This bit must be set to 0.
D3	DIV2	DIV2 is used in association with D5 (OPBITEN). This is explained further in Table 15. When DIV2 = 1, the MSB of the DAC data is passed directly to the VOUT pin. When DIV2 = 0, the MSB/2 of the DAC data is output at the VOUT pin.
D2	Reserved	This bit must be set to 0.
D1	Mode	This bit is used in association with OPBITEN (D5). The function of this bit is to control what is output at the VOUT pin when the on-chip DAC is connected to VOUT. This bit should be set to 0 if the control bit OPBITEN = 1. This is explained further in Table 15. When mode = 1, the SIN ROM is bypassed, resulting in a triangle output from the DAC. When mode = 0, the SIN ROM is used to convert the phase information into amplitude information, which results in a sinusoidal signal at the output.
D0	Reserved	This bit must be set to 0.

FREQUENCY AND PHASE REGISTERS

The AD9833 contains two frequency registers and two phase registers, which are described in Table 7.

Table 7. Frequency and Phase Registers

Register	Size	Description
FREQ0	28 bits	Frequency Register 0. When the FSELECT bit = 0, this register defines the output frequency as a fraction of the MCLK frequency.
FREQ1	28 bits	Frequency Register 1. When the FSELECT bit = 1, this register defines the output frequency as a fraction of the MCLK frequency.
PHASE0	12 bits	Phase Offset Register 0. When the PSELECT bit = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1	12 bits	Phase Offset Register 1. When the PSELECT bit = 1, the contents of this register are added to the output of the phase accumulator.

The analog output from the AD9833 is

$$f_{MCLK}/2^{28} \times FREQREG$$

where *FREQREG* is the value loaded into the selected frequency register. This signal is phase shifted by

$$2\pi/4096 \times PHASEREG$$

where *PHASEREG* is the value contained in the selected phase register. Consideration must be given to the relationship of the selected output frequency and the reference clock frequency to avoid unwanted output anomalies.

The flowchart in Figure 28 shows the routine for writing to the frequency and phase registers of the AD9833.

Writing to a Frequency Register

When writing to a frequency register, Bit D15 and Bit D14 give the address of the frequency register.

Table 8. Frequency Register Bits

D15	D14	D13	D0
0	1	MSB 14 FREQ0 REG bits	LSB
1	0	MSB 14 FREQ1 REG bits	LSB

If the user wants to change the entire contents of a frequency register, two consecutive writes to the same address must be performed because the frequency registers are 28 bits wide. The first write contains the 14 LSBs, and the second write contains the 14 MSBs. For this mode of operation, the B28 (D13) control bit should be set to 1. An example of a 28-bit write is shown in Table 9.

Table 9. Writing 0xFFFC000 to the FREQ0 Register

SDATA Input	Result of Input Word
0010 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 1, HLB (D12) = X
0100 0000 0000 0000	FREQ0 register write (D15, D14 = 01), 14 LSBs = 0x0000
0111 1111 1111 1111	FREQ0 register write (D15, D14 = 01), 14 MSBs = 0x3FFF

In some applications, the user does not need to alter all 28 bits of the frequency register. With coarse tuning, only the 14 MSBs are altered, while with fine tuning, only the 14 LSBs are altered. By setting the B28 (D13) control bit to 0, the 28-bit frequency register operates as two, 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs, and vice versa. Bit HLB (D12) in the control register identifies which 14 bits are being altered. Examples of this are shown in Table 10 and Table 11.

Table 10. Writing 0x3FFF to the 14 LSBs of the FREQ1 Register

SDATA Input	Result of Input Word
0000 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0; HLB (D12) = 0, that is, LSBs
1011 1111 1111 1111	FREQ1 REG write (D15, D14 = 10), 14 LSBs = 0x3FFF

Table 11. Writing 0x00FF to the 14 MSBs of the FREQ0 Register

SDATA Input	Result of Input Word
0001 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 1, that is, MSBs
0100 0000 1111 1111	FREQ0 REG write (D15, D14 = 01), 14 MSBs = 0x00FF

Writing to a Phase Register

When writing to a phase register, Bit D15 and Bit D14 are set to 11. Bit D13 identifies which phase register is being loaded.

Table 12. Phase Register Bits

D15	D14	D13	D12	D11	D0
1	1	0	X	MSB 12 PHASE0 bits	LSB
1	1	1	X	MSB 12 PHASE1 bits	LSB

RESET FUNCTION

The reset function resets appropriate internal registers to 0 to provide an analog output of midscale. Reset does not reset the phase, frequency, or control registers. When the AD9833 is powered up, the part should be reset. To reset the AD9833, set the reset bit to 1. To take the part out of reset, set the bit to 0. A signal appears at the DAC to output eight MCLK cycles after reset is set to 0.

Table 13. Applying the Reset Function

Reset Bit	Result
0	No reset applied
1	Internal registers reset

SLEEP FUNCTION

Sections of the AD9833 that are not in use can be powered down to minimize power consumption. This is done using the sleep function. The parts of the chip that can be powered down are the internal clock and the DAC. The bits required for the sleep function are outlined in Table 14.

Table 14. Applying the Sleep Function

SLEEP1 Bit	SLEEP12 Bit	Result
0	0	No power-down
0	1	DAC powered down
1	0	Internal clock disabled
1	1	Both the DAC powered down and the internal clock disabled

DAC Powered Down

This is useful when the AD9833 is used to output the MSB of the DAC data only. In this case, the DAC is not required; therefore, it can be powered down to reduce power consumption.

Internal Clock Disabled

When the internal clock of the AD9833 is disabled, the DAC output remains at its present value because the NCO is no longer accumulating. New frequency, phase, and control words can be written to the part when the SLEEP1 control bit is active. The synchronizing clock is still active, which means that the selected frequency and phase registers can also be changed using the control bits. Setting the SLEEP1 bit to 0 enables the MCLK. Any changes made to the registers while SLEEP1 is active will be seen at the output after a latency period.

VOUT PIN

The AD9833 offers a variety of outputs from the chip, all of which are available from the VOUT pin. The choice of outputs is the MSB of the DAC data, a sinusoidal output, or a triangle output.

The OPBITEN (D5) and mode (D1) bits in the control register are used to decide which output is available from the AD9833.

MSB of the DAC Data

The MSB of the DAC data can be output from the AD9833. By setting the OPBITEN (D5) control bit to 1, the MSB of the DAC data is available at the VOUT pin. This is useful as a coarse clock source. This square wave can also be divided by 2 before being output. The DIV2 (D3) bit in the control register controls the frequency of this output from the VOUT pin.

Sinusoidal Output

The SIN ROM is used to convert the phase information from the frequency and phase registers into amplitude information that results in a sinusoidal signal at the output. To have a sinusoidal output from the VOUT pin, set the mode (D1) bit to 0 and the OPBITEN (D5) bit to 0.

Triangle Output

The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC will produce a 10-bit linear triangular function. To have a triangle output from the VOUT pin, set the mode (D1) bit = 1.

Note that the SLEEP12 bit must be 0 (that is, the DAC is enabled) when using this pin.

Table 15. Outputs from the VOUT Pin

OPBITEN Bit	Mode Bit	DIV2 Bit	VOUT Pin
0	0	X[1]	Sinusoid
0	1	X[1]	Triangle
1	0	0	DAC data MSB/2
1	0	1	DAC data MSB
1	1	X[1]	Reserved

[1] X = don't care.

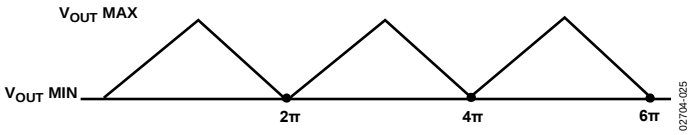

Figure 25. Triangle Output

APPLICATIONS INFORMATION

Because of the various output options available from the part, the AD9833 can be configured to suit a wide variety of applications.

One of the areas where the AD9833 is suitable is in modulation applications. The part can be used to perform simple modulation, such as FSK. More complex modulation schemes, such as GMSK and QPSK, can also be implemented using the AD9833.

In an FSK application, the two frequency registers of the AD9833 are loaded with different values. One frequency represents the space frequency, while the other represents the mark frequency. Using the FSELECT bit in the control register of the AD9833, the user can modulate the carrier frequency between the two values.

The AD9833 has two phase registers, which enables the part to perform PSK. With phase-shift keying, the carrier frequency is phase shifted, the phase being altered by an amount that is related to the bit stream being input to the modulator.

The AD9833 is also suitable for signal generator applications. Because the MSB of the DAC data is available at the VOUT pin, the device can be used to generate a square wave.

With its low current consumption, the part is suitable for applications in which it can be used as a local oscillator.

GROUNDING AND LAYOUT

The printed circuit board (PCB) that houses the AD9833 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in one place only. If the AD9833 is the only device requiring an AGND-to-DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD9833. If the AD9833 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9833.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD9833 to avoid noise coupling. The power supply lines to the AD9833 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the other side.

Good decoupling is important. The AD9833 should have supply bypassing of 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best performance from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device.

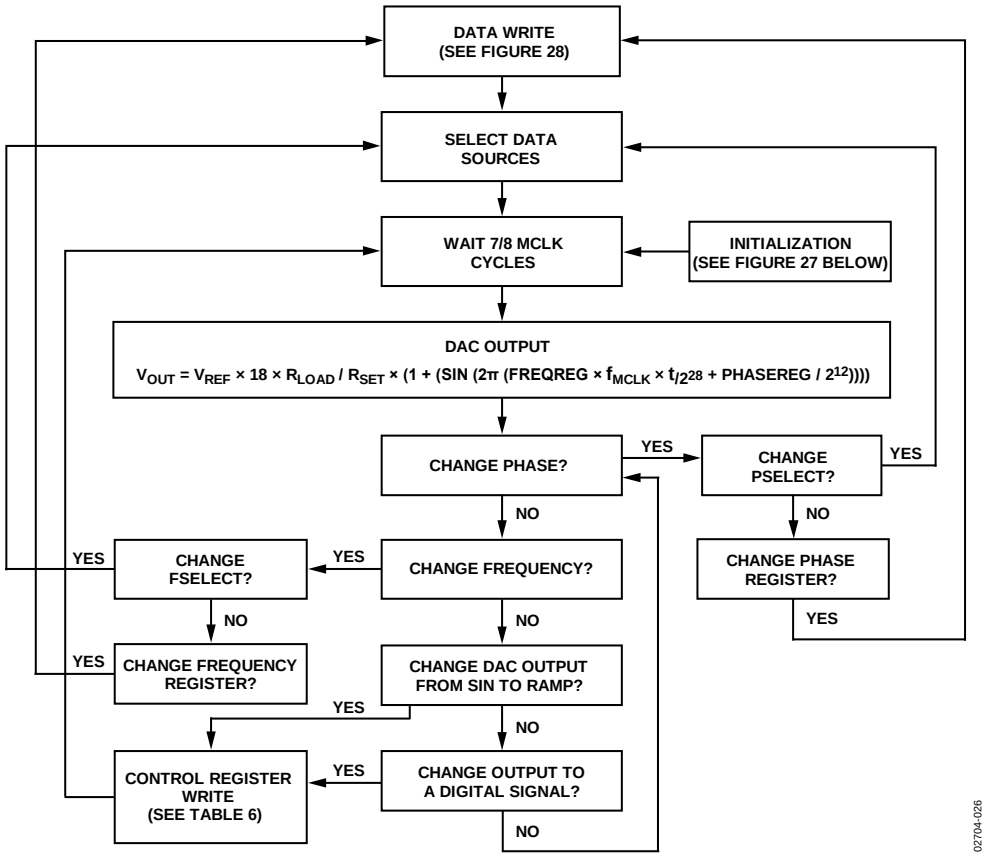

Figure 26. Flowchart for AD9833 Initialization and Operation

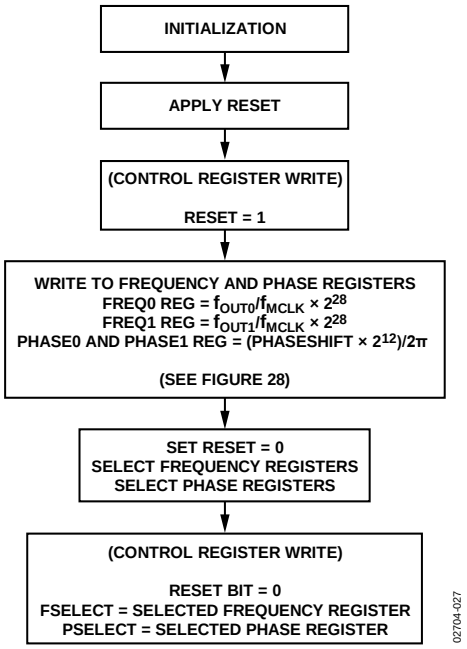

Figure 27. Flowchart for Initialization

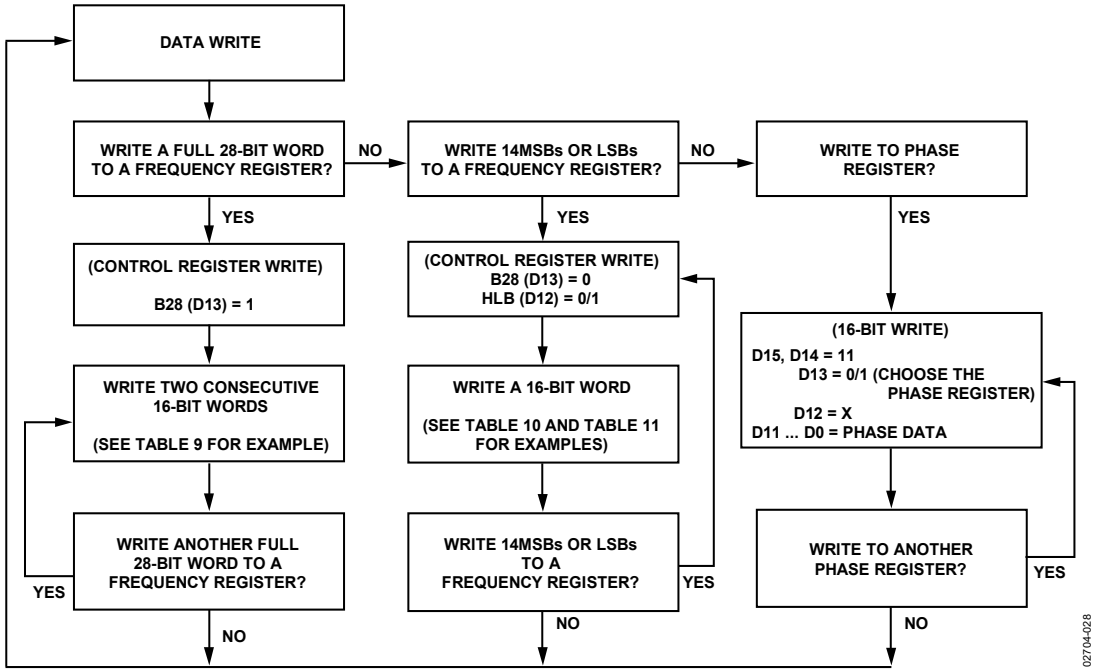

Figure 28. Flowchart for Data Writes

INTERFACING TO MICROPROCESSORS

The AD9833 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data or control information into the device. The serial clock can have a frequency of 40 MHz maximum. The serial clock can be continuous, or it can idle high or low between write operations. When data or control information is written to the AD9833, FSYNC is taken low and is held low until the 16 bits of data are written into the AD9833. The FSYNC signal frames the 16 bits of information that are loaded into the AD9833.

AD9833 TO 68HC11/68L11 INTERFACE

Figure 29 shows the serial interface between the AD9833 and the 68HC11/68L11 microcontroller. The microcontroller is configured as the master by setting the MSTR bit in the SPCR to 1. This setting provides a serial clock on SCK; the MOSI output drives the serial data line SDATA. Because the microcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows:

- SCK idles high between write operations (CPOL = 1)
- Data is valid on the SCK falling edge (CPHA = 0)

When data is being transmitted to the AD9833, the FSYNC line is taken low (PC7). Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data into the AD9833, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the AD9833. Only after the second eight bits are transferred should FSYNC be taken high again.

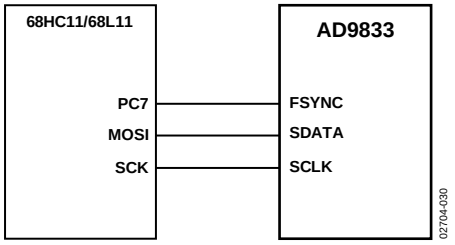

Figure 29. 68HC11/68L11 to AD9833 Interface

AD9833 TO 80C51/80L51 INTERFACE

Figure 30 shows the serial interface between the AD9833 and the 80C51/80L51 microcontroller. The microcontroller is operated in Mode 0 so that TxD of the 80C51/80L51 drives SCLK of the AD9833, and RxD drives the serial data line SDATA. The FSYNC signal is derived from a bit programmable pin on the port (P3.3 is shown in Figure 30).

When data is to be transmitted to the AD9833, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes, thus only eight falling SCLK edges occur in each cycle. To load the remaining eight bits to the AD9833, P3.3 is held low after the first eight bits are transmitted, and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations.

The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD9833 accepts the MSB first (the four MSBs are the control information, the next four bits are the address, and the eight LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must take this into account and rearrange the bits so that the MSB is output first.

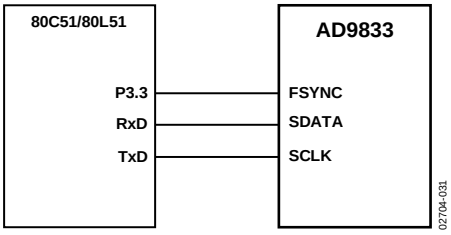

Figure 30. 80C51/80L51 to AD9833 Interface

AD9833 TO DSP56002 INTERFACE

Figure 31 shows the interface between the AD9833 and the DSP56002. The DSP56002 is configured for normal mode asynchronous operation with a gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16 bits wide (WL1 = 1, WL0 = 0), and the frame sync signal frames the 16 bits (FSL = 0). The frame sync signal is available on the SC2 pin, but it must be inverted before it is applied to the AD9833. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

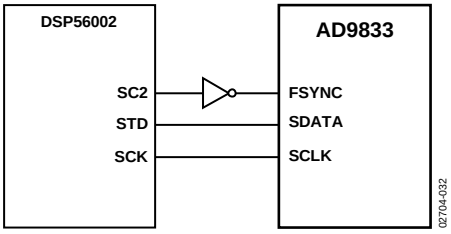

Figure 31. DSP56002 to AD9833 Interface