Data Sheet

AD9914S

Commercial Space Product

3.5 GPSP Direct Digital Synthesizer with 12-Bit DAC

FEATURES

- 3.5 GSPS internal clock speed
- Integrated 12-bit DAC
- Frequency tuning resolution to 190 pHz
- 16-bit phase tuning resolution
- 12-bit amplitude scaling
- Programmable modulus
- Automatic linear and nonlinear frequency sweeping capability
- 32-bit parallel datapath interface
- 8 frequency/phase offset profiles
- Phase noise: −128 dBc/Hz (1 kHz offset at 1396 MHz)
- Wideband SFDR < −50 dBc
- Serial or parallel input/output control
- 1.8 V/3.3 V power supplies
- Software and hardware controlled power-down
- 88-lead LFCSP package
- PLL REF CLK multiplier
- Phase modulation capability
- Amplitude modulation capability

COMMERCIAL SPACE FEATURES

- Supports aerospace applications
- Wafer diffusion lot traceability
- Radiation lot acceptance test (RLAT)
  - Total ionizing dose (TID)
- Radiation benchmark
  - Single event latch-up (SEL)

APPLICATIONS

- Low Earth orbit (LEO) space payloads
- Agile LO frequency synthesis
- Programmable clock generators
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar modulators
- Fast frequency hopping

FUNCTIONAL BLOCK DIAGRAM

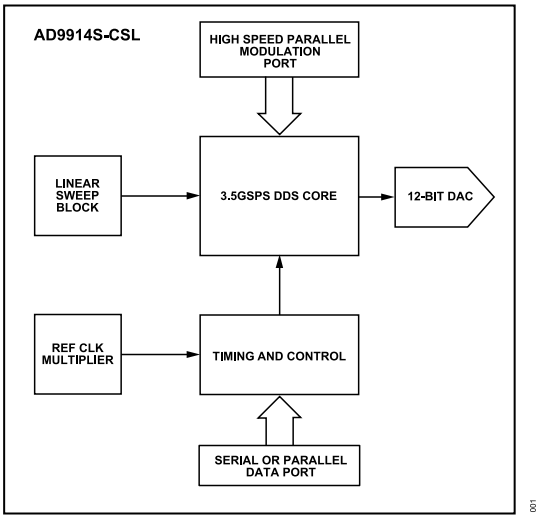

Figure 1.

GENERAL DESCRIPTION

The AD9914S-CSL is a direct digital synthesizer (DDS) featuring a 12-bit digital-to-analog converter (DAC). The AD9914S-CSL uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 1.4 GHz. The AD9914S-CSL enables fast frequency hopping and fine tuning resolution (64-bit capable using programmable modulus mode). The AD9914S-CSL also offers fast phase and amplitude hopping capability. The frequency tuning and control words are loaded into the AD9914S-CSL via a serial or parallel input/output port. The AD9914S-CSL also supports a user defined linear sweep mode of operation for generating linear swept waveforms of frequency, phase, or amplitude. A high speed, 32-bit parallel data input port is included, enabling high data rates for polar modulation schemes and fast reprogramming of the phase, frequency, and amplitude tuning words.

The AD9914S-CSL is specified to operate over the extended industrial temperature range (see the Absolute Maximum Ratings section). Additional application and technical information can be found in the Commercial Space Products Program brochure and the AD9914 data sheet.

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. 0

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REVISION HISTORY

5/2022—Revision 0: Initial Version

DETAILED BLOCK DIAGRAM

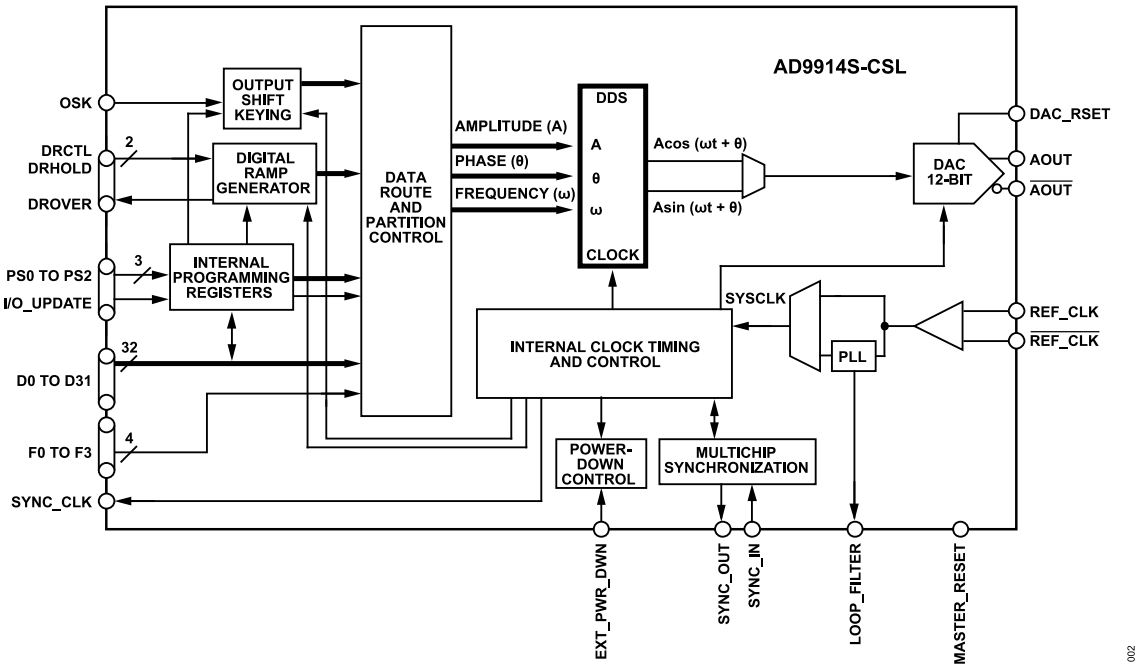

Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) and DVDD_I/O (3.3 V) = 3.3 V ± 5%, T_A = 25°C, setting resistor connected to DAC_RSET pin (R_{SET}) = 3.3 kΩ, output current (I_{OUT}) = 20 mA, external reference clock frequency = 3.5 GHz with reference clock (REF CLK) multiplier bypassed, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O	3.135	3.30	3.465	V	Pin 16, Pin 83
DVDD	1.71	1.80	1.89	V	Pin 6, Pin 23, Pin 73
AVDD (3.3 V)	3.135	3.30	3.465	V	Pin 34, Pin 36, Pin 39, Pin 40, Pin 43, Pin 47, Pin 50, Pin 52, Pin 53, Pin 60
AVDD (1.8 V)	1.71	1.80	1.89	V	Pin 32, Pin 56, Pin 57
SUPPLY CURRENT					See also the total power dissipation specifications
DVDD_I/O Current ($I_{DVDD\_I/O}$)			20	mA	Pin 16, Pin 83
DVDD Current (I_{DVDD})			433	mA	Pin 6, Pin 23, Pin 73
AVDD (3.3V) Current ($I_{AVDD(3.3V)}$)			640	mA	Pin 34, Pin 36, Pin 39, Pin 40, Pin 43, Pin 47, Pin 50, Pin 52, Pin 53, Pin 60
AVDD (1.8V) Current ($I_{AVDD(1.8V)}$)			178	mA	Pin 32, Pin 56, Pin 57
TOTAL POWER DISSIPATION					
Base DDS Power, Phase-Locked Loop (PLL) Disabled		2392	3091	mW	3.5 GHz, single-tone mode, modules disabled, linear sweep disabled, amplitude scaler disabled
Base DDS Power, PLL Enabled		2237	2627	mW	2.5 GHz, single-tone mode, modules disabled, linear sweep disabled, amplitude scaler disabled
Linear Sweep Additional Power		28		mW	
Modulus Additional Power		20		mW	
Amplitude Scaler Additional Power		138		mW	Manual or automatic
Full Power-Down Mode		400	616	mW	Using either the power-down and enable register or the EXT_PWR_DWN pin
CMOS LOGIC INPUTS					
Input High Voltage (V_{IH})	2.0		DVDD_I/O	V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±60	±200	µA	At V_{IN} = 0 V and V_{IN} = DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CMOS LOGIC OUTPUTS					
Output High Voltage (V_{OH})	2.7		DVDD_I/O	V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1 mA
REF CLK INPUT CHARACTERISTICS					REF CLK inputs must always be ac-coupled (both single-ended and differential)
REF CLK Multiplier Bypassed					
Input Capacitance		1		pF	Single-ended, each pin
Input Resistance		1.4		kΩ	Differential
Internally Generated DC Bias Voltage		2		V	
Differential Input Voltage		0.8	1.5	V p-p	
REF CLK Multiplier Enabled					
Input Capacitance		1		pF	Single-ended, each pin
Input Resistance		1.4		kΩ	Differential
Internally Generated DC Bias Voltage		2		V	
Differential Input Voltage		0.8	1.5	V p-p	

SPECIFICATIONS

AC SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD3 (3.3 V) and DVDD_I/O (3.3 V) = 3.3 V ± 5%, T_A = 25°C, R_{SET} = 3.3 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 3.5 GHz with REF CLK multiplier bypassed, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF CLK INPUT					Input frequency range
REF CLK Multiplier Bypassed					
Input Frequency Range	500		3500	MHz	Maximum output frequency (f_{OUT}) is 0.4 × SYSCLK frequency (f_{SYSCLK})
Duty Cycle	45	50	55	%	
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
System Clock (SYSCLK) PLL Enabled					
VCO Frequency Range	2400		2500	MHz	
VCO Gain (K_V)		60		MHz/V	
Maximum PFD Rate			125	MHz	
CLOCK DRIVERS					
SYNC_CLK Output Driver					
Frequency Range			146	MHz	
Duty Cycle		33		%	See Figure 22
Rise Time and Fall Time (20% to 80%)		650		ps	
SYNC_OUT Output Driver					10 pF load
Frequency Range			9.1	MHz	
Duty Cycle	33		66	%	CFR2 register, Bit 9 = 1
Rise Time (20% to 80%)		1350		ps	10 pF load
Fall Time (20% to 80%)		1670		ps	10 pF load
DAC OUTPUT CHARACTERISTICS					
Output Frequency Range (First Nyquist Zone)	0		1750	MHz	
Output Resistance		50		Ω	Single-ended (each pin internally terminated to AVDD (3.3 V))
Output Capacitance		1		pF	
Full-Scale Output Current			20.48	mA	Range depends on DAC R_{SET} resistor
Gain Error	−10		+10	% FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVDD − 0.50		AVDD + 0.50	V	
Wideband Spurious-Free Dynamic Range (SFDR)					See the Typical Performance Characteristics section
101.1 MHz Output		−66		dBc	0 MHz to 1750 MHz
427.5 MHz Output		−65		dBc	0 MHz to 1750 MHz
696.5 MHz Output		−57		dBc	0 MHz to 1750 MHz
1396.5 MHz Output		−52		dBc	0 MHz to 1750 MHz
Narrow-Band SFDR					See the Typical Performance Characteristics section
100.5 MHz Output		−95		dBc	±500 kHz
427.5 MHz Output		−95		dBc	±500 kHz
696.5 MHz Output		−95		dBc	±500 kHz
1396.5 MHz Output		−92		dBc	±500 kHz
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power-Down		45		ns	Power-down mode loses DAC/PLL calibration settings
Time Required to Leave Power-Down		250		ns	Must recalibrate DAC/PLL
Minimum Master Reset Time	24			SYSCLK cycles	

SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Maximum DAC Calibration Time (t_{CAL})			135	µs	See the DAC calibration output information in the AD9914 data sheet for this formula
Maximum PLL Calibration Time (t_{REF_CLK})			16	ms	PFD rate = 25 MHz
			8	ms	PFD rate = 50 MHz
Maximum Profile Toggle Rate			2	SYNC_CLK period	
PARALLEL PORT TIMING					
Write Timing					
Address Setup Time to $\overline{WR}$ Active	1			ns	
Address Hold Time to Inactive			0	ns	
Data Setup Time to $\overline{WR}$ Inactive	3.8			ns	
Data Hold Time to $\overline{WR}$ Inactive			0	ns	
$\overline{WR}$ Minimum Low Time			2.1	ns	
$\overline{WR}$ Minimum High Time			3.8	ns	
Minimum $\overline{WR}$ Time			10.5	ns	
Read Timing					
Address to Data Valid			92	ns	
Address Hold to $\overline{RD}$ Inactive			0	ns	
$\overline{RD}$ Active to Data Valid			69	ns	
$\overline{RD}$ Inactive to Data Tristate			50	ns	
$\overline{RD}$ Minimum Low Time			69	ns	
$\overline{RD}$ Minimum High Time			50	ns	
SERIAL PORT TIMING					
SCLK Clock Rate ($1/t_{CLK}$)			80	MHz	SCLK duty cycle = 50%, maximum SCLK rate applies only to write cycles, read cycles are constrained to < 3 MHz
SCLK Pulse Width High, t_{HIGH}	1.5			ns	
SCLK Pulse Width Low, t_{LOW}	5.1			ns	
SDIO to SCLK Setup Time, t_{DS}	4.9			ns	
SDIO to SCLK Hold Time, t_{DH}			0	ns	
SCLK Falling Edge to Valid Data on SDIO/SDO, t_{DV}			78	ns	
$\overline{CS}$ to SCLK Setup Time, t_S	4			ns	
$\overline{CS}$ to SCLK Hold Time, t_H			0	ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	4			ns	
DATA PORT TIMING					
D31 to D0 Setup Time to SYNC_CLK	2			ns	
D31 to D0 Hold Time to SYNC_CLK			0	ns	
F3 to F0 Setup Time to SYNC_CLK	2			ns	
F3 to F0 Hold Time to SYNC_CLK			0	ns	
I/O_UPDATE Pin Setup Time to SYNC_CLK	2			ns	
I/O_UPDATE Pin Hold Time to SYNC_CLK			0	ns	
Profile Pin Setup Time to SYNC_CLK	2			ns	
Profile Pin Hold Time to SYNC_CLK			0	ns	
DR_CTL/DR_HOLD Setup Time to SYNC_CLK	2			ns	
DR_CTL/DR_HOLD Hold Time to SYNC_CLK			0	ns	
DATA LATENCY (PIPELINE DELAY)					1 SYSCLK cycle = 1 period of the system clock ($1/f_S$)
Single Tone Mode or Profile Mode (Matched Latency Disabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled

SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Phase		294		SYSCLK cycles	OSK disabled
		318		SYSCLK cycles	OSK enabled
Amplitude		102		SYSCLK cycles	OSK enabled
Single Tone Mode or Profile Mode (Matched Latency Enabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Amplitude		342		SYSCLK cycles	OSK enabled
Modulation Mode with 32-Bit Parallel Port (Matched Latency Disabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		294		SYSCLK cycles	OSK disabled
		318		SYSCLK cycles	OSK enabled
Amplitude		102		SYSCLK cycles	OSK enabled
Modulation Mode with 32-Bit Parallel Port (Matched Latency Enabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Amplitude		342		SYSCLK cycles	OSK enabled
Sweep Mode (Match Latency Disabled)					
Frequency		342		SYSCLK cycles	OSK disabled
		366		SYSCLK cycles	OSK enabled
Phase		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Amplitude		126		SYSCLK cycles	OSK enabled
Sweep Mode (Match Latency Enabled)					
Frequency		342		SYSCLK cycles	OSK disabled
		366		SYSCLK cycles	OSK enabled
Phase		342		SYSCLK cycles	OSK disabled
		366		SYSCLK cycles	OSK enabled
Amplitude		366		SYSCLK cycles	OSK enabled

RADIATION TEST AND LIMIT SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) and DVDD_I/O (3.3 V) = 3.3 V ± 5%, T_A = 25°C, R_{SET} = 3.3 kΩ, I_{OUT} = 20 mA, and external reference clock frequency = 3.5 GHz with REF CLK multiplier bypassed, unless otherwise noted. Total ionizing dose (TID) testing characterized to 50 krads (30 krads + 50% overstress) with biased annealing at 100°C for 168 hours. Once characterized, TID testing is performed to 30 krads only.

Table 3.

Parameter	Min	Typ	Max	Unit
DC SPECIFICATIONS				
DVDD_I/O	3.135	3.3	3.465	V
Full Power-Down Mode		400	606	mW
Internally Generated DC Bias Voltage		2		V
Maximum Current		0.93	1	A
Maximum Power		2.5	2.75	W
DIGITAL INPUT AND OUTPUT LEAKAGE CURRENT				
Low	20	35	50	µA
High	50		120	µA
AC SPECIFICATIONS				
Offset Error	−15		+15	mV
Gain Error	−10		+10	%FS

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD (1.8 V), DVDD (1.8 V) Supplies	2 V
AVDD (3.3 V), DVDD_I/O (3.3 V) Supplies	4 V
Digital Input Voltage	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (10 sec Soldering)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL PERFORMANCE

Table 5.

Symbol	Description	Value[1]	Unit
θ_{JA}	Junction-to-ambient thermal resistance (still air) per JEDEC JESD51-2	24.1	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance (1.0 m/sec airflow) per JEDEC JESD51-6	21.3	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance (2.0 m/sec air flow) per JEDEC JESD51-6	20.0	°C/W
θ_{JB}	Junction-to-board thermal resistance (still air) per JEDEC JESD51-8	13.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (still air) per JEDEC JESD51-6	12.8	°C/W
θ_{JC}	Junction-to-case thermal resistance	2.21	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter (still air) per JEDEC JESD51-2	0.23	°C/W

[1] Results are from simulations. Printed circuit board (PCB) is JEDEC multilayer. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

OUTGAS TESTING

The criteria used for the acceptance and rejection of materials must be determined by the user and based upon specific component and system requirements. Historically, a total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% have been used as screening levels for rejection of spacecraft materials.

Table 6. Outgas Testing

Specification (Tested per ASTM E595 -15)	Value	Unit
Total Mass Lost	0.12	%
Collected Volatile Condensable Material	<0.01	%
Water Vapor Recovered	0.03	%

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

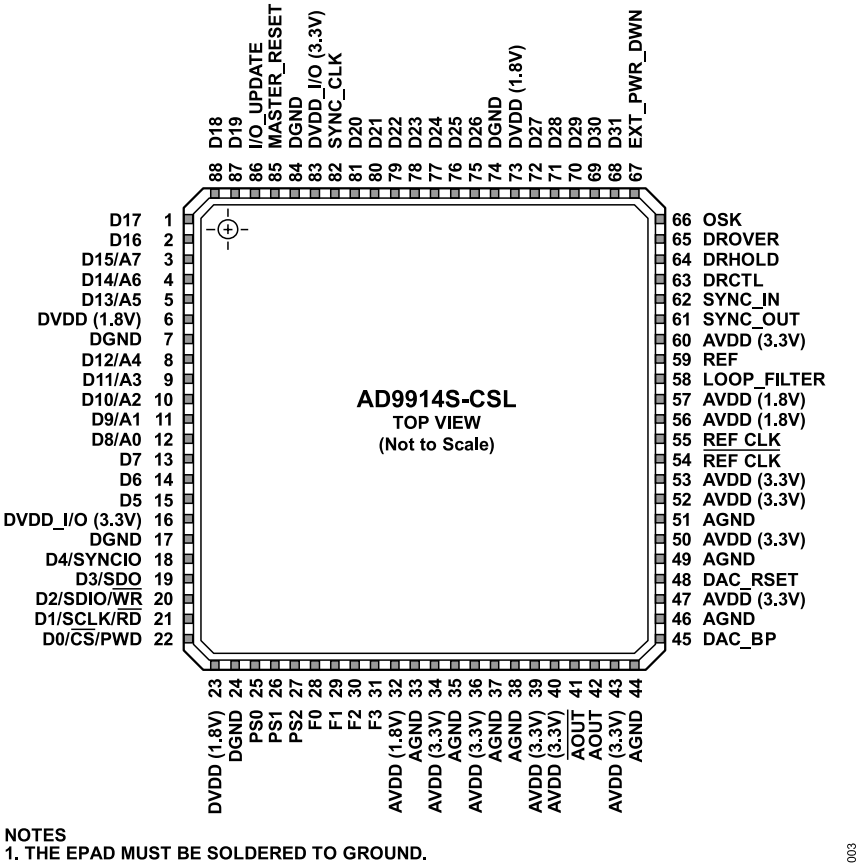

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 2, 13 to 15, 68 to 72, 75 to 81, 87, 88	D5 to D7, D16 to D31, D27 to D31	I/O	Parallel Port Pins. The 32-bit parallel port offers the option for serial or parallel programming of the internal registers. In addition, the parallel port can be configured to provide direct frequency-shift keying (FSK), phase-shift keying (PSK), or amplitude-shift keying (ASK) (or combinations thereof) modulation data. The 32-bit parallel port configuration is set by the state of the four function pins (F0 to F3).
3	D15/A7	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
4	D14/A6	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
5	D13/A5	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
8	D12/A4	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
9	D11/A3	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
10	D10/A2	I/O	Parallel Port Pin/Address Line. Multipurpose pin depending on the state of the function pins (F0 to F3). The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
11	D9/A1	I/O	Parallel Port Pin/Address Line. Multipurpose pin depending on the state of the function pins (F0 to F3). The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
12	D8/A0	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
18	D4/SYNCIO	I	Parallel Port Pin/Serial Port Synchronization Pin. This pin is D4 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin resets the serial port.
19	D3/SDO	I/O	Parallel Port Pin/Serial Data Output. This pin is D3 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for readback mode for serial operation.
20	D2/SDIO/$\overline{WR}$	I/O	Parallel Port Pin/Serial Data Input and Output/Write Input. This pin is D2 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for the SDIO for serial operation. If parallel mode is enabled, write to this pin to change the values of the internal registers.
21	D1/SCLK/$\overline{RD}$	I	Parallel Port Pin/Serial Clock/Read Input. This pin is D1 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for SCLK for serial operation. If parallel mode is enabled, this pin reads back the value of the internal registers.
22	D0/$\overline{CS}$/PWD	I	Parallel Port Pin/Chip Select/Parallel Width. This pin is D0 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for the chip select for serial operation. If parallel mode is enabled, this pin sets either 8-bit data or16-bit data.
6, 23, 73	DVDD (1.8V)	I	Digital Core Supplies (1.8 V).
7, 17, 24, 74, 84	DGND	I	Digital Ground.
16, 83	DVDD_I/O (3.3V)	I	Digital Input and Output Supplies (3.3 V).
32, 56, 57	AVDD (1.8V)	I	Analog Core Supplies (1.8 V).
33, 35, 37, 38, 44, 46, 49, 51	AGND	I	Analog Ground.
34, 36, 39, 40, 43, 47, 50, 52, 53, 60	AVDD (3.3V)	I	Analog DAC Supplies (3.3 V).
25, 26, 27	PS0 to PS2	I	Profile Select Pins. Digital inputs (active high). Use these pins to select one of the eight phase and frequency profiles for the DDS. Changing the state of one of these pins transfers the current contents of all input and output buffers to the corresponding registers. State changes must be set up on the SYNC_CLK pin (Pin 82).
28, 29, 30, 31	F0 to F3	I	Function Pins. Digital inputs. The state of these pins determines if a serial or parallel interface is used. In addition, the function pins determine how the 32-bit parallel data-word is partitioned for FSK, PSK, or ASK modulation mode.
41	$\overline{AOUT}$	O	DAC Complementary Output Source. Analog output (voltage mode). This pin is internally connected through a 50 Ω resistor to AVDD (3.3 V).
42	AOUT	O	DAC Output Source. Analog output (voltage mode). This pin is internally connected through a 50 Ω resistor to AVDD (3.3 V).
45	DAC_BP	I	DAC Bypass Pin. This pin provides access to the common control node of the DAC current sources. Connecting a capacitor between this pin and ground can improve noise performance at the DAC output.
48	DAC_RSET	O	Analog Reference. This pin programs the DAC output full-scale reference current. Connect a 3.3 kΩ resistor to AGND.
54	$\overline{REF\_CLK}$	I	Complementary Reference Clock Input. Analog input.
55	REF_CLK	I	Reference Clock Input. Analog input.
58	LOOP_FILTER	O	External PLL Loop Filter Node.
59	REF	O	Local PLL Reference Supply. Typically at 2.05 V.
61	SYNC_OUT	O	Digital Synchronization Output. This pin synchronizes multiple chips.
62	SYNC_IN	I	Digital Synchronization Input. This pin synchronizes multiple chips.
63	DRCTL	I	Ramp Control. Digital input (active high). This pin controls the sweep direction (up/down).
64	DRHOLD	I	Ramp Hold. Digital input (active high). Pauses the sweep when active.
65	DROVER	O	Ramp Over. Digital output (active high). This pin switches to Logic 1 when the digital ramp generator reaches the programmed upper or lower limit.
66	OSK	I	Output Shift Keying. Digital input (active high). When the OSK features are placed in either manual or automatic mode, this pin controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to 0 and a high sweeps the amplitude up to the amplitude scale factor.
67	EXT_PWR_DWN	I	External Power-Down. Digital input (active high). A high level on this pin initiates the currently programmed power-down mode.
82	SYNC_CLK	O	Clock Output. Digital output. Many of the digital inputs on the chip, such as I/O_UPDATE, PS2 to PS0, and the parallel data port (D0 to D31), must be set up on the rising edge of this signal.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
85	MASTER_RESET	I	Master Reset. Digital input (active high). This pin clears all memory elements and sets registers to default values.
86	I/O_UPDATE	I	Input and Output Update. Digital input (active high). A high on this pin transfers the contents of the input and output buffers to the corresponding internal registers.
	EPAD		Exposed Pad. The EPAD must be soldered to ground.

[1] I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

Nominal supply voltage, DAC R_{SET} = 3.3 kΩ, and T_A = 25°C, unless otherwise noted.

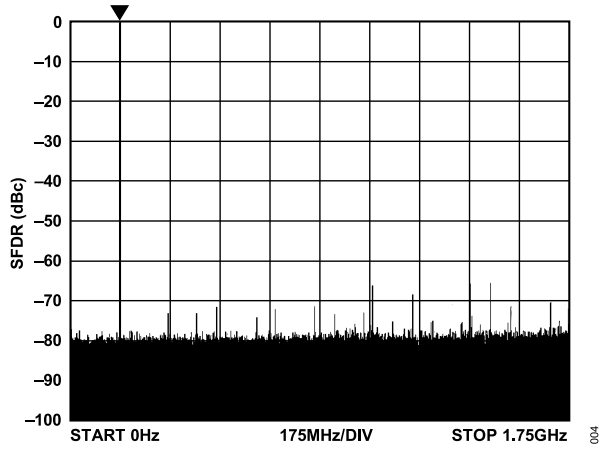

Figure 4. Wideband SFDR at 171.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

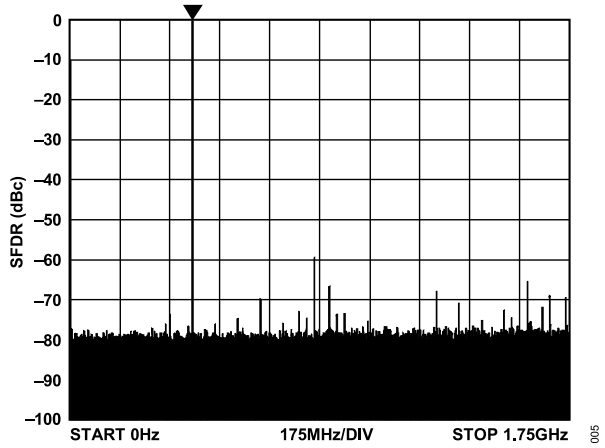

Figure 5. Wideband SFDR at 427.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

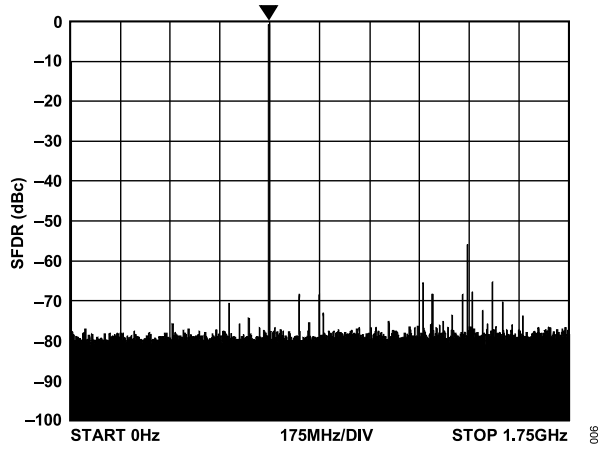

Figure 6. Wideband SFDR at 696.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

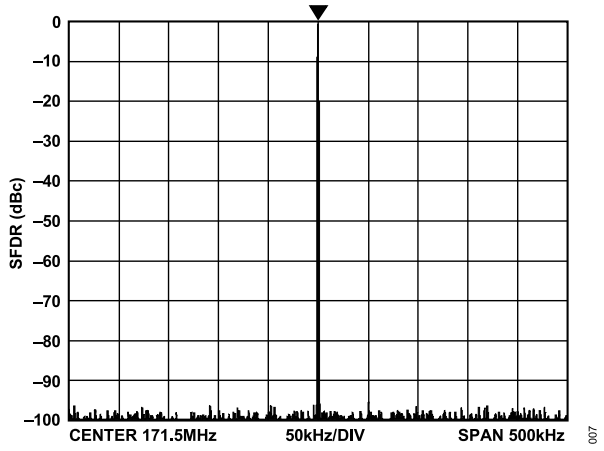

Figure 7. Narrow-Band SFDR at 171.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

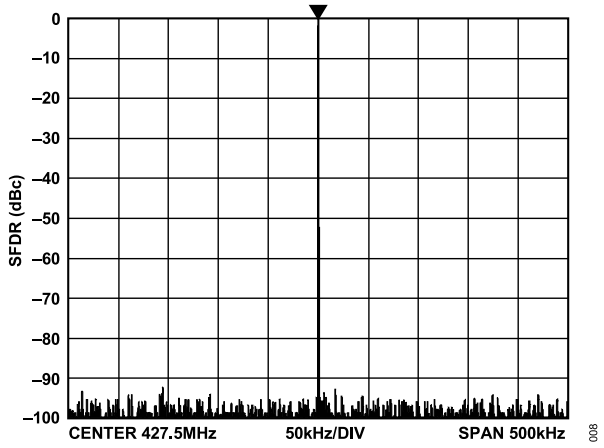

Figure 8. Narrow-Band SFDR at 427.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

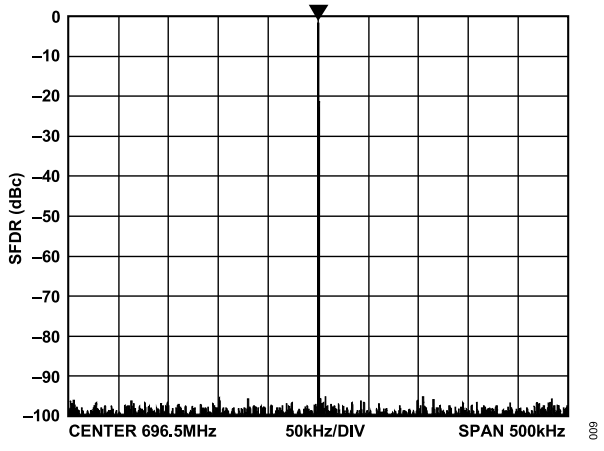

Figure 9. Narrow-Band SFDR at 696.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

TYPICAL PERFORMANCE CHARACTERISTICS

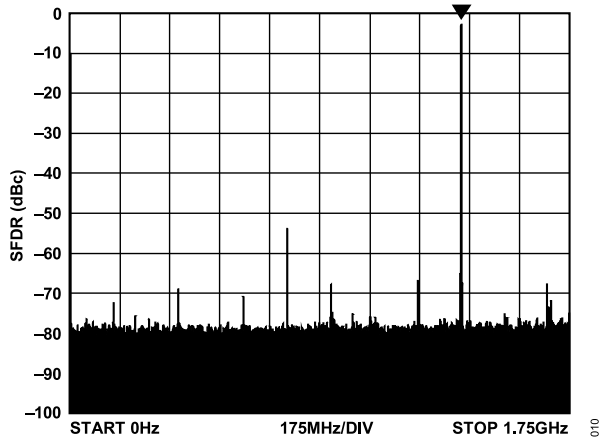

Figure 10. Wideband SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

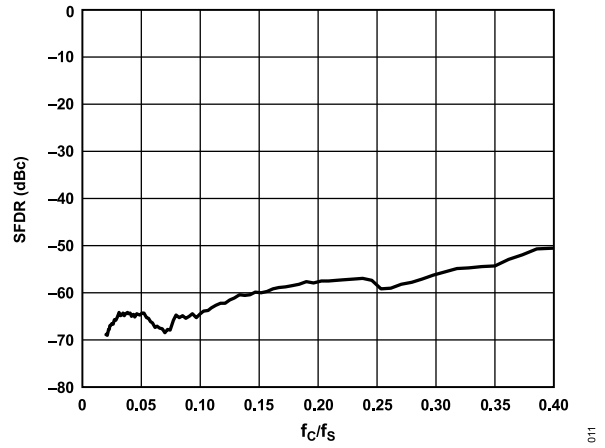

Figure 11. Wideband SFDR vs. Normalized f_{OUT}, SYSCLK = 3.5 GHz

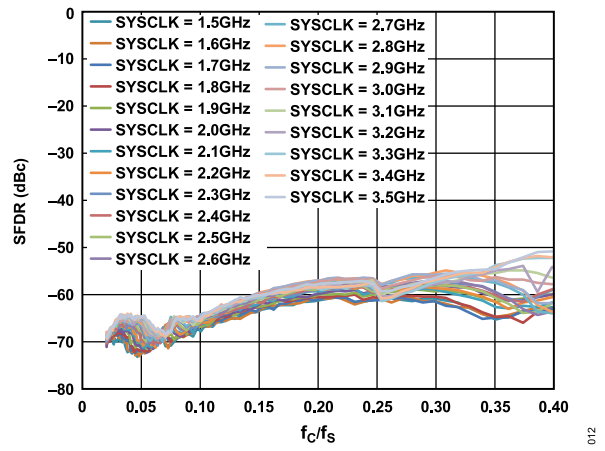

Figure 12. Wideband SFDR vs. Normalized f_{OUT}, SYSCLK = 2.5 GHz to 3.5 GHz

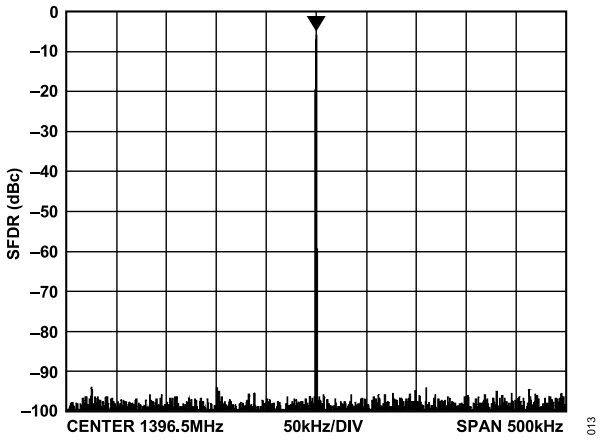

Figure 13. Narrow-Band SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

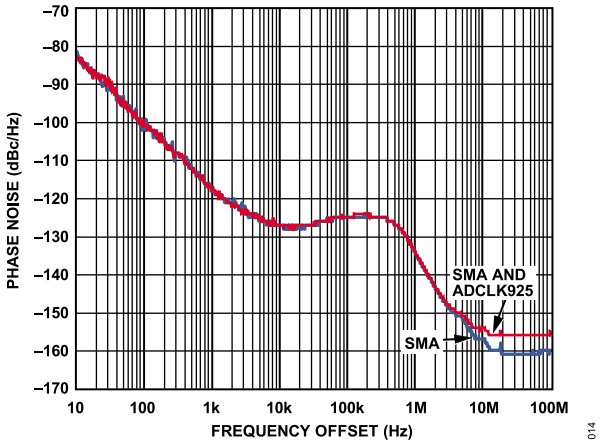

Figure 14. Absolute Phase Noise of REF CLK Source (Rohde & Schwarz SMA100 Signal Generator at 3.5 GHz Buffered by Series ADCLK925) Driving AD9914S

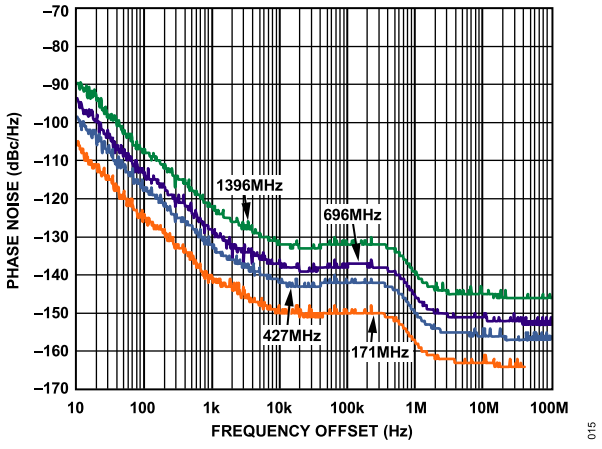

Figure 15. Absolute Phase Noise Curves of DDS Output at 3.5 GHz Operation

TYPICAL PERFORMANCE CHARACTERISTICS

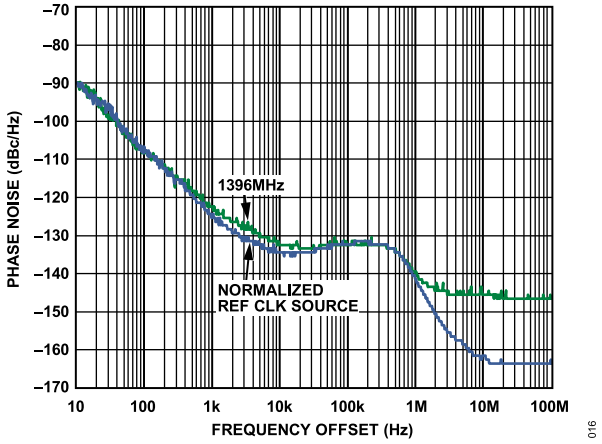

Figure 16. Absolute Phase Noise Curves of Normalized REF CLK Source to DDS Output at 1396 MHz (SYSCLK = 3.5 GHz)

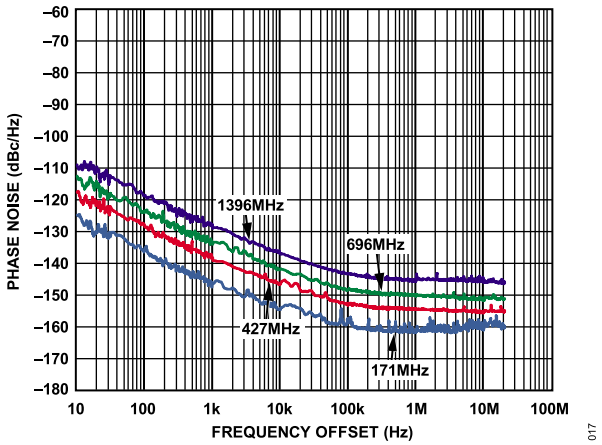

Figure 17. Residual Phase Noise Curves

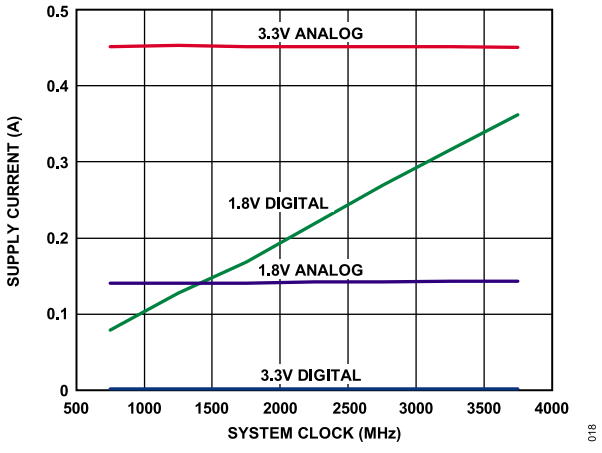

Figure 18. Power Supply Current vs. SYSCLK

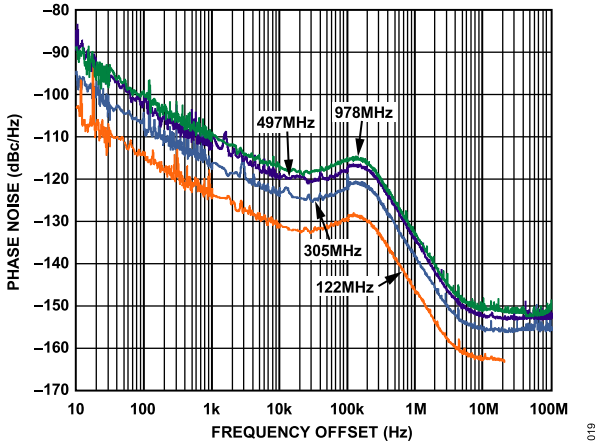

Figure 19. Absolute Phase Noise Curves of DDS Output Using Internal PLL at 2.5 GHz Operation

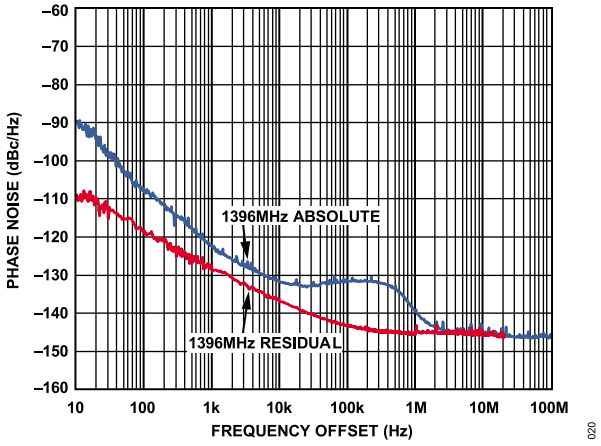

Figure 20. Residual Phase Noise vs. Absolute Phase Noise Measurement Curves at 1396 MHz

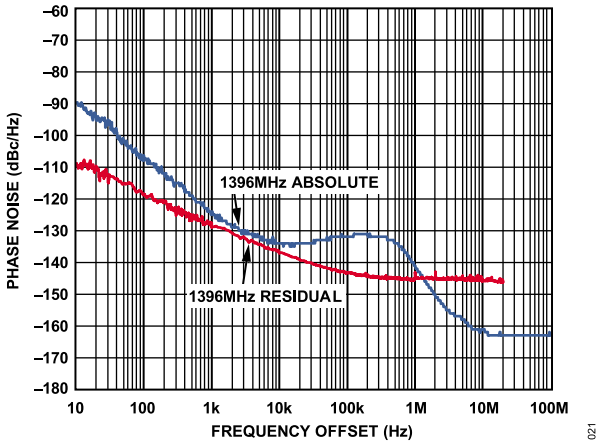

Figure 21. Residual Phase Noise vs. Normalized Absolute REF CLK Source Phase Noise at 1396 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

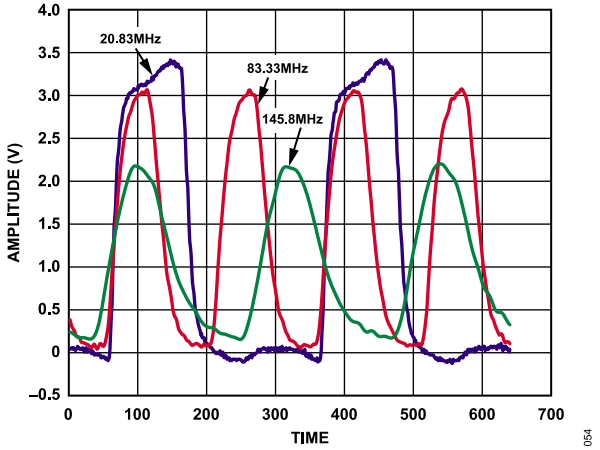

Figure 22. SYNC_CLK Waveform vs. Frequency (f_{SYSCLK}/24), Measured at the SYNC_CLK Pin Using an Active Probe (1 GHz Bandwidth, 1 MΩ, 1 pF) with the SYNC_CLK Pin Loaded by a 1 Inch PCB Trace Connected to an Open Subminiature Version A (SMA) Connector

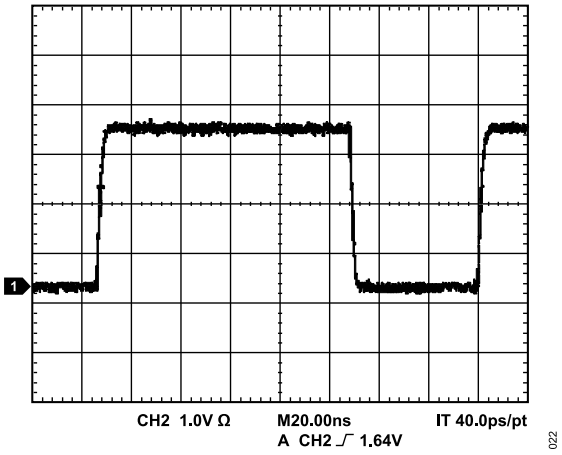

Figure 23. SYNC_OUT (f_{SYSCLK}/384)

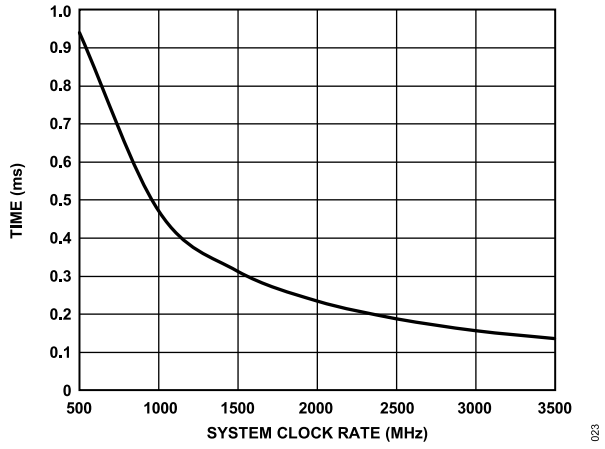

Figure 24. DAC Calibration Time vs. SYSCLK Rate (See the DAC Calibration Output Information in the AD9914 Data Sheet for the Formula)

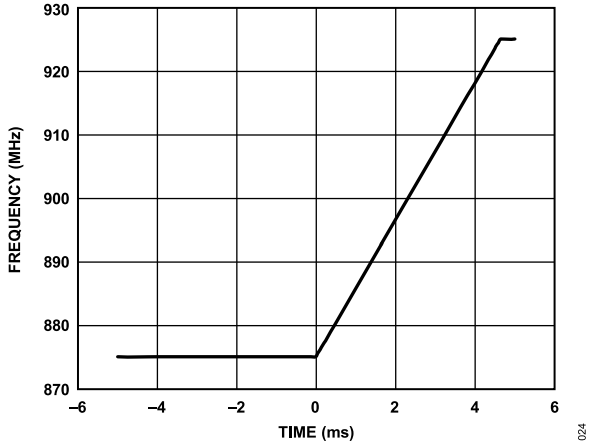

Figure 25. Measured Rising Linear Frequency Sweep

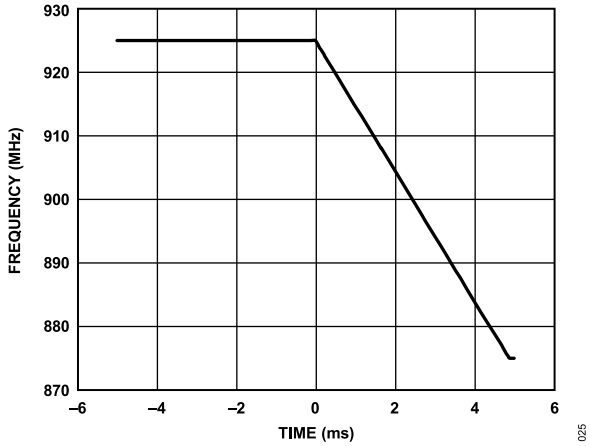

Figure 26. Measured Falling Linear Frequency Sweep