

Figure 1.

DESCRIPTION

This data sheet describes the AD9956/PCB evaluation board hardware and software. The current version of software provides a graphical user interface (GUI) that allows easy communication with the many on-chip functions of the device.

The AD9956 is a highly sophisticated *AgileRF* synthesizer with numerous user-programmable functions. See the AD9956 data sheet for detailed information about the part.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Hardware	3	Clock Driver Control, Phase-Frequency Detector & Charge Pump Dialog Box	7
System Requirements.....	3	DUT Signals Dialog Box	8
Setup.....	3	DUT I/O Dialog Box	8
Software	4	Debug Window.....	9
Setup.....	4	Ordering Information.....	10
Running and Using the Software.....	4	Ordering Guide	10
Control Dialog Box	5	ESD Caution.....	10
Profile Dialog Box	6		

REVISION HISTORY

1/05—Revision 0: Initial Version

HARDWARE

SYSTEM REQUIREMENTS

To use the evaluation board and run the software, you need the minimum system requirements listed in Table 1 on the evaluation PC.

Table 1. System Requirements

Item	Requirement
Operating System	Windows® 95 or greater
Processor	Pentium® I or better
Memory	128 MB or better
Ports	One USB port
Clocking	Signal generator capable of generating sine waves of at least 3 dBm power, up to at least 10 MHz
Power Supplies	Capability to generate at least 3 independent dc voltages
Measurement	Appropriate measurement device, such as a spectrum analyzer or a high bandwidth oscilloscope

SETUP

Powering the Part

The AD9956/PCB evaluation board has three power supply connectors: TB1, J14, and J17. TB1 powers the DDS, the phase detector, and the PC interface logic. J14 powers the VCO (when populated). J17 powers the CML output driver. Table 2 shows the necessary connections and the appropriate biasing voltage.

Table 2. Connections and Biasing Voltage

Connector	Pin No.	Label	Voltage (V)
TB1	1	VCC	3.3
TB1	2	DVDD	1.8
TB1	3	GND	0
TB1	4	DVDD_I/O	3.3
TB1	5	AVDD	1.8
J14		VCO + 5 V	5
J17		AVDD_CP	3.3

Clocking the Part

The AD9956 can be configured in multiple ways to put the device into a variety of different loops. The configuration determines the device input that serves as the input to the loop. To clock the RF divider/DDS directly, connect the external clocking signal to the DUT RF IN SMA connector, J1. This input leads to the REFCLK/REFCLK inputs of the AD9956. In many closed-loop applications, the VCO supplies this signal.

When using the part in this kind of application, the external signal should be applied to the DUT REF IN connector, J2. This leads to the AD9956 Pins PLLREF/PLLREF, the reference input of the AD9956's phase frequency detector. See the AD9956 data sheet for details on the maximum input speeds and input sensitivities of these two inputs.

Communicating with the Part

Two interface standards are available on the AD9956/PCB evaluation board:

- USB 2.0 interface
- Header row (U9, U12), which places the part under the control of an external controller (such as a μ P, an FPGA, or a DSP)

Analog Devices offers a GUI for the PC; it does not offer control software for external controllers.

Use the jumper settings listed in Table 3 to enable different modes of communication.

Table 3. Jumper Settings for Communication Modes

Mode	Settings
PC control, USB port	Set W4 to PC. Place a jumper on W15.
External control	Set W3 to parallel, set W4 to manual, and remove W15 (or leave it stored as a shunt).

Master/Slave Configuration

To allow multiple devices to be driven by a common controller, the evaluation hardware and software allow master/slave configurations. When a board is configured as a master, it can be connected directly to the USB port or the parallel port of a PC. A slave can talk to the evaluation software only through another AD9956 board, which acts as the master.

To configure two boards for this master/slave relationship, connect a 26-wire ribbon cable from the master port (U9) of the master board to the slave port (U12) of the slave board. On the master board, set all the master/slave jumpers (W5 to W13) to master. On the slave board, set W5 to W12 to slave. Once the master/slave configuration is set, the evaluation software can communicate with both because each of the dialog boxes has an area for the master board and the slave board.

SOFTWARE

SETUP

To install the software on the your PC:

1. Insert the AD9956/PCB evaluation software CD-ROM into the CD-ROM drive.
2. Use Windows Explorer to navigate to the CD-ROM drive.
3. The folders at the root level are labeled **Datashts**, **DDS_Tut**, **Instruct**, **Layout**, **Schematic**, and **Software**. The **Datashts** folder contains the data sheet for the AD9956. **DDS_Tut** contains the DDS tutorial. **Instruct** contains the evaluation board software and hardware instructions (this document). **Layout** contains the PCB layout files for the evaluation board. **Software** contains the **setup.exe** file for the evaluation software and the file **install.pdf**.
4. Read **install.pdf** completely and then follow the instructions in this file to install the software on your PC.

RUNNING AND USING THE SOFTWARE

To launch the evaluation software:

1. Find the executable, **AD9956v.exe**, in the following folder: **c:\Program Files\ADI\AD9956 Evaluation Software**
2. Double-click the icon to launch the evaluation software. A status window similar to Figure 2 appears in the center of the **AD9956 Evaluation Software** dialog box as progress is made in loading the evaluation software (a black window with green text). If the software loads successfully, the text remains green and the “software up and running” message is displayed. If the loading fails, the text turns red, and a message describing the failure is displayed.

Three dialog boxes are automatically loaded: **Control**, **Profile**, and **DUT Signals**. You can load other dialog boxes from the **View** menu. You can also program the registers of the device directly from the **Debug Window**, which you can access from the **View** menu.

At startup, the software searches for the presence of a functioning AD9956 evaluation board. If it detects the evaluation board, a green splash screen appears, as shown in Figure 2. If it fails to detect a working part, a red error message is displayed.

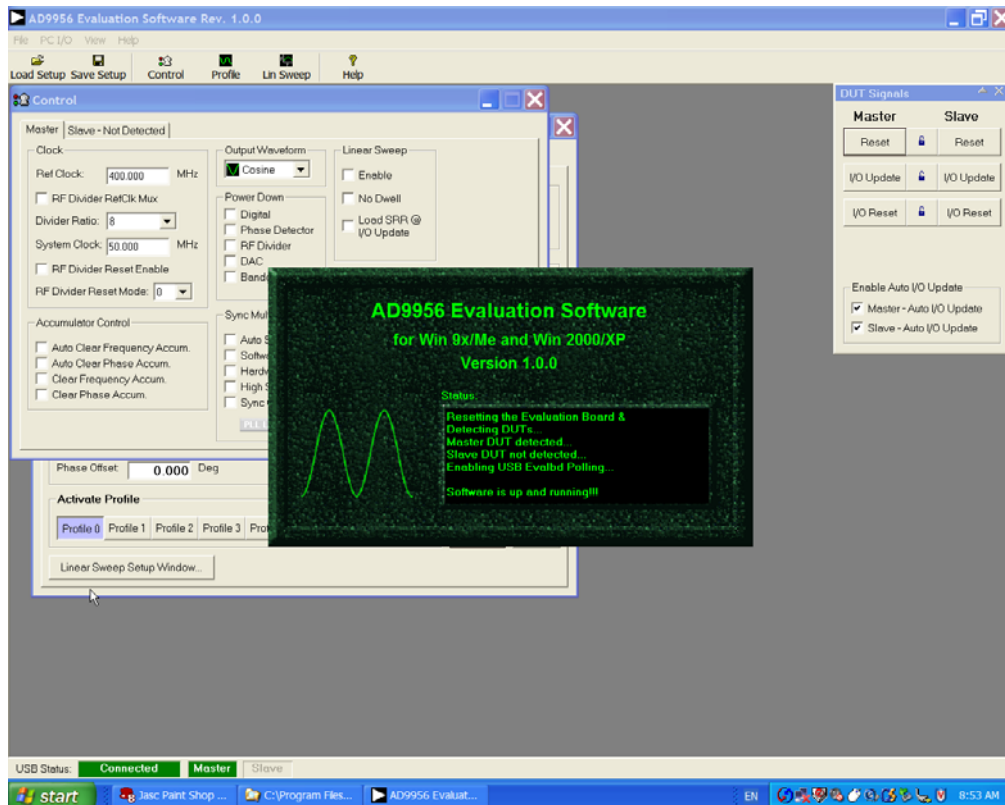


Figure 2. AD9956/PCB Evaluation Board Software Status Message upon Successful Load

CONTROL DIALOG BOX

Use the **Control** dialog box to enable and disable individual device functions, program the input clock speed, and toggle various other options. Figure 3 shows the sections of the **Control** dialog box: **Clock**, **Output Waveform**, **Linear Sweep**, **Power Down**, **Accumulator Control**, and **Sync Multi DUT's**.

Click **Charge Pump/Clock Driver Window**, **I/O Interface Window**, or **DUT Signals Window** to access these dialog boxes.

LOAD and READ

At the bottom right of the dialog box are the **LOAD** and **READ** buttons.

After you have made changes to the evaluation software, click **LOAD** to send the data to the device. In addition to sending data, you can also configure **LOAD** to automatically send an I/O update signal to the DUT when the software finishes sending data. See the DUT Signals Dialog Box section for details. When new data is ready to be sent, **LOAD** flashes green, indicating that you need to issue a **LOAD**.

Click **READ** to perform a readback of the currently programmed status of the device and to update the GUI with the current settings.

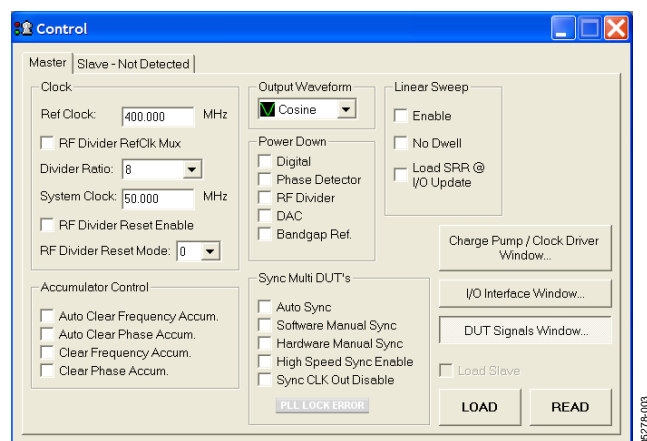


Figure 3. Control Dialog Box

Clock

To program the reference clock and the RF prescaler values:

1. In the **Ref Clock** box, type the operating frequency of the external reference clock. The maximum is 2.7 GHz.
2. In the **Divider Ratio** box, select a divider value for the RF prescaler. The value must be in the range of 1 and 8.
3. Click **LOAD**.

To bypass the RF divider and pipe the REFCLK input directly to the DDS core, select **RF Divider RefClk Mux**. Even though the divider operates at $/1$, $/2$, $/4$, or $/8$, and this divided signal can be ported to the PECL driver, the raw, undivided REFCLK is used as the internal system clock when this box is checked. Do *not* select this box, if the REFCLK input is greater than 400 MHz.

Output Waveform

In the **Output Waveform** box, select either a cosine(x) or a sine(x) function for the angle-to-amplitude conversion.

Linear Sweep

Use the **Linear Sweep** section to enable the linear sweep functions of the DDS. See the AD9956 data sheet for a detailed explanation of these modes of operation.

Select **Enable** to turn on the frequency accumulator. If the **No Dwell** box is not checked, the part is set in ordinary linear sweep mode.

Select both **Enable** and **No Dwell** to put the part into linear sweep no-dwell mode.

When you select **Load SRR @ I/O Update**, the current countdown of the sweep ramp rate is cleared every time an I/O_UPDATE signal is sent to the part. When using manual programming through the GUI, it is almost impossible to notice the effect of this function because the sweep ramp rates cycle through their countdown timers in less than 655 μ s, even when programmed to a maximum value.

The linear sweep parameters (delta frequencies and ramp rates) are controlled in the **Linear Sweep** section (see Figure 3). The sweep itself, however, is controlled by the **Ramp Up** and **Ramp Down** buttons, which appear at the bottom of the **Profile** dialog box when the **Linear Sweep Enable** box is checked. See the Profile Dialog Box section for details.

Power Down

In the **Power Down** section, select the check boxes for the circuit blocks that you want to power down.

Accumulator Control

This section controls the clear functions for the phase and frequency accumulators.

Select **Auto Clear Frequency Accum.** or **Auto Clear Phase Accum.** to clear and release the corresponding accumulator. The auto clear function sets the accumulator to a known value of 0 and then begins accumulating.

Select **Clear Frequency Accum.** or **Clear Phase Accum.** to clear and hold the corresponding accumulator. The clear function clears and then holds the contents of the corresponding accumulator to 0 until you uncheck the box.

Sync Multi DUTs

This section controls the multiple synchronization functions of the AD9956.

Select **Auto Sync** and then click **LOAD** to turn on the auto-synchronization routine of the DDS. When this function is on, the DDS aligns its internal DDS clock edge to a sync signal, supplied on the PLL_LOCK/SYNC_IN pin. Once the clock edge is aligned, this function should be turned off because it does not provide continuous monitoring.

Select **Software Manual Sync** to advance the SYNC-CLK rising edge by one system clock period. Once executed, the bit is cleared. To advance multiple system clock periods, select this box and then click **LOAD** several times.

Select **Hardware Manual Sync** to advance the sync clock rising edge by one system clock period for each rising edge detected on the SYNC_IN pin. This bit does not self-clear.

Select **High Speed Sync Enable** to turn on a high speed synchronization algorithm that you can use to synchronize multiple DDSs operating at a 250 MSPS system clock rate or faster. Do not select this box for system clock rates below 250 MSPS.

Select **Sync CLK Out Disable** to turn off the sync clock output. The PLL lock detect enable bit in the **Charge Pump** dialog box enables a PLL lock monitoring function, either through the PLL_LOCK_DETECT pin (externally) or by setting a flag in the control register, CFR1<24>, which is the PLL lock error bit.

When you turn on auto-synchronization or hardware manual synchronization, the PLL_LOCK/SYNC_IN pin becomes an input, and the ability to monitor the lock detect signal externally is lost. This flag is stored at CFR1<24> and clears itself when the register is read, that is, the flag is seen and then auto-cleared. If, during a readback, the evaluation software detects that this flag is set, the **PLL_LOCK_ERROR** bar at the bottom of this section flashes. The next time the flag is read, the bar stops flashing if the flag is cleared.

PROFILE DIALOG BOX

The DDS section of the AD9956 has eight programmable frequency and phase offset profiles. You can write values for these profiles in the **Profile** dialog box, shown in Figure 4.

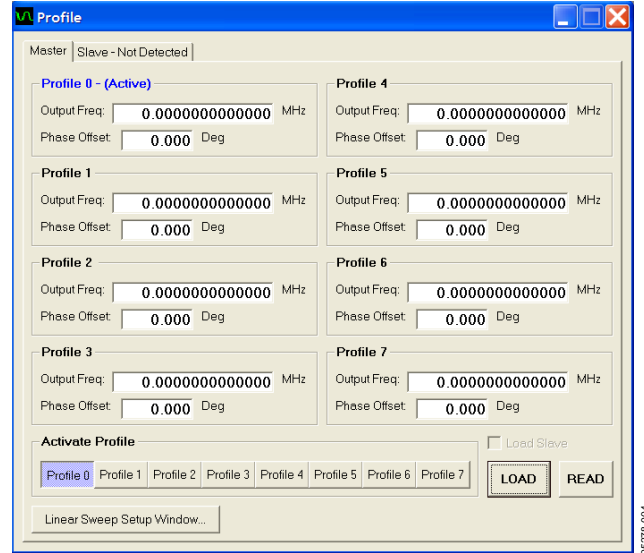


Figure 4. Profile Dialog Box

To select the active profile, click the corresponding **Active Profile** button (**Profile 0** to **Profile 7**) at the bottom of the dialog box. Changing profiles is an immediate selection; no **LOAD** is required.

During linear sweep modes of operation, the **Ramp Up** and **Ramp Down** buttons are displayed at the bottom of the **Profile** dialog box, as shown in Figure 5. Click the appropriate button to either ramp the part up to the value stored in Profile 1 or to ramp the part down to the value stored in Profile 0.

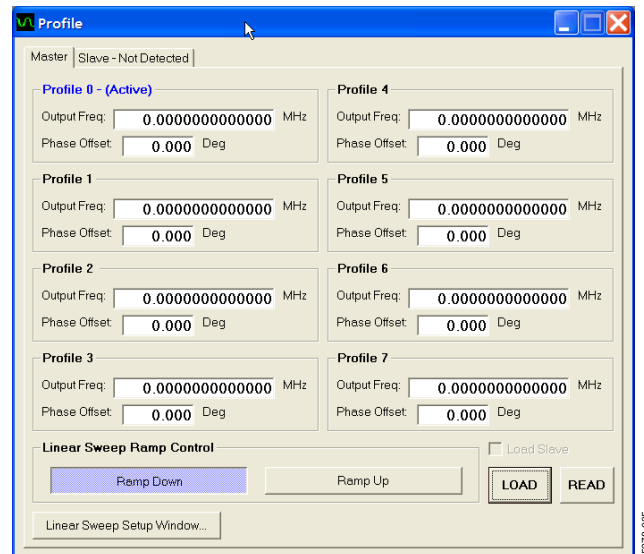


Figure 5. Profile Dialog Box when Linear Sweep Is Enabled

CLOCK DRIVER CONTROL, PHASE-FREQUENCY DETECTOR & CHARGE PUMP DIALOG BOX

This dialog box controls the phase detector, charge pump, and PECL driver components of the device. Use this dialog box to modify the parameters that control these functions. The dialog box has two sections: **(CML) Clock Driver** and **Phase-Frequency Detector/Charge Pump**, shown in Figure 6.

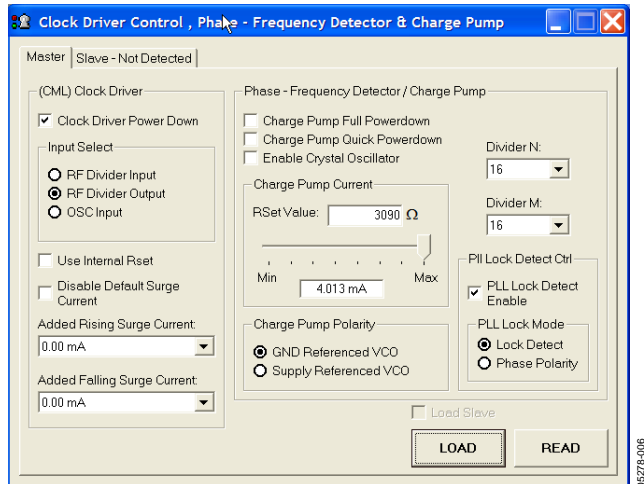


Figure 6. Clock Driver Control, Phase-Frequency Detector & Charge Pump Dialog Box

(CML) Clock Driver

The on-chip clock driver is current-mode logic (CML) that is PECL-compliant when properly terminated. The driver can operate at up to 650 MHz.

To power down the CML driver, select the **Clock Driver Power Down** check box.

Use the **Input Select** section to specify the signal that is fed to the input of the CML driver. Select **RF Divider Input** (REFCLK), **RF Divider Output** (SYSCLK), or the **OSC Input**.

The full-scale output current for the CML driver is normally programmed by connecting an external resistor from the DUT pin, DRV_RSET, to analog ground. However, if you want to use an internal current programming resistor, select **Use Internal Rset**.

Use the **Adding Rise Surge Current** and **Adding Falling Surge Current** drop-down menus to change the slew rate of the output of the PECL driver in response to different capacitive loads to critically damp the response. See the AD9956 data sheet for a description of how these values impact the slew rate.

Phase-Frequency Detector/Charge Pump

This section controls the PLL components of the AD9956 and the CML (PECL-compliant when properly terminated) clock driver circuits. The first two check boxes allow you to power down the phase detector and charge pump.

Select **Charge Pump Full Powerdown** to power down the entire charge pump. A delay occurs when coming out of this power-down to reestablish the correct charge pump current.

Select **Charge Pump Quick Powerdown** to power down the phase-detector logic while keeping the charge pump current flowing. No settling time is needed to reestablish the charge pump current.

Select **Enable Crystal Oscillator** to turn on an oscillator function in the phase detector REFERENCE input. When this function is selected, you can use an external crystal on the REFERENCE input to stimulate an internal oscillator as the reference for the PLL.

Move the **Charge Pump Current** slider to set the multiplier value for the charge pump reference current. The actual current from the charge pump, based on the external Rset value, is shown beneath the slider. The charge pump reference current is equal to $1.51/CP_Rset$, in mA, by the default setting of 3.09 k Ω on the evaluation board. The base output current of the charge pump is 500 μ A, which can be gained up to 4 mA. The charge pump polarity changes the loop polarity for a ground-referenced VCO or a supply-referenced VCO.

The phase detector IF prescalers, **Divider N** and **Divider M**, set the divide-by value on the inputs to the phase detector. The dividers operate at up to 650 MHz, although the phase detector inputs themselves operate only up to 200 MHz. You must use these dividers for any frequencies sent to the phase detector beyond 200 MHz.

The **PLL Lock Detect Ctrl** section controls the lock detect functionality of the AD9956. To enable the lock detect signal, select the **Lock Detect Enable** check box. The lock detect signal can work in two modes. When you select **Lock Detect**, Logic 1 indicates that the loop has achieved a locked state, and Logic 0 indicates that the loop is unlocked. When you select **Phase Polarity**, Logic 0 indicates that the reference signal leads the feedback signal, and Logic 1 indicates that the reference signal lags behind the feedback signal.

DUT SIGNALS DIALOG BOX

This dialog box controls the reset, I/O update, and I/O reset signals for the master and slave devices. Click the lock icon between the corresponding Master and Slave buttons to lock the two together. Click **Master** or **Slave Reset, I/O Update, or I/O Reset**, to specify the unit that issues the command to both devices.

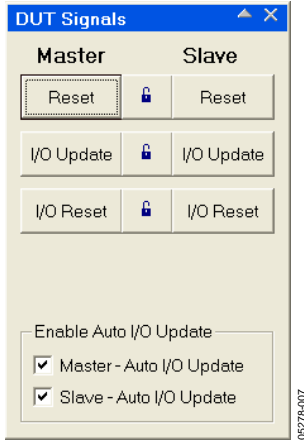


Figure 7. DUT Signals Dialog Box

The auto I/O update function is controlled in the **Enable Auto I/O Update** section. Select either **Master–Auto I/O Update**, **Slave–Auto I/O Update**, or both to send an I/O update to the device(s) every time you click **LOAD** (default on). If you want a device to wait for a manually sent I/O update signal, clear the corresponding check box.

DUT I/O DIALOG BOX

This dialog box controls the I/O configuration for the device.

Click **I/O Reset Master** or **I/O Reset Slave** to send an I/O reset to the corresponding serial port state machine.

Select **LSB First** to change the data format to LSB first. The default is MSB first.

In the **Serial I/O Mode** section, select either **2 Wire** or **3 Wire** from the drop-down list to specify the part as either, respectively, a 2-wire serial port, in which the serial data line is I/O, or a 3-wire serial port, in which the serial data is input on SDI/O and read back on SDO.

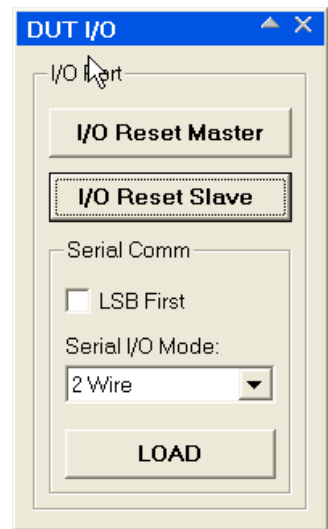


Figure 8. DUT I/O Dialog Box

DEBUG WINDOW

The **Debug Window**, shown in Figure 9, lets you directly write to any of the internal registers and subsequently read them back. You can also directly toggle the states of any external inputs such as PS0, PS1, or PS2.

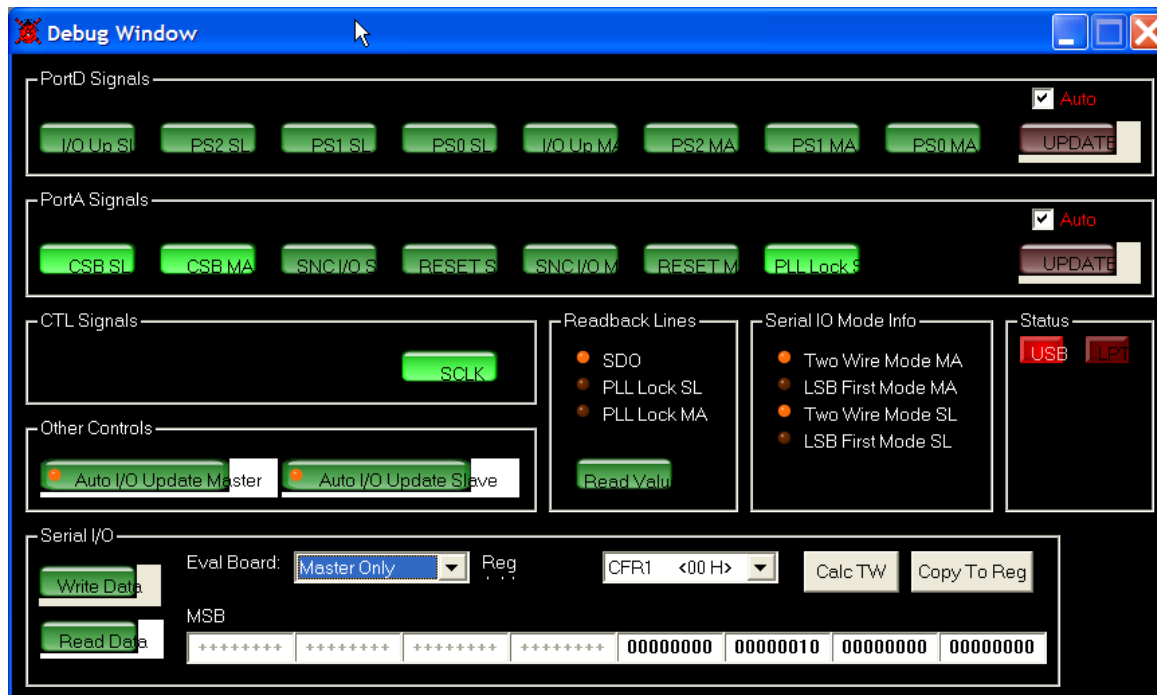


Figure 9. Debug Window

AD9956/PCB

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
AD9956/PCB	Evaluation Board
AD9956-VCO/PCB	Evaluation Board with 2.4 GHz VCO and Charge Pump Filter

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



NOTES