

### FEATURES

**High slew rate:** 20 V/ $\mu$ s  
**Fast settling time**  
**Low offset voltage:** 1.70 mV maximum  
**Bias current:** 40 pA maximum  
 **$\pm 4$  V to  $\pm 18$  V operation**  
**Low voltage noise:** 16 nV/ $\sqrt{\text{Hz}}$   
**Unity gain stable**  
**Common-mode voltage includes +V<sub>s</sub>**  
**Wide bandwidth:** 5 MHz

### APPLICATIONS

**Reference gain/buffers**  
**Level shift/driving**  
**Active filters**  
**Power line monitoring/control**  
**Current/voltage sense or monitoring**  
**Data acquisition**  
**Sample-and-hold circuits**  
**Integrators**

### GENERAL DESCRIPTION

The ADA4000-1/ADA4000-2/ADA4000-4 are junction field effect transistor (JFET) input operational amplifiers featuring precision, very low bias current, and low power. Combining high input impedance, low input bias current, wide bandwidth, fast slew rate, and fast settling time, the ADA4000-1/ADA4000-2/ADA4000-4 are ideal amplifiers for driving analog-to-digital inputs and buffering digital-to-analog converter outputs. The input common-mode voltage includes the positive power supply, which makes the device an excellent choice for high-side signal conditioning.

Additional applications for the ADA4000-1/ADA4000-2/ADA4000-4 include electronic instruments, automated test equipment (ATE) amplification, buffering, integrator circuits, instrumentation-quality photodiode amplification, and fast precision filters (including phase-locked loop filters). The devices also include utility functions, such as reference buffering, level shifting, control input/output interface, power supply control, and monitoring functions.

### PIN CONFIGURATIONS

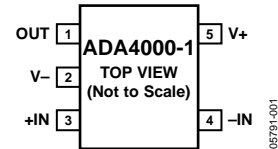


Figure 1. 5-Lead TSOT (UJ-5)

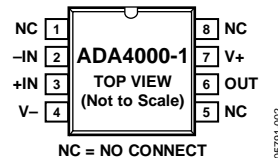


Figure 2. 8-Lead SOIC (R-8)

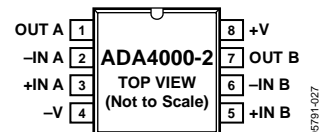


Figure 3. 8-Lead SOIC (R-8)

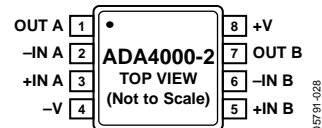


Figure 4. 8-Lead MSOP (RM-8)

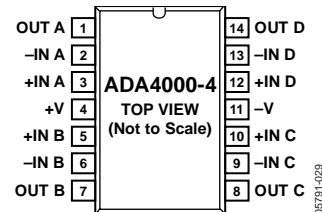


Figure 5. 14-Lead SOIC (R-14)

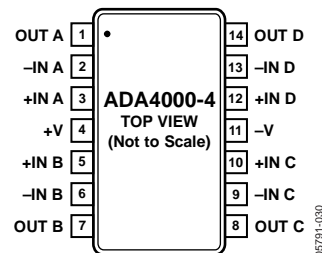


Figure 6. 14-Lead TSSOP (RU-14)

**TABLE OF CONTENTS**

Features .....	1	Power Sequencing .....	5
Applications.....	1	ESD Caution.....	5
General Description .....	1	Typical Performance Characteristics .....	6
Pin Configurations .....	1	Applications Information .....	10
Revision History .....	2	Output Phase Reversal and Input Noise .....	10
Specifications.....	3	Capacitive Load Drive .....	10
Electrical Characteristics .....	3	Settling Time.....	11
Absolute Maximum Ratings.....	5	Outline Dimensions .....	12
Thermal Resistance .....	5	Ordering Guide .....	14

**REVISION HISTORY**

**3/16—Rev. A to Rev. B**

Change to Figure 12 Caption .....	6
Changes to Output Phase Reversal and Input Noise Section and Capacitive Load Drive Section .....	10
Updated Outline Dimensions .....	13

**3/09—Rev. 0 to Rev. A**

Changes to Input Voltage Range Parameter .....	4
Changes to Common-Mode Rejection Ration Parameter .....	4
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	14

**5/07—Revision 0: Initial Version**

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$V_S = \pm 15.0\text{ V}$ ,  $V_{CM} = V_S/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.2	1.70	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	3.0	mV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			40	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			170	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	4.5	nA
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			40	pA
Input Voltage Range	IVR	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			80	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			500	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-11		+15	V
Common-Mode Rejection Ratio	CMRR	$-11\text{ V} \leq V_{CM} \leq +15\text{ V}$	80	100		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		100		dB
Open-Loop Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$	100	110		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to ground	13.60	13.90		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.40			V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to ground		-13.4	-13.0	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-12.80	V
Short-Circuit Current	$I_{SC}$			$\pm 28$		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.0\text{ V}$ to $\pm 18.0\text{ V}$	82	92		dB
Supply Current/Amplifier	$I_{SY}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.35	1.65	mA
					1.80	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$V_I = 10\text{ V}$ , $R_L = 2\text{ k}\Omega$		20		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	$\Phi_M$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		1		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		16		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
INPUT IMPEDANCE						
Differential Mode	$(R  C)_{IN-DIFF}$			10  4		$\text{G}\Omega  \text{pF}$
Common Mode	$(R  C)_{IN-CM}$			10 <sup>3</sup>   5.5		$\text{G}\Omega  \text{pF}$

$V_S = \pm 5\text{ V}$ ,  $V_{CM} = V_S/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.20	1.70	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	3.0	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			170	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	3	nA
Input Voltage Range	IVR	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			40	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			80	pA
						500
Common-Mode Rejection Ratio	CMRR	$-1.0\text{ V} \leq V_{CM} \leq +5.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-1.0	72	80	dB
Open-Loop Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = \pm 2.5\text{ V}$	106	114		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.0	4.20		V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				V
					-3.45	-3.20
Short-Circuit Current	$I_{SC}$					V
						-3.00
				$\pm 28$		mA
<b>POWER SUPPLY</b>						
Supply Current/Amplifier	$I_{SY}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.25	1.65	mA
					1.80	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$V_I = 10\text{ V}$ , $R_L = 2\text{ k}\Omega$		20		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	$\Phi_M$			55		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		1		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		16		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
<b>INPUT IMPEDANCE</b>						
Differential Mode	$(R  C)_{IN-DIFF}$			10  4		$\text{G}\Omega  \text{pF}$
Common Mode	$(R  C)_{IN-CM}$			10 <sup>3</sup>   5.5		$\text{G}\Omega  \text{pF}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18$ V
Input Voltage	$\pm V$ supply
Differential Input Voltage	$\pm V$ supply
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Junction Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-Lead TSOT (UJ-5)	172.92	61.76	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC (R-8)	112.38	61.6	$^{\circ}\text{C}/\text{W}$
8-Lead MSOP (RM-8)	141.9	43.7	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC (R-14)	88.2	56.3	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU-14)	114	23.3	$^{\circ}\text{C}/\text{W}$

## POWER SEQUENCING

The operational amplifier supply voltages must be established simultaneously with, or before, any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

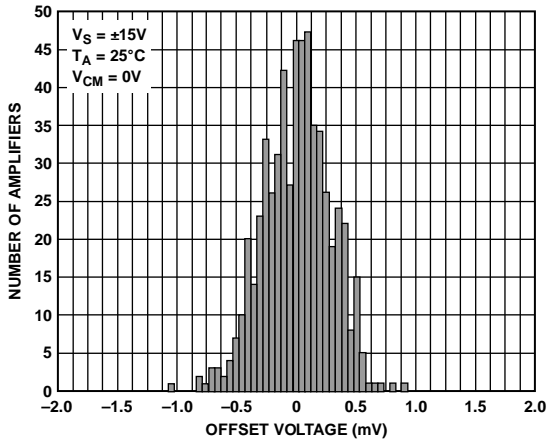


Figure 7. Input Offset Voltage Distribution,  $V_S = \pm 15 V$

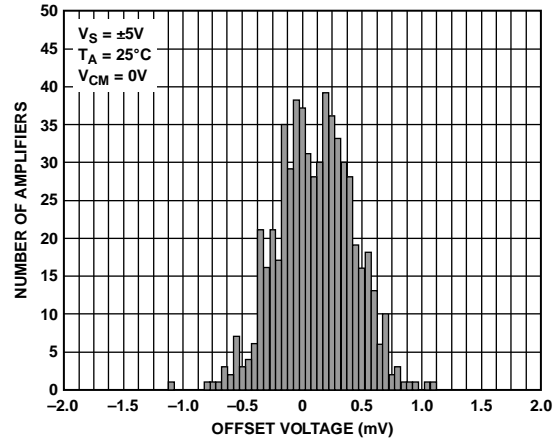


Figure 10. Input Offset Voltage Distribution,  $V_S = \pm 5 V$

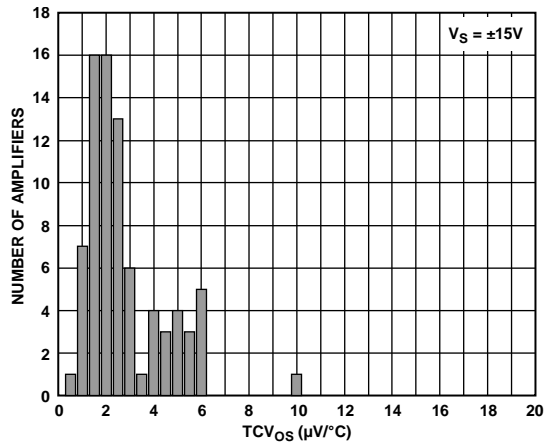


Figure 8. Offset Voltage Drift Distribution,  $V_S = \pm 15 V$

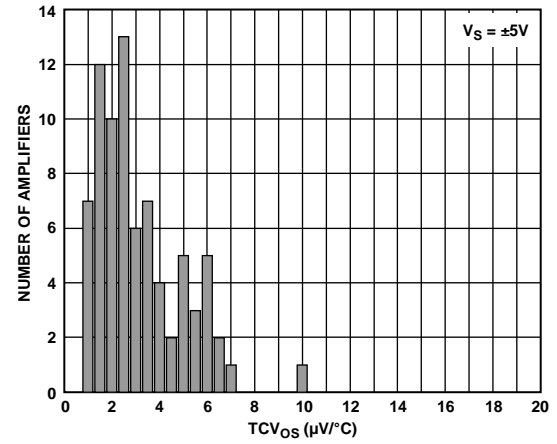


Figure 11. Offset Voltage Drift Distribution,  $V_S = \pm 5 V$

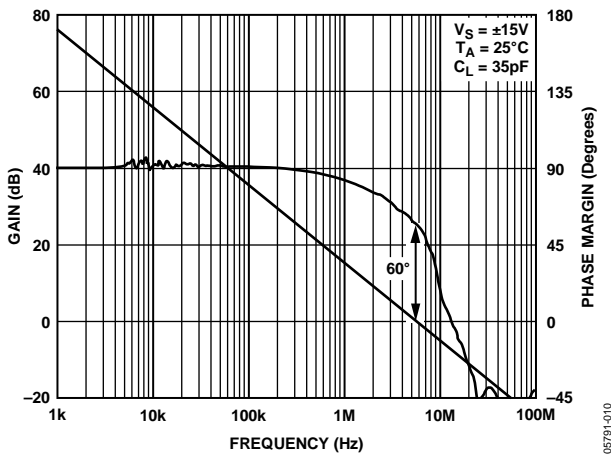


Figure 9. Open-Loop Gain and Phase Margin vs. Frequency,  $V_S = \pm 15 V$

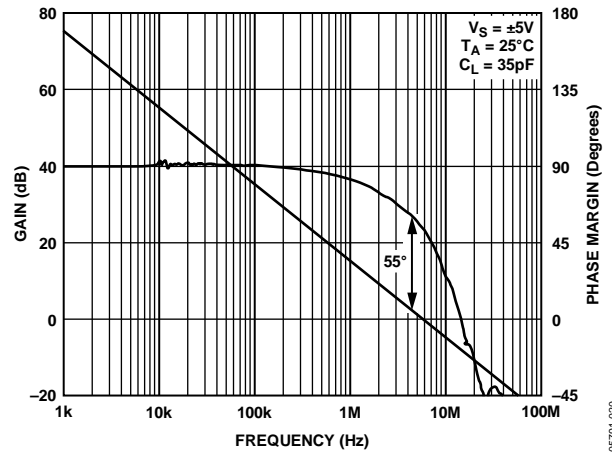


Figure 12. Open-Loop Gain and Phase Margin vs. Frequency,  $V_S = \pm 5 V$

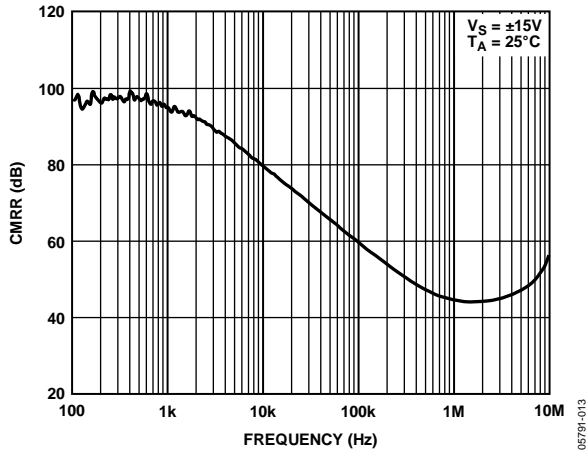


Figure 13. Common-Mode Rejection Ratio vs. Frequency,  $V_S = \pm 15 V$

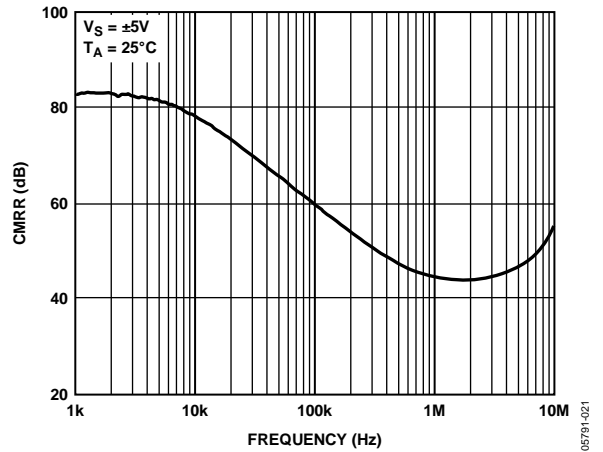


Figure 16. Common-Mode Rejection Ratio vs. Frequency,  $V_S = \pm 5 V$

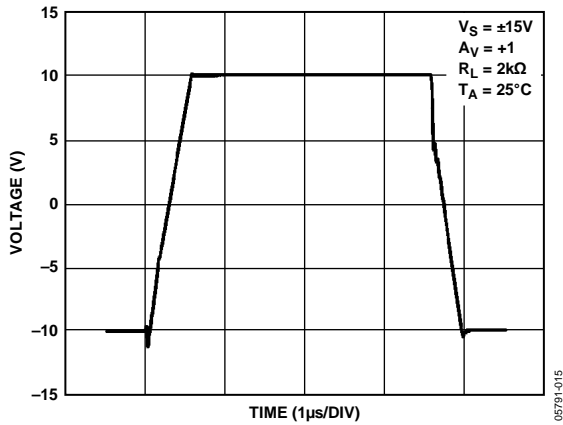


Figure 14. Large Signal Transient Response,  $V_S = \pm 15 V$

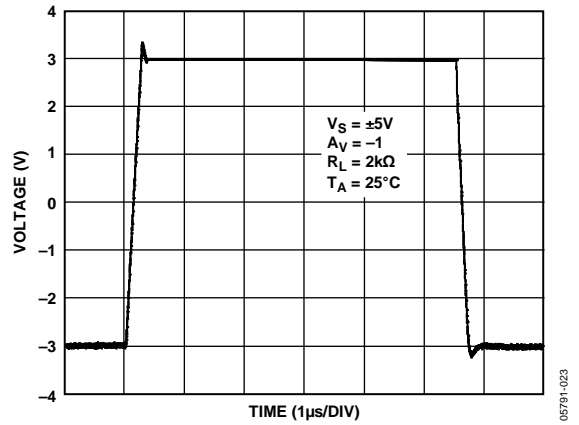


Figure 17. Large Signal Transient Response,  $V_S = \pm 5 V$

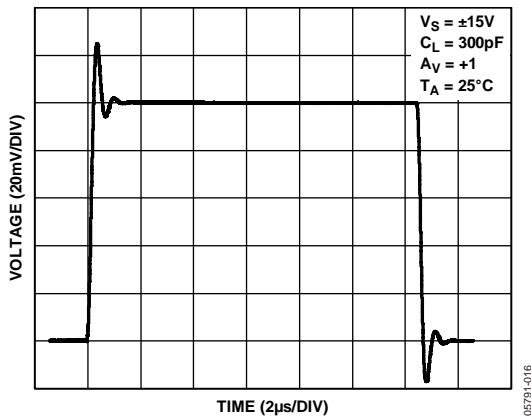


Figure 15. Small Signal Transient Response,  $V_S = \pm 15 V$

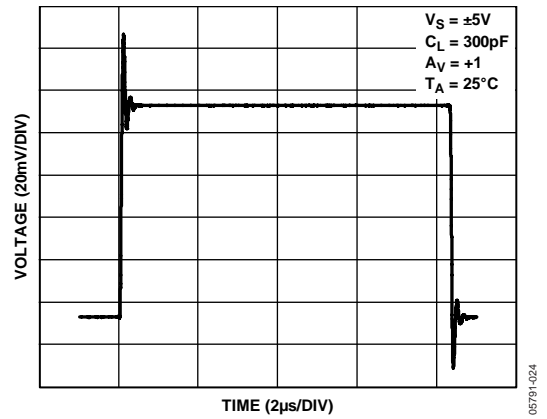


Figure 18. Small Signal Transient Response,  $V_S = \pm 5 V$

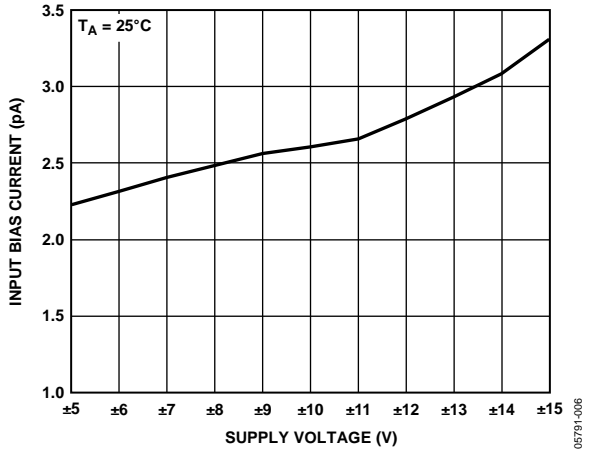


Figure 19. Input Bias Current vs. Supply Voltage

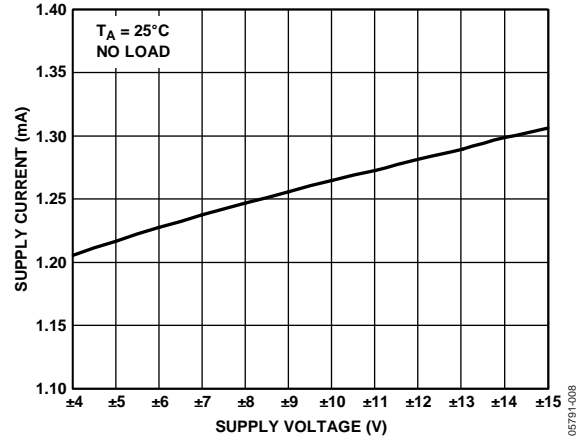


Figure 22. Supply Current vs. Supply Voltage

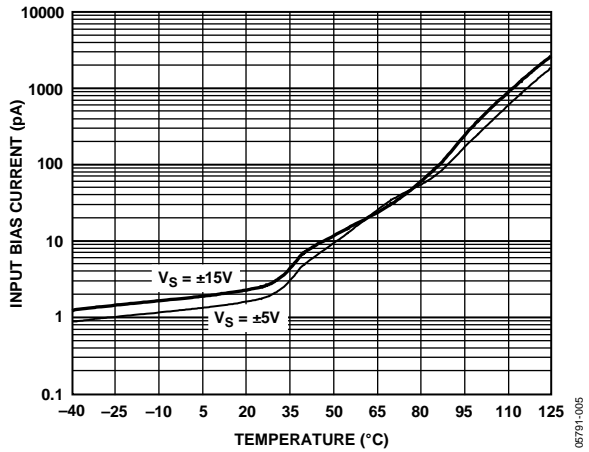


Figure 20. Input Bias Current vs. Temperature

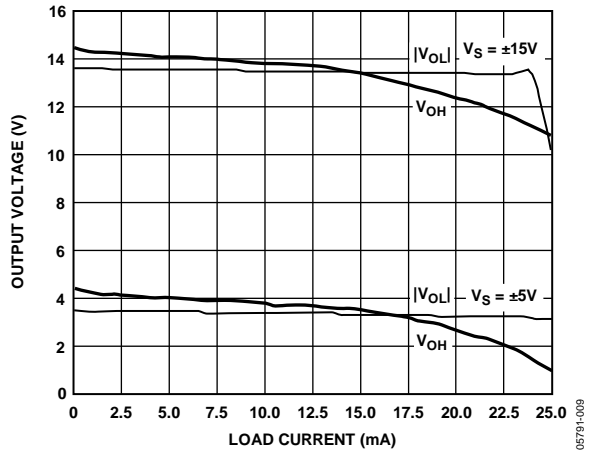


Figure 23. Output Voltage vs. Load Current

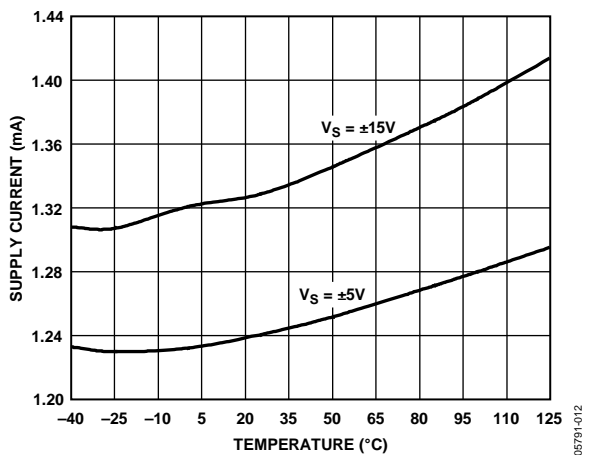


Figure 21. Supply Current vs. Temperature

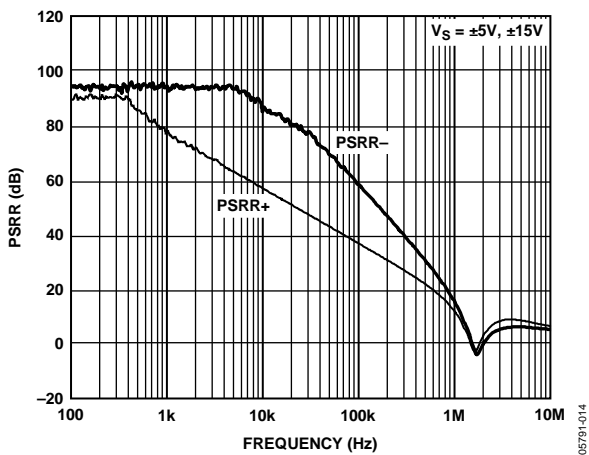


Figure 24. PSRR vs. Frequency



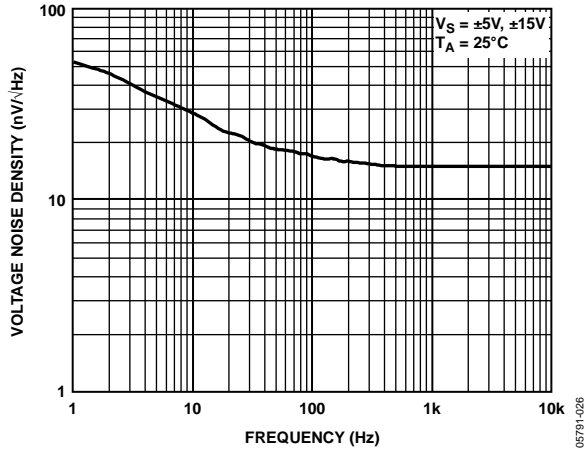


Figure 25. Voltage Noise Density vs. Frequency

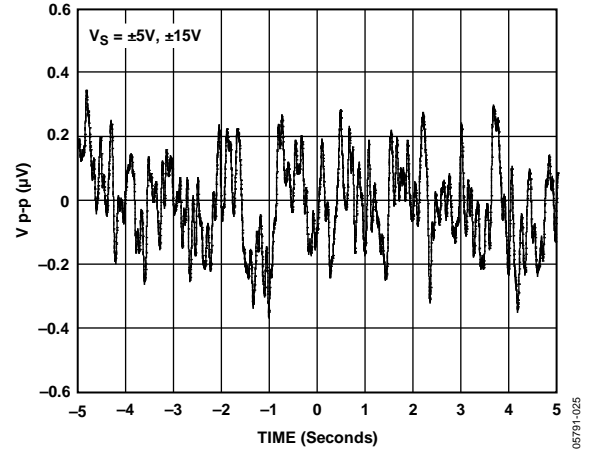


Figure 28. 0.1 Hz to 10 Hz Input Voltage Noise

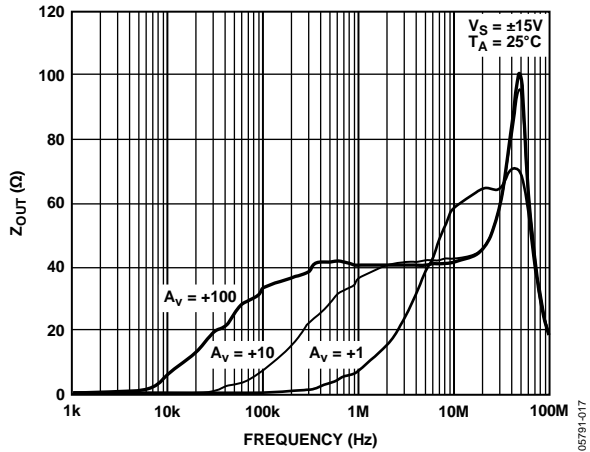


Figure 26. Output Impedance vs. Frequency

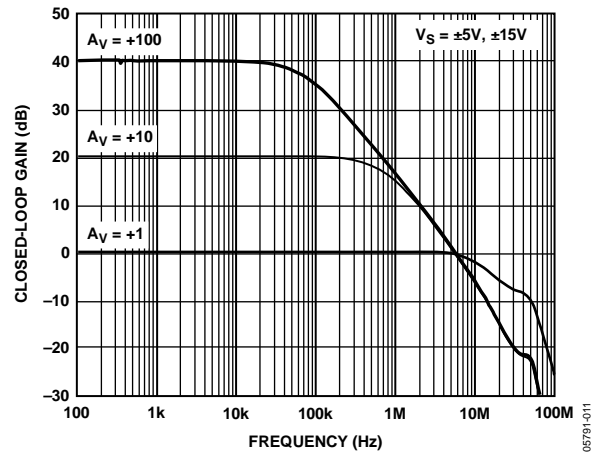


Figure 29. Closed-Loop Gain vs. Frequency

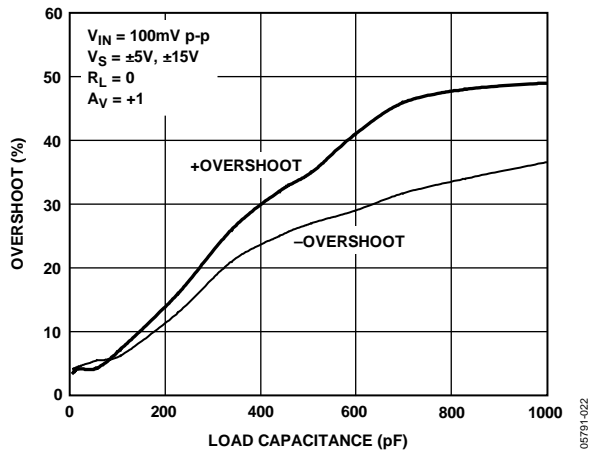


Figure 27. Overshoot vs. Load Capacitance

## APPLICATIONS INFORMATION

### OUTPUT PHASE REVERSAL AND INPUT NOISE

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of the amplifier exceeds the maximum common-mode voltage. Phase reversal happens when the device is configured in the gain of 1.

Most JFET amplifiers invert the phase of the input signal if the input exceeds the common-mode input. Phase reversal is a temporary behavior of the ADA4000-1/ADA4000-2/ADA4000-4 family. Each device returns to normal operation by bringing back the common-mode voltage. The cause of this effect is saturation of the input stage, which leads to the forward-biasing of a drain-gate diode. In noninverting applications, a simple fix for this is to insert a series resistor between the input signal and the non-inverting terminal of the amplifier. The value of the resistor depends on the application, because adding a resistor adds to the total input noise of the amplifier. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_s)^2 + 4kTR_s}$$

where:

$e_n$  is the input voltage noise density of the device.

$i_n$  is the input current noise density of the device.

$R_s$  is the source resistance at the noninverting terminal.

$k$  is Boltzmann's constant ( $1.38 \times 10^{-23}$  J/K).

$T$  is the ambient temperature in Kelvin ( $T = 273 + ^\circ\text{C}$ ).

In general, it is good practice to limit the input current to less than 5 mA to avoid driving a great deal of current into the amplifier inputs.

### CAPACITIVE LOAD DRIVE

The ADA4000-1/ADA4000-2/ADA4000-4 are stable at all gains in both inverting and noninverting configurations. The devices are capable of driving up to 1000 pF of capacitive loads without oscillations in unity gain configurations.

However, as with most amplifiers, driving larger capacitive loads in a unity gain configuration can cause excessive overshoot and ringing. A simple solution to this problem is to use a snubber network (see Figure 30).

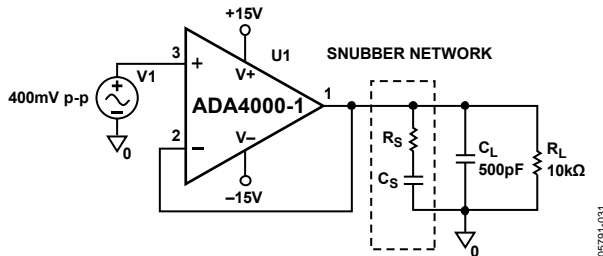


Figure 30. Snubber Network Configuration

The advantage of this compensation method is that the swing at the output is not reduced because  $R_s$  is out of the feedback network, and the gain accuracy does not change. Depending on the capacitive loading of the circuit, the values of  $R_s$  and  $C_s$  change, and the optimum value can be determined empirically. In Figure 31, the oscilloscope image shows the output of the ADA4000-1/ADA4000-2/ADA4000-4 family in response to a 400 mV pulse. The circuit is configured in the unity gain configuration with 500 pF in parallel with 10 kΩ of load capacitive.

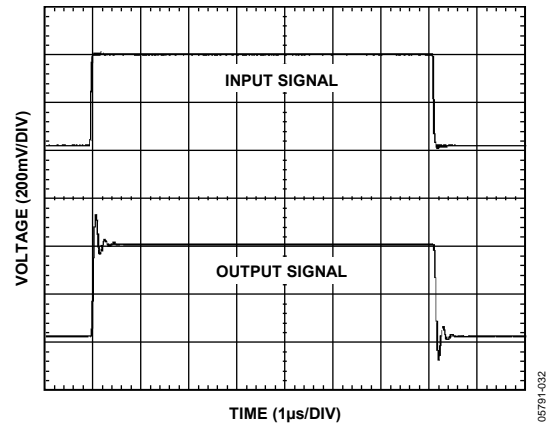


Figure 31. Capacitive Load Drive Without Snubber Network

When the snubber circuit is used, the overshoot is reduced from 30% to 6% with the same load capacitance. Ringing is virtually eliminated, as shown in Figure 32. In this circuit,  $R_s$  is 41 Ω and  $C_s$  is 10 nF.

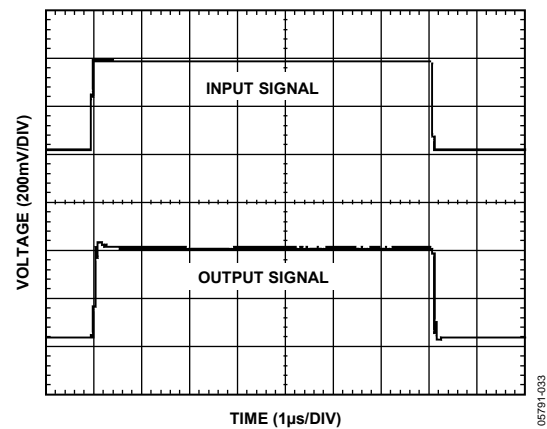


Figure 32. Capacitive Load with Snubber Network

**SETTLING TIME**

Settling time is the amount of time it takes the amplifier output to reach and remain within a percentage of the final value. This is an important parameter in data acquisition systems. Because most bipolar DAC converters have current output, an external operational amplifier is required to convert the current to voltage. Therefore, the amplifier settling time plays a role in the total settling time of the output signal. A good approximation for the total settling time is

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The ADA4000-1/ADA4000-2/ADA4000-4 settle to within 0.1% of their final value in less than 1.2 μs. The settling time has been tested by using the configuration circuit in Figure 34.

The input signal is a 10 V pulse and the output is the error signal for the settling time shown in Figure 33.

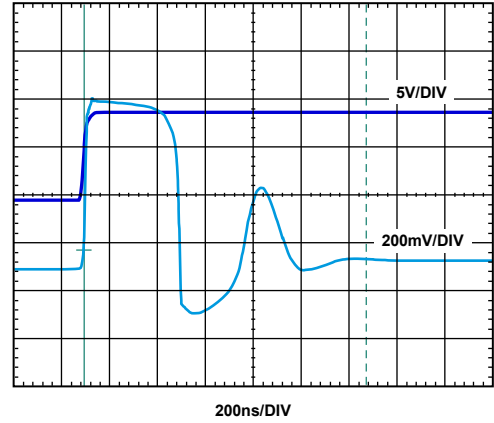


Figure 33. Settling Time Measurement Using the False Summing Node Method

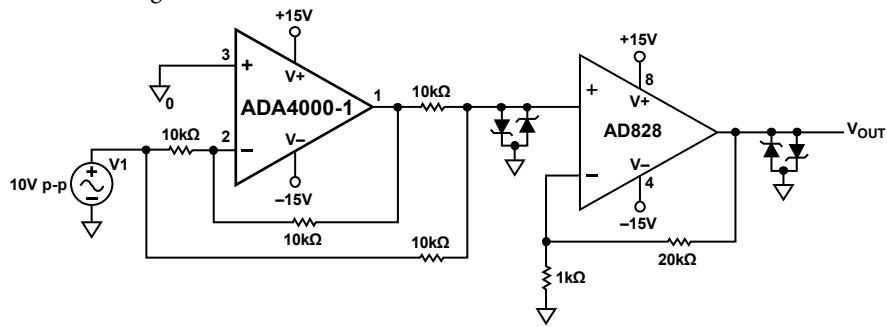
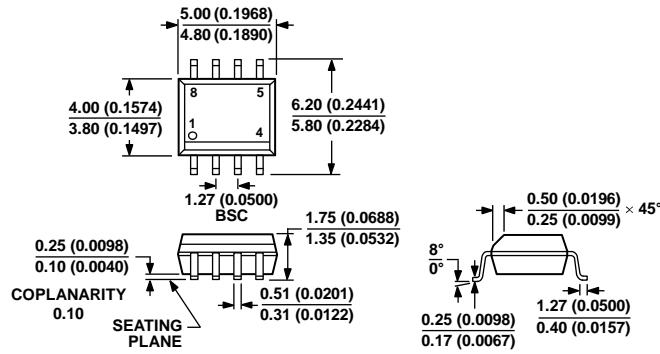


Figure 34. Settling Time Test Circuit

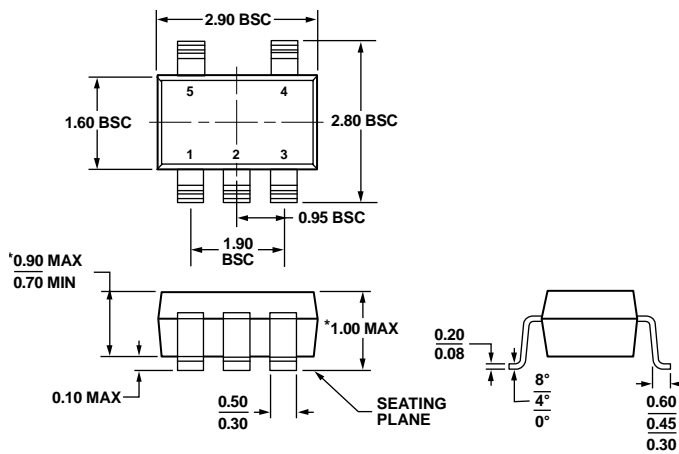
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-A A  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

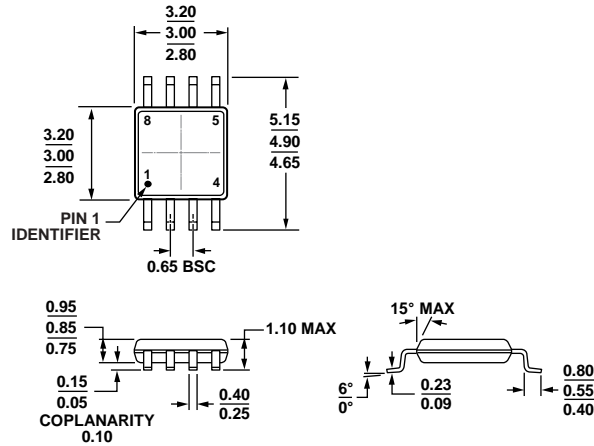
Dimensions shown in millimeters and (inches)



\*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH  
 THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 36. 5-Lead Thin Small Outline Transistor Package [TSOT]  
 (UJ-5)

Dimensions shown in millimeters

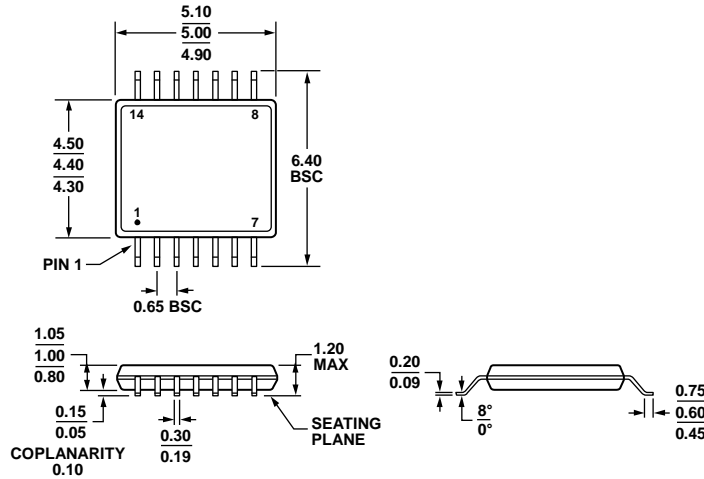


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 37. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2008-B

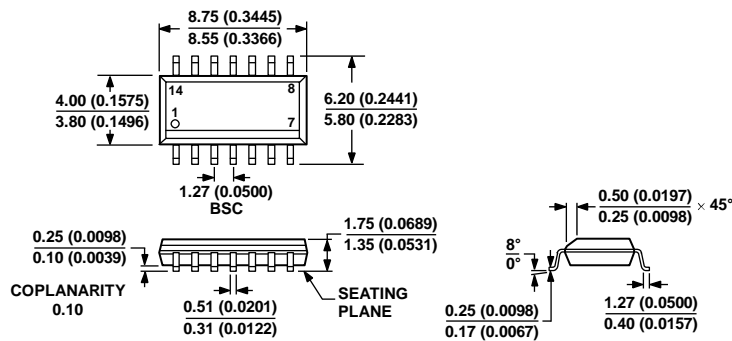


COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 38. 14-Lead Standard Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061908-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 14-Lead Standard Small Outline Package [SOIC\_N] (R-14)

Dimensions shown in millimeters

060606-A

**ORDERING GUIDE**

<b>Model<sup>1</sup></b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>	<b>Branding</b>
ADA4000-1ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-1ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-1ARZ-RL	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-1AUJZ-R2	-40°C to +125°C	5-Lead TSOT	UJ-5	A14
ADA4000-1AUJZ-R7	-40°C to +125°C	5-Lead TSOT	UJ-5	A14
ADA4000-1AUJZ-RL	-40°C to +125°C	5-Lead TSOT	UJ-5	A14
ADA4000-2ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-2ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-2ARZ-RL	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4000-2ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A1H
ADA4000-2ARMZ-RL	-40°C to +125°C	8-Lead MSOP	RM-8	A1H
ADA4000-4ARZ	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4000-4ARZ-R7	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4000-4ARZ-RL	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4000-4ARUZ	-40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4000-4ARUZ-RL	-40°C to +125°C	14-Lead TSSOP	RU-14	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**